2.22 The circuit in Fig. P2.22 is frequently used to provide an output voltage v_o proportional to an input signal current i_i.

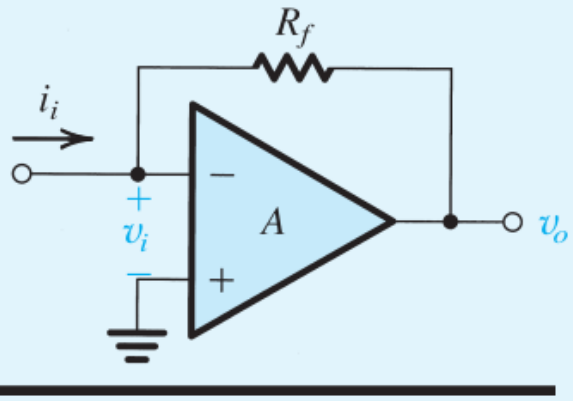
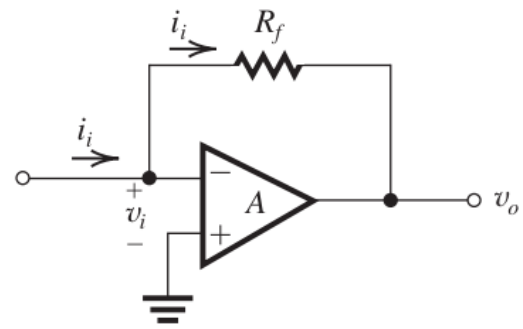


Figure P2.22

Derive expressions for the transresistance $R_m \equiv v_o/i_i$ and the input resistance $R_i \equiv v_i/i_i$ for the following cases:

(a) A is infinite.
(b) A is finite.



(a) For $A = \infty$: $v_i = 0$

$$v_o = -i_i R_f$$

$$R_m = \frac{v_o}{i_i} = -R_f$$

$$R_{\text{in}} = \frac{v_i}{i_i} = 0$$

(b) For A finite: $v_i = -\dfrac{v_o}{A}$, $v_o = v_i - i_i R_f$

$$\Rightarrow v_o = \frac{-v_o}{A} - i_i R_f \Rightarrow R_m = \frac{v_o}{i_i} = -\frac{R_f}{1 + \dfrac{1}{A}}$$

$$R_i = \frac{v_i}{i_i} = \frac{R_f}{1 + A}$$

***2.25** Figure P2.25 shows an op amp that is ideal except for having a finite open-loop gain and is used to realize an inverting amplifier whose gain has a nominal magnitude $G = R_2/R_1$. To compensate for the gain reduction due to

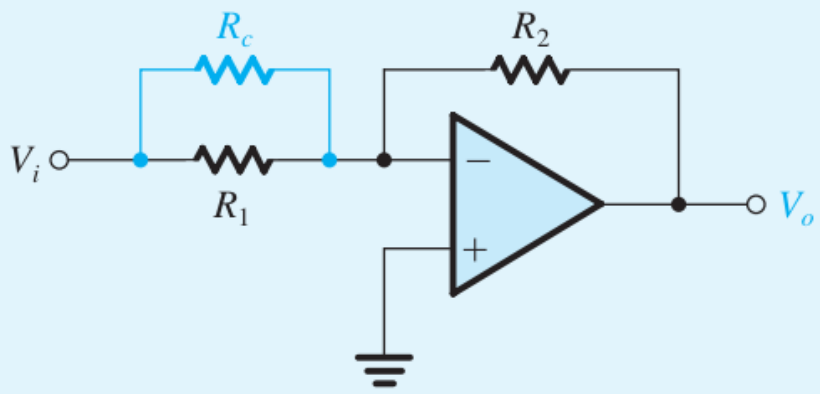


Figure P2.25

the finite A, a resistor R_c is shunted across R_1. Show that perfect compensation is achieved when R_c is selected according to

$$\frac{R_c}{R_1} = \frac{A - G}{1 + G}$$

$$\frac{V_o}{V_i} = \frac{-R_2/R_1'}{1 + \dfrac{1 + R_2/R_1'}{A}}$$

where

$$R_1' = R_1 \| R_c$$

Thus,

$$\frac{1}{R_1'} = \frac{1}{R_1} + \frac{1}{R_c}$$

Substituting in Eq. (1),

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1} \frac{1 + \dfrac{R_1}{R_c}}{1 + \dfrac{1 + \dfrac{R_2}{R_1} + \dfrac{R_2}{R_c}}{A}}$$

To make $\dfrac{V_o}{V_i} = -\dfrac{R_2}{R_1}$, we have to make

$$\frac{R_1}{R_c} = \frac{1 + \dfrac{R_2}{R_1} + \dfrac{R_2}{R_c}}{A}$$

That is,

$$A\frac{R_1}{R_c} = 1 + G + G\frac{R_1}{R_c}$$

which yields

$$\frac{R_c}{R_1} = \frac{A - G}{1 + G} \qquad \text{Q.E.D}$$

D 2.34 Assuming the op amp to be ideal, it is required to design the circuit shown in Fig. P2.34 to implement a current amplifier with gain $i_L/i_I = 11$ A/A.

(a) Find the required value for R.
(b) What are the input and the output resistance of this current amplifier?
(c) If $R_L = 1$ kΩ and the op amp operates in an ideal manner as long as v_O is in the range ±12 V, what range of i_I is possible?
(d) If the amplifier is fed with a current source having a current of 0.2 mA and a source resistance of 10 kΩ, find i_L.

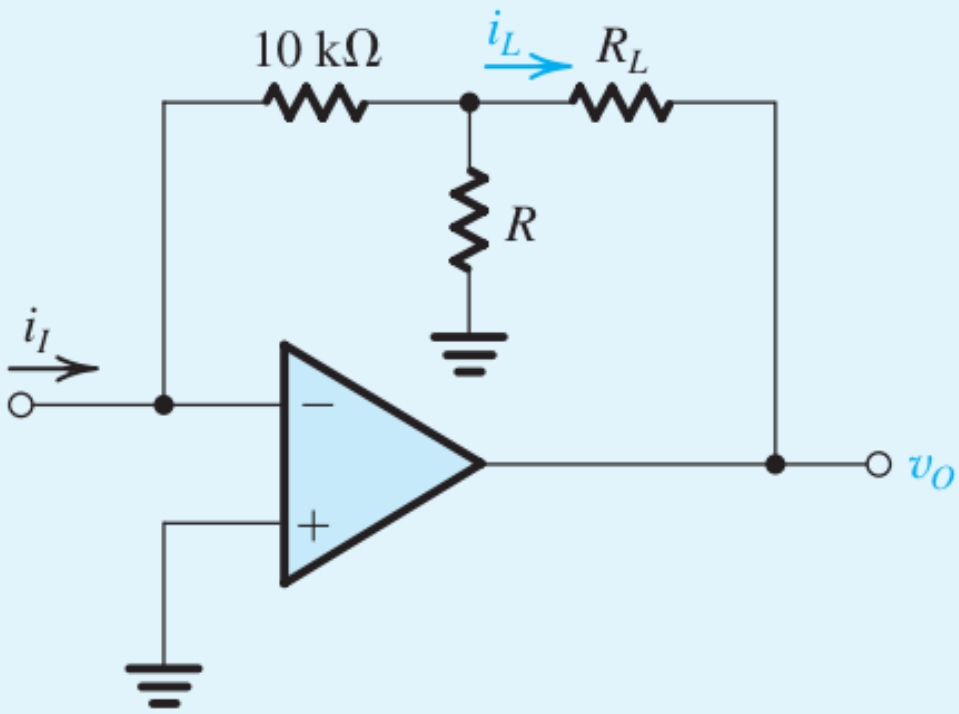
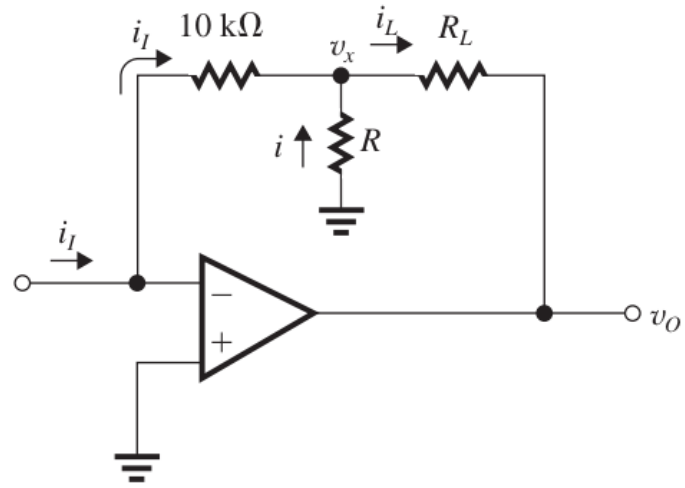


Figure P2.34



(a) $v_x = -i_I \times 10$

$i = -v_x/R = i_I(10/R)$

$$i_L = i_I + i = i_I\left(1 + \frac{10}{R}\right)$$

Thus,

$$\frac{i_L}{i_I} = 1 + \frac{10}{R}$$

For $\frac{i_L}{i_I} = 11 \Rightarrow R = 1$ kΩ.

(b) $R_{\text{in}} = 0$ Ω (because of the virtual ground at the input). $R_o = \infty$ Ω (because i_L is independent of the value of R_L).

(c) If i_I is in the direction shown in the figure above, the maximum allowable value of i_I will be determined by v_O reaching −12 V, at which point

$v_x = -i_{I\max} \times 10$

and

$v_O = -12 = v_x - i_{L\max} \times 1 = -10\, i_{I\max} - 11\, i_{I\max}$

$$\Rightarrow i_{I\max} = \frac{12}{21} = 0.57 \text{ mA}$$

If i_I is in a direction opposite to that shown in the figure, then

$v_x = 10 i_I$

$v_O = v_x + i_L R_L = 10 i_I + 11 i_I = 21 i_I$

The maximum value of i_I will result in $v_O = +12$ V. Thus

$$12 = 21 i_{I\max} \Rightarrow i_{I\max} = \frac{12}{21} = 0.57 \text{ mA}$$

Thus, the allowable range of i_I is

$-0.57 \text{ mA} \le i_I \le +0.57 \text{ mA}$

(d) Since $R_{\text{in}} = 0$, the value of the source resistance will have no effect on the resulting i_L,

$i_L = 0.2 \times 11 = 2.2$ mA

9.2 For the PMOS differential amplifier shown in Fig. P9.2 let $V_{tp} = -0.8$ V and $k_p'W/L = 4$ mA/V^2. Neglect channel-length modulation.

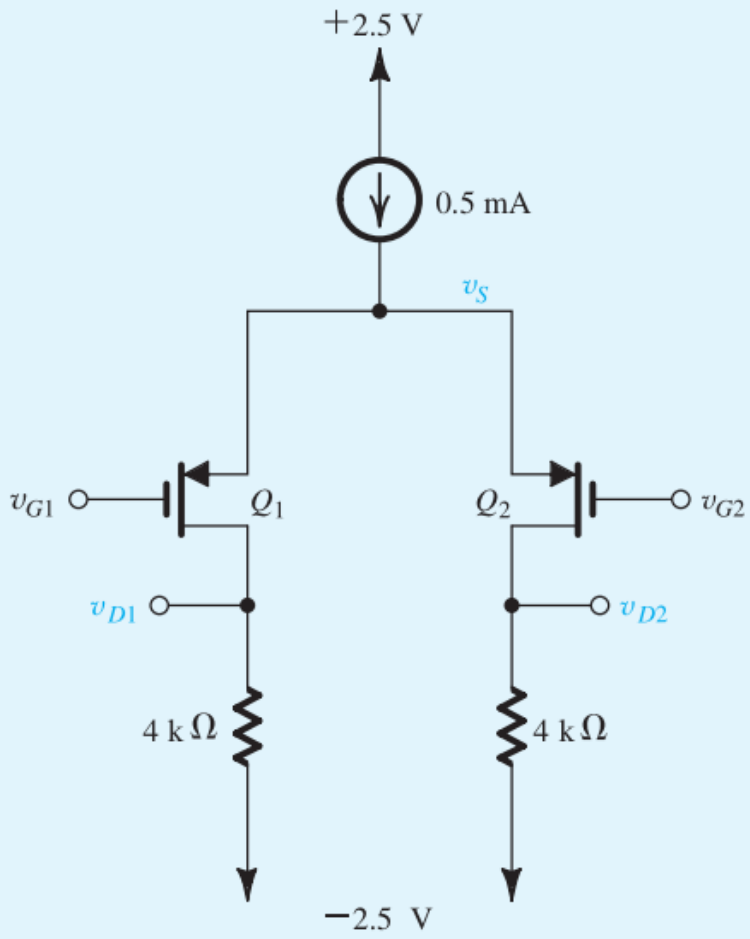


Figure P9.2

(a) For $v_{G1} = v_{G2} = 0$ V, find $|V_{OV}|$ and V_{SG} for each of Q_1 and Q_2. Also find V_S, V_{D1}, and V_{D2}.

(b) If the current source requires a minimum voltage of 0.4 V, find the input common-mode range.

(a) For $v_{G1} = v_{G2} = 0$ V,

$$I_{D1} = I_{D2} = \frac{1}{2} \times 0.5 = 0.25 \text{ mA}$$

$$I_{D1,2} = \frac{1}{2} k_p' \left(\frac{W}{L} \right) |V_{OV}|^2$$

$$0.25 = \frac{1}{2} \times 4 \times |V_{OV}|^2$$

$$\Rightarrow |V_{OV}| = 0.35 \text{ V}$$

$$V_{SG} = |V_{tp}| + |V_{OV}|$$

$$= 0.8 + 0.35 = 1.15 \text{ V}$$

$$V_S = 0 + V_{SG} = +1.15 \text{ V}$$

$$V_{D1} = V_{D2} = -V_{SS} + I_D R_D$$

$$= -2.5 + 0.25 \times 4$$

$$= -1.5 \text{ V}$$

Since for each of Q_1 and Q_2,

$$V_{SD} = 1.15 - (-1.5)$$

$$= 2.65 \text{ V}$$

which is greater than $|V_{OV}|$, Q_1 and Q_2 are operating in saturation as implicitly assumed.

(b) The highest value of V_{CM} is limited by the need to keep a minimum of 0.4 V across the current source, thus

$$V_{CM\,\max} = +2.5 - 0.4 - V_{SG}$$

$$= +2.5 - 0.4 - 1.15 = +0.95 \text{ V}$$

The lowest value of V_{CM} is limited by the need to keep Q_1 and Q_2 in saturation, thus

$$V_{CM\,\min} = V_{D1,2} - |V_{tp}|$$

$$= -1.5 - 0.8 = -2.3 \text{ V}$$

Thus,

$$-2.3 \text{ V} \leq V_{ICM} \leq +0.95 \text{ V}$$

D 9.6 Design the circuit in Fig. P9.6 to obtain a dc voltage of +0.1 V at each of the drains of Q_1 and Q_2 when $v_{G1} = v_{G2} = 0$ V. Operate all transistors at $V_{OV} = 0.15$ V

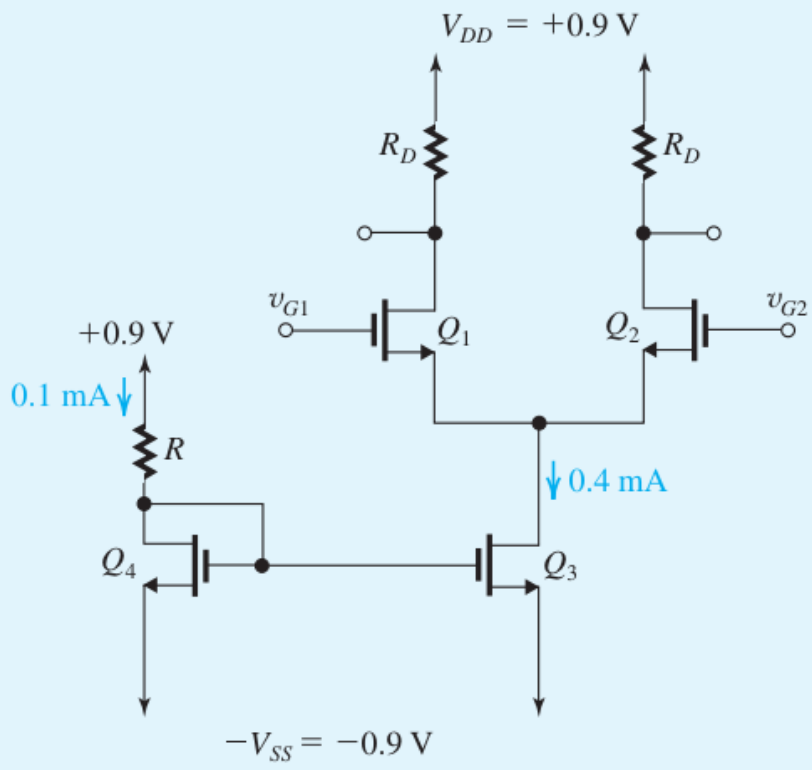


Figure P9.6

and assume that for the process technology in which the circuit is fabricated, $V_{tn} = 0.4$ V and $\mu_n C_{ox} = 400\ \mu\text{A/V}^2$. Neglect channel-length modulation. Determine the values of R, R_D, and the W/L ratios of Q_1, Q_2, Q_3, and Q_4. What is the input common-mode voltage range for your design?

For $v_{G1} = v_{G2} = 0$ V,

$$I_{D1} = I_{D2} = \frac{0.4}{2} = 0.2 \text{ mA}$$

To obtain

$$V_{D1} = V_{D2} = +0.1 \text{ V}$$

$$V_{DD} - I_{D1,2} R_D = 0.1$$

$$0.9 - 0.2 R_D = 0.1$$

$$\Rightarrow R_D = 4 \text{ k}\Omega$$

For Q_1 and Q_2,

$$I_{D1,2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{1,2} V_{OV}^2$$

$$0.2 = \frac{1}{2} \times 0.4\left(\frac{W}{L}\right)_{1,2} \times 0.15^2$$

$$\Rightarrow \left(\frac{W}{L}\right)_{1,2} = 44.4$$

For Q_3,

$$0.4 = \frac{1}{2} \times 0.4 \times \left(\frac{W}{L}\right)_3 \times 0.15^2$$

$$\Rightarrow \left(\frac{W}{L}\right)_3 = 88.8$$

Since Q_3 and Q_4 form a current mirror with $I_{D3} = 4I_{D4}$,

$$\left(\frac{W}{L}\right)_4 = \frac{1}{4}\left(\frac{W}{L}\right)_3 = 22.2$$

$$V_{GS4} = V_{GS3} = V_{tn} + V_{OV} = 0.4 + 0.15$$

$$= 0.55 \text{ V}$$

$$R = \frac{0.9 - (-0.9) - 0.55}{0.1}$$

$$= 12.5 \text{ k}\Omega$$

The lower limit on V_{CM} is determined by the need to keep Q_3 operating in saturation. For this to happen, the minimum value of V_{DS3} is $V_{OV} = 0.15$ V. Thus,

$$V_{ICM\,\text{min}} = -V_{SS} + V_{OV3} + V_{GS1,2}$$

$$= -0.9 + 0.15 + 0.4 + 0.15$$

$$= -0.2 \text{ V}$$

The upper limit on V_{CM} is determined by the need to keep Q_1 and Q_2 in saturation, thus

$$V_{ICM\,\text{max}} = V_{D1,2} + V_{tn}$$

$$= 0.1 + 0.4 = 0.5 \text{ V}$$

Thus,

$$-0.2 \text{ V} \leq V_{ICM} \leq +0.5 \text{ V}$$

D 9.19 Figure P9.19 shows a MOS differential amplifer with the drain resistors R_D implemented using diode-connected PMOS transistors, Q_3 and Q_4. Let Q_1 and Q_2 be matched, and Q_3 and Q_4 be matched.

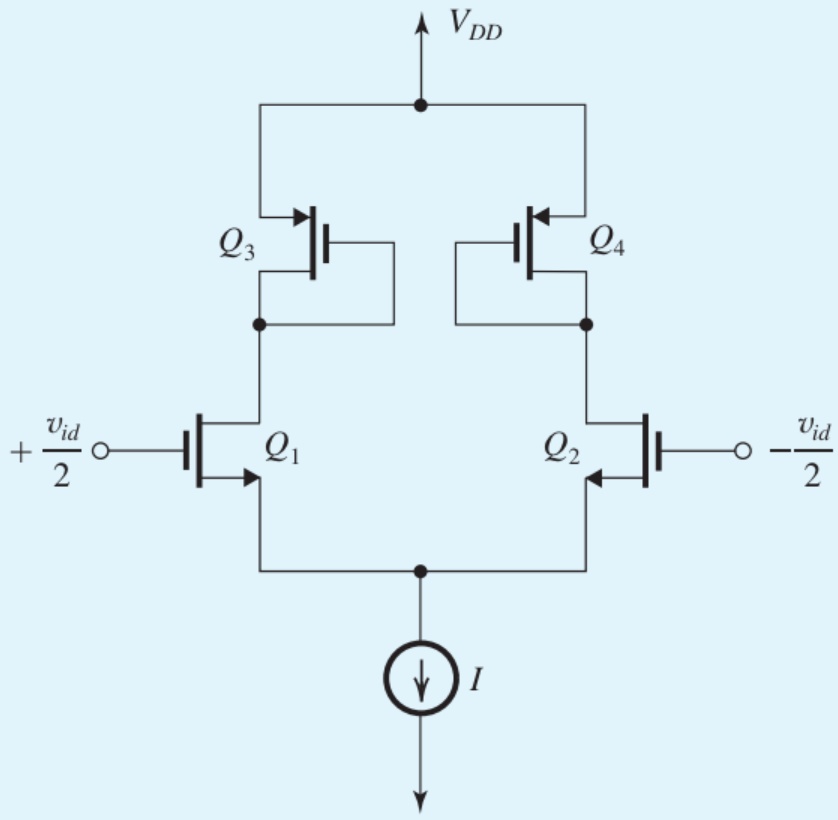
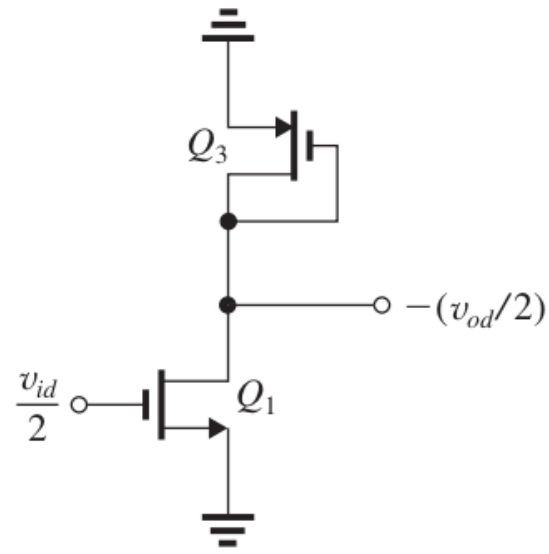


Figure P9.19

(a) Find the differential half-circuit and use it to derive an expression for A_d in terms of $g_{m1,2}$, $g_{m3,4}$, $r_{o1,2}$, and $r_{o3,4}$.

(b) Neglecting the effect of the output resistances r_o, find A_d in terms of μ_n, μ_p, $(W/L)_{1,2}$ and $(W/L)_{3,4}$.

(c) If $\mu_n = 4\mu_p$ and all four transistors have the same channel length, find $(W_{1,2}/W_{3,4})$ that results in $A_d = 10$ V/V.



(a) The figure shows the differential half-circuit. Recalling that the incremental (small-signal) resistance of a diode-connected transistor is given by $\left(\frac{1}{g_m} \parallel r_o\right)$, the equivalent load resistance of Q_1 will be

$$R_D = \frac{1}{g_{m3}} \parallel r_{o3}$$

and the differential gain of the amplifier in Fig. P8.17 will be

$$A_d \equiv \frac{v_{od}}{v_{id}} = g_{m1}\left[\frac{1}{g_{m3}} \parallel r_{o3} \parallel r_{o1}\right]$$

Since both sides of the amplifier are matched, this expression can be written in a more general way as

$$A_d = g_{m1,2}\left[\frac{1}{g_{m3,4}} \parallel r_{o3,4} \parallel r_{o1,2}\right]$$

(b) Neglecting $r_{o1,2}$ and $r_{o3,4}$ (much larger that $1/g_{m3,4}$),

$$A_d \simeq \frac{g_{m1,2}}{g_{m3,4}}$$

$$= \frac{\sqrt{2\mu_n C_{ox}(W/L)_{1,2}(I/2)}}{\sqrt{2\mu_p C_{ox}(W/L)_{3,4}(I/2)}}$$

$$= \sqrt{\frac{\mu_n (W/L)_{1,2}}{\mu_p (W/L)_{3,4}}}$$

(c) $\mu_n = 4\mu_p$ and all channel lengths are equal,

$$A_d = 2\sqrt{\frac{W_{1,2}}{W_{3,4}}}$$

For $A_d = 10$,

$$10 = 2\sqrt{\frac{W_{1,2}}{W_{3,4}}}$$

$$\Rightarrow \frac{W_{1,2}}{W_{3,4}} = 25$$

***9.21** The resistance R_s in the circuit of Fig. P9.20 can be implemented by using a MOSFET operated in the triode region, as shown in Fig. P9.21. Here Q_3 implements R_s, with the value of R_s determined by the voltage V_C at the gate of Q_3.

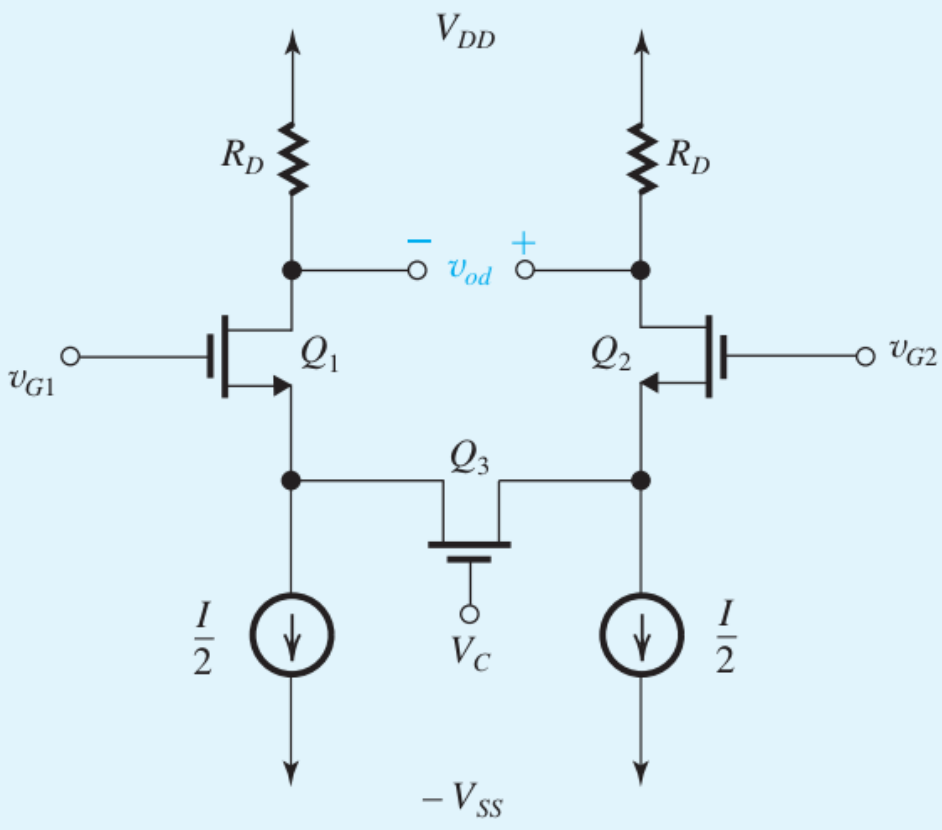


Figure P9.21

(a) With $v_{G1} = v_{G2} = 0$ V, and assuming that Q_1 and Q_2 are operating in saturation, what dc voltages appear at the sources of Q_1 and Q_2? Express these in terms of the overdrive voltage V_{OV} at which each of Q_1 and Q_2 operates, and V_t.

(b) For the situation in (a), what current flows in Q_3? What overdrive voltage V_{OV3} is Q_3 operating at, in terms of V_C, V_{OV}, and V_t?

(c) Now consider the case $v_{G1} = +v_{id}/2$ and $v_{G2} = -v_{id}/2$, where v_{id} is a small signal. Convince yourself that Q_3 now conducts current and operates in the triode region with a small v_{DS}. What resistance r_{DS} does it have, expressed in terms of the overdrive voltage V_{OV3} at which it is operating? This is the resistance R_s. Now if all three transistors have the same W/L, express R_s in terms of V_{OV}, V_{OV3}, and $g_{m1,2}$.

(d) Find V_{OV3} and hence V_C that result in (i) $R_s = 1/g_{m1,2}$; (ii) $R_s = 0.5/g_{m1,2}$.

(a) With $v_{G1} = v_{G2} = 0$,

$$v_{GS1} = v_{GS2} = V_{OV1,2} + V_{tn}$$

Thus

$$V_{S1} = V_{S2} = -(V_{OV1,2} + V_{tn})$$

(b) For the situation in (a), V_{DS} of Q_3 is zero, thus zero current flows in Q_3. Transistor Q_3 will have an overdrive voltage of

$$V_{OV3} = V_C - V_{S1,2} - V_{tn}$$

$$= V_C + (V_{OV1,2} + V_{tn}) - V_{tn}$$

$$= V_C + V_{OV1,2}$$

(c) With $v_{G1} = v_{id}/2$ and $v_{G2} = -v_{id}/2$ where v_{id} is a small signal, a small signal will appear between drain and source of Q_3. Transistor Q_3 will be operating in the triode region and its drain-source resistance r_{DS} will be given by

$$r_{DS} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3 V_{OV3}}$$

Thus,

$$R_s = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3 V_{OV3}}$$

Now,

$$g_{m1,2} = (\mu_n C_{ox})\left(\frac{W}{L}\right)_{1,2} V_{OV1,2}$$

$$g_{m3} = (\mu_n C_{ox})\left(\frac{W}{L}\right)_3 V_{OV3}$$

For $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_{1,2}$,

$$\mu_n C_{ox}\left(\frac{W}{L}\right) = \frac{g_{m1,2}}{V_{OV1,2}}$$

Thus,

$$R_s = \frac{1}{\frac{g_{m1,2}}{V_{OV1,2}} \times V_{OV3}} = \frac{1}{g_{m1,2}} \frac{V_{OV1,2}}{V_{OV3}}$$

(d) (i) $R_s = \dfrac{1}{g_{m1,2}}$

$$V_{OV3} = V_{OV1,2}$$

But

$$V_{OV3} = V_C + V_{OV1,2}$$

$$\Rightarrow V_C = 0$$

(ii) $R_s = \dfrac{0.5}{g_{m1,2}}$

$$\Rightarrow V_{OV3} = 2\, V_{OV1,2}$$

But

$$V_{OV3} = V_C + V_{OV1,2}$$

$$\Rightarrow V_C = V_{OV1,2}$$

9.47 For each of the emitter-degenerated differential amplifiers shown in Fig. P9.47, find the differential half-circuit and derive expressions for the differential gain A_d and differential input resistance R_{id}. For each circuit, what dc voltage appears across the bias current source(s) in the quiescent state (i.e., with $v_{id} = 0$)? Hence, which of the two circuits will allow a larger negative V_{CM}?

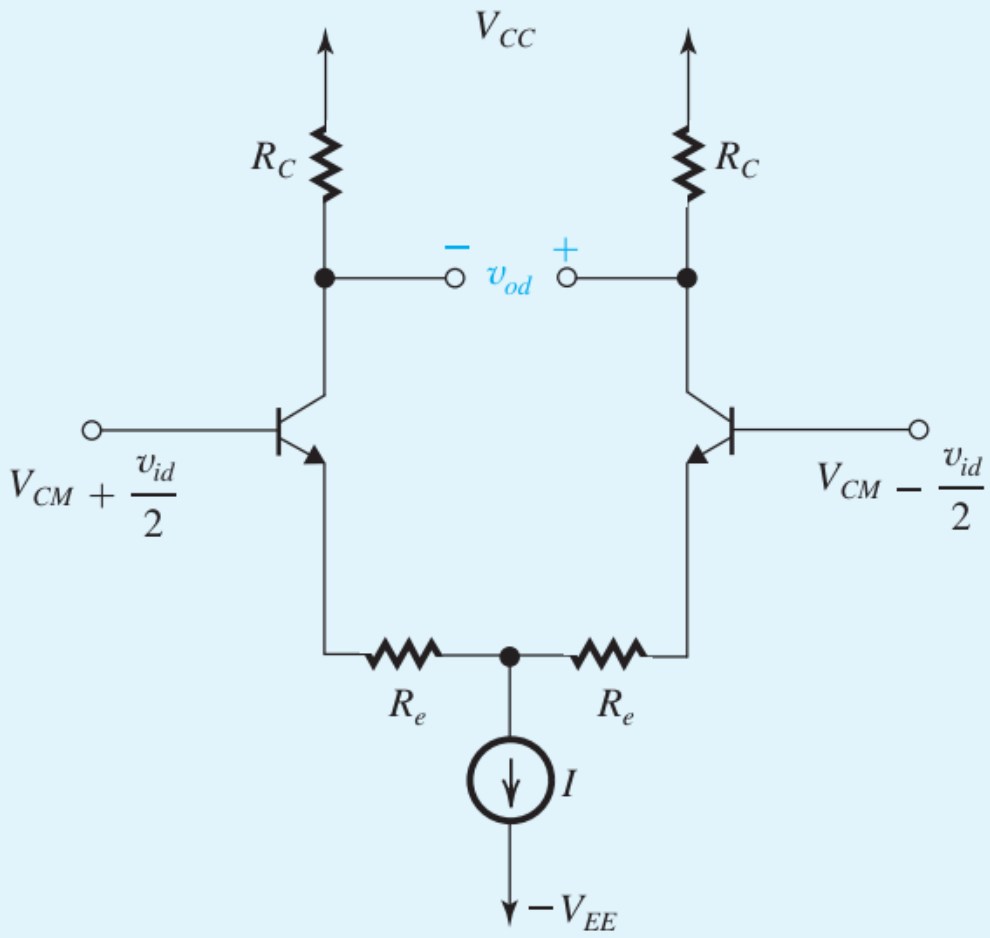
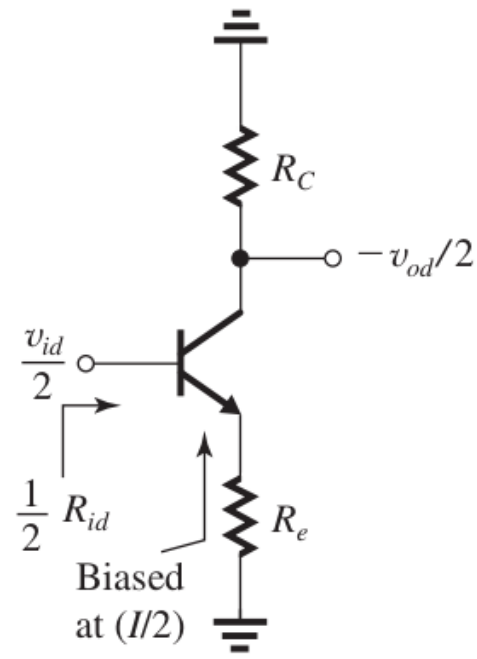


Figure P9.47



Both circuits have the same differential half-circuit shown in the figure. Thus, for both

$$A_d = \frac{\alpha R_C}{r_e + R_e}$$

$$R_{id} = (\beta + 1)(2r_e + 2R_e)$$

$$= 2(\beta + 1)(r_e + R_e)$$

With $v_{id} = 0$, the dc voltage appearing at the top end of the bias current source will be

(a) $V_{CM} - V_{BE} - \left(\frac{I}{2}\right)R_C$

(b) $V_{CM} - V_{BE}$

Since circuit (b) results in a larger voltage across the current source and given that the minimum value of V_{CM} is limited by the need to keep a certain specified minimum voltage across the current source, we see that circuit (b) will allow a larger negative V_{CM}.

SIM D *9.57 The differential amplifier in Fig. P9.57 utilizes a resistor R_{SS} to establish a 1-mA dc bias current. Note that this amplifier uses a single 5-V supply and thus the dc common-mode voltage V_{CM} cannot be zero. Transistors Q_1 and Q_2 have $k_n'W/L = 2.5\ \text{mA/V}^2$, $V_t = 0.7$ V, and $\lambda = 0$.

(a) Find the required value of V_{CM}.
(b) Find the value of R_D that results in a differential gain A_d of 8 V/V.
(c) Determine the dc voltage at the drains.
(d) Determine the single-ended-output common-mode gain $\Delta V_{D1}/\Delta V_{CM}$. (*Hint:* You need to take $1/g_m$ into account.)

(e) Use the common-mode gain found in (d) to determine the change in V_{CM} that results in Q_1 and Q_2 entering the triode region.

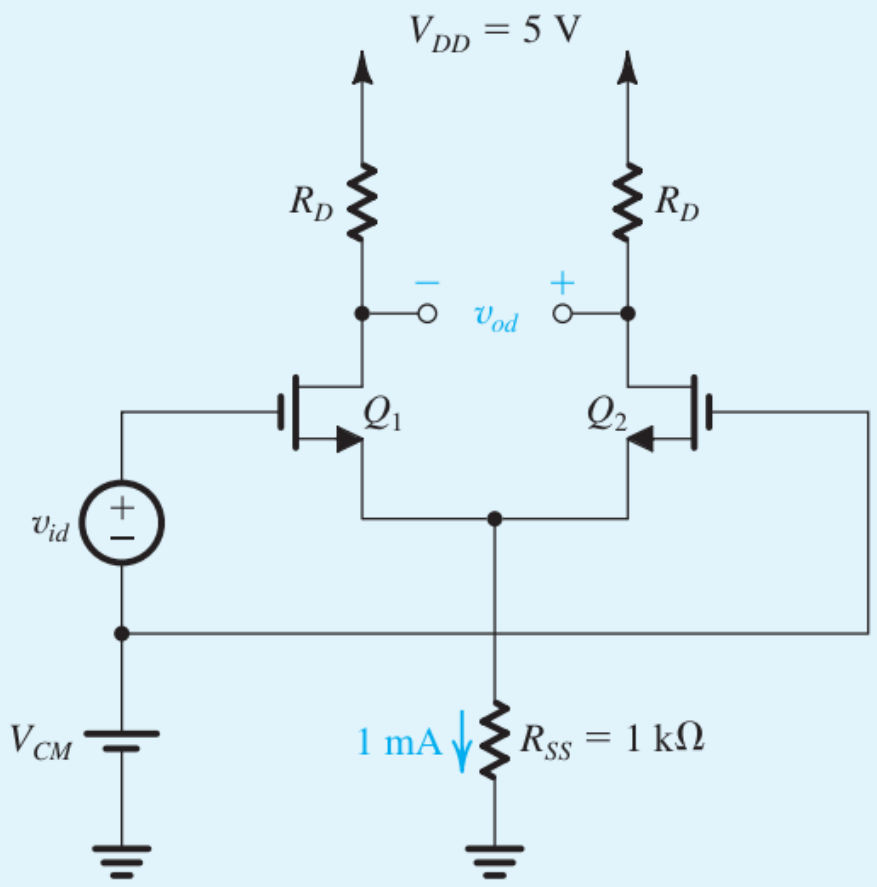


Figure P9.57

(a) Assume $v_{id} = 0$ and the two sides of the differential amplifier are matched. Thus,

$$I_{D1} = I_{D2} = 0.5\ \text{mA}$$

$$I_{D1,2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{OV}^2$$

$$0.5 = \frac{1}{2} \times 2.5 \times V_{OV}^2$$

$$\Rightarrow V_{OV} = 0.632\ \text{V}$$

$$V_{CM} = V_{GS} + 1\ \text{mA} \times R_{SS}$$

$$= V_t + V_{OV} + 1 \times R_{SS}$$

$$= 0.7 + 0.632 + 1$$

$$= 2.332\ \text{V}$$

(b) $$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \times 0.5}{0.632} = 1.58\ \text{mA/V}$$

$$A_d = g_m R_D$$

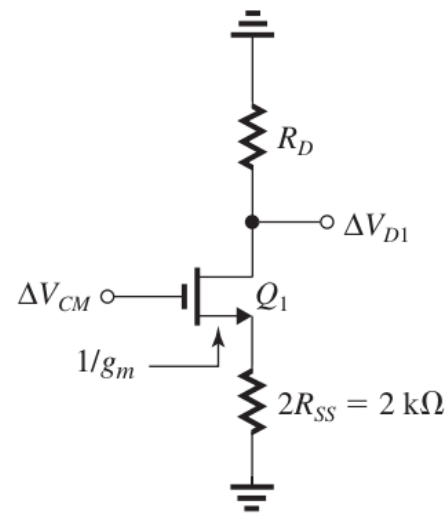
$$8 = 1.38 \times R_D$$

$$\Rightarrow R_D = 5.06\ \text{k}\Omega$$

(c) $$V_{D1} = V_{D2} = V_{DD} - I_D R_D$$

$$= 5 - 0.5 \times 5.06 = 2.47\ \text{V}$$

(d)



The figure shows the common-mode half-circuit,

$$\frac{\Delta V_{D1}}{\Delta V_{CM}} = -\frac{R_D}{\frac{1}{g_m} + 2R_{SS}}$$

$$\frac{\Delta V_{D1}}{\Delta V_{CM}} = -\frac{5.06}{\frac{1}{1.58} + 2} = -1.92\ \text{V/V}$$

(e) For Q_1 and Q_2 to enter the triode region

$$V_{CM} + \Delta V_{CM} = V_t + V_{D1} + \Delta V_{D1}$$

Substituting $V_{CM} = 2.332$, $V_t = 0.7$ V, $V_{D1} = 2.47$ V, and $\Delta V_{D1} = -1.92\Delta V_{CM}$ results in

$$2.332 + \Delta V_{CM} = 0.7 + 2.47 - 1.92\Delta V_{CM}$$

$$\Rightarrow \Delta V_{CM} = 0.287\ \text{V}$$

With this change, $V_{CM} = 2.619$ V and $V_{D1,2} = 1.919$ V; thus $V_{CM} = V_t + V_{D1,2}$.

9.81 One approach to "offset correction" involves the adjustment of the values of R_{C1} and R_{C2} so as to reduce the differential output voltage to zero when both input terminals are grounded. This offset-nulling process can be accomplished by utilizing a potentiometer in the collector circuit, as shown in Fig. P9.81. We wish to find the potentiometer setting, represented by the fraction x of its value connected in series with R_{C1}, that is required for nulling the output offset voltage that results from:

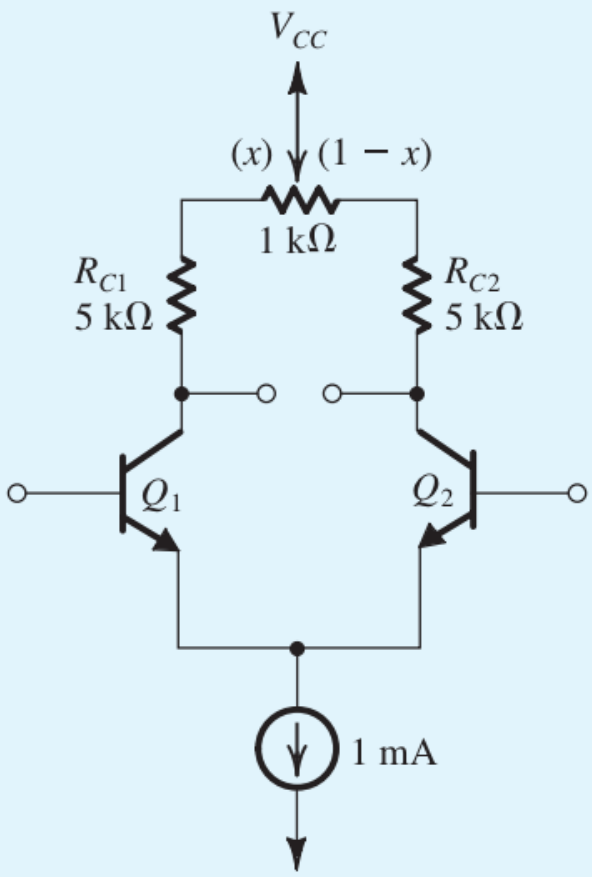


Figure P9.81

(a) R_{C1} being 4% higher than nominal and R_{C2} 4% lower than nominal

(b) Q_1 having an area 5% larger than nominal, while Q_2 has area 5% smaller than nominal.

(a) $R_{C1} = 1.04 \times 5 = 5.20\ \text{k}\Omega$

$R_{C2} = 0.96 \times 5 = 4.80\ \text{k}\Omega$

To equalize the total resistance in each collector, we adjust the potentiometer so that

$$R_{C1} + x \times 1\ \text{k}\Omega = R_{C2} + (1-x) \times 1\ \text{k}\Omega$$

$$5.2 + x = 4.8 + 1 - x$$

$$\Rightarrow x = 0.3\ \text{k}\Omega$$

(b) If the area of Q_1 and hence I_{S1} is 5% larger than nominal, then we have

$$I_{S1} = 1.05 I_S$$

and the area of Q_2 and hence I_{S2} is 5% smaller than nominal,

$$I_{S2} = 0.95 I_S$$

Thus,

$$I_{E1} = 0.5 \times 1.05 = 0.525\ \text{mA}$$

$$I_{E2} = 0.5 \times 0.95 = 0.475\ \text{mA}$$

Assuming $\alpha \simeq 1$, we obtain

$$I_{C1} = 0.525\ \text{mA} \quad I_{C2} = 0.475\ \text{mA}$$

To reduce the resulting offset to zero, we adjust the potentiometer so that

$$V_{C1} = V_{C2}$$

$$\Rightarrow V_{CC} - (R_{C1} + x) I_{C1} = V_{CC} - (R_{C2} + 1 - x) I_{C2}$$

$$I_{C1}(R_{C1} + x) = I_{C2}(R_{C2} + 1 - x)$$

$$0.525(5 + x) = 0.475(5 + 1 - x)$$

$$\Rightarrow x = 0.225$$

D 10.5 The amplifier in Fig. P10.5 is biased to operate at $g_m = 2$ mA/V. Neglect r_o.

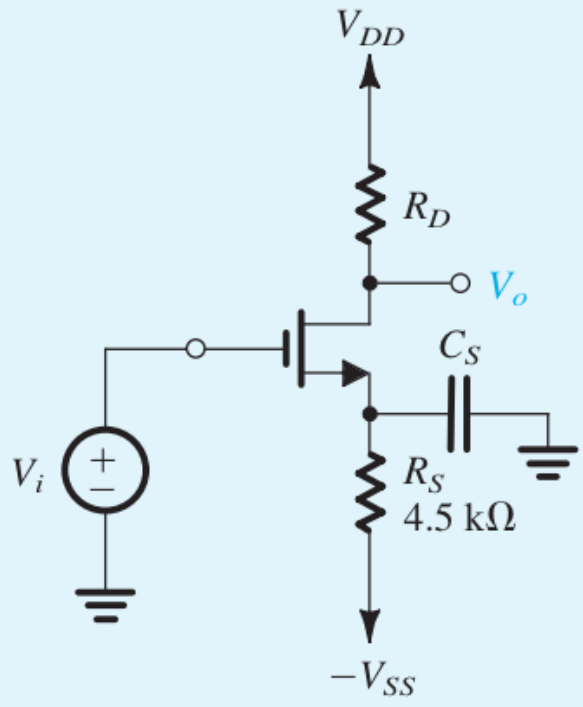


Figure P10.5

(a) Determine the value of R_D that results in a midband gain of −20 V/V.

(b) Determine the value of C_S that results in a pole frequency of 100 Hz.

(c) What is the frequency of the transmission zero introduced by C_S?

(d) Give an approximate value for the 3-dB frequency f_L.

(e) Sketch a Bode plot for the gain of this amplifier. What does the plot tell you about the gain at dc? Does this make sense? Why or why not?

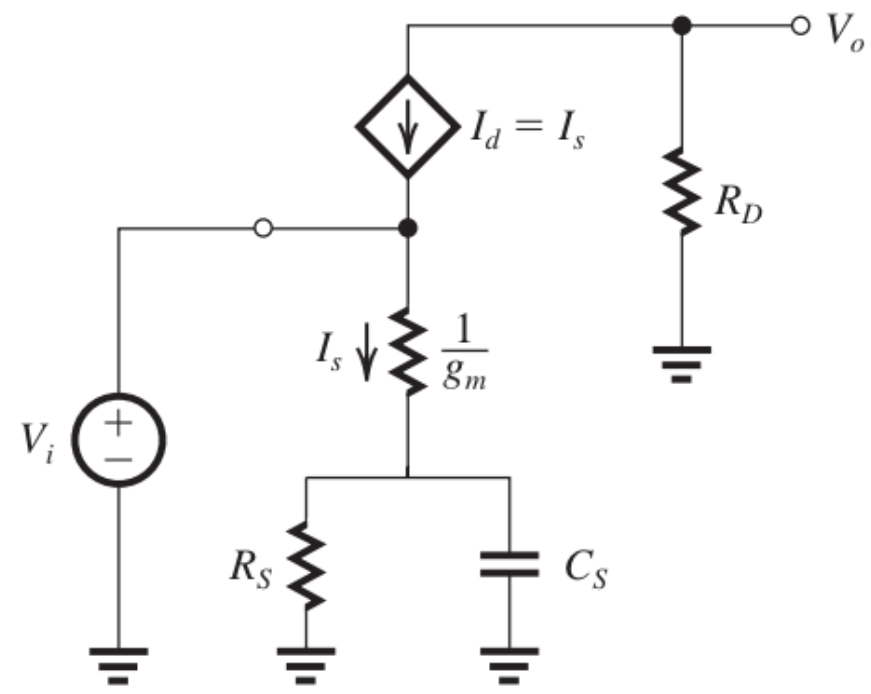


Figure 1

Replacing the MOSFET with its T model results in the circuit shown in Fig. 1.

(a) $$A_M \equiv \frac{V_o}{V_i} = -g_m R_D$$

$$-20 = -2 \times R_D$$

$$\Rightarrow R_D = 10 \text{ k}\Omega$$

(b) $$f_P = \frac{g_m + 1/R_S}{2\pi C_S}$$

$$100 = \frac{2 \times 10^{-3} + (1/4.5 \times 10^3)}{2\pi C_S}$$

$$\Rightarrow C_S = 3.53 \ \mu\text{F}$$

(c) $$f_Z = \frac{1}{2\pi C_S R_S} =$$

$$\frac{1}{2\pi \times 3.53 \times 10^{-6} \times 4.5 \times 10^3} = 10 \text{ Hz}$$

(d) Since $f_P \gg f_Z$,

$$f_L \simeq f_P = 100 \text{ Hz}$$

(e) The Bode plot for the gain is shown in Fig. 2.

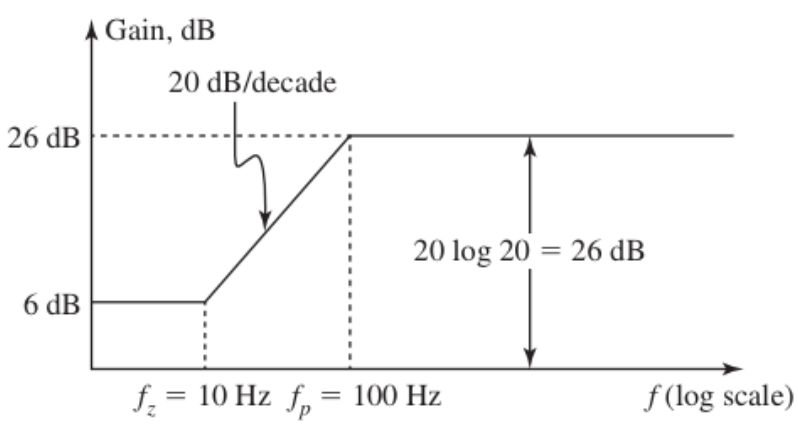


Figure 2

Observe that the dc gain is 6 dB, i.e. 2 V/V. This makes perfect sense since from Fig. 1 we see that at dc, capacitor C_S behaves as open circuit and the gain becomes

$$\text{DC gain} = -\frac{R_D}{\frac{1}{g_m} + R_S} = -\frac{10 \text{ k}\Omega}{\left(\frac{1}{2} + 4.5\right)}$$

$$= -2 \text{ V/V}$$

10.15 Starting from the expression of f_T for a MOSFET,

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

and making the approximation that $C_{gs} \gg C_{gd}$ and that the overlap component of C_{gs} is negligibly small, show that

$$f_T \simeq \frac{1.5}{\pi L}\sqrt{\frac{\mu_n I_D}{2C_{ox}WL}}$$

Thus note that to obtain a high f_T from a given device, it must be operated at a high current. Also note that faster operation is obtained from smaller devices.

9.15 $f_T = \dfrac{g_m}{2\pi(C_{gs} + C_{gd})}$

For $C_{gs} \gg C_{gd}$

$$f_T \simeq \frac{g_m}{2\pi C_{gs}} \qquad (1)$$

$$C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox}$$

If the overlap component ($WL_{ov}C_{ox}$) is small, we get

$$C_{gs} \simeq \frac{2}{3}WLC_{ox} \qquad (2)$$

The transconductance g_m is given by

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)I_D} \qquad (3)$$

Substituting from (2) and (3) into (1), we get

$$f_T = \frac{\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)I_D}}{2\pi \times \frac{2}{3}WLC_{ox}}$$

$$= \frac{1.5}{\pi L}\sqrt{\frac{\mu_n I_D}{2C_{ox}WL}} \qquad \text{Q.E.D.}$$

We observe that for a given device, f_T is proportional to $\sqrt{I_D}$; thus to obtain faster operation the MOSFET is operated at a higher I_D.

Also, we observe that f_T is inversely proportional to $L\sqrt{WL}$; thus faster operation is obtained from smaller devices.

10.20 An *npn* transistor is operated at $I_C = 1$ mA and $V_{CB} = 2$ V. It has $\beta_0 = 100$, $V_A = 50$ V, $\tau_F = 30$ ps, $C_{je0} = 20$ fF, $C_{\mu 0} = 30$ fF, $V_{0c} = 0.75$ V, $m_{CBJ} = 0.5$, and $r_x = 100\ \Omega$. Sketch the complete hybrid-π model, and specify the values of all its components. Also, find f_T.

9.19 $r_x = 100\ \Omega$

$$g_m = \frac{I_C}{V_T} = \frac{1\text{ mA}}{0.025\text{ V}} = 40\text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{40} = 2.5\text{ k}\Omega$$

$$r_o = \frac{V_A}{I_C} = \frac{50}{1} = 50\text{ k}\Omega$$

$$C_{de} = \tau_F g_m = 30 \times 10^{-12} \times 40 \times 10^{-3} = 1.2\text{ pF}$$

$$C_{je0} = 20\text{ pF}$$

$$C_\pi = C_{de} + 2C_{je0} = 1.2 + 2 \times 0.02 = 1.24\text{ pF}$$

$$C_\mu = \frac{C_{je0}}{\left(1 + \frac{V_{CB}}{V_{0c}}\right)^m}$$

$$C_\mu = \frac{20}{\left(1 + \frac{2}{0.75}\right)^{0.5}} \text{ ~~= 10.4 fF~~}$$

* $C_\mu = \frac{30}{\left(1 + \frac{2}{0.75}\right)^{0.5}}$

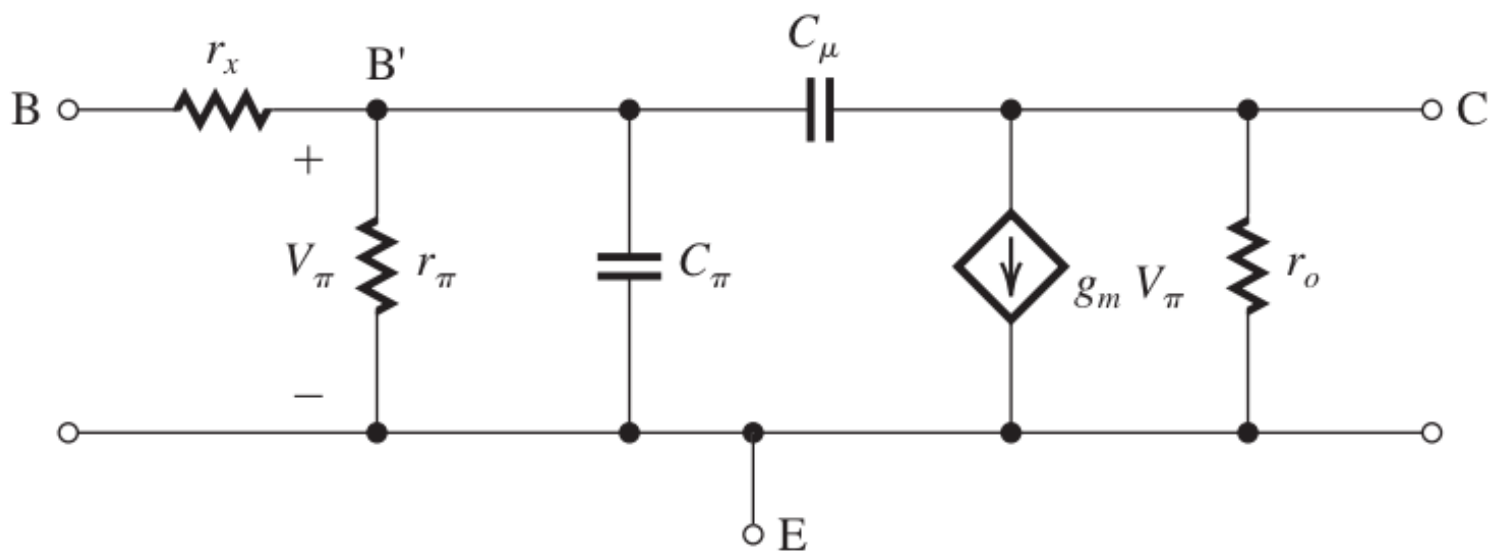
$= 15.667$ fF

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

$$= \frac{40 \times 10^{-3}}{2\pi(1.24 + 0.01) \times 10^{-12}}$$

~~= 5.1 GHz~~ 5.07 GHz

This figure belongs to Problem 9.18.



10.32 A discrete MOSFET common-source amplifier has $R_G = 2$ MΩ, $g_m = 5$ mA/V, $r_o = 100$ kΩ, $R_D = 20$ kΩ, $C_{gs} = 3$ pF, and $C_{gd} = 0.5$ pF. The amplifier is fed from a voltage source with an internal resistance of 500 kΩ and is connected to a 20-kΩ load. Find:

(a) the overall midband gain A_M
(b) the upper 3-dB frequency f_H
(c) the frequency of the transmission zero, f_Z.

9.29 (a) $A_M = -\dfrac{R_G}{R_G + R_{\text{sig}}} g_m R'_L$

where

$R'_L = R_D \parallel R_L \parallel r_o$

$= 20\ \text{k}\Omega \parallel 20\ \text{k}\Omega \parallel 100\ \text{k}\Omega$

$= 9.1\ \text{k}\Omega$

$A_M = -\dfrac{2\ \text{M}\Omega}{2\ \text{M}\Omega + 0.5\ \text{M}\Omega} \times 5 \times 9.1$

$= -36.4\ \text{V/V}$

(b) $f_H = \dfrac{1}{2\pi C_{\text{in}} R'_{\text{sig}}}$

where

$C_{\text{in}} = C_{gs} + C_{gd}(1 + g_m R'_L)$

$= 3 + 0.5(1 + 5 \times 9.1)$

$= 26.25\ \text{pF}$

and

$R'_{\text{sig}} = R_{\text{sig}} \parallel R_G$

$= 500\ \text{k}\Omega \parallel 2000\ \text{k}\Omega$

$= 400\ \text{k}\Omega$

Thus,

$f_H = \dfrac{1}{2\pi \times 26.25 \times 10^{-12} \times 400 \times 10^3}$

$= 15.2\ \text{kHz}$

(c) $f_Z = \dfrac{g_m}{2\pi C_{gd}}$

$= \dfrac{5 \times 10^{-3}}{2\pi \times 0.5 \times 10^{-12}}$

$= 1.6\ \text{GHz}$

10.52 An amplifier with a dc gain of 60 dB has a single-pole, high-frequency response with a 3-dB frequency of 100 kHz.

(a) Give an expression for the gain function $A(s)$.
(b) Sketch Bode diagrams for the gain magnitude and phase.
(c) What is the gain–bandwidth product?
(d) What is the unity-gain frequency?
(e) If a change in the amplifier circuit causes its transfer function to acquire another pole at 1 MHz, sketch the resulting gain magnitude and specify the unity-gain frequency. Note that this is an example of an amplifier with a unity-gain bandwidth that is different from its gain–bandwidth product.

9.47 (a) $A(s) = 1000\dfrac{1}{1 + s/(2\pi \times 10^5)}$

(b)

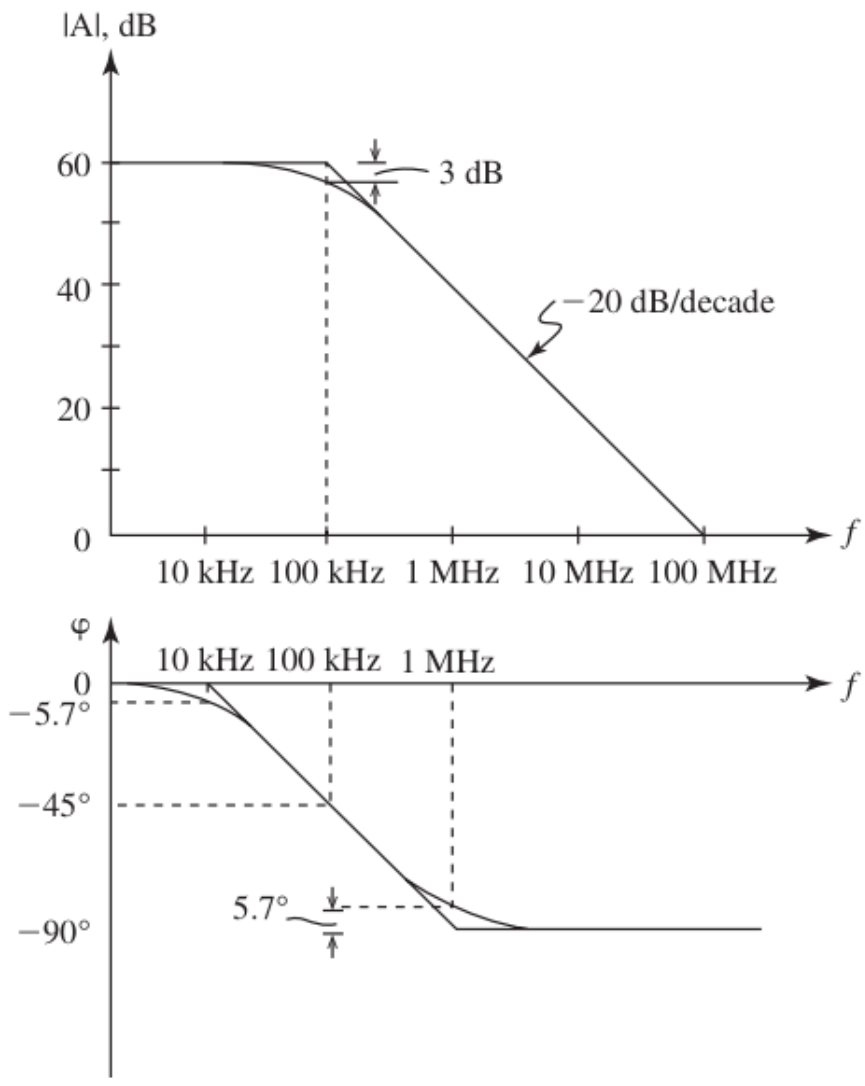


Figure 1

Figure 1 shows the Bode plot for the gain magnitude and phase.

(c) GB = 1000 × 100 kHz = 100 MHz

(d) The unity-gain frequency f_t is

$f_t = 100$ MHz

(e)

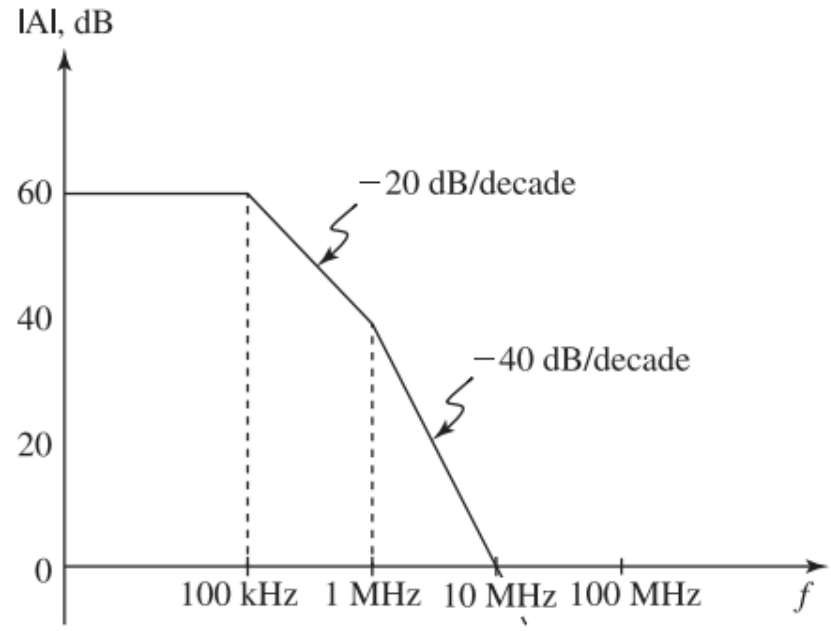


Figure 2

Figure 2 shows the magnitude response when a second pole at 1 MHz appears in the transfer function. The unity-gain frequency f_t now is

$f_t = 10$ MHz

which is different from the gain-bandwidth product,

GB = 100 MHz