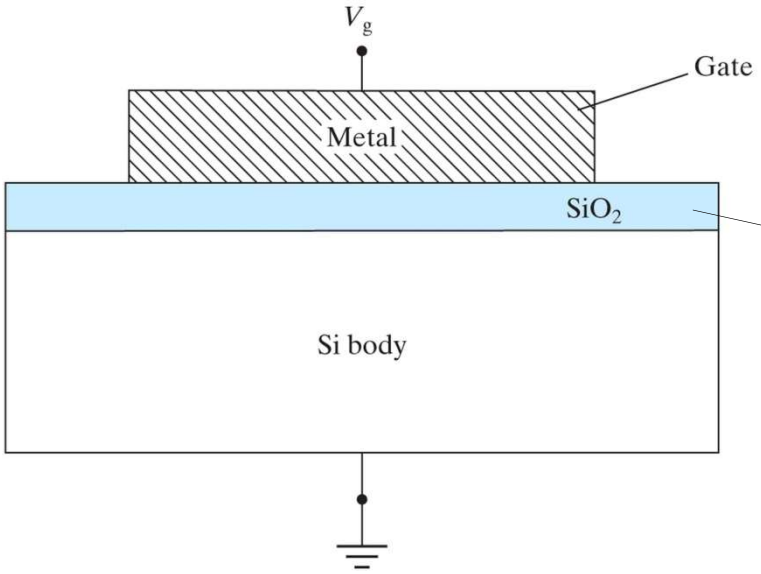
Chapter 5

MOS Capacitor

OBJECTIVES

1. **Understand the modern MOS structures.**
2. **Understand the concepts of surface depletion, threshold, and inversion.**
3. **Understand the MOS capacitor C-V**
4. **Build the foundation for understanding the MOSFETs.**

MOS (Metal-Oxide-Semiconductor) Capacitor

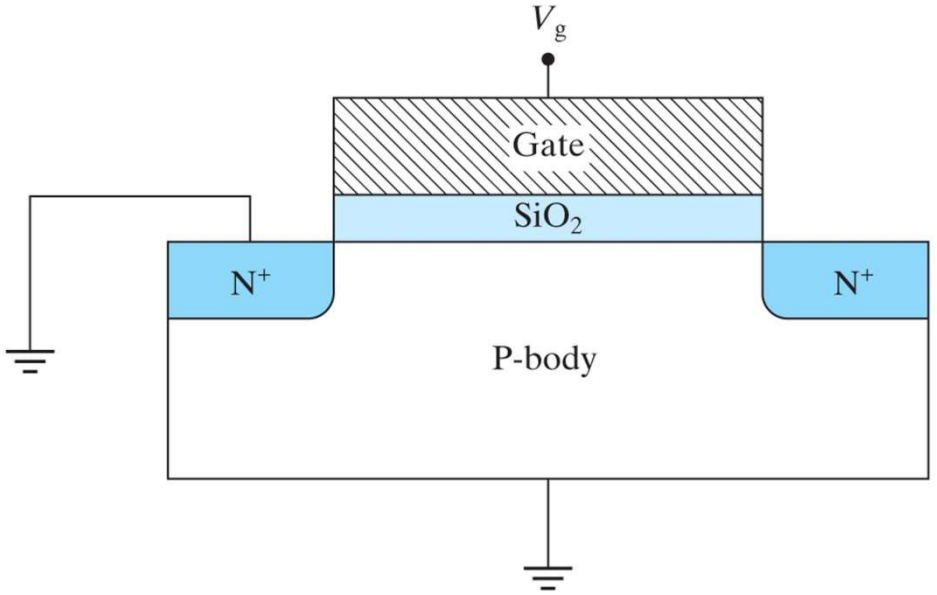


The MOS capacitor

Al (before 1970),
Heavily doped polycrystalline silicon (after 1970)
; withstanding high T without reacting with SiO_2
Various metals (after 2008)

Thickness: as thin as ~ 1.5 nm
Silicon dioxide (almost perfect insulator)
Advanced dielectrics (after 2008)

The MOS capacitor: the simplest of MOS devices and the structural heart of all MOS devices including MOSFETs.



An MOS transistor is an MOS capacitor with PN junctions at two ends.

Revisiting Chapter 4

Metal-Semiconductor Contact

Part III: Metal-Semiconductor Junction

Two different types of MS contacts:

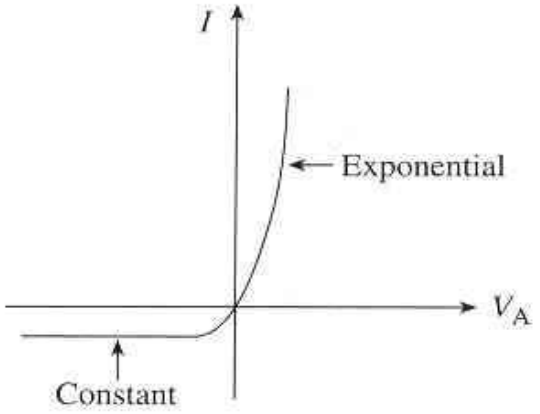
(1) Rectifying contacts (Schottky contact)

- Similar I-V characteristics to those of P-N junctions
- Operates with single type of carrier (majority carrier)

→ Simple to fabricate

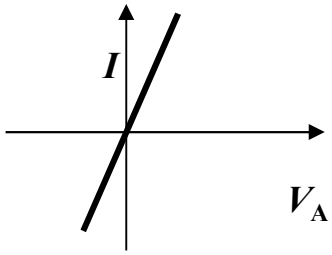
→ No stored-charge effect

→ Switching speed is much higher than that of p-n junction diodes



(2) Ohmic contacts

- Linear I-V characteristics
- To carry current into and out of the semiconductor device



❑ Metal-Semiconductor Junctions (n-type S)

Rectifying contacts (Schottky contact) : $\Phi_M > \Phi_S$

Vacuum level, E_0

- the minimum energy for electrons to be completely free itself from the material.

Workfunction, $q\Phi$ [eV]

- The difference between vacuum level and Fermi-level of materials.

$q\Phi_m$ is an invariant property of metal.
It is the minimum energy required to free up electrons from metal.

(Mg:3.66 eV, Al:4.3eV, Au:4.8eV, Ni:5.15eV)

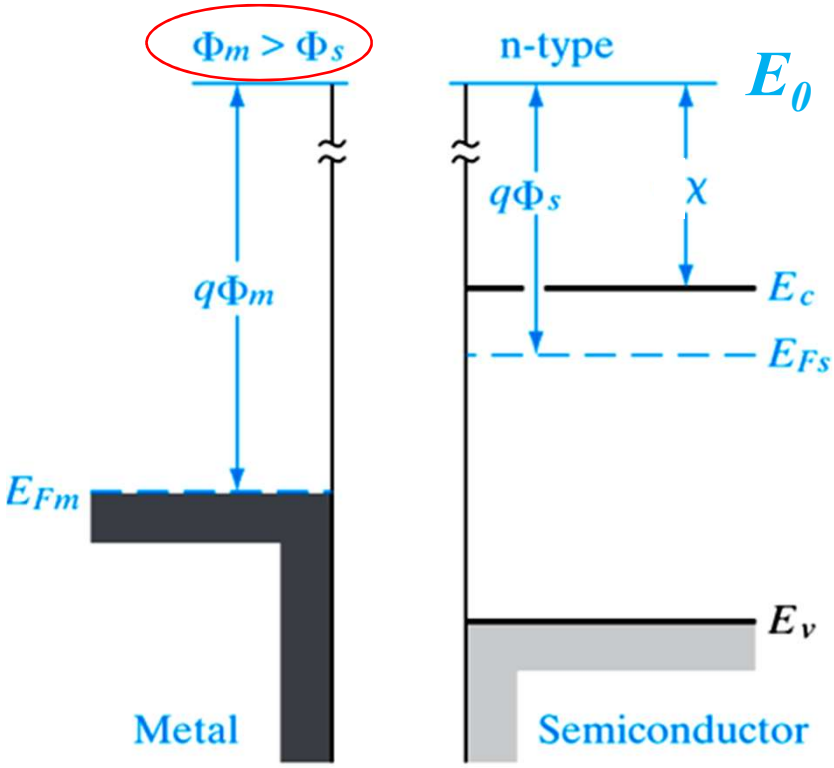
$q\Phi_s$ depends on the doping.

$$q\Phi_s = \chi + (E_C - E_F)_{FB}$$

χ: Fixed material constant

$(E_C - E_F)_{FB}$: Variable by doping concentration

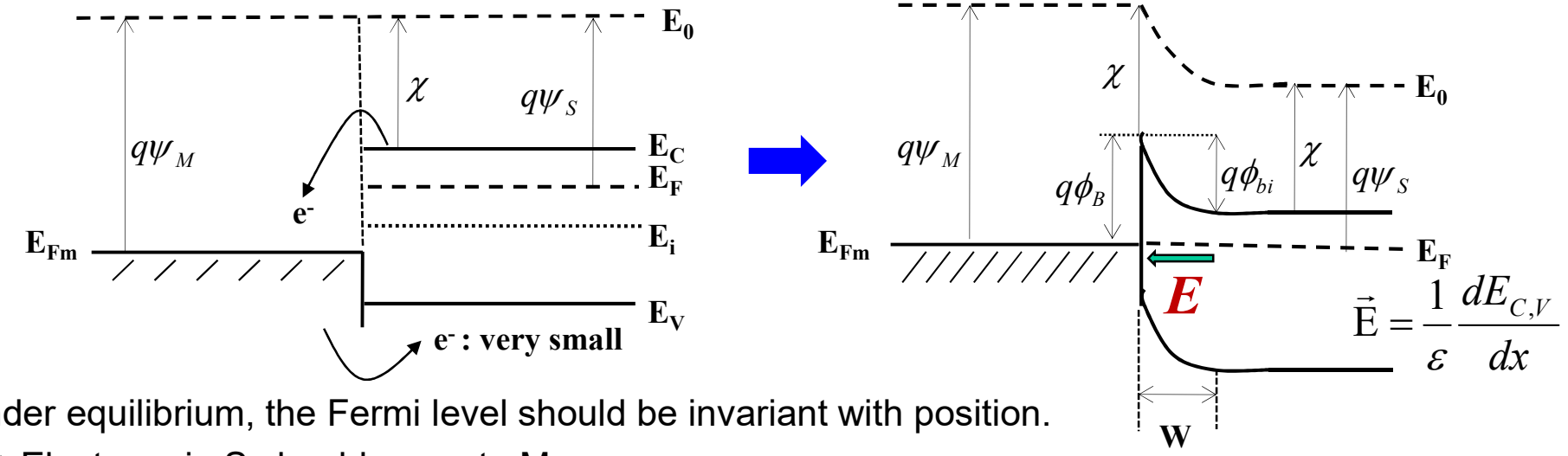
Flat band=zero field condition



where $\chi = (E_0 - E_C)|_{SURFACE}$ is a fundamental property of the semiconductor, so-called electron affinity.

(Example: χ = 4.0 eV, 4.05 eV and 4.07 eV for Ge, Si and GaAs, respectively)

$\Phi_M > \Phi_S$



$$\vec{E} = \frac{1}{\varepsilon}\frac{dE_{C,V}}{dx}$$

Under equilibrium, the Fermi level should be invariant with position.

⟹ Electrons in S should move to M.

⟹ Net loss of electrons from S creates a surface depletion region and growing barrier to electron transfer from the S to M until the Fermi level become flat.

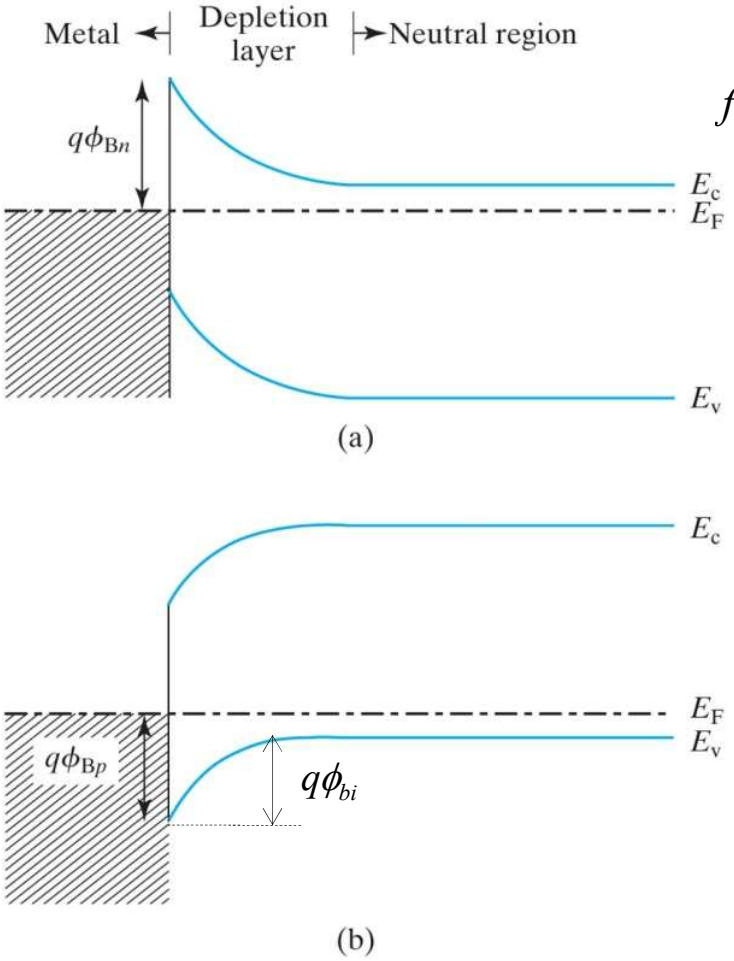
(To align two E_F, the electrostatic potential of S must be raised (i.e. the electron energies must be lowered) relative to that of the metal.)

$$Schottky\ barrier\ height,\ \phi_B = (\psi_M - \chi/q)$$; Invariant !

$$Built-in\ potential,\ \phi_{bi} = (\psi_M - \psi_S) = [\phi_B - \frac{1}{q}(E_C - E_F)_{FB}]$$

; prevents further net electron diffusion from S to M.

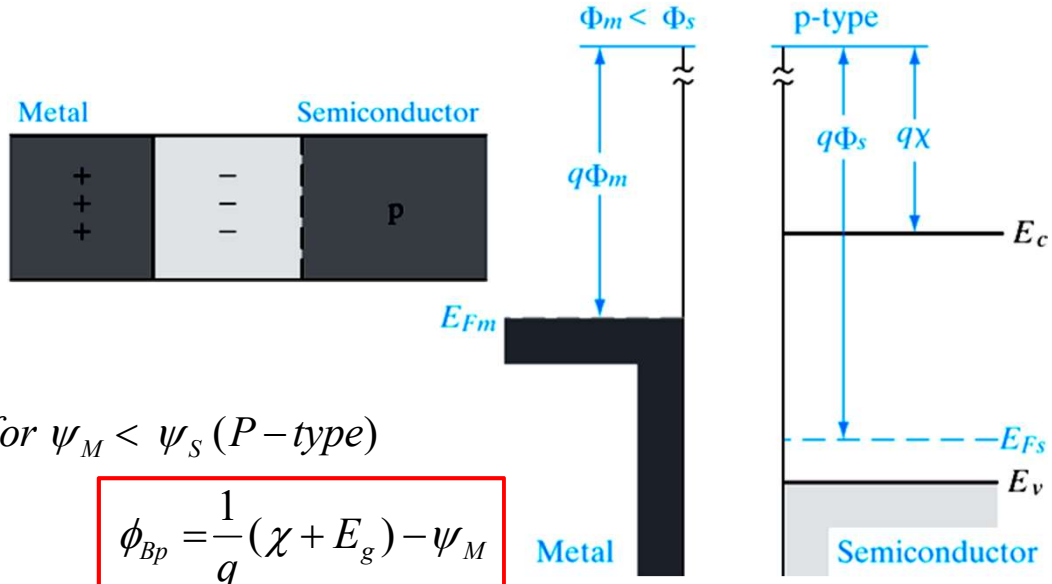
; can be decreased or increased by the application of either forward- or reverse-bias voltage.



$$for\ \psi_M > \psi_S\ (N-type)$$

$$\phi_{Bn} = (\psi_M - \chi/q),\ called\ "Affinity\ Rule"$$

$$\phi_{bi} = (\psi_M - \psi_S) = [\phi_B - \frac{1}{q}(E_C - E_F)_{FB}]$$



$$for\ \psi_M < \psi_S\ (P-type)$$

$$\phi_{Bp} = \frac{1}{q}(\chi + E_g) - \psi_M$$

$$\phi_{bi} = \psi_M - \psi_S = \psi_M - [\frac{\chi}{q} + \frac{E_g}{q} - \frac{(E_F - E_V)}{q}] : negative$$

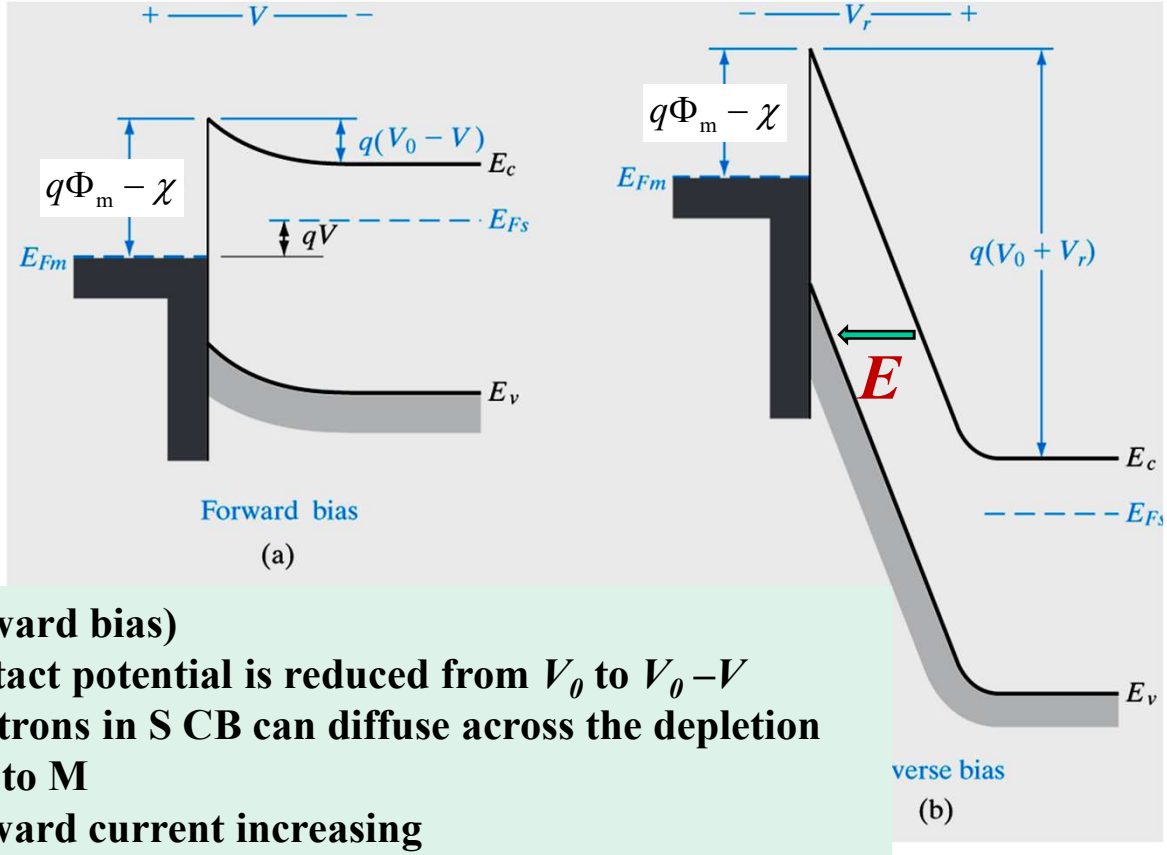
$$\phi_B = \begin{cases} \phi_{Bn} : barrier\ against\ electron\ flow\ in\ N\ type \\ \phi_{Bp} : \quad barrier\ against\ hole\ flow\ in\ P\ type \end{cases}$$

$$\phi_{Bn} + \phi_{Bp} = (\psi_M - \chi/q) + (\chi/q + E_g - \psi_M) = E_g$$

❑ Metal-Semiconductor Junctions (n-type S)

Rectifying contacts (Schottky contact) : $\Phi_M > \Phi_S$

The barrier height $(q\Phi_m - \chi)$ ***from M to S remains the same! → Rectifying***

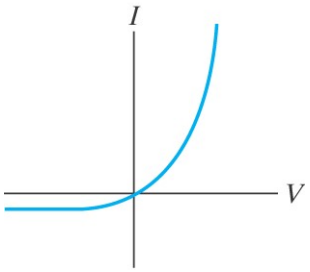


Majority carriers (electrons) contribute to the current for both cases.

→ Absence of minority carriers
→ Short delay time

→
High-frequency properties and switching speed are therefore generally better than typical p-n junctions.
+
Simple fabrication steps
+
Dense integration

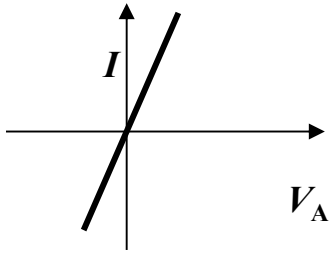
***V* (forward bias)**
→ contact potential is reduced from V_0 to $V_0 - V$
→ electrons in S CB can diffuse across the depletion region to M
→ forward current increasing



***V_r* (reverse bias)**
→ contact potential is increased from V_0 to $V_0 + V_r$
→ electrons in S CB canNOT diffuse across the depletion region to M
→ negligible constant reverse current

❑ Metal-Semiconductor Junctions

❑ Ohmic contacts

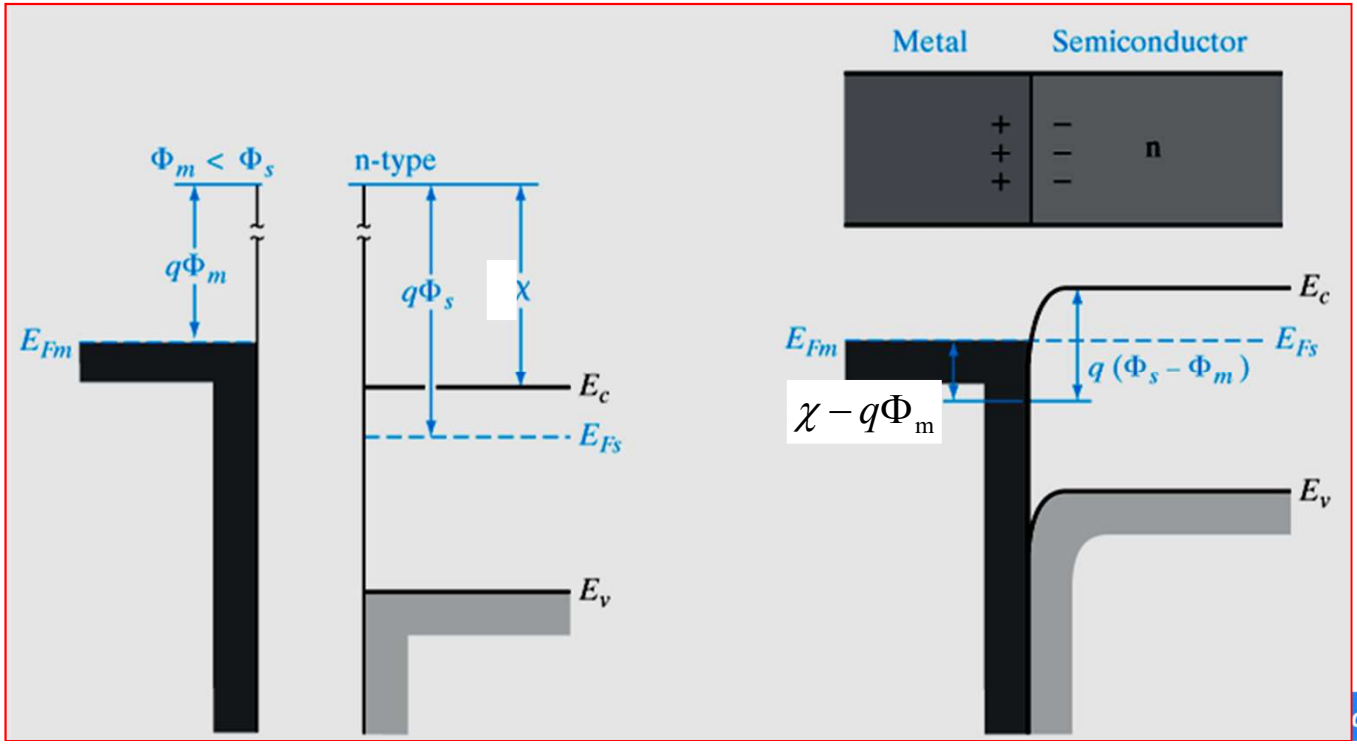


- ✓ Linear I-V characteristic in both biasing directions
- ✓ Minimal resistance and no tendency to rectify signals
- ✓ For example: $\Phi_m < \Phi_s$ (n-type),

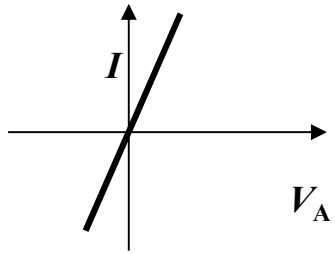
  The barrier to electron flow between the metal and the semiconductor is small and easily overcome by a small voltage

  ; Even a small V_A>0 gives rise to a large forward bias current

  ; Under reverse biasing, there is a small barrier for electron flow from metal to the semiconductor

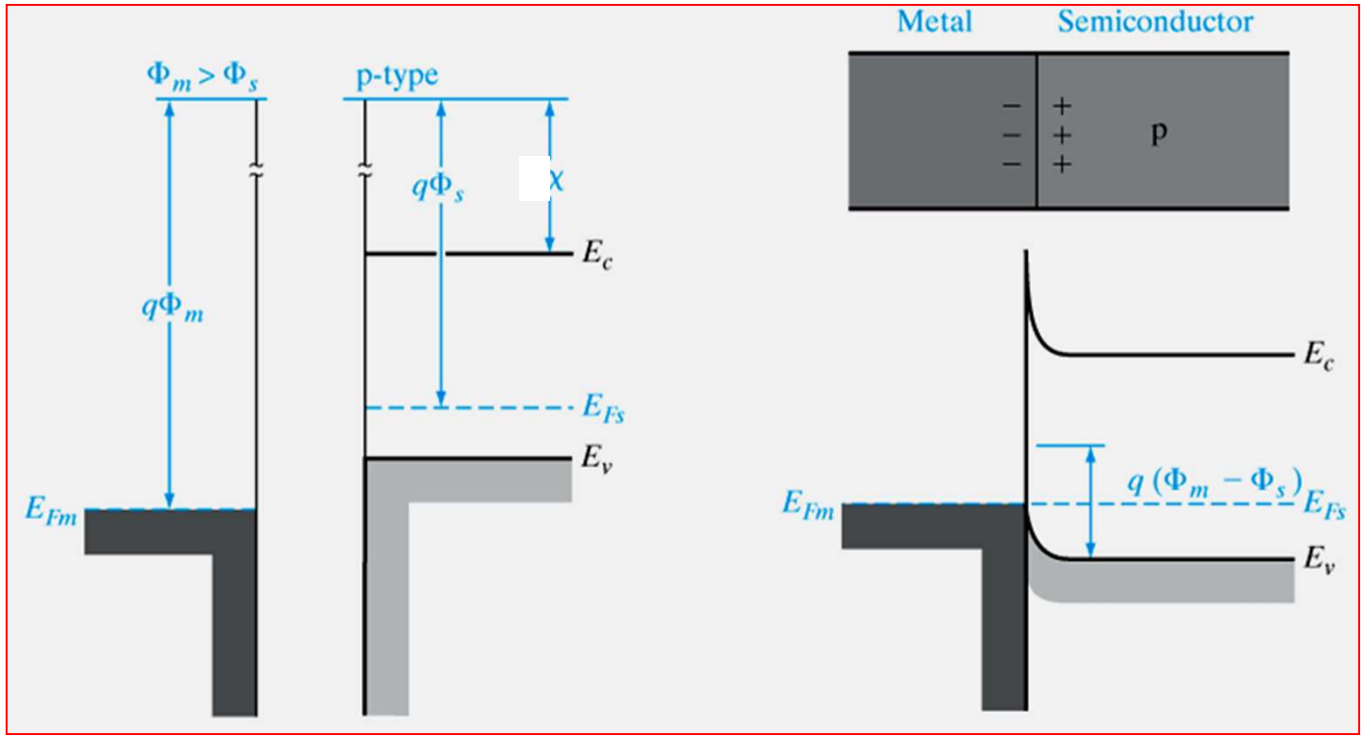


❑ Metal-Semiconductor Junctions



❑ Ohmic contacts

✓ **Next example of Ohmic contact: $\Phi_m > \Phi_s$ (p-type)**
Easy hole flow across the junction

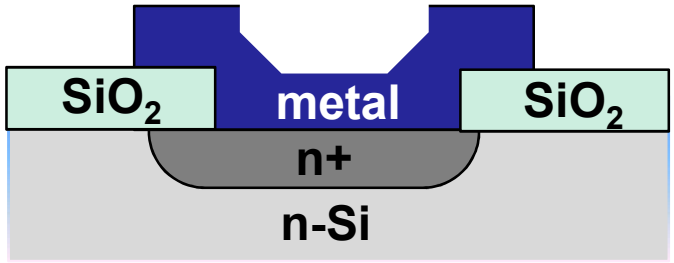


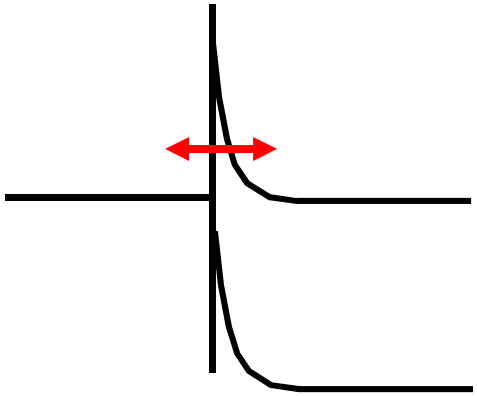
✓ **No depletion region occurs in the semiconductor unlikely the rectifying contact (the electrostatic potential difference required to align the Fermi levels at equilibrium calls for accumulation of majority carriers in S)**

❑ Metal-Semiconductor Junctions

❑ Ohmic contacts : practical method

- ✓ A practical method for forming Ohmic contacts regardless of the biasing polarity and relative work functions between S & M is by doping the semiconductor heavily ($10^{17}/cm^3$~$10^{19}/cm^3$) in the contact (surface) region.
- ✓ Barrier height is not affected by an increase in the semiconductor doping. Thus if a barrier exists at the interface, the depletion width is small enough to allow carriers to tunnel through the barrier.



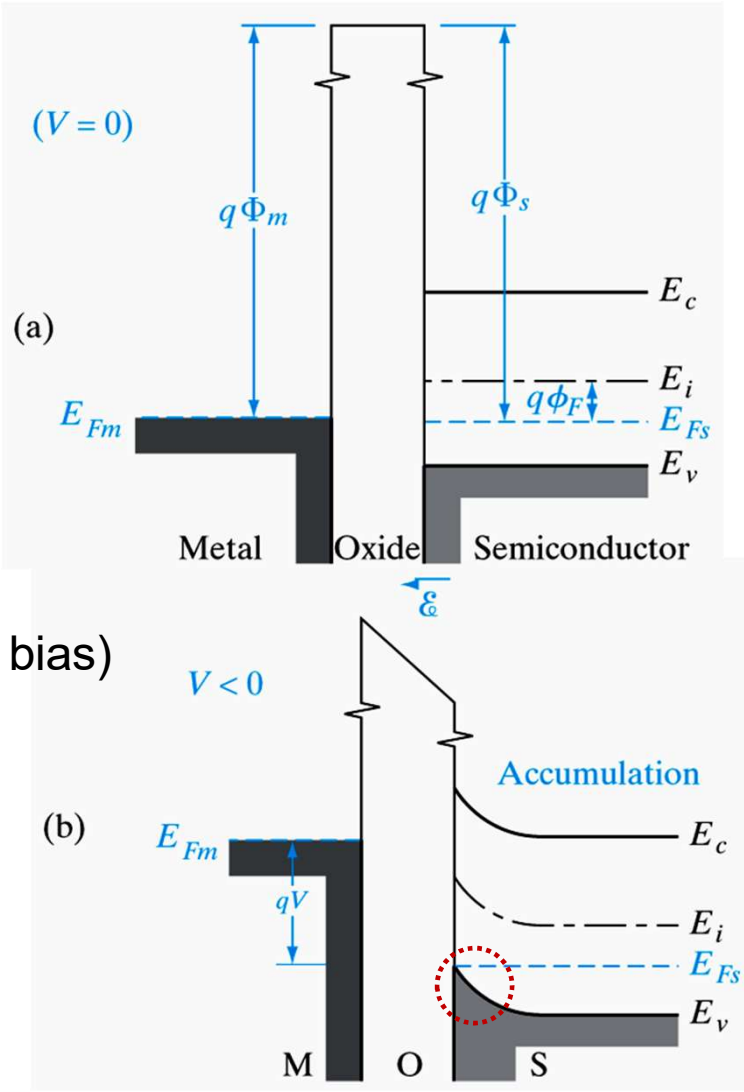


Electrical nature of Ideal MS contacts

	n-type Semiconductor	p-type Semiconductor
$\Phi_M > \Phi_S$	Rectifying	Ohmic
$\Phi_M < \Phi_S$	Ohmic	Rectifying

• The Ideal MOS Capacitor

- ✓ Modified work function $q\Phi_m$: measured from the metal Fermi level to the conduction band of the oxide
- ✓ Assumption: $\Phi_m = \Phi_S$
- ✓ A negative gate bias
  → the electron energies are raised in metal relative to the semiconductor by qV (V: applied bias)
- ✓ A negative gate bias
  → a negative charge on the metal
  → an equal net positive charge to accumulate at the surface of the semiconductor
- ✓ Φ_m and Φ_S do not change with applied voltage, moving E_{Fm} up in energy relative to E_{Fs} causes a tilt in the oxide conduction band
- ✓ An electric field causes a gradient in E_i

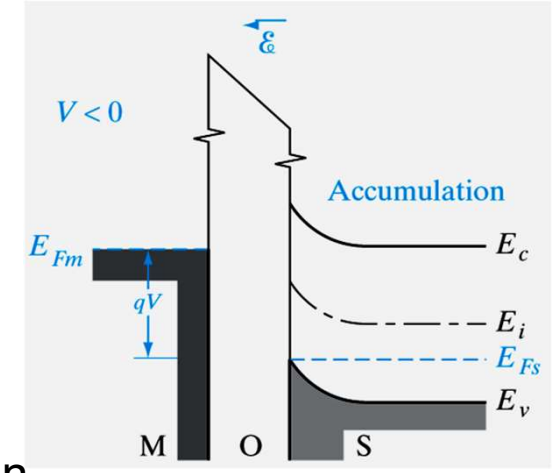


hole accumulation

$$\mathscr{E}(x) = \frac{1}{q}\frac{dE_i}{dx}$$

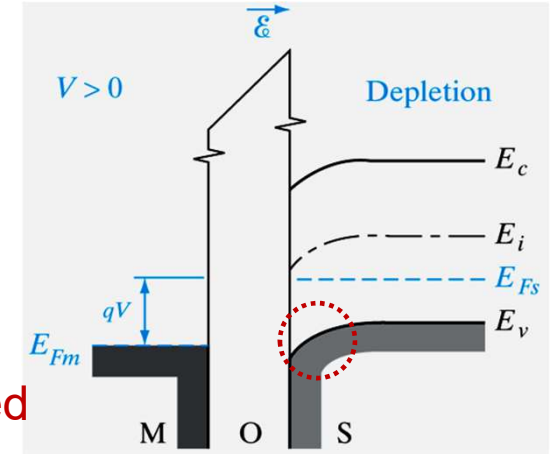
✓ The *accumulation* of holes near the interface → hole increase

$$p = n_i e^{(E_i - E_F)/kT}$$



✓ Since no current passes through the MOS structure, there can be no variation in the Fermi level within the semiconductor

✓ E_i-E_F ↑ → E_i moving up (band bending)
→ E_F lies closer to the E_V → a larger hole concentration



hole depletion

✓ A positive gate bias → lowering the metal Fermi level by qV in metal

✓ A positive gate voltage → positive charge on the metal → a corresponding net negative charge at the surface of the semiconductor (*depletion* of holes from the region near the surface, leaving behind uncompensated ionized acceptors)

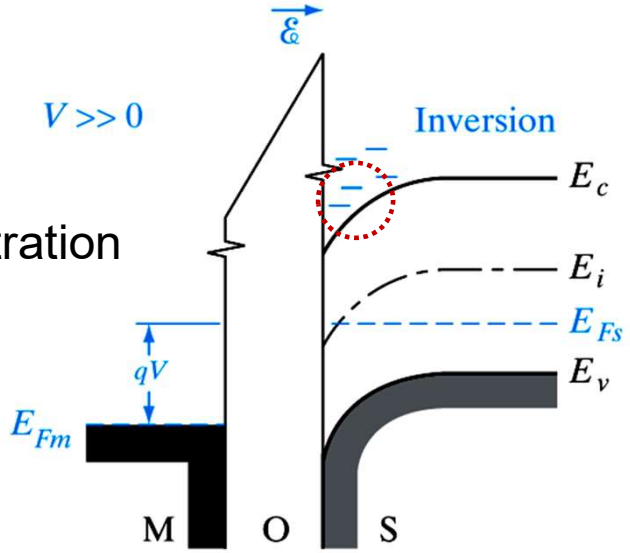
✓ For a positive gate bias, moving E_i closer to E_F, and bending the bands down near the semiconductor surface

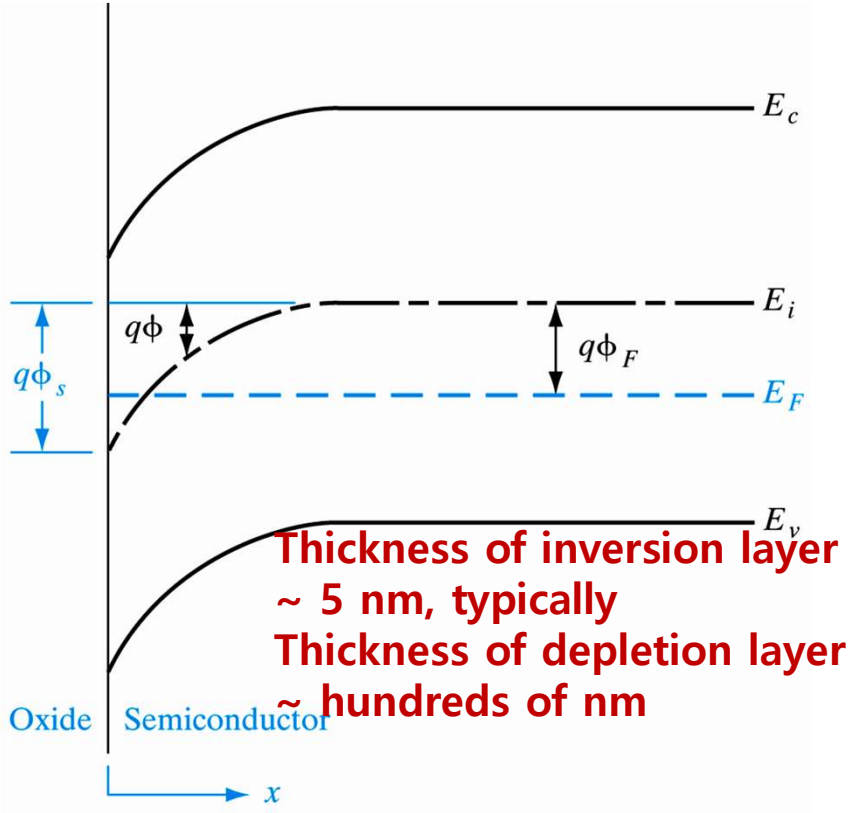
✓For a higher positive gate bias, the bands at the semiconductor surface bend down more strongly

→ E_i below E_F ($E_i < E_F$) → a larger electron concentration

→ The n-type surface layer is formed not by doping, but instead by inversion of the originally p-type semiconductor

→ it becomes the channel in the FET





Thickness of inversion layer ~ 5 nm, typically
Thickness of depletion layer ~ hundreds of nm

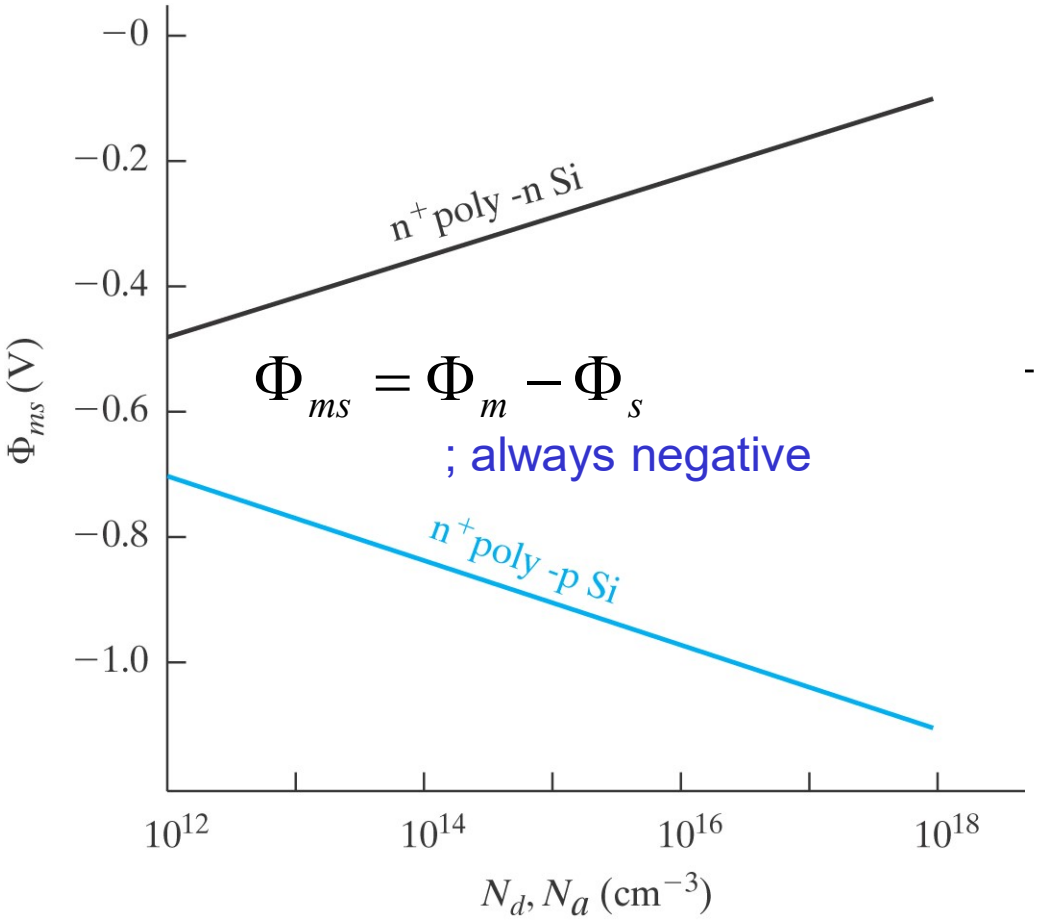
- ✓ $q\phi$: the extent of band bending at *x*
- ✓ $q\phi_s$: the band bending at the surface
- ✓ ϕ_s =0: *flat band*
- ✓ ϕ_s < 0: bend up, accumulation
- ✓ ϕ_s > 0: bend down, depletion
- ✓ $\phi_s > \phi_F$: $E_i < E_F$, inversion
- ✓ E_F-E_i @ surface =$q\phi_F$ → **strong inversion**

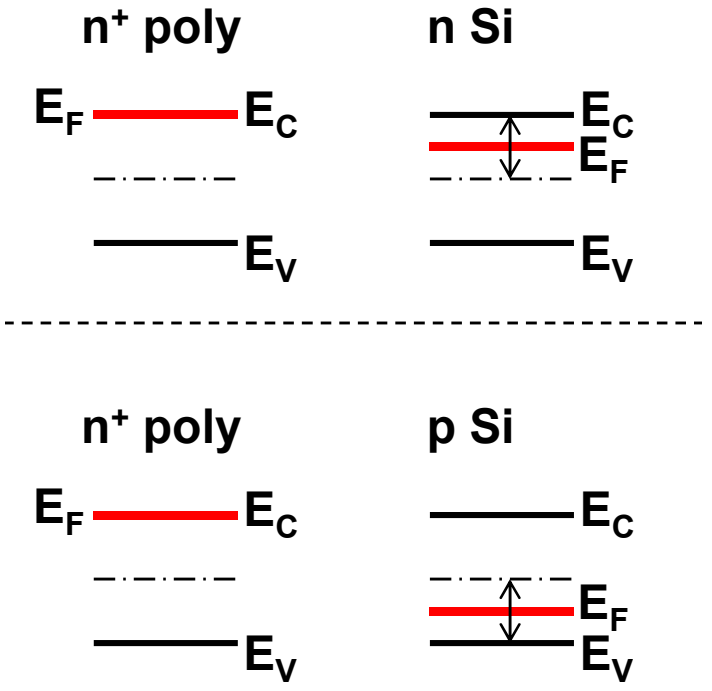
true n-type conduction channel

$$\phi_s(\text{inv.}) = 2\phi_F = 2\frac{kT}{q}\ln\frac{N_a}{n_i} \qquad p = n_i e^{(E_i - E_F)/kT}$$

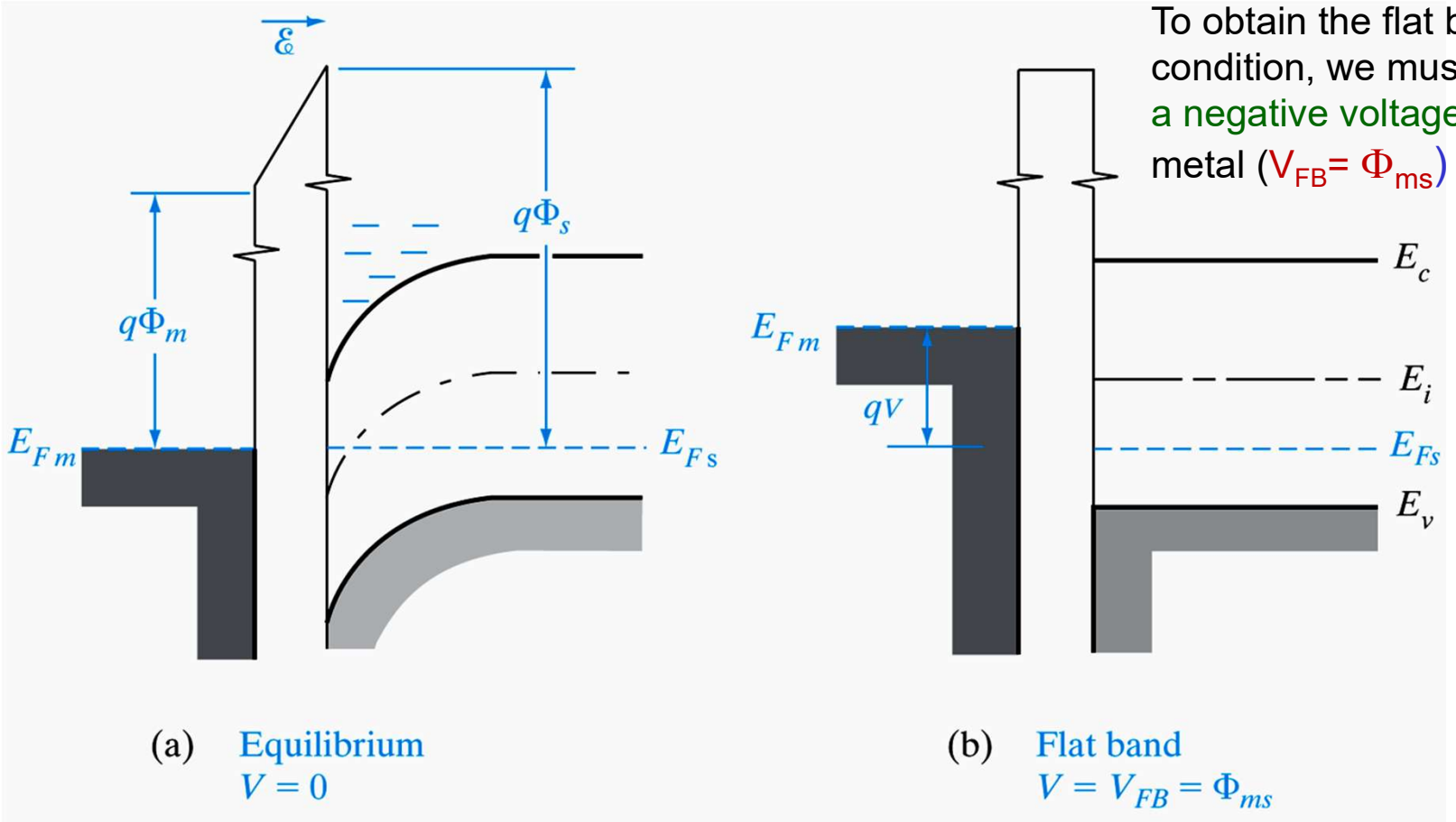
❑ Effects of Real Surfaces

- **Effect of Surfaces**: *Work function potential difference*
  - ✓ Φ_s depends on the doping of the semiconductor since the Fermi level changes with the doping





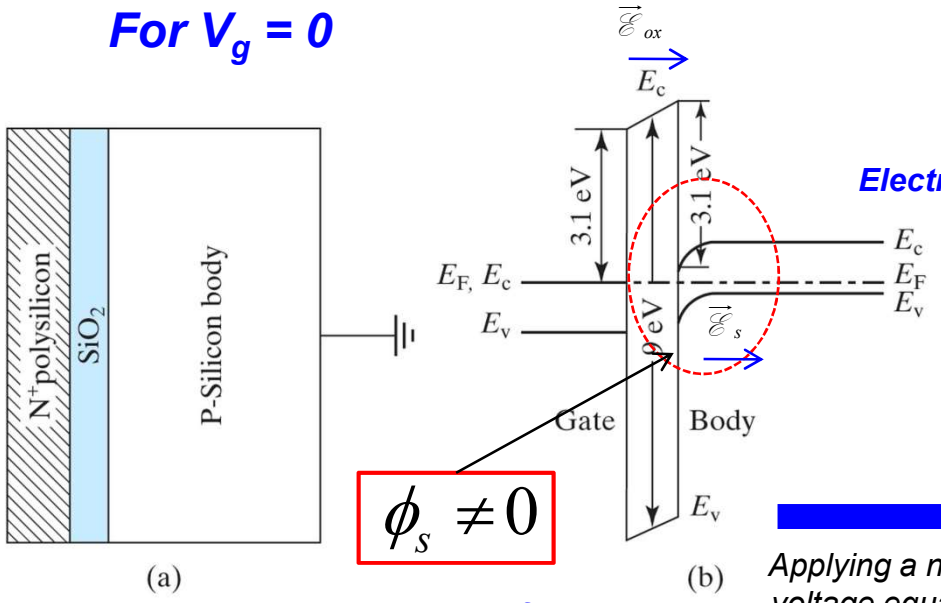
- ✓ The bands bend down near the semiconductor surface
- ✓ If Φ_{ms} is sufficiently negative, an inversion region can exist with no external voltage applied
- ✓ In aligning E_F we must include a tilt in the oxide conduction band (implying an electric field)



To obtain the flat band condition, we must apply a negative voltage to the metal ($V_{FB} = \Phi_{ms}$)

Flat-Band Condition and Flat-Band Voltage

For $V_g = 0$

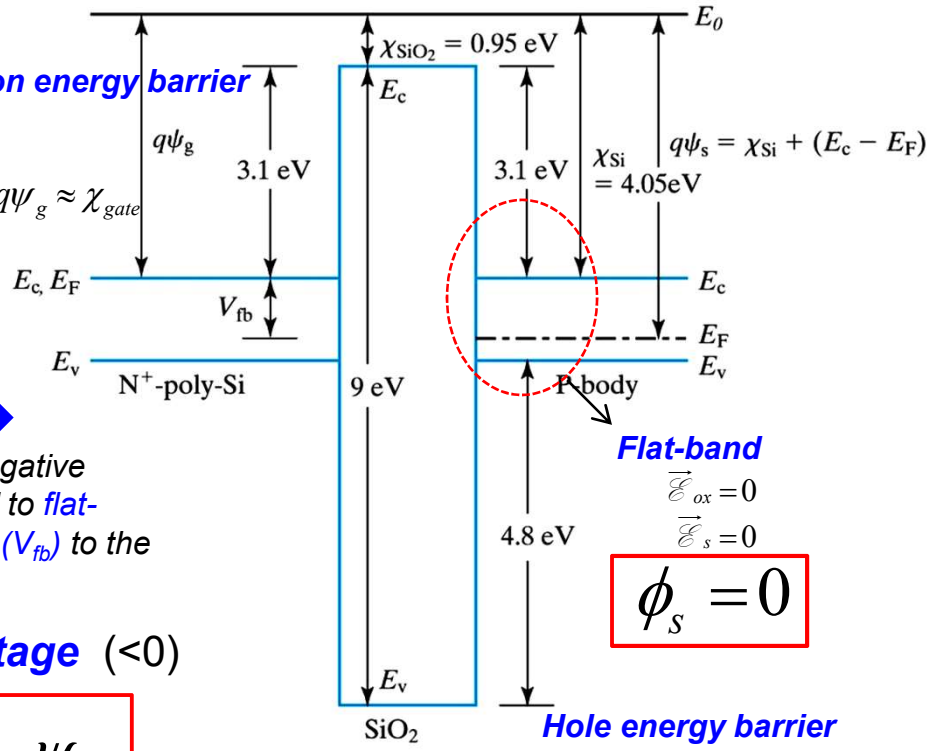


$$\phi_s \neq 0$$

Band is not flat.

Applying a negative voltage equal to flat-band voltage (V_{fb}) to the gate.

Flat-Band Condition (for $V_g = V_{fb}$)



Flat-Band Voltage (<0)

$$V_{fb} = \psi_g - \psi_s$$

E_0 : *vacuum level*

ψ_g : *work function of gate material* $[V]$

ψ_s : *work function of semiconductor* $[V]$

χ_{Si} : *electron affinnity of silicon* $[eV]$

χ_{SiO_2} : *electron affinnity of oxide* $[eV]$

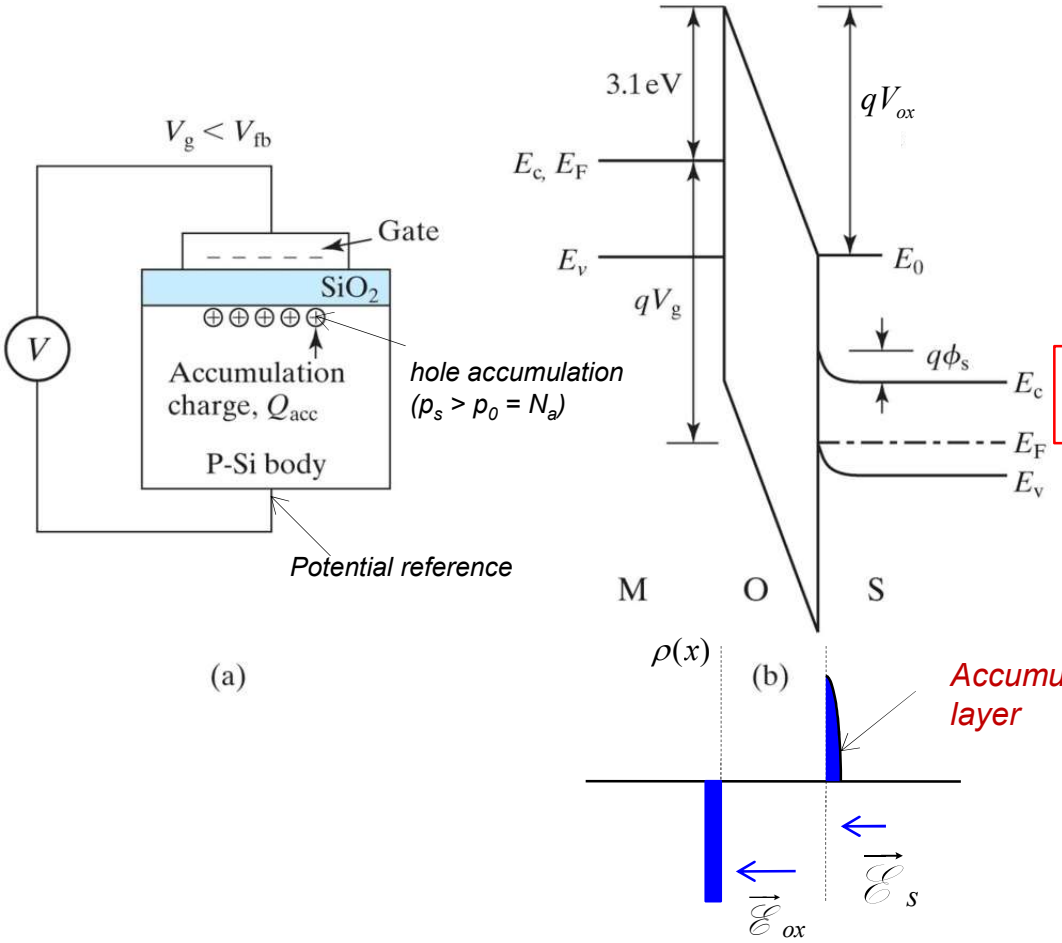
In SiO_2, the exact position of E_F has no significance.

$\because \quad n = N_C \exp[(E_C - E_F)/kT \approx 10^{-60}\ cm^{-3}$

,assuming E_F is around in the middle of the SiO_2 band gap.

Surface Accumulation

For $V_g < V_{fb}$



ϕ_s : surface potential $[V]$

$q\phi_s$: band bending $[eV]$

V_{ox} : oxide voltage

$$\phi_s = \begin{cases} \text{negative}, & \text{if } E_C \text{ bends upward.} \\ \text{positive}, & \text{if } E_C \text{ bends downward.} \end{cases}$$

$$V_g = \left(E_{Fm} - E_{Fs}\right)/q = V_{fb} + \phi_s + V_{ox}$$

At flat-band, $V_g = V_{fb}$, $\phi_s = V_{ox} = 0$

$$p_s = N_a e^{-q\phi_s/kT} \gg N_a \approx p_o,$$

$$\text{if } \phi_s \approx -100 \sim -200\, mV$$

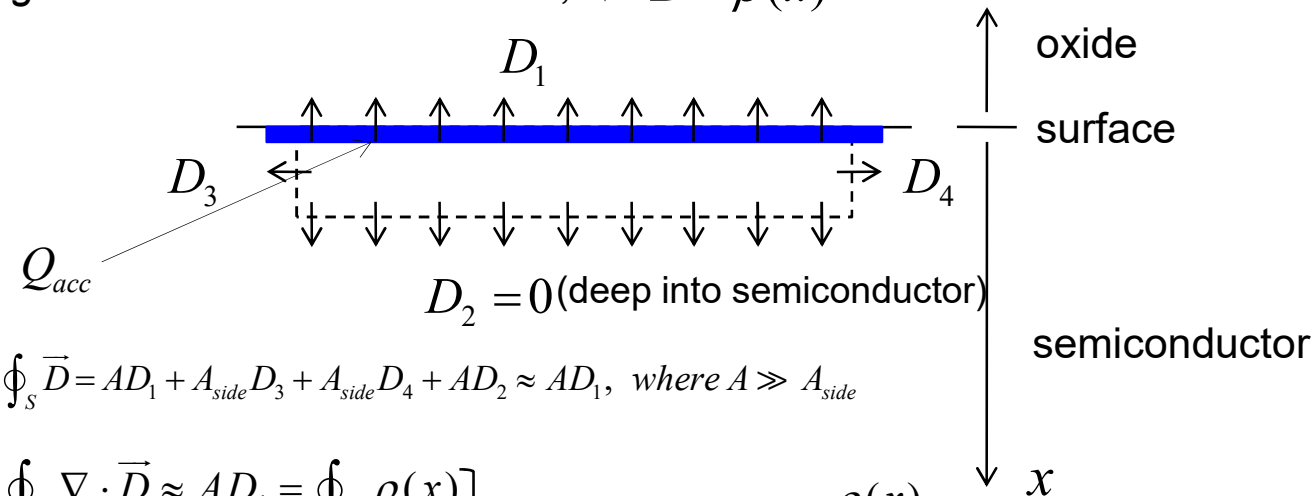
$$\phi_s < 0$$

$$Q_{acc} \ [C/cm^2]$$

In the case of surface accumulation, ϕ_s is small in a first-order model.

$$V_{ox} = V_g - V_{fb}$$

Using Gauss's Law at the surface, $\nabla \cdot \vec{D} = \rho(x)$



$$\oint_S \vec{D} = AD_1 + A_{side}D_3 + A_{side}D_4 + AD_2 \approx AD_1, \quad where\ A \gg A_{side}$$

$$\Rightarrow \oint_V \nabla \cdot \vec{D} \approx AD_1 = \oint_V \rho(x)$$

$$D_1 = -\varepsilon_s \mathscr{E}_s = -\varepsilon_{ox}\mathscr{E}_{ox}$$

$$\varepsilon_s \mathscr{E}_s = \varepsilon_{ox}\mathscr{E}_{ox} = -\oint_V \frac{\rho(x)}{A} = -Q_{acc}$$

$$\therefore \boxed{\mathscr{E}_{ox} = -\frac{Q_{acc}}{\varepsilon_{ox}}} \qquad \boxed{V_{ox} = \mathscr{E}_{ox} T_{ox} = -\frac{Q_{acc}}{C_{ox}}}$$

In general, $\boxed{V_{ox} = -\frac{Q_{sub}}{C_{ox}}}$

All the charge that may be present in the substrate, including Q_{acc}.

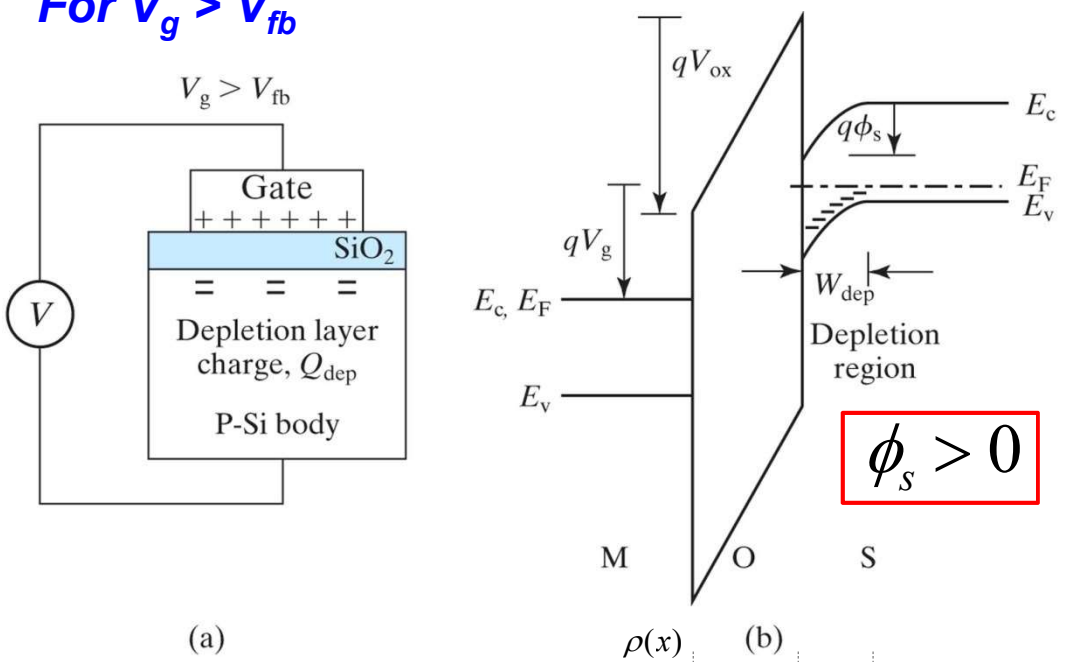
$$where, \quad C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \ [F/cm^2]$$

$$\boxed{Q_{acc} = -C_{ox}(V_g - V_{fb})}$$

The MOS capacitor in accumulation behaves like a capacitor but with a shift in V by V_{fb}.

Surface Depletion

For $V_g > V_{fb}$



$$\phi_s > 0$$

The MOS capacitor is biased into surface depletion.
(a) Types of charge present;
(b) energy band diagram.

***Negative* due to acceptor ions**

$$V_{ox} = -\frac{Q_{sub}}{C_{ox}} = -\frac{Q_{dep}}{C_{ox}}$$

$$= \frac{qN_aW_{dep}}{C_{ox}} = \frac{\sqrt{qN_a 2\varepsilon_s\phi_s}}{C_{ox}}$$

$$\phi_s = \frac{qN_aW_{dep}^2}{2\varepsilon_s}$$

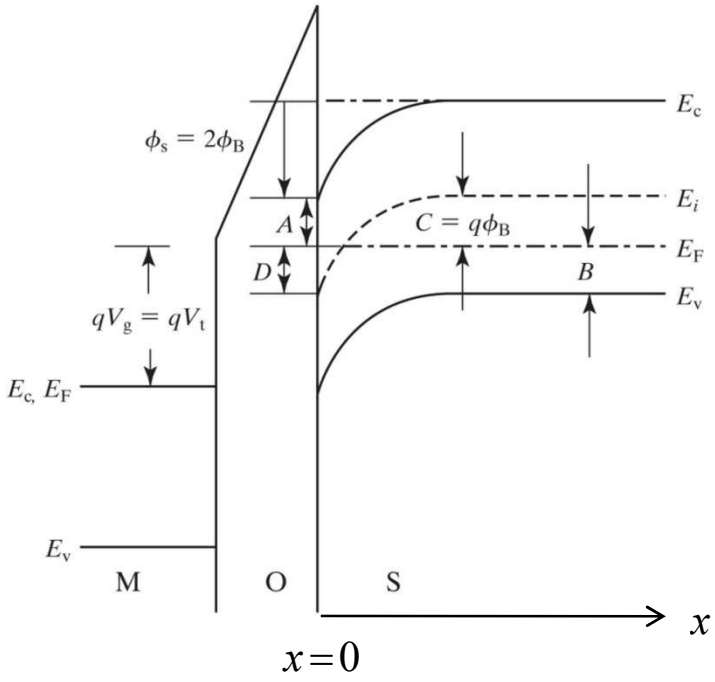
$$W_{dep} = \sqrt{\frac{2\varepsilon_s\phi_s}{qN_a}}$$

$$p_s = N_a e^{-q\phi_s/kT} \ll N_a \approx p$$

$$V_g = V_{fb} + \phi_s + V_{ox} = V_{fb} + \frac{qN_aW_{dep}^2}{2\varepsilon_s} + \frac{qN_aW_{dep}}{C_{ox}}$$

Threshold Condition and Threshold Voltage

For more positive ($V_g = V_t > V_{fb}$)



Fermi potential energy

$$q\phi_B = (E_i - E_F)_{bulk}$$

Threshold condition

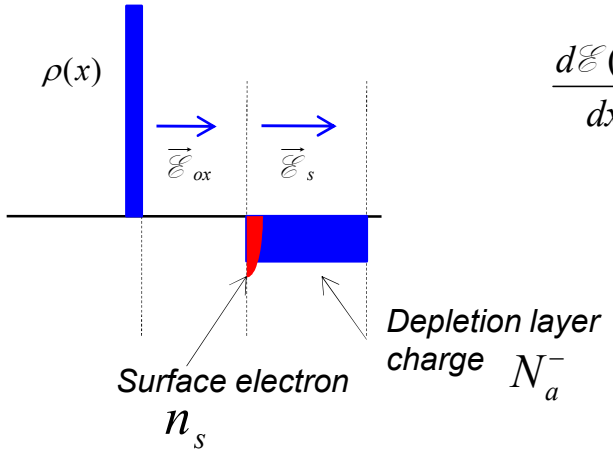
$$\phi_s = \phi_{st} = 2\phi_B > 0$$

$$(E_C - E_F)_{surface} = (E_F - E_V)_{bulk} \qquad A = B$$

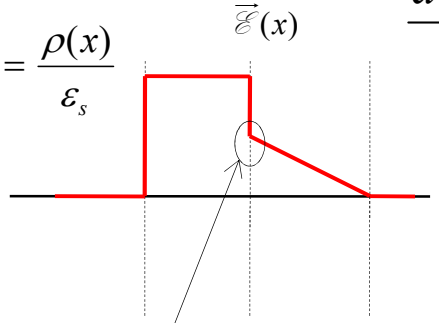
$$(E_i - E_F)_{bulk} = (E_F - E_i)_{surface} \qquad C = D$$

$$n_s = N_a$$

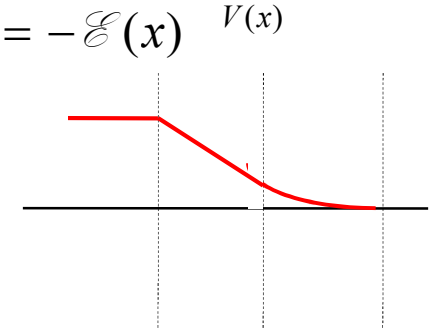
$$Q_{sub} = Q_{dep} + Q_{inv} \approx Q_{dep}$$



$$\frac{d\mathscr{E}(x)}{dx} = \frac{\rho(x)}{\varepsilon_s}$$



$$\frac{dV(x)}{dx} = -\mathscr{E}(x)$$



$$\varepsilon_s \mathscr{E}_s(0) = \varepsilon_{ox} \mathscr{E}_{ox}(0)$$

Fermi potential energy

$$q\phi_B = (E_i - E_F)_{bulk} = kT \ln \frac{N_a}{n_i}$$

$$n_i = N_C \exp[-(E_C - E_i)/kT]$$
$$p = N_V \exp[-(E_F - E_V)/kT]$$
$$n_i^2 = N_C N_V \exp[-E_g/kT]$$

At threshold,

$$\phi_s = \phi_{st} = 2\phi_B = \frac{2kT}{q} \ln \frac{N_a}{n_i}$$

Threshold Voltage, V_t (V_g at the threshold condition)

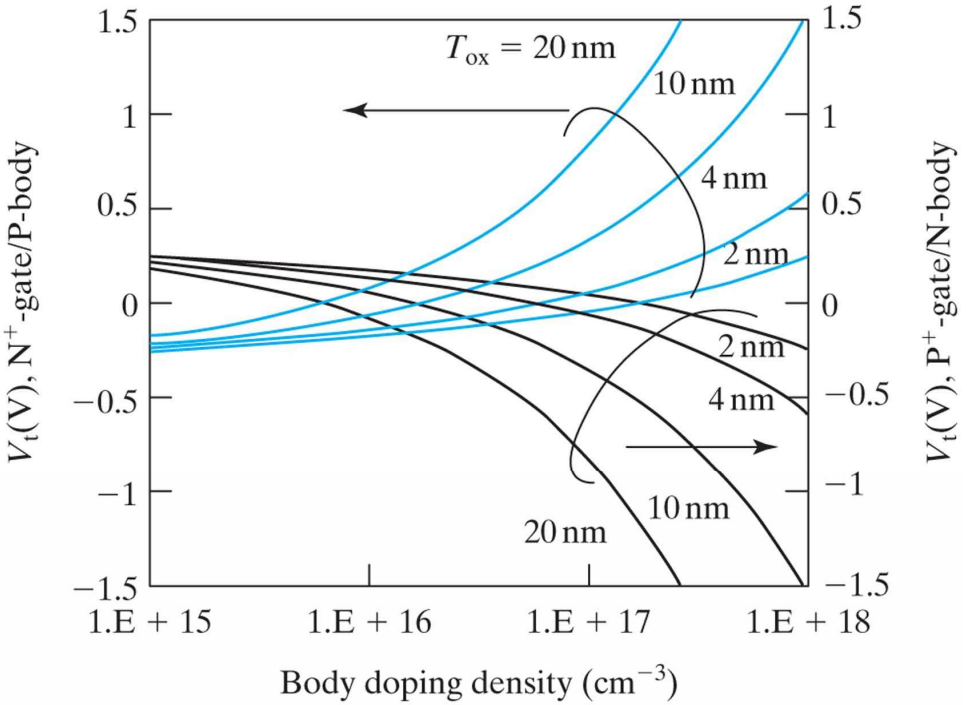
$$V_t = V_g \Big|_{\phi_s = 2\phi_B} = V_{fb} + \phi_s + V_{ox}$$

$$= V_{fb} + \frac{qN_a W_{dep}^2}{2\varepsilon_s} + \frac{qN_a W_{dep}}{C_{ox}}$$

$$\therefore \quad V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}}$$

For P-Type Body

Theoretical threshold voltage vs. body doping concentration.



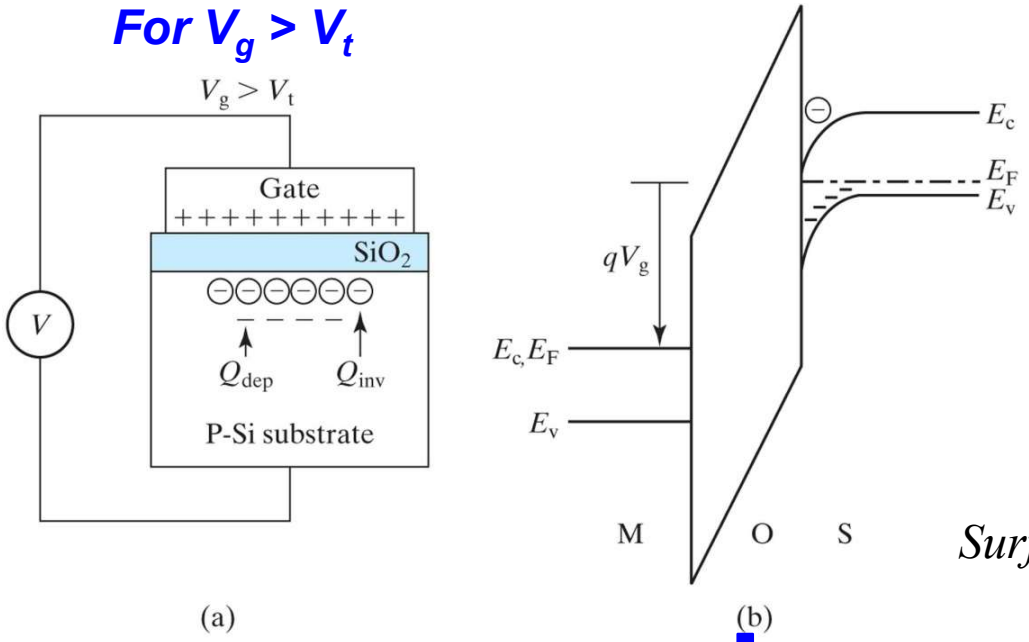
For N-Type Body

$$V_t = V_{fb} + \phi_{st} - \frac{\sqrt{qN_d 2\varepsilon_s |\phi_{st}|}}{C_{ox}}$$

$$\phi_{st} = -2\phi_B, \quad \phi_B = \frac{kT}{q} \ln \frac{N_d}{n_i}$$

Strong Inversion beyond Threshold

For $V_g > V_t$

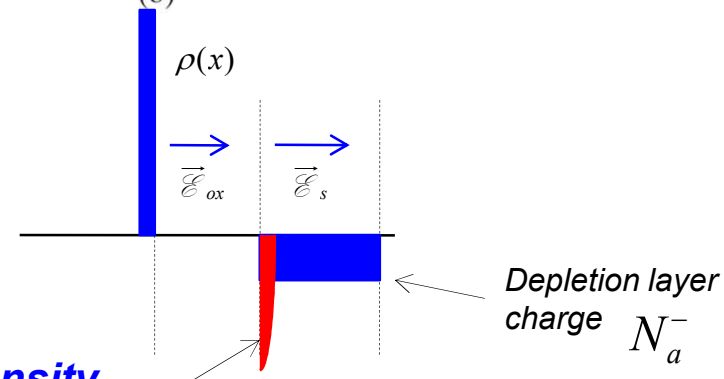


An MOS capacitor is biased into inversion.

With $V_g > V_t$, ϕ_s does not increase much further beyond $2\phi_B$ since even small increase in ϕ_s would induce a much larger surface electron density and therefore a larger V_{ox} that would soak up the V_g.

$$\Rightarrow \boxed{\phi_s \approx 2\phi_B}$$

Surface potential is essentially pinned at $2\phi_B$.



Inversion layer charge density

$$Q_{inv}[C/cm^2]$$

$$\boxed{Q_{sub} = Q_{dep} + Q_{inv}}$$

$$\boxed{n_s >> N_a}$$

Surface becomes N-type.

$$If\ \phi_s \approx 2\phi_B, \quad W_{dep} \Rightarrow W_{d\max} = \sqrt{\frac{2\varepsilon_s 2\phi_B}{qN_a}}$$; Depletion width is pinched

$$V_g = V_{fb} + \phi_s + V_{ox} = V_{fb} + 2\phi_B - \frac{Q_{sub}}{C_{ox}}$$

$$\begin{cases} V_{ox} = -\dfrac{Q_{sub}}{C_{ox}} \\ Q_{sub} = Q_{dep} + Q_{inv} \end{cases}$$

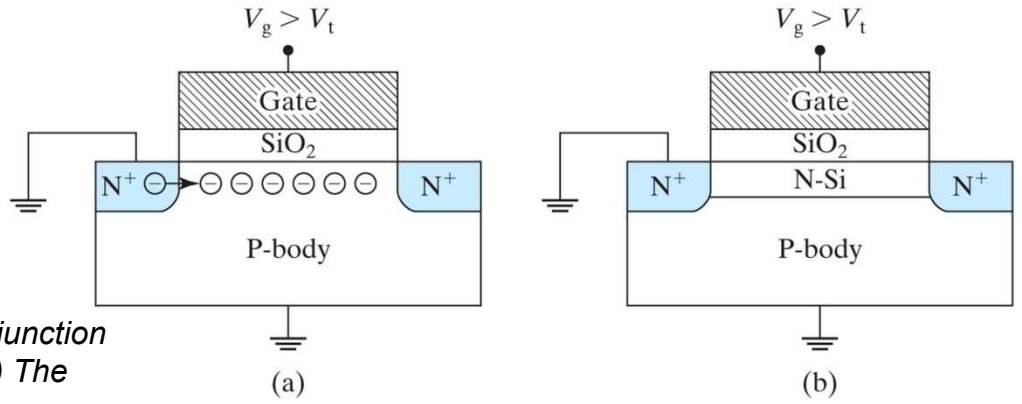
$$= V_{fb} + 2\phi_B - \frac{Q_{dep}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}}$$

$$= V_t - \frac{Q_{inv}}{C_{ox}} \qquad \therefore \quad \boxed{Q_{inv} = -C_{ox}(V_g - V_t)}$$

The MOS capacitor in strong inversion behaves like a capacitor except for a voltage offset of V_t.

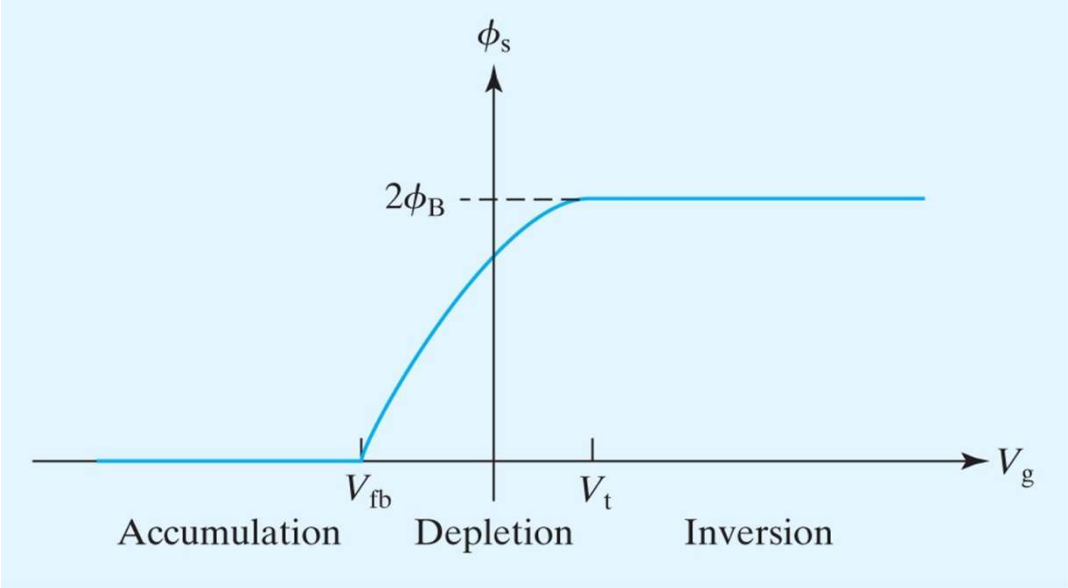
There are few electrons in the P-type body, and it can take minutes for thermal generation to generate the necessary electrons to form the inversion layer.

How to solve this problem?



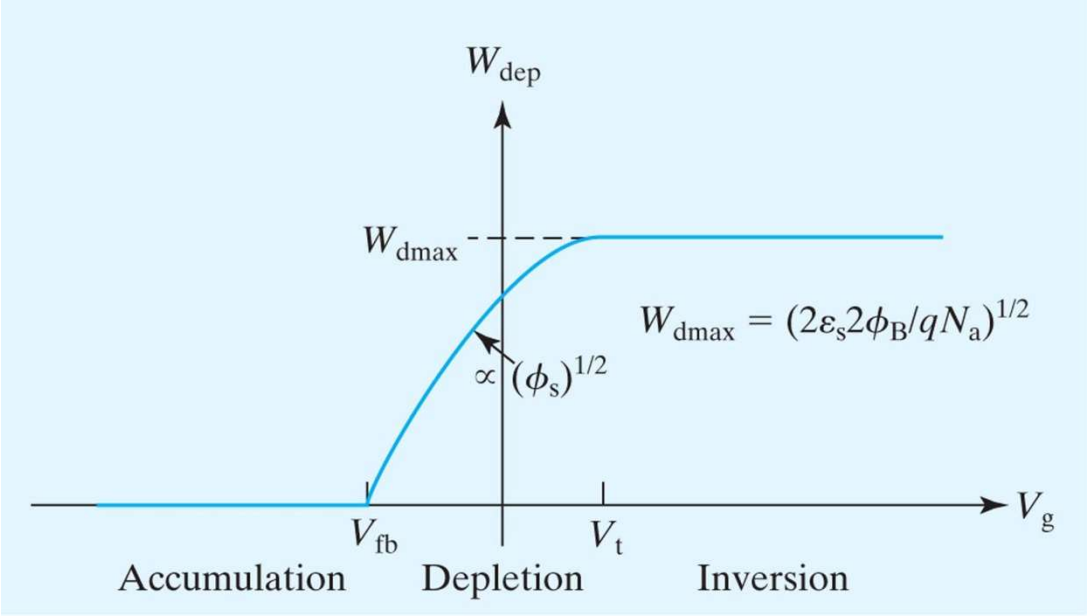
(a) The surface inversion behavior is best studied with a PN junction butting the MOS capacitor to supply the inversion charge. (b) The inversion layer may be thought of as a thin N-type layer.

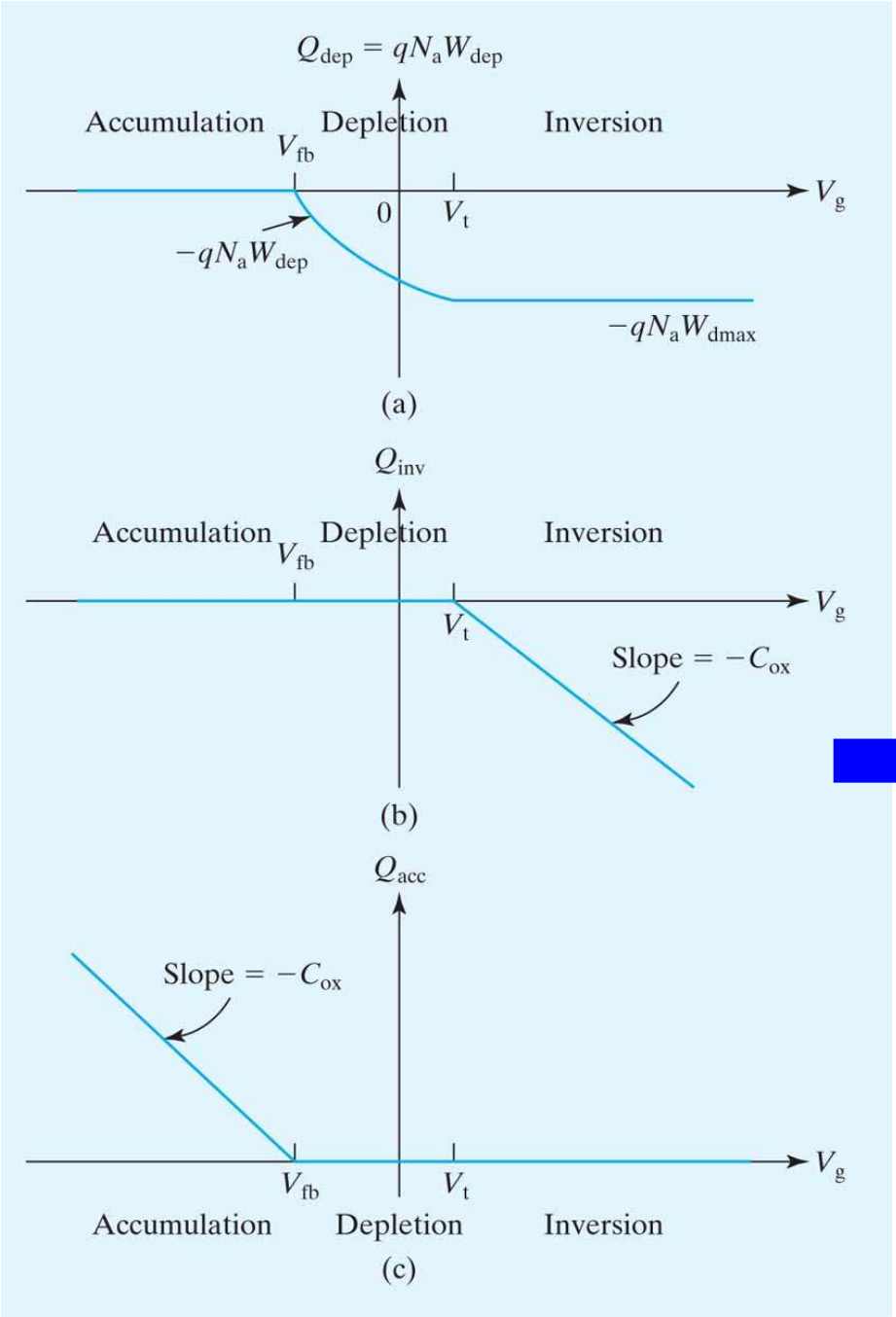
Review: Basic MOS Capacitor Theory



Surface potential saturates at $2\phi_B$ in inversion when V_g is larger than V_t and saturates at V_{fb} in accumulation.

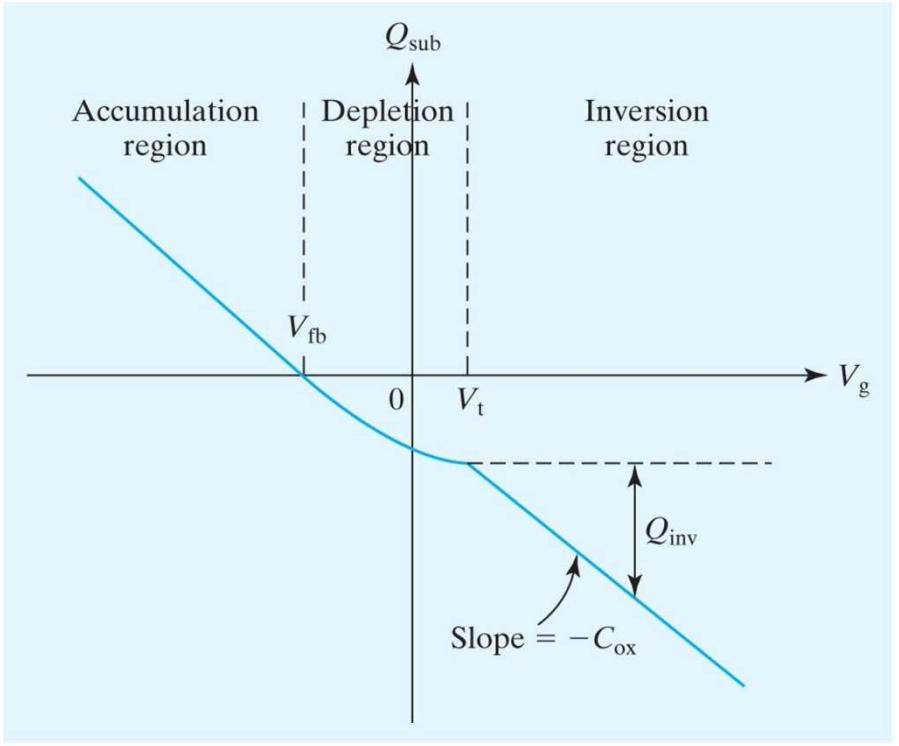
Depletion-region width in the body of an MOS capacitor.



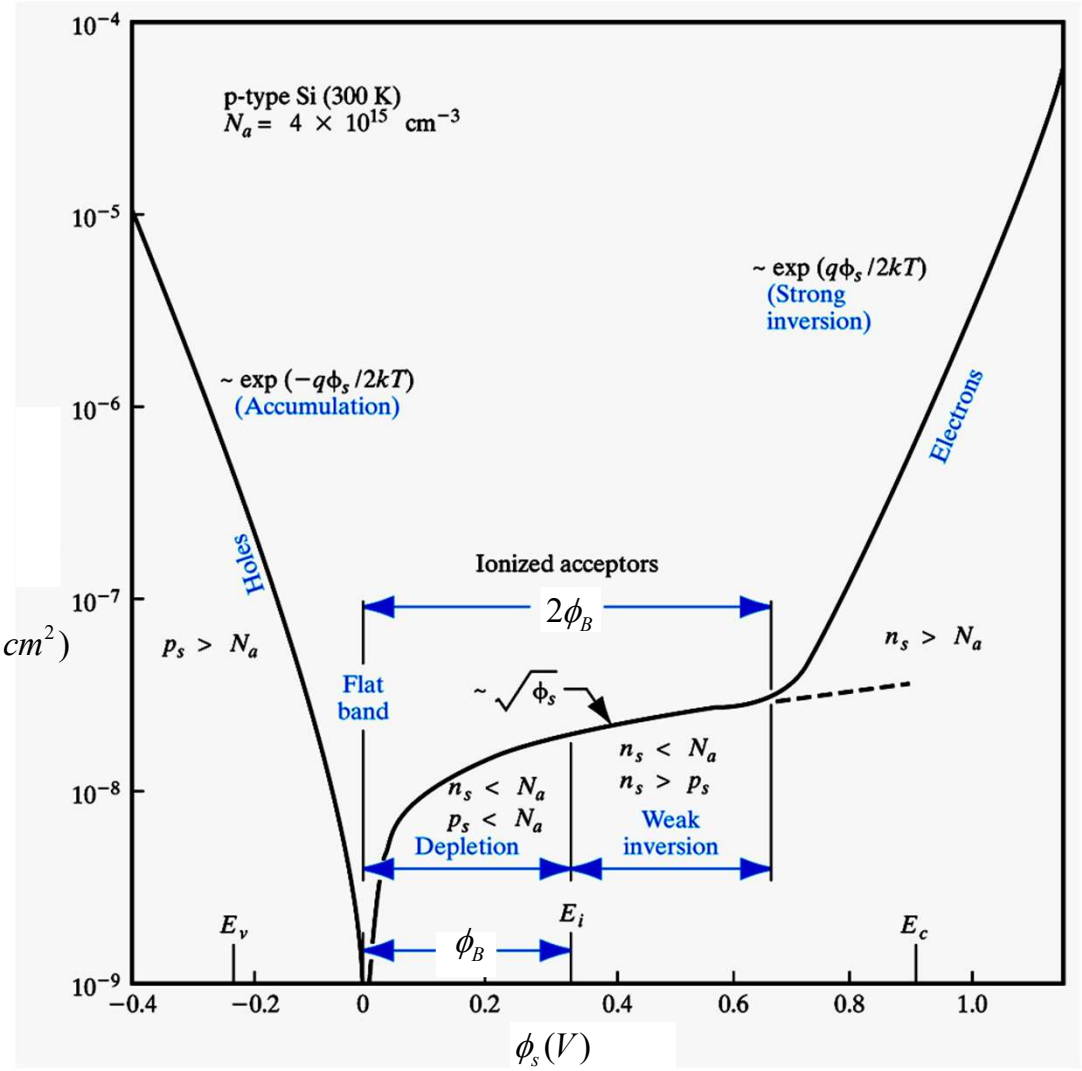


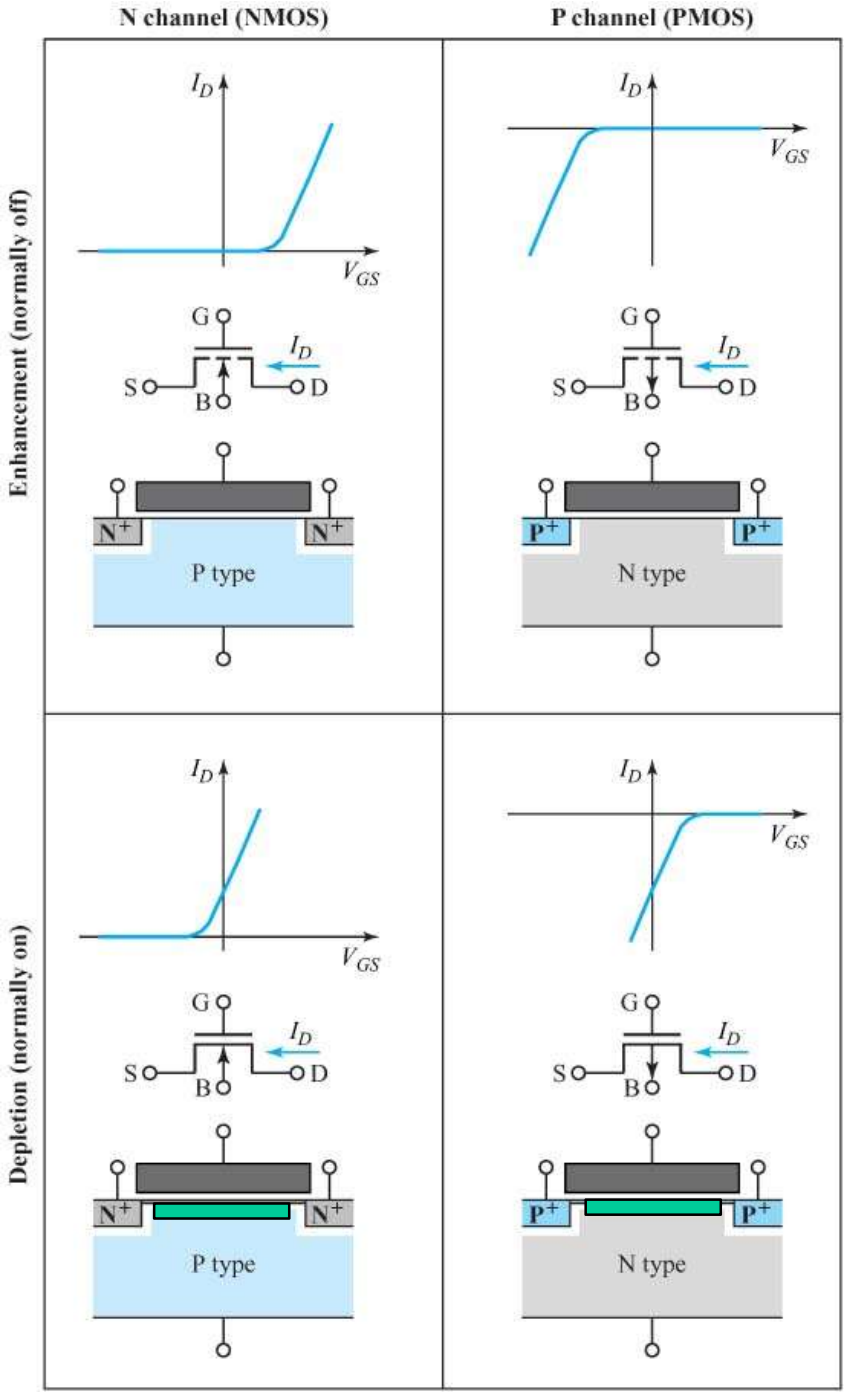
Components of charge (C/cm²) in the MOS capacitor substrate: *(a) depletion-layer charge; (b) inversion-layer charge; and (c) accumulation-layer charge.*

The total substrate charge, Q_{sub} (C/cm²), is the sum of Q_{acc}, Q_{dep}, and Q_{inv}.



Q_{sub} Vs. Surface Potential





❑ The Metal-Insulator-Semiconductor FET

Types of MOSFETs

Normally-off MOSFETs
(Enhancement type)

The main MOSFET type is the N-channel enhancement type. The P-channel enhancement type is used as a complementary transistor in circuits known as CMOS (Complementary MOS) technology.

Normally-on MOSFETs
(Depletion type)

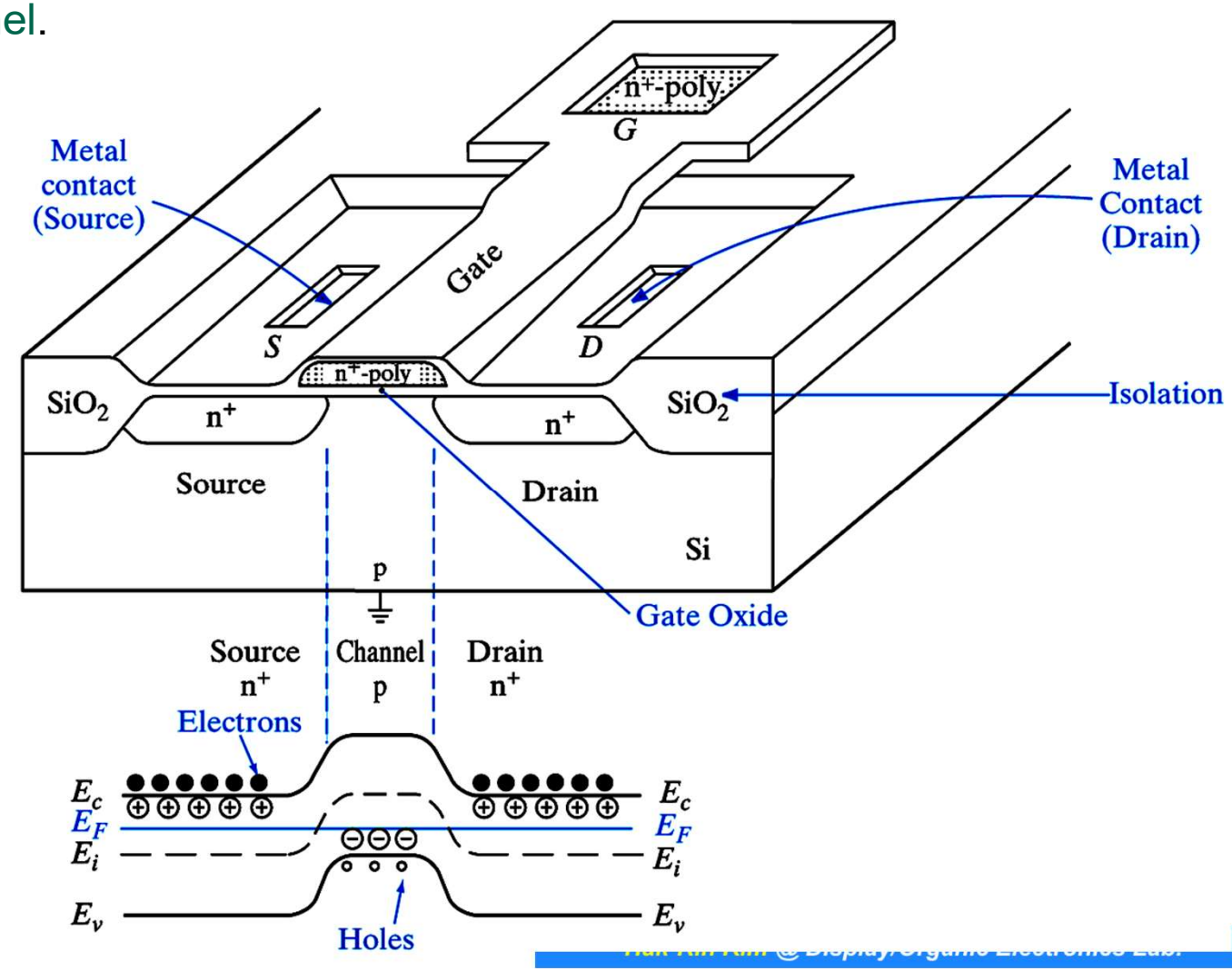
To turn them off, the channels have to be depleted of electrons or holes
→ depletion type

❑ The Metal-Insulator-Semiconductor FET

• Basic Operation and Fabrication

- ✓ Basic MOS transistor: **enhancement-mode n-channel device**
- ✓ No current flows from drain to source without a conducting n channel between them. The Fermi level is flat in equilibrium.
- ✓ There is a potential barrier for an electron to go from the source to the drain, corresponding to the built-in potential of the back-to-back p-n junctions between the source and drain.
- ✓ When a positive voltage is applied to the gate relative to the substrate, negative charges are induced in the underlying Si, by the formation of a depletion region and a thin surface region containing mobile electrons.
  → induced electron → current flow
- ✓ The effect of the gate voltage is to vary the conductance of this induced channel for low drain-to-source voltage

- ✓ If the barrier is reduced sufficiently by applying a gate voltage in excess of what is known as the threshold voltage, V_T, there is significant current flow from the source to the drain.
- ✓ The threshold voltage V_T is the minimum gate voltage required to induce the channel.



- ✓ Similarly, a p-channel device (made on an n-type substrate with p-type source and drain implants or diffusions) requires a gate voltage more negative than some threshold value to induce the required positive charge (mobile holes) in the channel.
- ✓ A normally on device is called a ***depletion-mode transistor***, since gate voltage is used to deplete a channel which exists at equilibrium.
- ✓ The more common MOS transistor is normally off with zero gate voltage, and operates in the *enhancement mode*

- ✓ If the gate voltage exceeds V_T in an n-channel device, electrons are induced in the p-type substrate → like an induced n-type resistor
- ✓ As the V_G increases, more electron charge is induced in the channel and the channel becomes more conducting.
- ✓ The drain current initially increases linearly with the drain bias
  → the *linear* regime

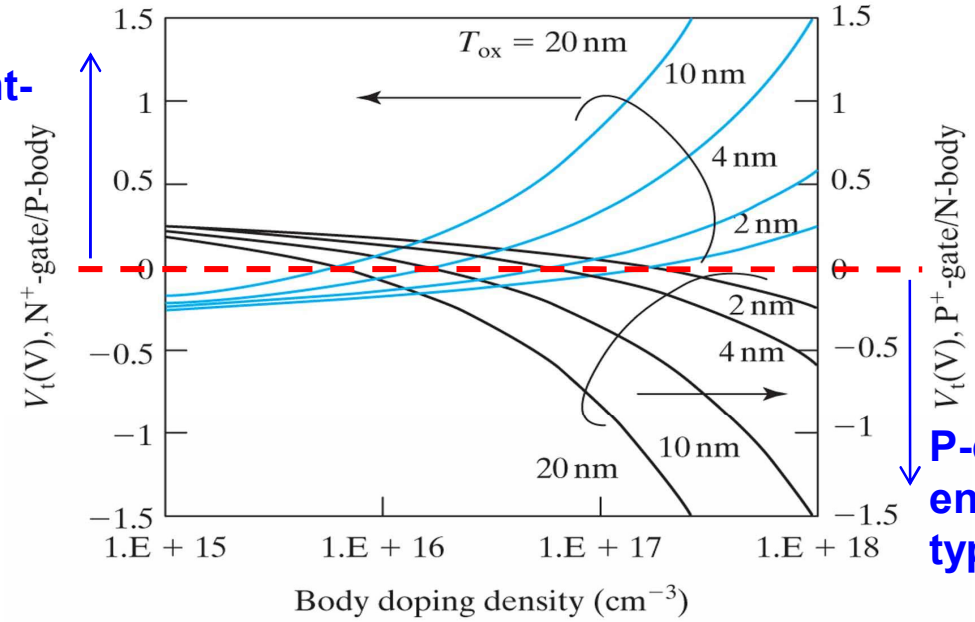
Gate-controlled potential barrier device
or Gate-controlled resistor

Choice of V_t and Gate Doping Type

To make circuit design easier, it is routine to set V_t at a small positive value, e.g., 0.4 V, so that, at $V_g = 0$, the transistor does not have an inversion layer and current does not flow between the two N^+ regions.

Enhancement-Type Device

N-channel enhancement-type



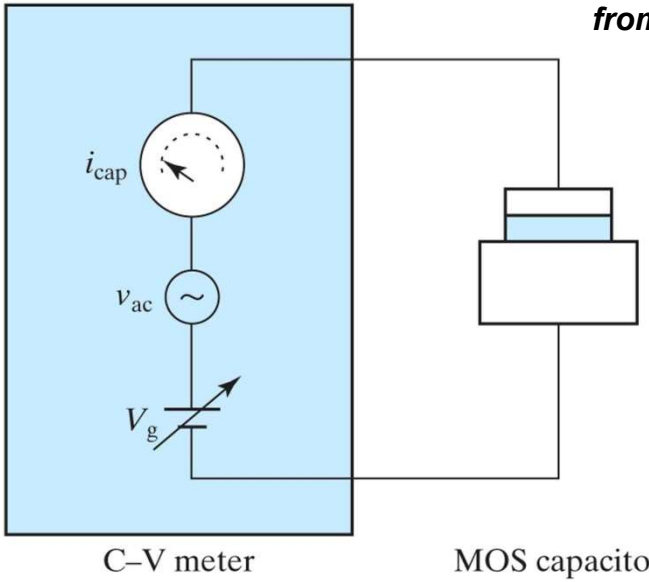
P-channel enhancement-type

P-type body is almost always paired with N^+ gate to achieve a small positive threshold voltage, and N-type body is normally paired with P^+ gate to achieve a small negative threshold voltage.

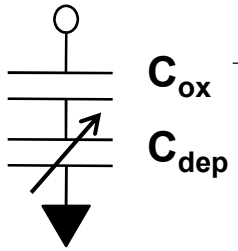
For the case of P-type body paired with P^+ gate, V_t would be too large (over 1 V) and necessitate a larger power supply voltage. This would lead to larger power consumption and heat generation.

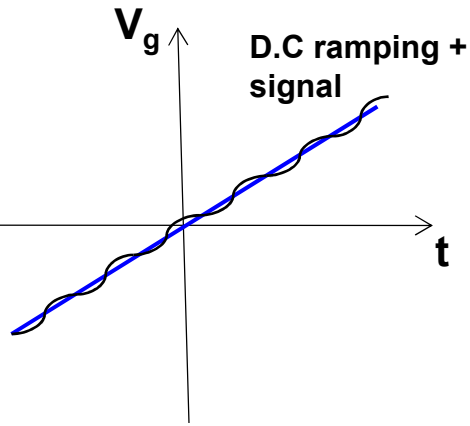
MOS C-V Characteristics for measuring T_{ox}, N_a or N_d, V_{Th}, or V_{FB}

Setup for the C–V measurement.



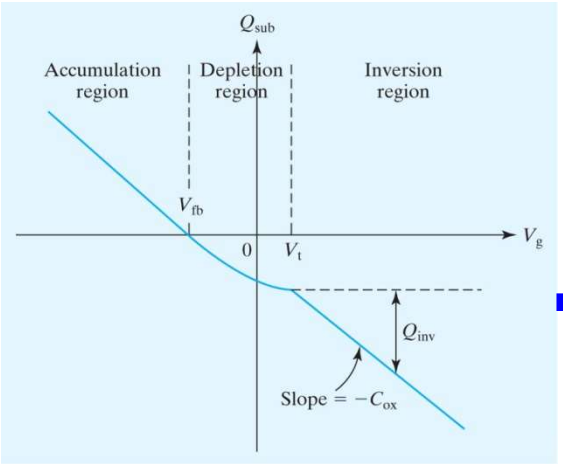
The capacitance is calculated from, $\frac{i_{cap}}{v_{ac}} = \omega C$





D.C ramping + a.c small signal

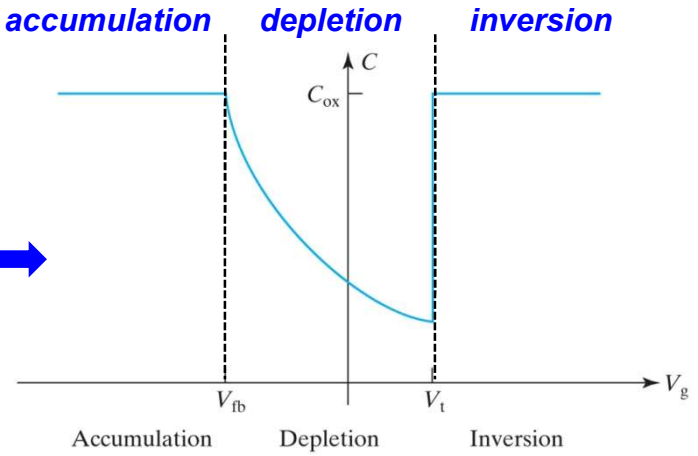
$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} = \sqrt{\frac{1}{C_{ox}^2} + \frac{2(V_g - V_{fb})}{qN_a\varepsilon_s}} \qquad C_{dep} = \frac{\varepsilon_s}{W_{dep}}$$



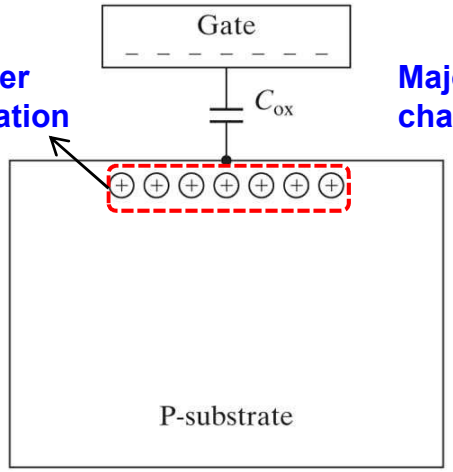
The capacitance in the MOS theory is always the **small-signal capacitance**.

$$C \equiv \frac{dQ_g}{dV_g} = -\frac{dQ_{sub}}{dV_g}$$

The quasi-static MOS C–V characteristics.

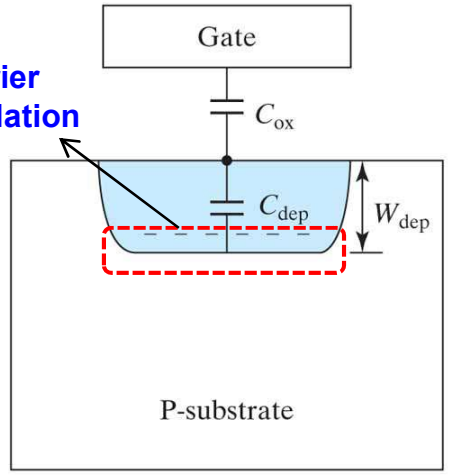


$$\frac{1}{C}=\frac{1}{C_{ox}}+\frac{1}{C_{dep}} \approx \frac{1}{C_{ox}}$$



Majority carrier charge oscillation

(a) **accumulation region**



Majority carrier charge oscillation

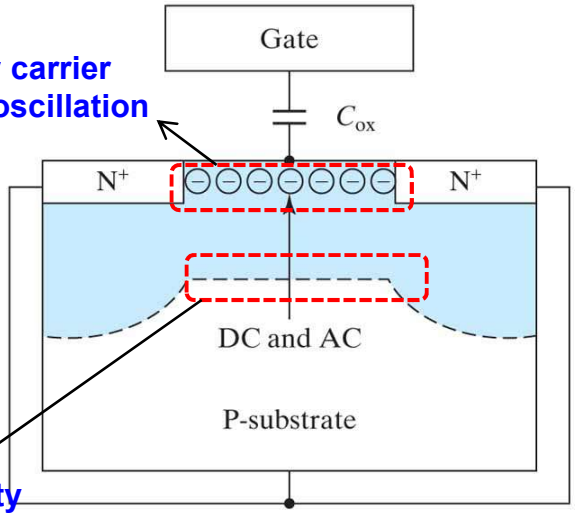
(b) **depletion region**

$$\downarrow C_{dep}=\frac{\varepsilon_s}{W_{dep}}\uparrow$$

$$\frac{1}{C\downarrow}=\frac{1}{C_{ox}}+\frac{1}{C_{dep}}$$

$$=\sqrt{\frac{1}{C_{ox}^2}+\frac{2(V_g-V_{fb})}{qN_a\varepsilon_s}}$$

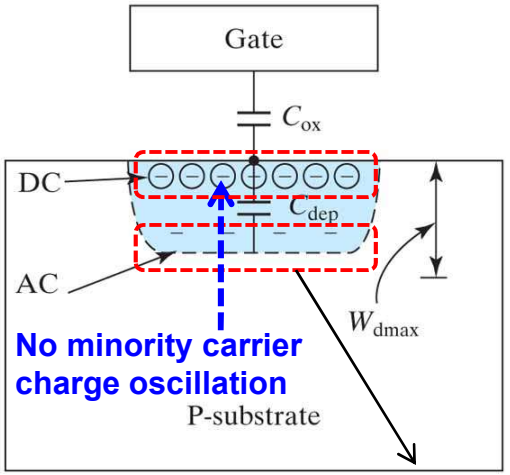
$$\frac{1}{C}=\frac{1}{C_{ox}}+\frac{1}{C_{dep}} \approx \frac{1}{C_{ox}}$$



Minority carrier charge oscillation

No need for majority carrier charge oscillation

(c)



Majority carrier charge oscillation

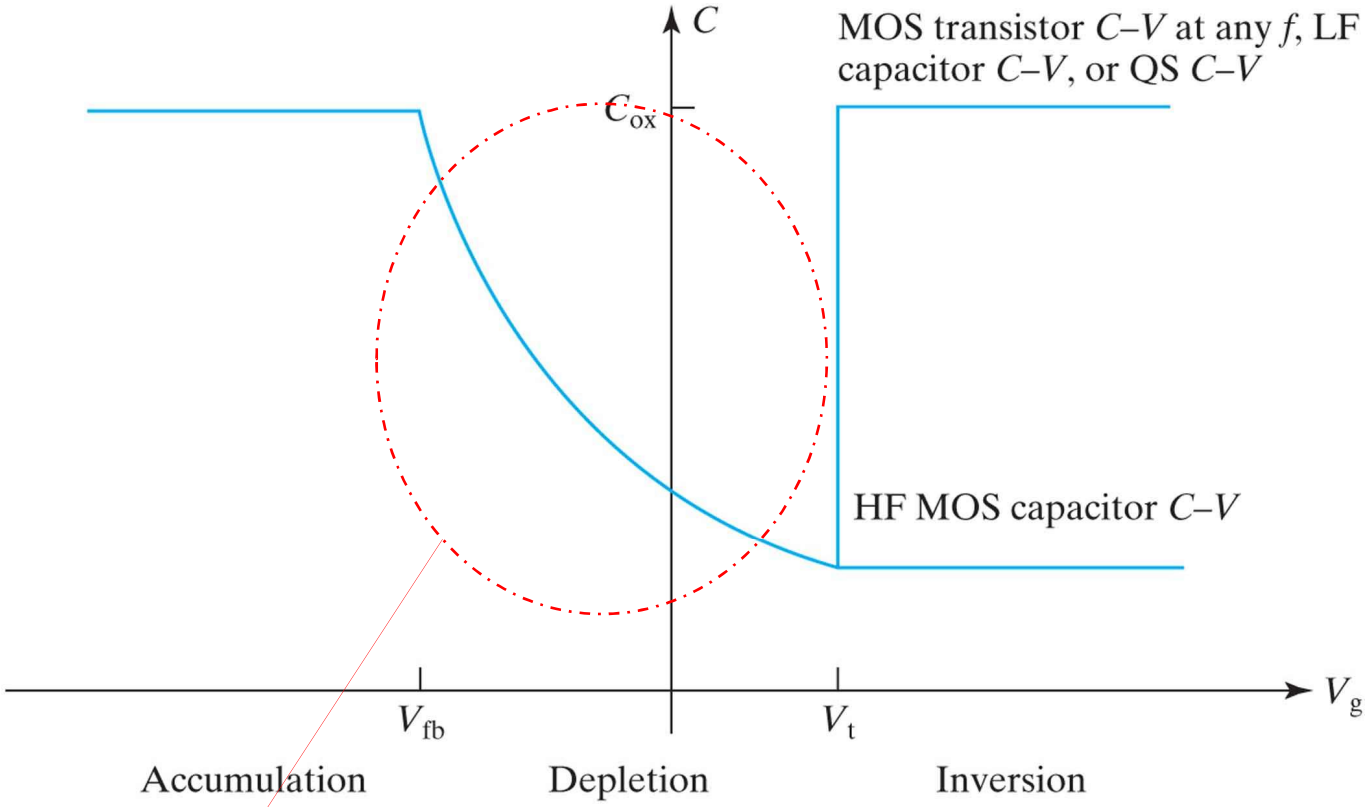
(d)

$$\frac{1}{C}=\frac{1}{C_{min}}=\frac{1}{C_{ox}}+\frac{1}{C_{d\,min}}$$

$$C_{d\,min}=\frac{\varepsilon_s}{W_{d\,max}}$$

inversion region with efficient supply of inversion electrons from the N region (corresponding to **the transistor *C–V* or the quasi-static *C–V***)

*inversion region with no supply of inversion electrons (or weak supply by thermal generation) corresponding to **the high-frequency capacitor C–V case**.*



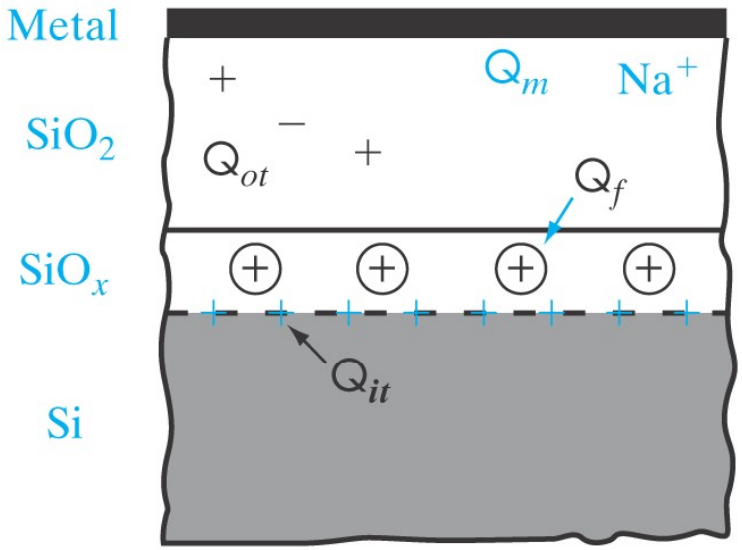
$$V_g = V_{fb} + \phi_s + V_{ox} = V_{fb} + \frac{qN_aW_{dep}^2}{2\varepsilon_s} + \frac{qN_aW_{dep}}{C_{ox}} \Rightarrow V_g - V_{fb} = \frac{qN_aW_{dep}^2}{2\varepsilon_s} + \frac{qN_aW_{dep}}{C_{ox}}$$

$$\Rightarrow \frac{2(V_g - V_{fb})}{qN_a\varepsilon_s} = \frac{W_{dep}^2}{\varepsilon_s^2} + \frac{2W_{dep}}{C_{ox}\varepsilon_s}$$

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} = \sqrt{\left(\frac{1}{C_{ox}} + \frac{1}{C_{dep}}\right)^2} = \sqrt{\frac{1}{C_{ox}^2} + \frac{2}{C_{ox}C_{dep}} + \frac{1}{C_{dep}^2}} = \sqrt{\frac{1}{C_{ox}^2} + \frac{2W_{dep}}{C_{ox}\varepsilon_s} + \frac{W_{dep}^2}{\varepsilon_s^2}} = \sqrt{\frac{1}{C_{ox}^2} + \frac{2(V_g - V_{fb})}{qN_a\varepsilon_s}}$$

where $C_{dep} = \frac{\varepsilon_s}{W_{dep}}$

Oxide Charge-A Modification to V_{fb} and V_t



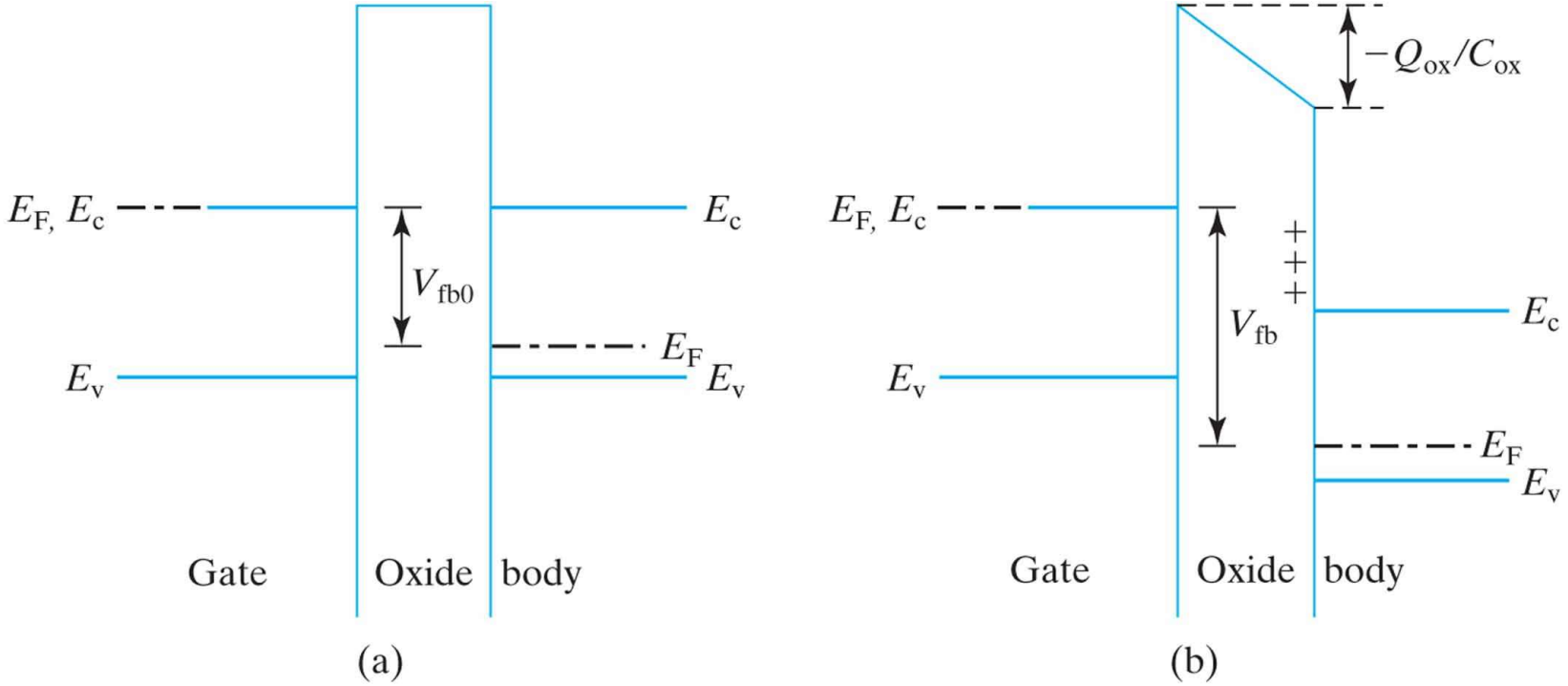
- **Q_m(mobile ionic charge);**
  cause instabilities in V_{fb} and V_t.
- **Q_{ot} (oxide trapped charge)**
- **Q_f (fixed oxide charge)**
- **Q_{it} (interface trapped charge);**
  degrade the substrate current of MOSFET.

Reliability

More Q_{it} and Q_f appear after the oxide is subjected to high field some time due to the breaking or rearrangement of chemical bonds

This raises a reliability concern because the V_t.

Oxide Charge-A Modification to V_{fb} and V_t



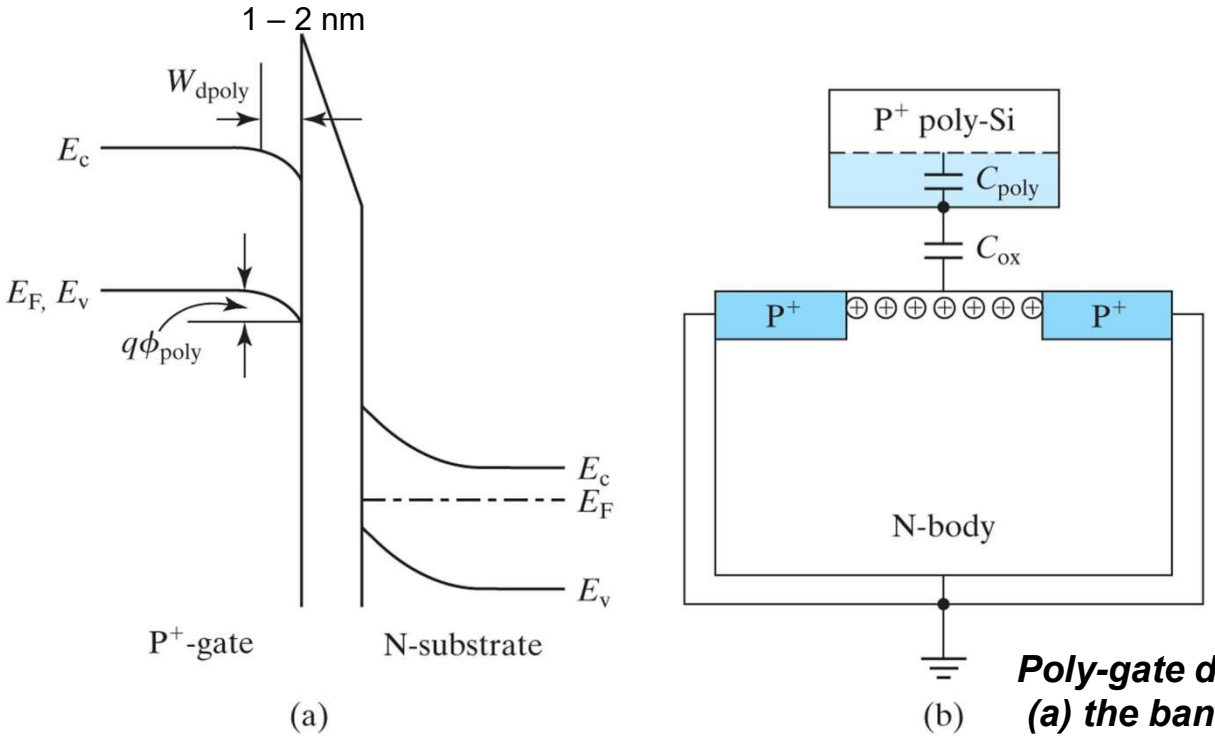
Flat-band condition (no band bending at body surface)

(a) without any oxide charge; (b) with Q_{ox} at the oxide–substrate interface.

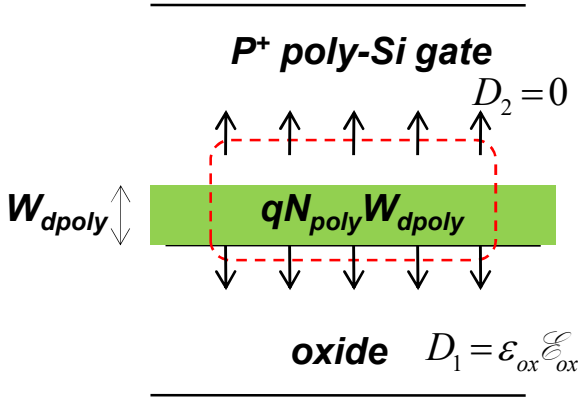
$$V_{fb0} = \psi_g - \psi_s \quad \Rightarrow \quad V_{fb} = V_{fb0} - \frac{Q_{ox}}{C_{ox}} = \psi_g - \psi_s - \frac{Q_{ox}}{C_{ox}}$$

$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}}$$

Poly-Si Gate Depletion-Effective Increase in T_{ox}



Poly-gate depletion effect illustrated with (a) the band diagram and (b) series capacitors representation. An N+ poly-Si gate can also be depleted.



According to Gauss's Law,

$$D_1 + D_2 = -\varepsilon_{ox}\mathscr{E}_{ox} = -qN_{poly}W_{dpoly}$$

$$W_{dpoly} = \frac{\varepsilon_{ox}\mathscr{E}_{ox}}{qN_{poly}}$$

Poly-Si Gate Depletion-Effective Increase in T_{ox}

The MOS capacitance in the inversion region becomes

$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_{poly}} \right)^{-1} = \left(\frac{T_{ox}}{\varepsilon_{ox}} + \frac{W_{dpoly}}{\varepsilon_s} \right)^{-1} = \frac{\varepsilon_{ox}}{T_{ox} + W_{dpoly}/3}$$

Poly-depletion effect effectively increases T_{ox} by $W_{dpoly}/3$, and can have a significant impact on the C-V curve if T_{ox} is thin.

$$where \frac{\varepsilon_s}{\varepsilon_{ox}} \approx 3$$

Solutions; 1) dope the **poly-Si heavily** (can cause dopant penetration from the gate through the oxide into the substrate).
2) use **poly-SiGe gate** to be doped to a higher concentration.
3) substitute the poly-Si gate with **a metal gate.**

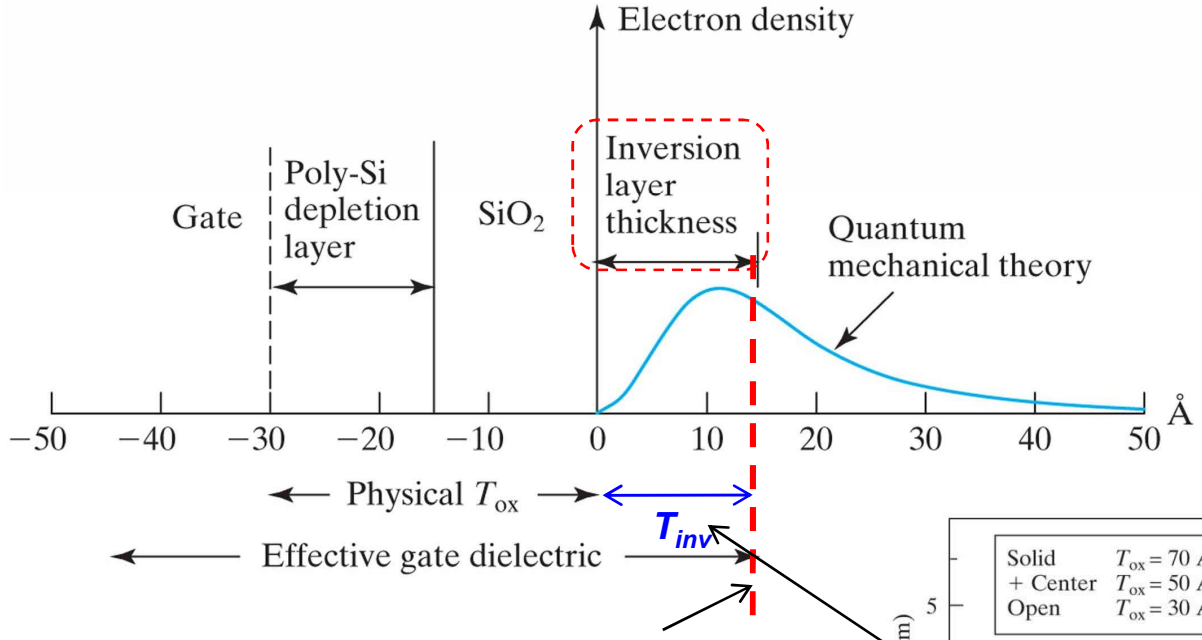
Poly-depletion effect is undesirable because a reduced C means reduced Q_{inv} and reduced transistor current.

$$Q_{inv} = -C_{ox}(V_g - \phi_{poly} - V_t)$$

Poly-gate depletion effectively reduces V_g by ϕ_{poly} .

Even 0.1 V ϕ_{poly} would be highly undesirable when the power-supply voltage is only around 1 V.

Inversion and Accumulation Charge-Layer Thicknesses and Quantum Mechanical Effect



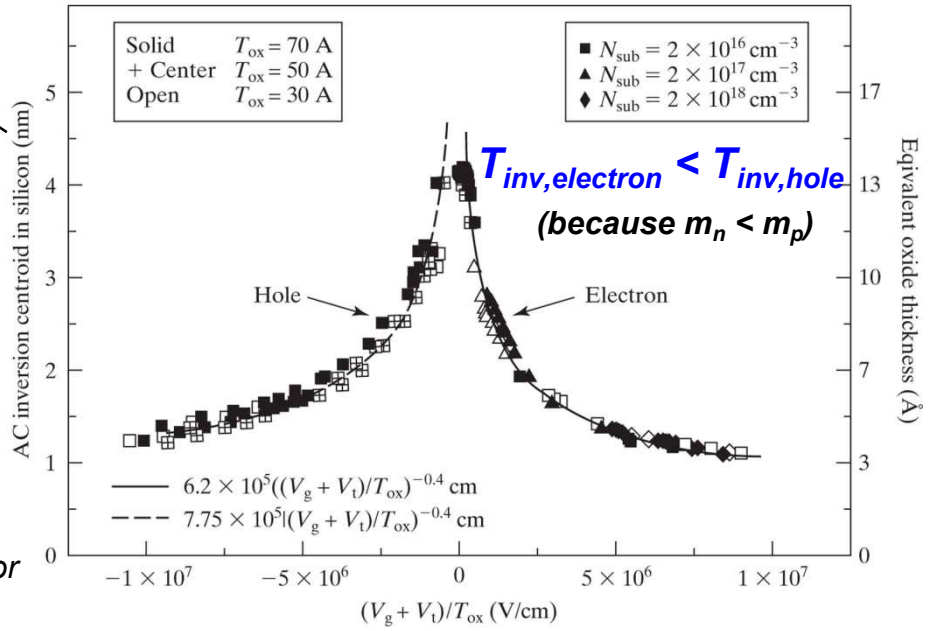
Effective bottom electrode of the MOS capacitor

$$Effective\ T_{ox} \approx T_{ox} + T_{inv}/3$$

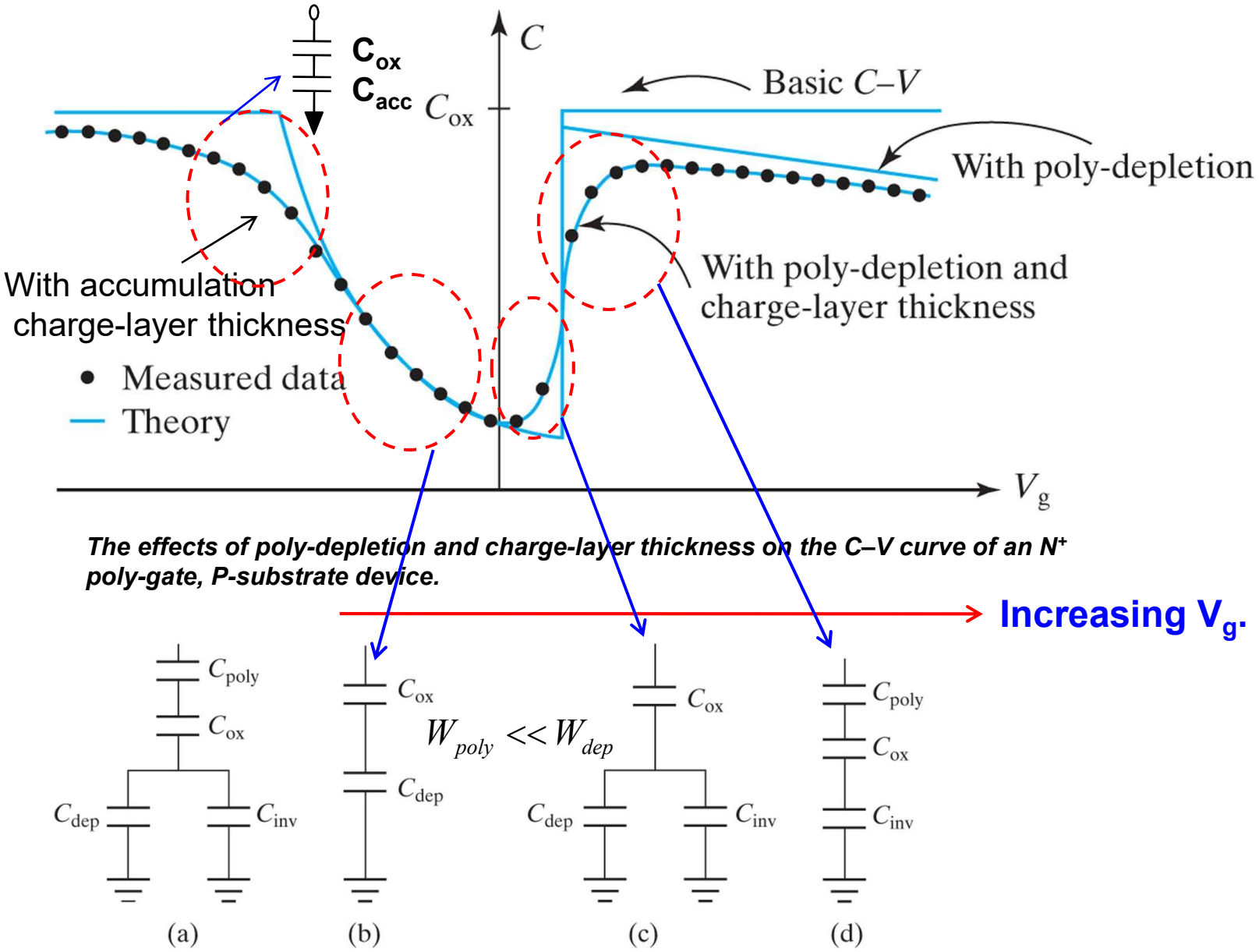
$$where\ 3 \approx \frac{\varepsilon_s}{\varepsilon_{ox}}$$

Average field in the inversion layer

$$= \frac{V_g + V_t}{6T_{ox}}$$



Average inversion-layer thickness (centroid) for electrons (in P body) and holes (in N body). (From [3]. © 1999 IEEE.)



The effects of poly-depletion and charge-layer thickness on the C–V curve of an N⁺ poly-gate, P-substrate device.

Equivalent circuit for understanding the C–V curve in the depletion region and the inversion region. (a) General case for both depletion and inversion regions; (b) in the depletion regions; (c) $V_g \approx V_t$; and (d) strong inversion.

Effective Oxide Thickness

- T_{inv} and W_{poly}: not negligible for thinner T_{ox} with thickness of < 10 nm
- Because it is difficult to separate T_{ox} from T_{inv} and W_{poly} by measurement, an **electrical oxide thickness, T_{oxe}**, is often used to characterize the total **effective oxide thickness.**
  (T_{oxe} is deduced from the inversion-region capacitance measured at $V_g = V_{dd}$.)
- **T_{oxe}** : an **effective oxide thickness** corresponding to an **effective gate capacitance, C_{oxe}.**

Total inversion charge per area, **Q_{inv}**, is

$$Q_{inv} = -C_{oxe}(V_g - V_t) = -\frac{\varepsilon_{ox}}{T_{oxe}}(V_g - V_t)$$

$$T_{oxe} = T_{ox} + W_{poly}/3 + T_{inv}/3 \qquad where \frac{\varepsilon_s}{\varepsilon_{ox}} \approx 3$$

Typically, T_{oxe} is larger than T_{ox} by 0.6-1.0 nm .

Quantum Effect on Threshold Voltage

At high substrate doping concentration, the high electric field in the substrate at the oxide interface causes energy levels to be **quantized** and effectively **increases E_g** and **decreases n_i**. This requires the band to bend down more before reaching threshold, i.e., causes ϕ_{st} to increase.

$$\phi_s = \phi_{st} = 2\phi_B = \frac{2kT}{q}\ln\frac{N_a}{n_i} \qquad V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}}$$

➡ The net effect is that the threshold voltage is increased by 100 mV or so depending on the doping concentration

CCD Imager and CMOS Imager

used in digital cameras and camcorders

- **CCD (Charge-Coupled Device) Imager:**
  1) high performance(good uniformity and contrast ratio)
  2) small number of sophisticated sensing circuits
  3) expensive.
- **CMOS Imager:**
  1) small area and less expensive
  2) compatible with CMOS IC technology
  3) easily integrated with signal processing and control circuits
  4) less power.

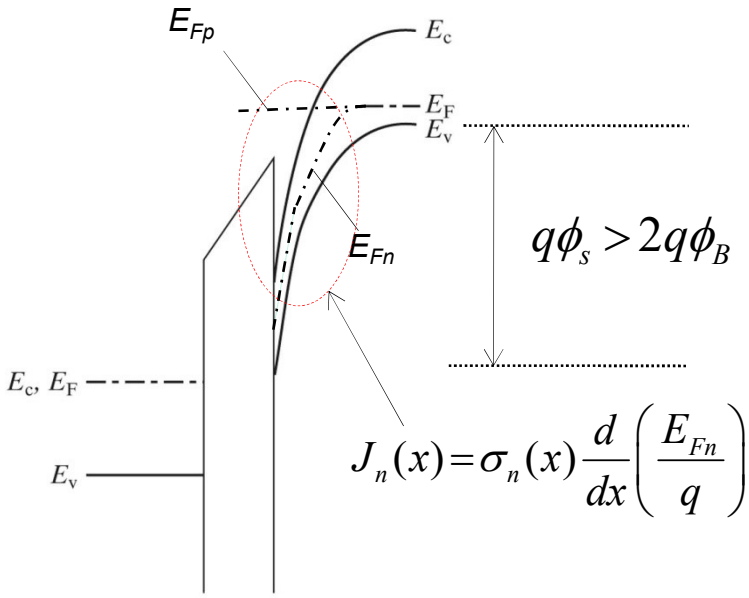
CCD Imager

The heart of a CCD imager is a large number of MOS capacitor densely packed in a two-dimensional array.

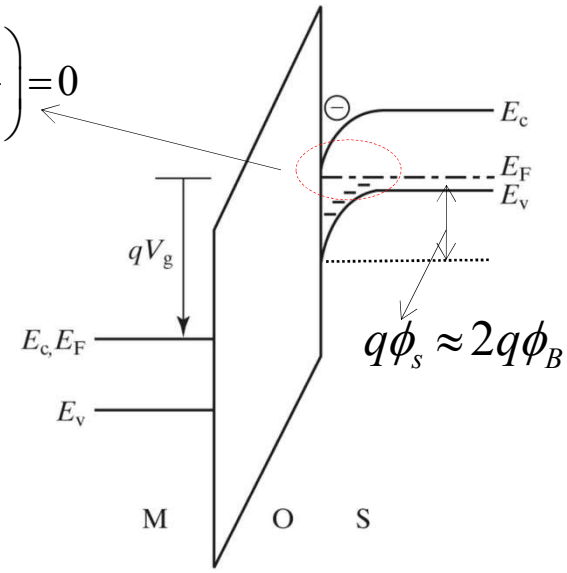
Deep Depletion

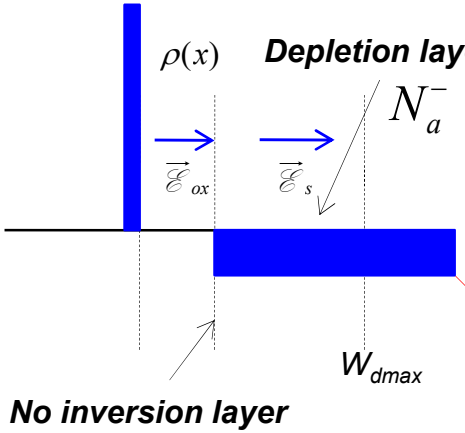
When a voltage, $V_g > V_t$, has been suddenly applied to the gate, an MOS capacitor is driven into nonequlibrium where *there are no electrons (no inversion layer) at the surface, because thermal generation is a slow process* ***and,*** in balancing the charge added to the gate, the depletion width becomes greater than W_{dmax} to offset the missing minority carriers. This called **"deep-depletion".**

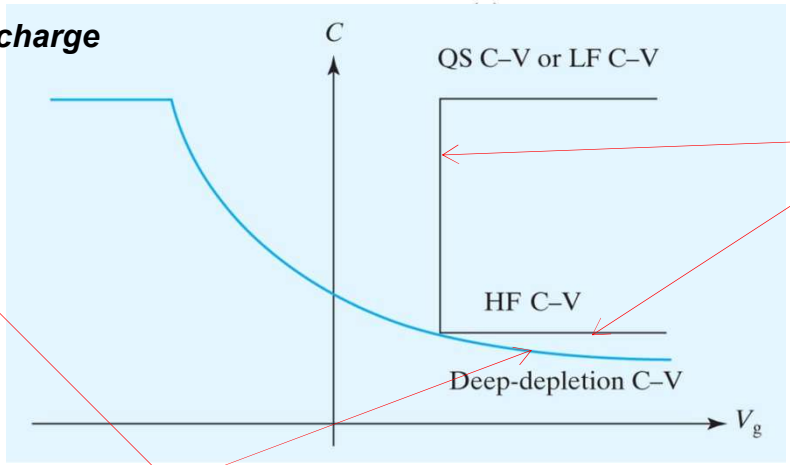
$$W_d > W_{d\max} \quad and \quad \phi_s > 2\phi_B$$

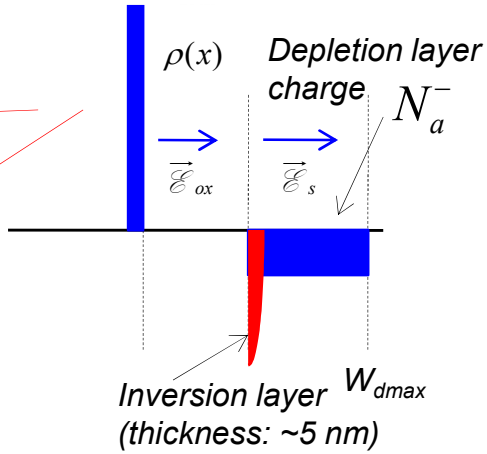


$$J_n(x) = \sigma_n(x)\frac{d}{dx}\left(\frac{E_{Fn}}{q}\right) = 0$$

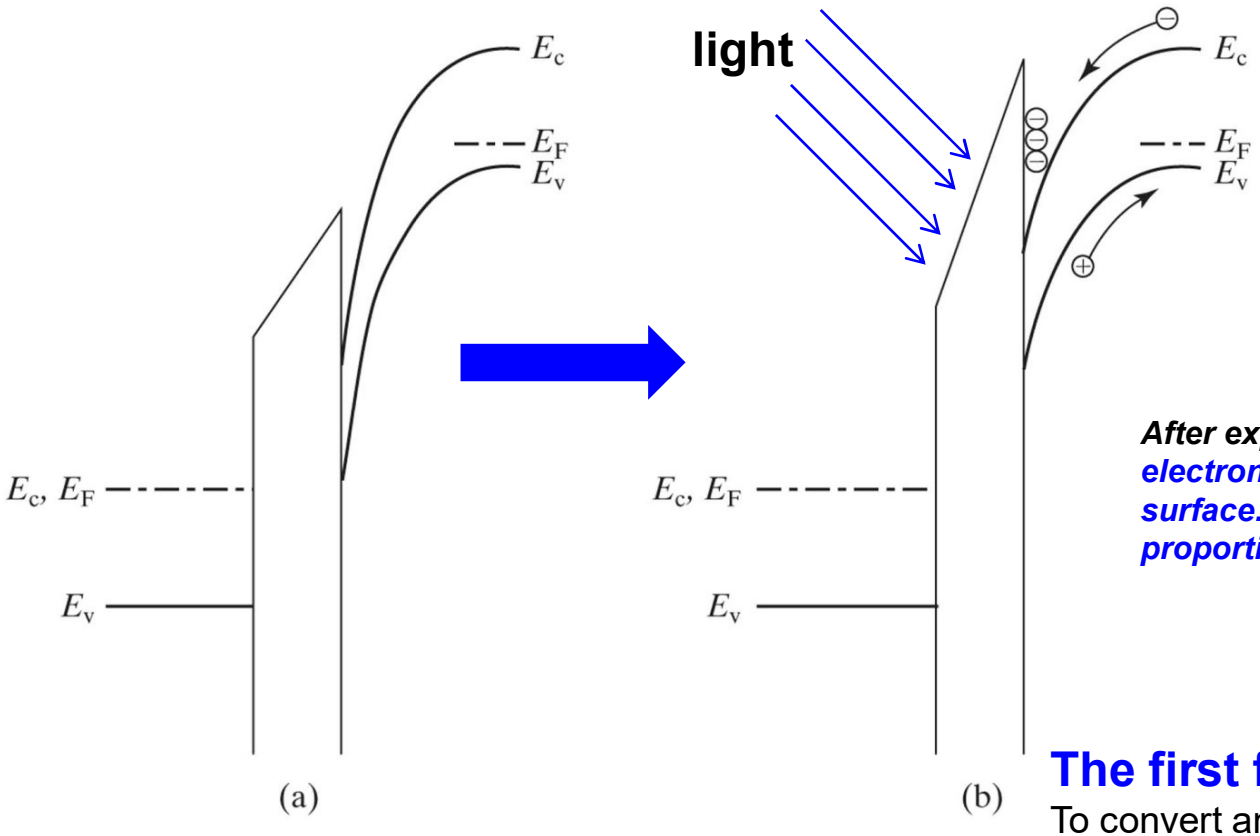








Deep-depletion C–V



After exposure to light, photo-generated electrons have been collected at the surface. The number of electrons is proportional to the light intensity.

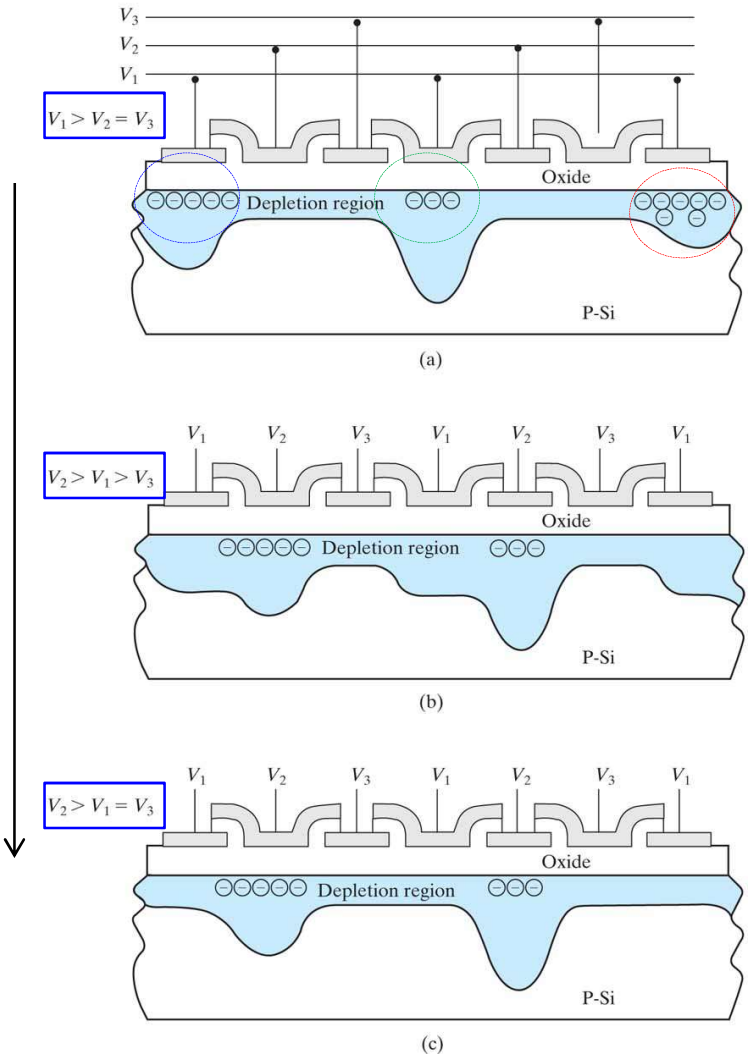
The first function of CCD array:

To convert an image(two-dimensional pattern of light intensity) into packets of electrons stored in a two-dimensional array of MOS capacitor

The second function of CCD array:

To transfer the collected charge packets to the edge of the array, where they can be read by a charge sensing circuit in a serial manner.

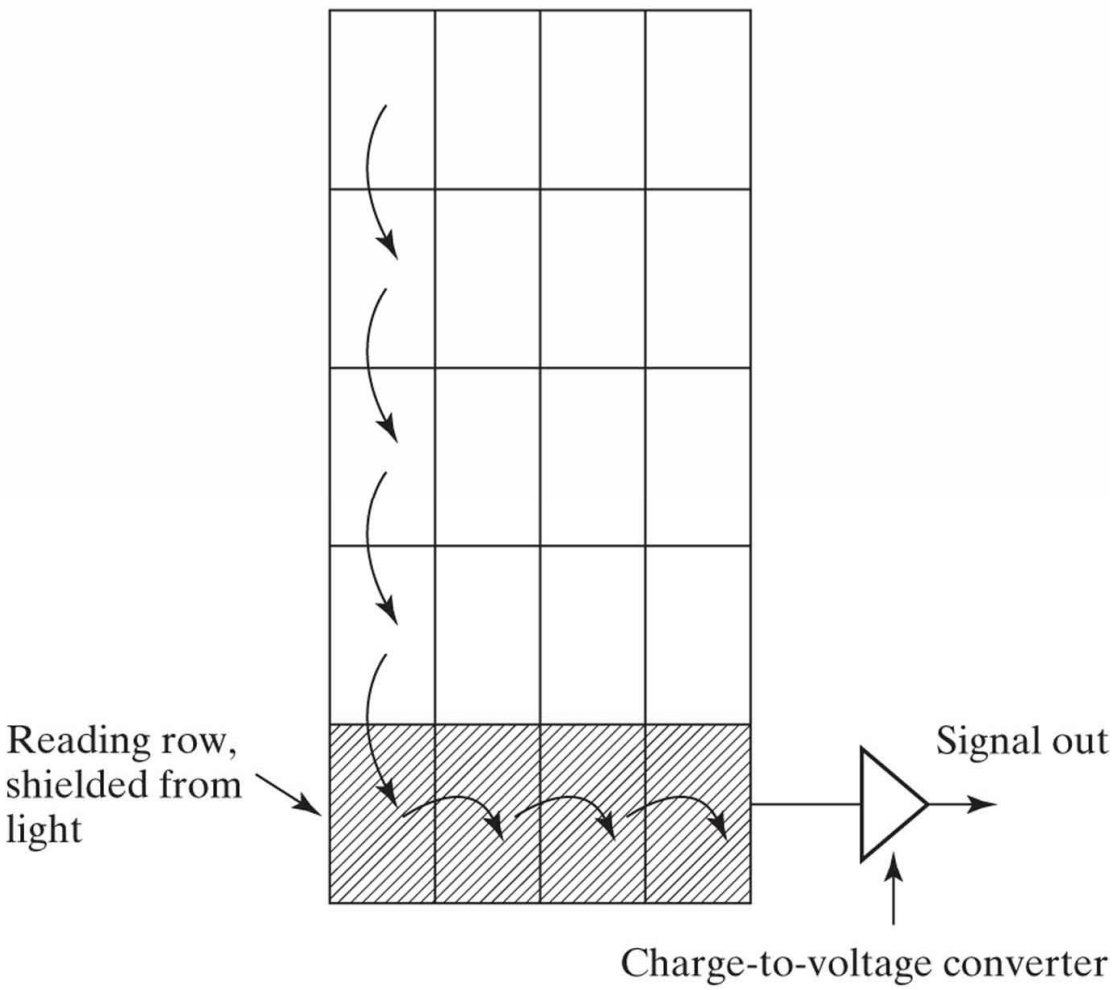
How does CCD shift the charge packets?



- **V_1 creates the deepest depletion.**
- Exposure to a lens-projected image has produced some electrons in the element on the right, even more in the element on the left and yet more in the middle element in proportion to the image light intensity around those three locations.
- **V_2 creates the deepest depletion.**
- The charge packets will move to the elements connected to V_2 (i.e., shifted to the right by one element. The choice of $V_1 > V_3$ ensures that no electrons are transferred to the left.
- **V_1 is reduced to the same values as V_3.**
- The drawing in (c) is identical to (a) but with all the charge packets shifted to the right by one capacitor element.

The array is biased in the sequence (a), (b), (c), (a), (b), (c), (a) ... .
In this manner the electron packets are shifted to the right element by element.

Waiting at the right edge of the array is a **charge-sensing circuit** that generates a serial voltage signal that faithfully represents the image light pattern.



[Architecture of a two-dimensional CCD imager]
The arrows show the path of the charge-packet movement.

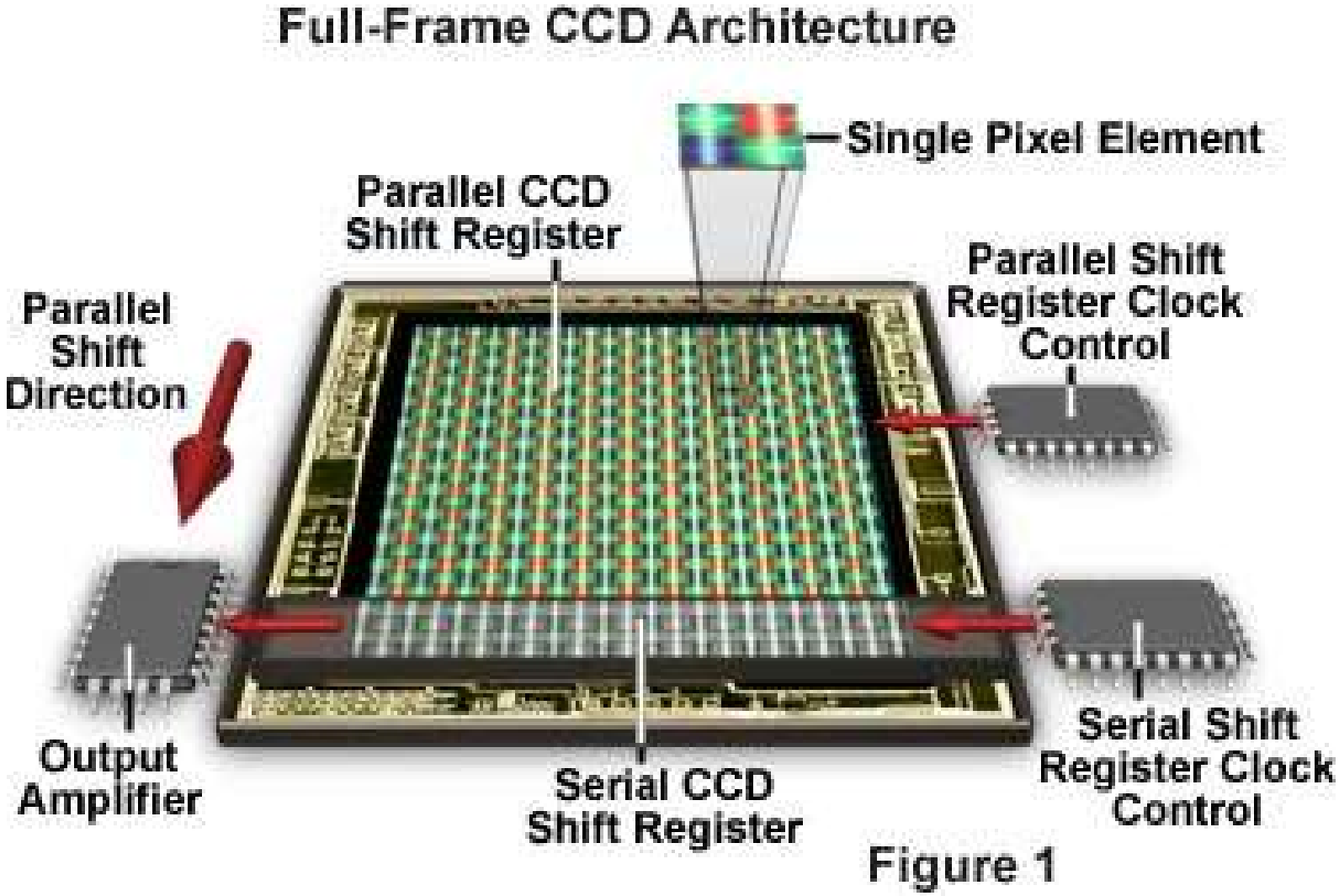
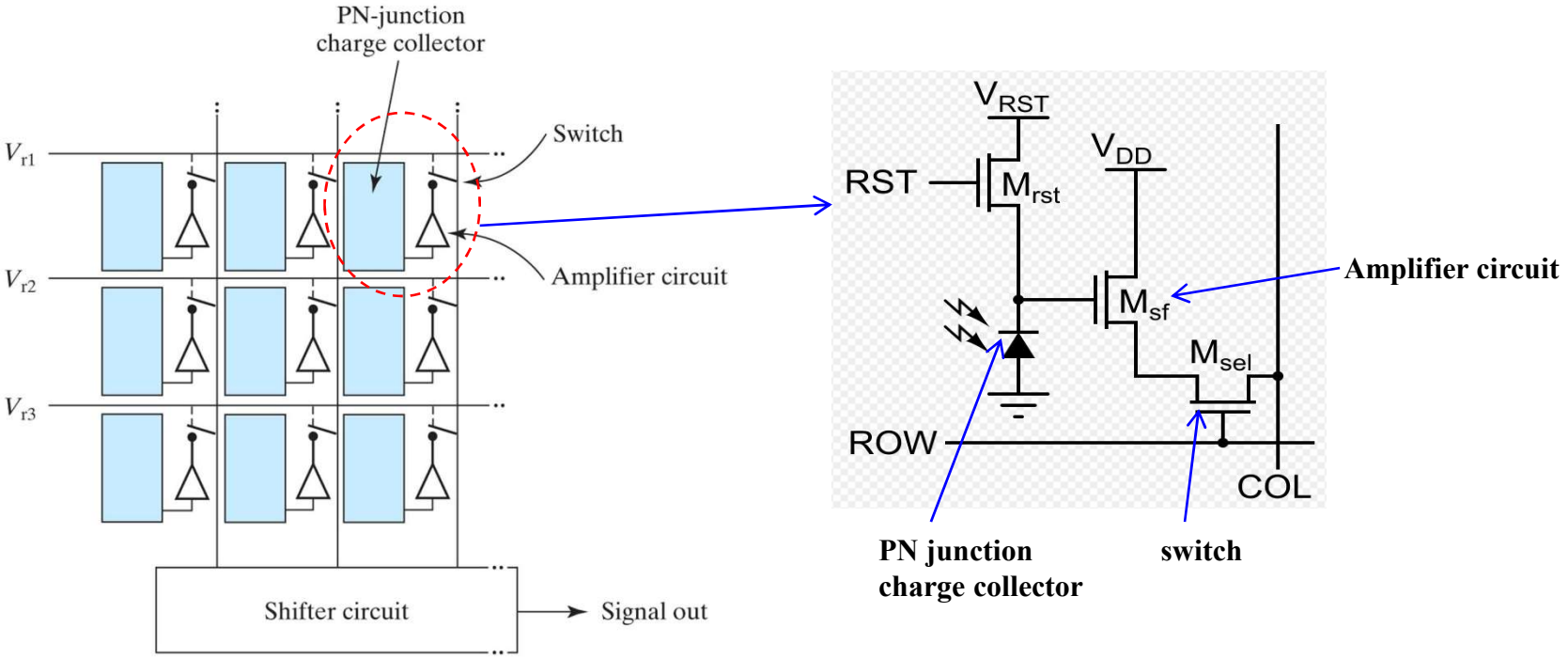

Full-Frame CCD Architecture
Single Pixel Element
Parallel CCD
Shift Register
Parallel Shift
Register Clock
Control
Parallel
Shift
Direction
Output
Amplifier
Serial CCD
Shift Register
Serial Shift
Register Clock
Control

Figure 1

CMOS Imager

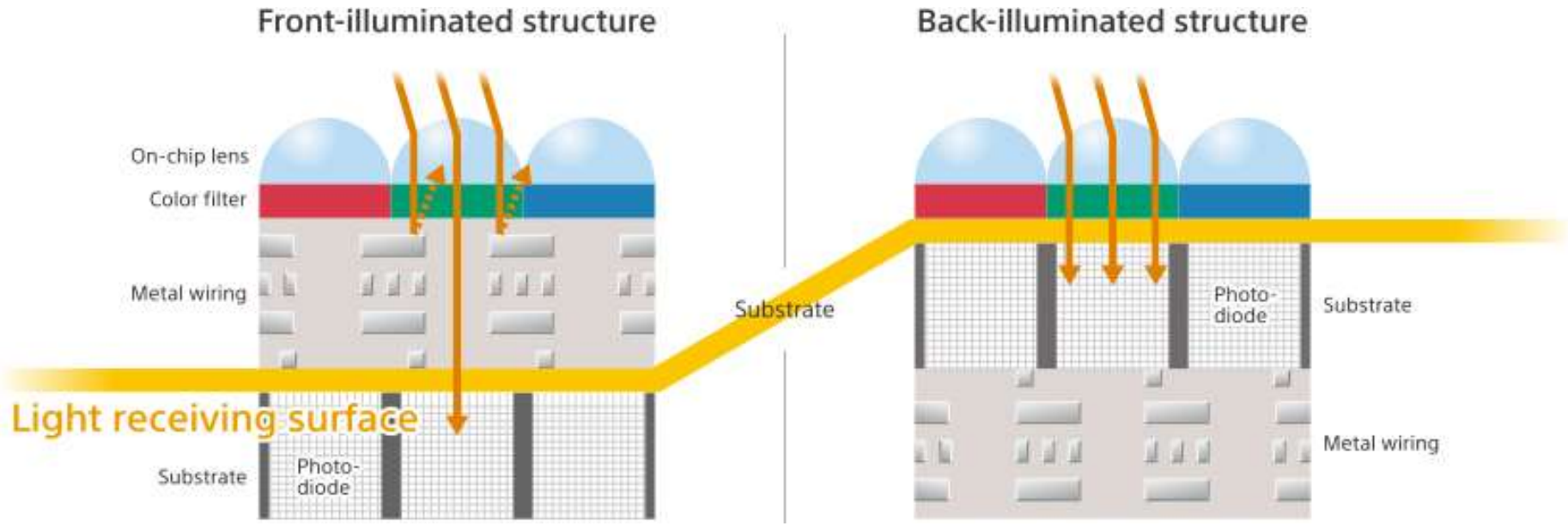
- Electrons generated by light near the PN junction diffuse to junction and get collected and stored in the thin N^+-region. Since the PN junction is a capacitor, the stored electrons change the capacitor voltage, i.e., the N^+-region voltage. This voltage is amplified in the pixel as shown in the figure below.

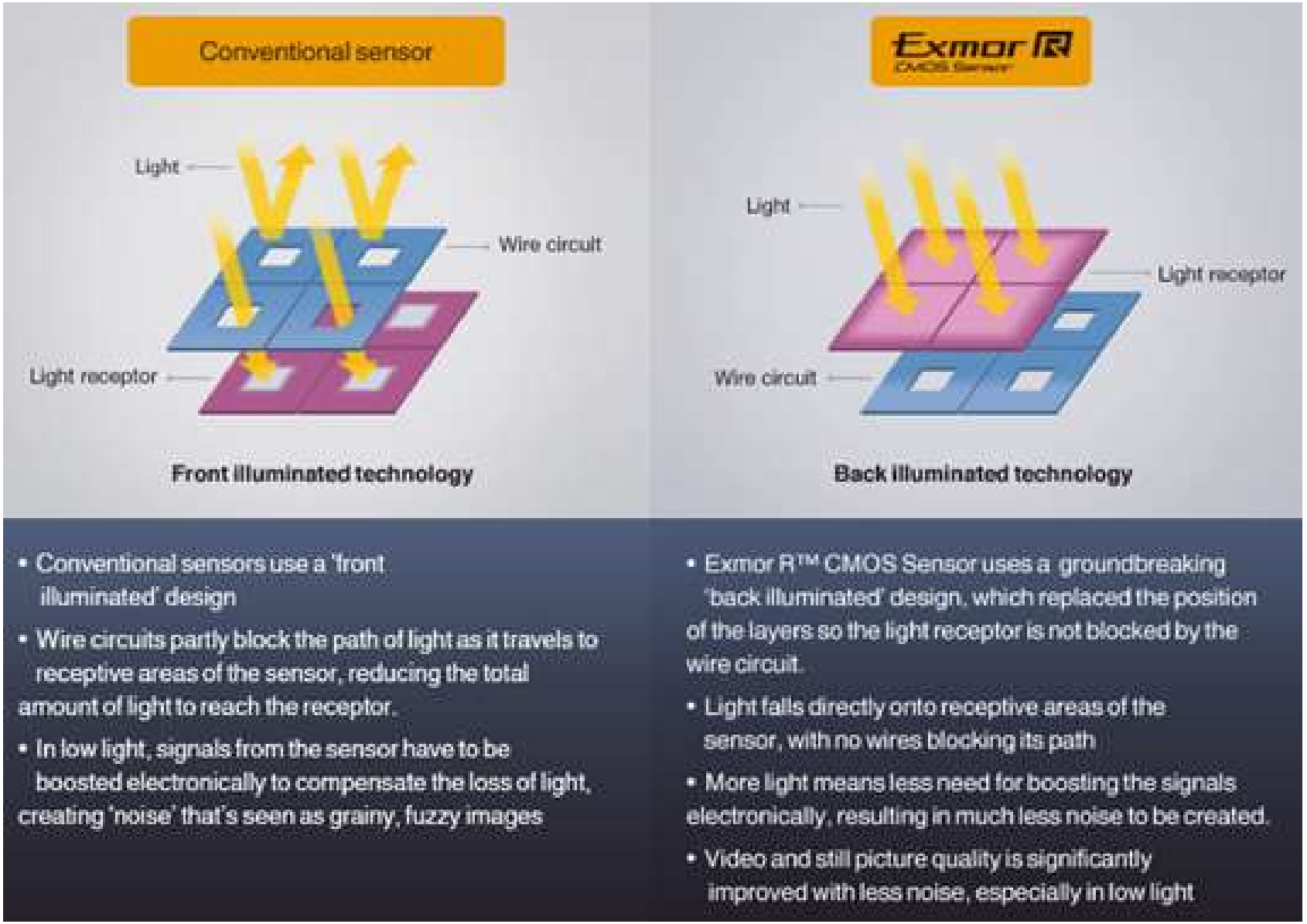
- Each pixel also contains a switch made of an MOS transistor and controlled by the voltage V_{r1}, V_{r2}, or V_{r3}. In order to read the top row of pixels, V_{r1} is raised to turn on (close) all the switches in the top row. This brings the signals from all the top-row pixels to the shifter circuit.

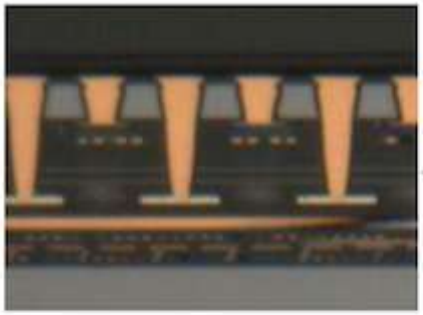


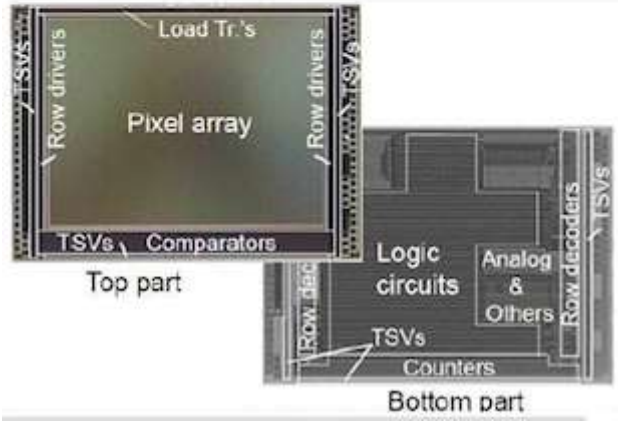
[Architecture of a CMOS imager]

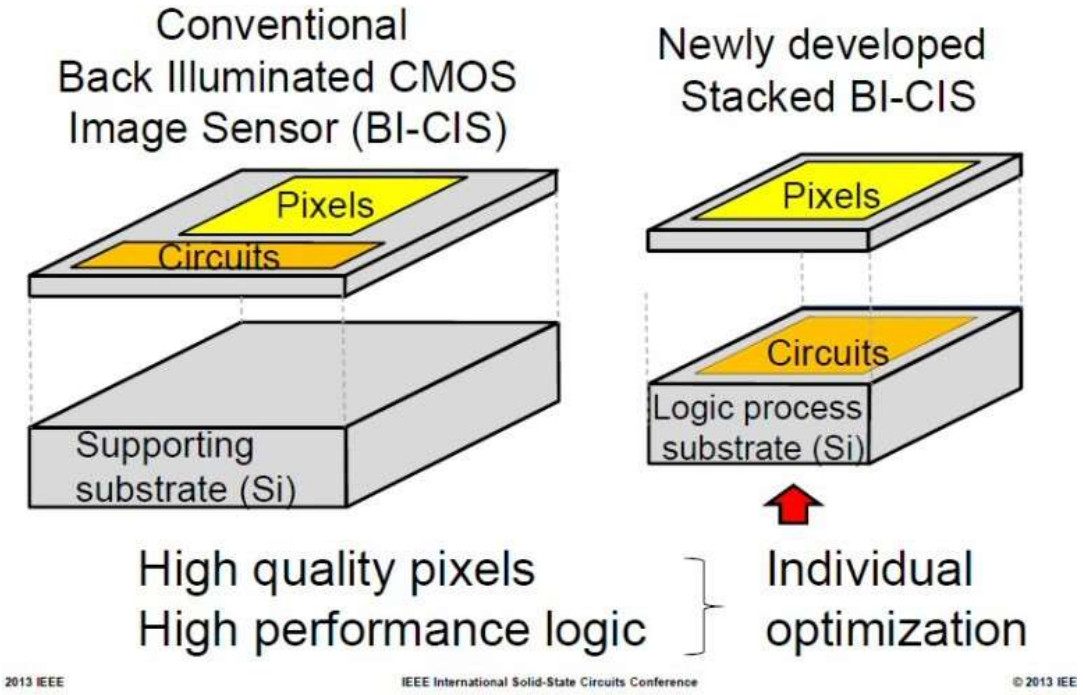
Each array element has its own charge-to-voltage converter represented by the triangle. Actual imagers may support hundreds to over a thousand rows and columns of pixels.


Front-illuminated structure
Back-illuminated structure
On-chip lens
Color filter
Metal wiring
Light receiving surface
Substrate
Photo-diode
Substrate
Photo-diode
Substrate
Metal wiring


Conventional sensor
Light
Wire circuit
Light receptor
Front illuminated technology
• Conventional sensors use a 'front illuminated' design
• Wire circuits partly block the path of light as it travels to receptive areas of the sensor, reducing the total amount of light to reach the receptor.
• In low light, signals from the sensor have to be boosted electronically to compensate the loss of light, creating 'noise' that's seen as grainy, fuzzy images
Exmor R
CMOS Sensor
Light
Light receptor
Wire circuit
Back illuminated technology
• Exmor R™ CMOS Sensor uses a groundbreaking 'back illuminated' design, which replaced the position of the layers so the light receptor is not blocked by the wire circuit.
• Light falls directly onto receptive areas of the sensor, with no wires blocking its path
• More light means less need for boosting the signals electronically, resulting in much less noise to be created.
• Video and still picture quality is significantly improved with less noise, especially in low light


top
layer
bottom
layer

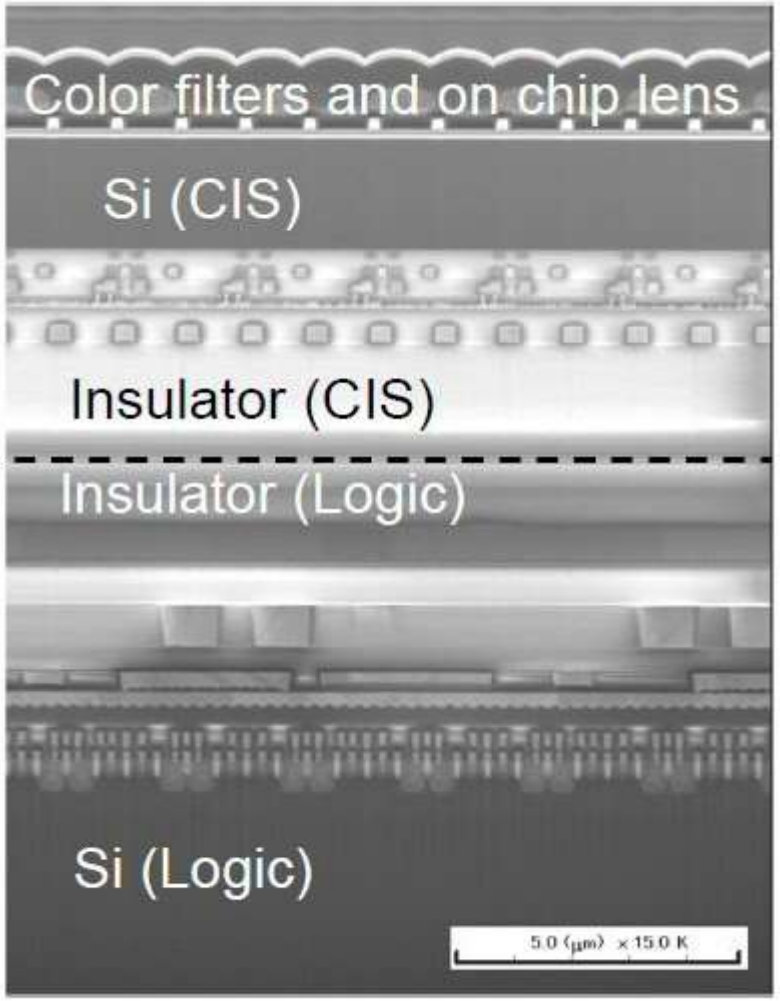

Load Tr.'s
Row drivers
Pixel array
Row drivers
TSVs
TSVs
Comparators
Top part
Logic
circuits
Analog
&
Others
Row decoders
TSVs
TSVs
Counters
Bottom part


Conventional
Back Illuminated CMOS
Image Sensor (BI-CIS)
Pixels
Circuits
Supporting
substrate (Si)
Newly developed
Stacked BI-CIS
Pixels
Circuits
Logic process
substrate (Si)
High quality pixels
High performance logic
Individual
optimization
2013 IEEE
IEEE International Solid-State Circuits Conference
© 2013 IEE

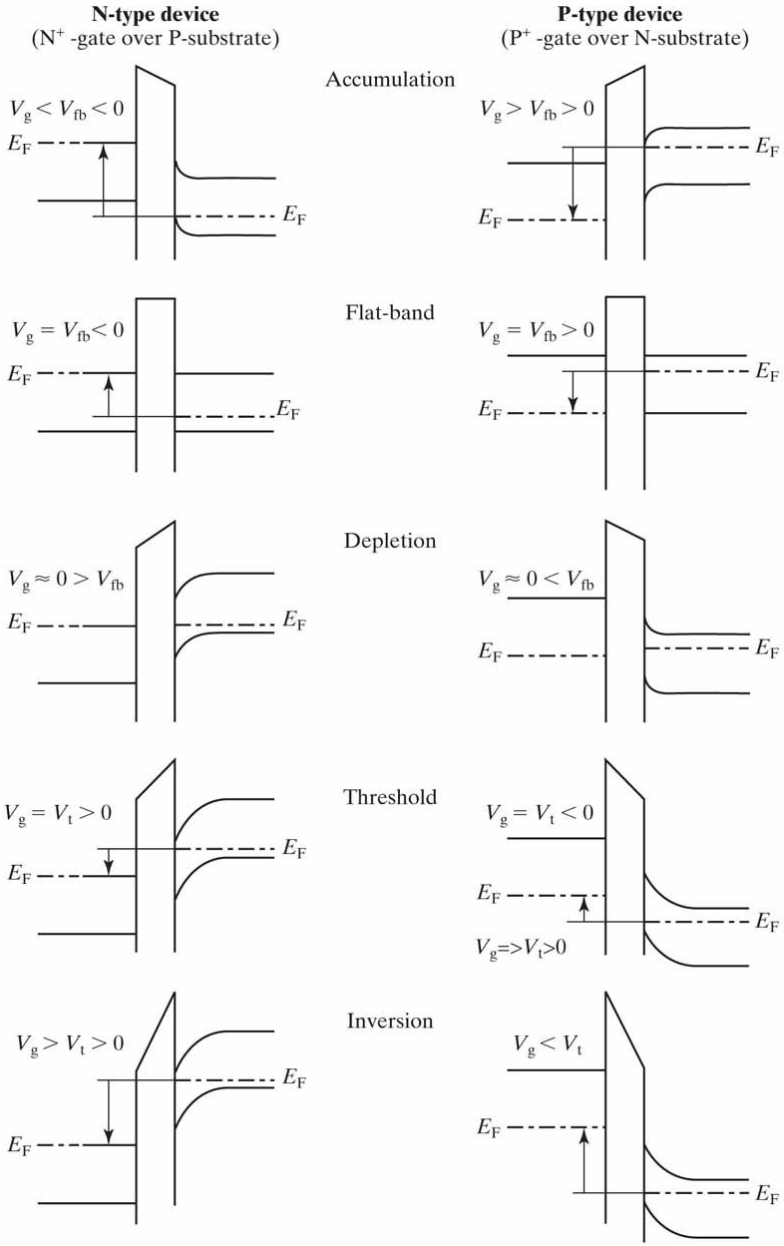
Top part
(BI-CIS
process technology)

Bottom part
(Logic
process technology)

Top-Bottom connections are
TSV type vertical interconnects.
(not described here)



Chapter Summary



Flat-band voltage

$$V_{fb} = \psi_g - \psi_s - Q_{ox} / C_{ox}$$

Gate voltage

$$V_g = V_{fb} + \phi_s + V_{ox} + \phi_{poly} = V_{fb} + \phi_s - Q_{sub} / C_{ox} + \phi_{poly}$$

Threshold voltage

$$V_t = V_g \Big|_{\phi_s = \phi_{st}} = V_{fb} + \phi_{st} + \frac{\sqrt{qN_{sub} 2\varepsilon_s |\phi_{st}|}}{C_{ox}}$$

$$\text{At threshold, } \phi_s = \phi_{st} = \pm 2\phi_B = \pm \frac{2kT}{q} \ln \frac{N_{sub}}{n_i}$$

Electrical oxide thickness

$$T_{oxe} = T_{ox} + W_{poly} / 3 + T_{inv} / 3$$