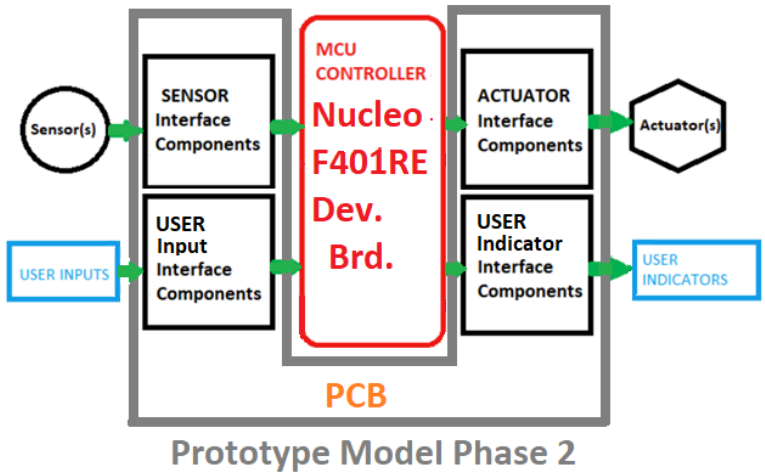
Lab 4 – Prototype Phase 2 - Instructions

ECE 298 – S2021

Overview

A final step in this prototype phase is to design a Printed Circuit Board (PCB) Layout that accounts for the required PCB dimensions (form factor), the component locations on the PCB (placement), and how the components are connected via copper "traces" (routing). The PCB will be a two-layer design, and you may place components on both sides of the board. The Lab 4 Proteus project file provides an initial layout that can connect mechanically to a NUCLEO-F401RE development board as a "daughter card".



Prototype Model Phase 2

Deliverables

Submit a single .zip file that contains all the required items from Proteus:

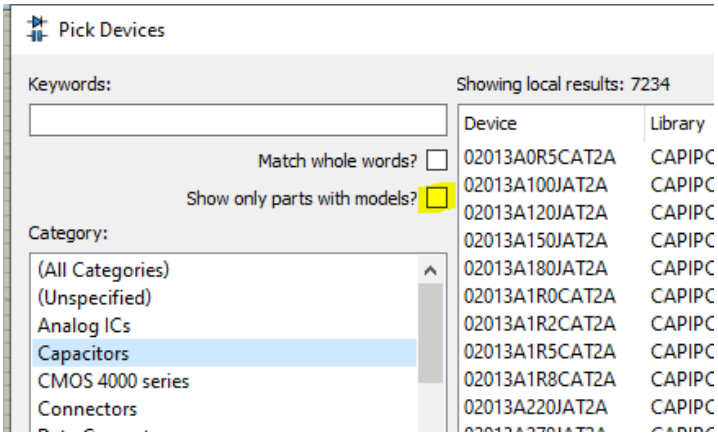
- A single Proteus project file (.pdsprj) that contains:
  - Schematic with all nets named and belonging to a net class
  - PCB Layout with proper power and signal routing, decoupling, and silkscreens
- Additional generated documents:
  - Netlist Report (Schematic Capture window, Tool → Netlist Compiler)
  - Pre-Production Check Report (PCB Layout window, Output → Pre-Production Check, copy and save to .txt file)
  - Pick and Place File (PCB Layout window, Output → Generate Pick and Place File – in .csv format)
  - The following Gerber layers and the corresponding READ-ME file: Copper, Silk, Resist, and Paste for both the Top and Bottom layers, and a Drill layer
  - 3D Visualizer views exported as .pdfs (Make a document of screen captures, or File → Print 3D View → Print to PDF for each view)
  - Bill of Materials window exported as a .pdf file

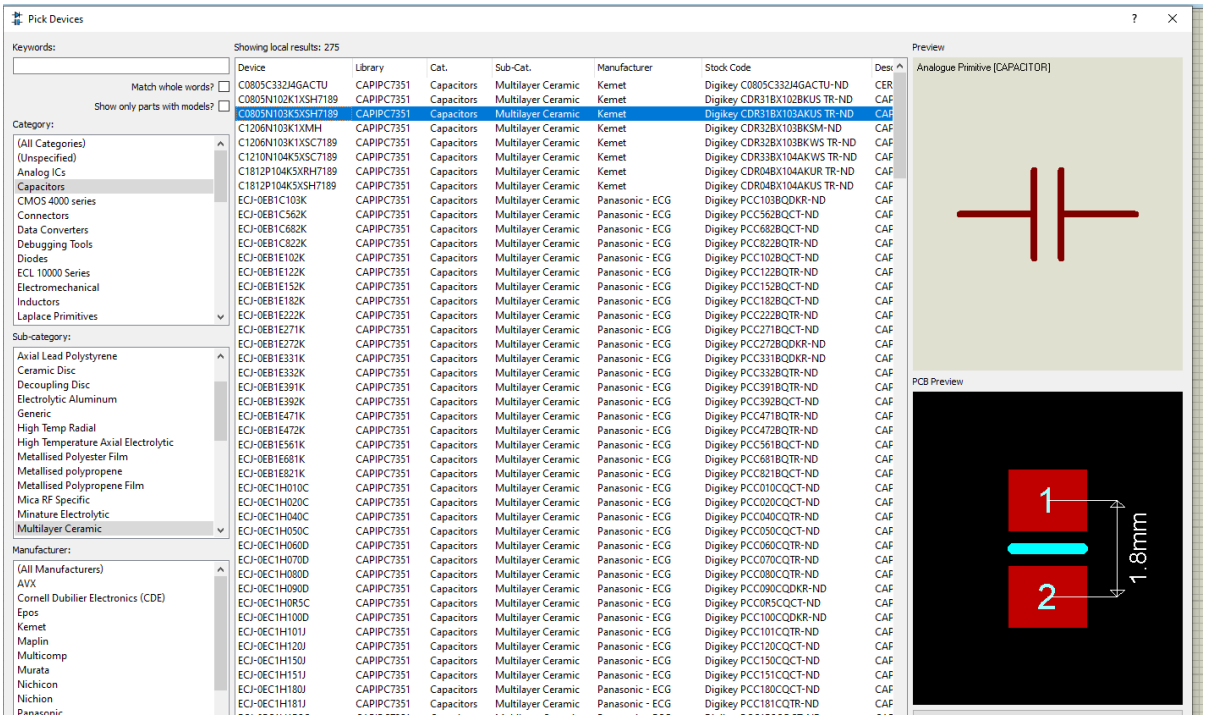
Instructions: Schematic Preparation

Open your Proteus Lab 3 project and copy your schematics from the "PROTO_ADAPTER_CKT1" child sheet to the clipboard. Open the Lab 4 project, which just uses one sheet, and paste the schematic contents. Now, we must modify the schematic so we can create a layout based on it.

Step 1: Replace Generic Components

We used generic components to get our designs quickly developed and tested in simulation. For example, we used ECE298_GEN_RES to model any resistor we needed. Still, in reality, we must order a specific resistor (e.g., here are two very different 1 kΩ resistors from Digi-Key: A massive 2500 W resistor and a teeny tiny 200 µm wide surface mount chip resistor). Since the design is now confirmed by simulation, we must replace generic components with "real-world" parts. Comb through your design and **replace any generic passive components (ECE298_GEN_xxx) with parts from the Proteus Libraries that have a PCB footprint and part number details.** For this activity, make sure that in the parts search, that the checkbox for models is unchecked.





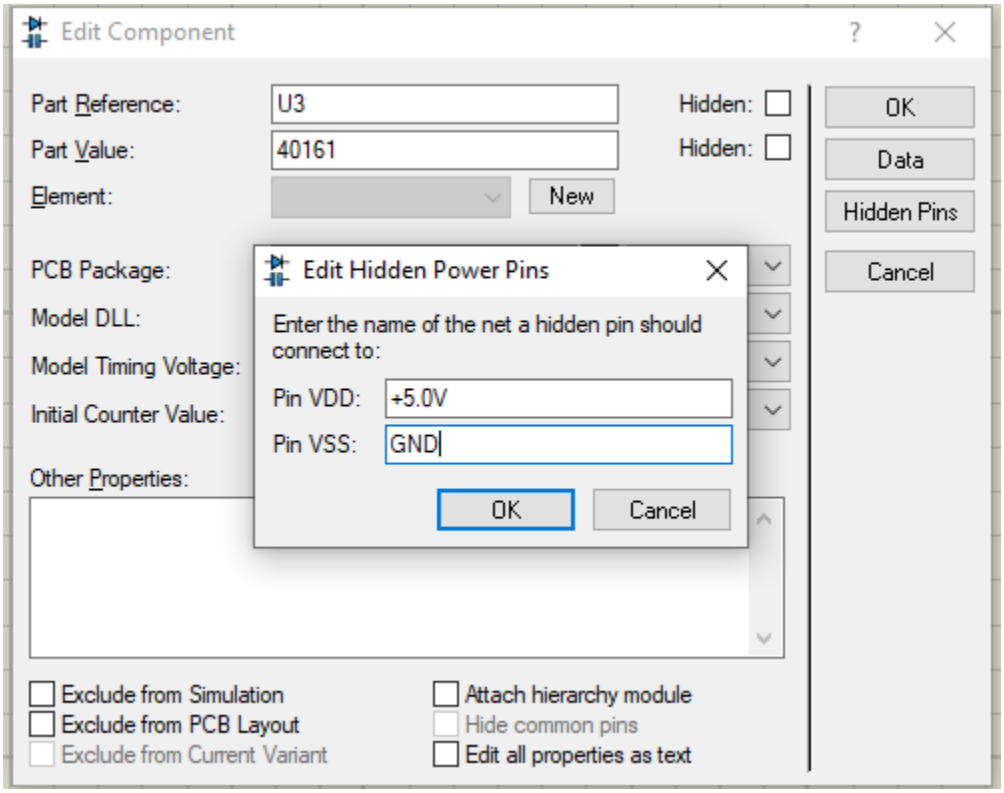
Leave Reference Designators As-Is

Components have default auto-numbered reference designators, like resistors are "R?", capacitors are "C?", etc. When you place the component, the "?" is replaced with an autoincremented number. **Leave**

the default reference designators as-is. The letter prefixes follow a standard that indicates what kind of part it is: https://en.wikipedia.org/wiki/Reference_designator. You may change the numbers of any parts you add, but the numbers must be unique. You can add descriptive text on the schematic and PCB layout (place text on the top or bottom silkscreen layer), but leave the reference designators to conform to the standard.

Step 2: Clarify Component Power Pins

Since VCC/VDD and VEE/VSS can be somewhat ambiguous in a design, we want to replace them with known voltages. Change the power pin connections of any device with "Hidden Power Pins" to use +5.0V and GND. This requirement is specific to Proteus because, realistically, every component must be powered with its specified voltage, which is more likely to be 3.3V or lower for most ICs. For Motor/Encoders, the hidden pins pertain to the Encoder power only (+5.0V). The non-hidden pins for Motor power connect to the high-current motor windings where higher voltages can be applied (related to +12.0V power, perhaps provided through a Motor Controller). Any VSS pin must be changed to a GND connection. For all ICs, (TTL or CMOS from the Proteus libraries), the VCC or VDD is +5.0V.



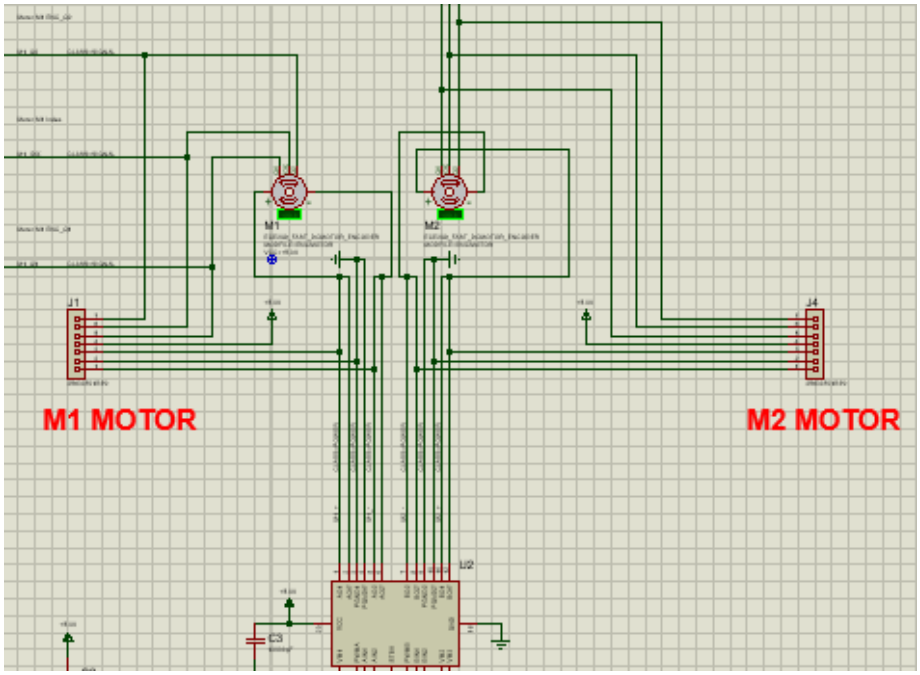
Step 3: Add Connectors

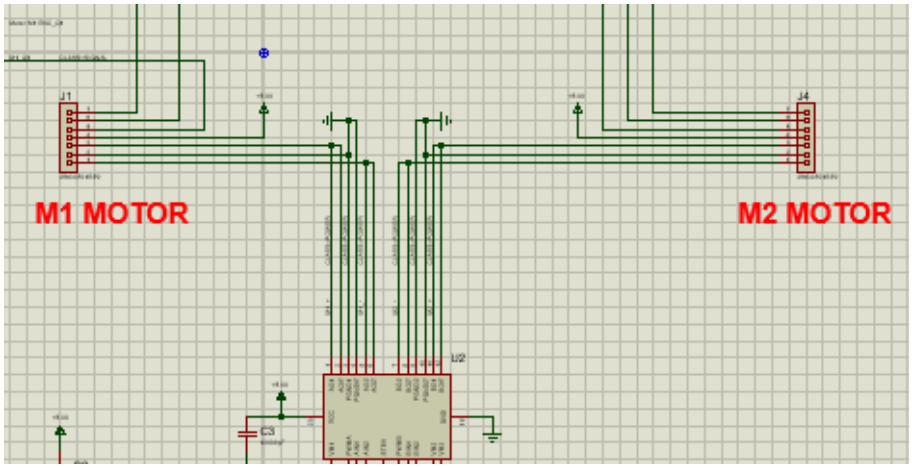
Recall that the sensors, user inputs (including switches), actuators, and some user outputs are to be "off-board", meaning connected by wires to the PCB via on-board connectors. There are a dizzying number of connector types (Digi-Key overview of connector types), and their choice depends on application and cost. We will be using two types commonly found on PCBs: Rectangular connectors for device connections and terminal blocks for high-current power connections.

Non-Power Connectors

A simple connector type to choose from is a 100 mil or 2.00 mm pitch header with standard pin-to-pin spacings. Such a standard pin spacing allows you to try different parts without having to redo the PCB since many connectors would fit. **Remove the off-board devices from your schematic and replace each one with a multi-pin connector to your schematic for each off-board device** (25630x01RP2, CONN-SILx, or CONN-DILx components in Proteus). The device connector must contain pins for power, ground, and signals. **If you have multiple devices of the same type used in your schematic, you must use the same connector type and pinout connections for each one.** Add text to describe the connector's purpose.

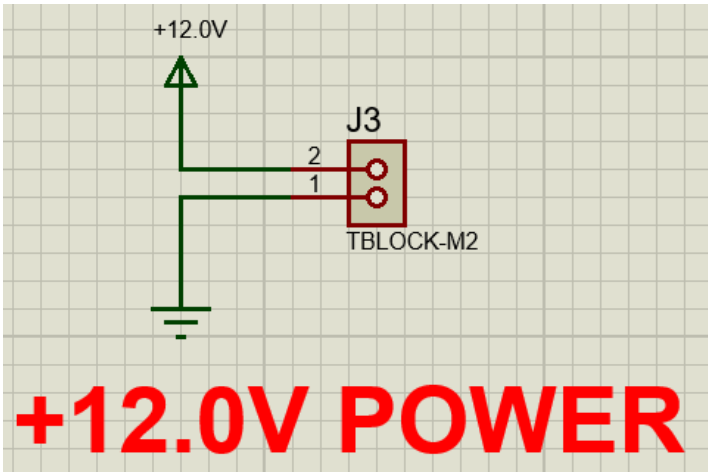
Below you can see the schematic with connectors added for the M1 and M2 motors before and after the original motor components are removed.





Power Connectors

Add a two-pin power connector to your schematic for +12.0V and GND. The Nucleo-64 development board supplies the +3.3V, +5.0V, and GND power rails. But there must be an additional power connection for the +12.0V and GND required by external devices. Use the TBLOCK-Ix or TBLOCK-Mx components in Proteus. If you were having the PCB fabricated and populated, you would choose a wire-to-board screw terminal that can handle a higher current than a regular rectangular connector (>3A).



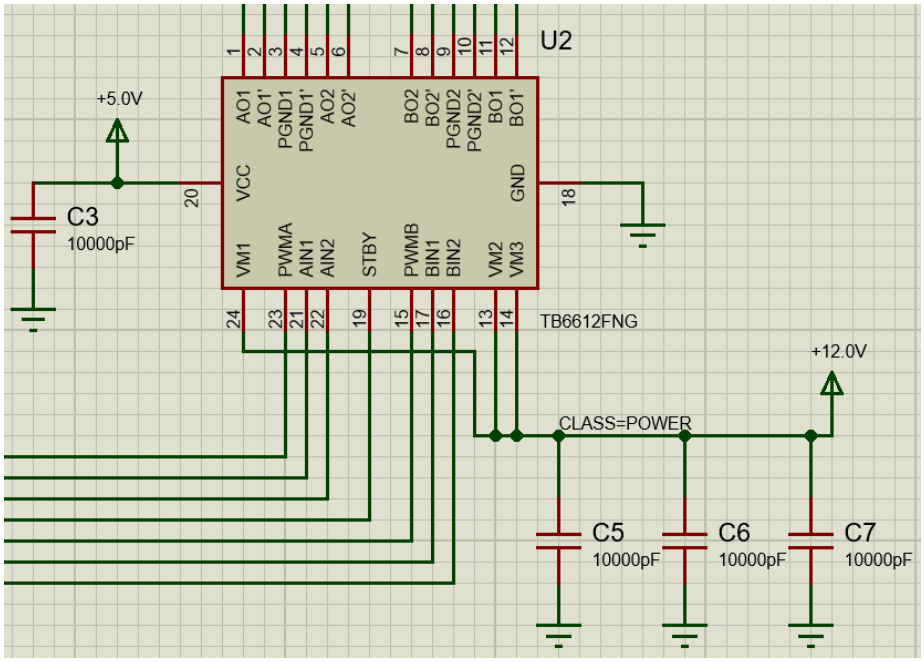
Step 4: Add Decoupling Capacitors

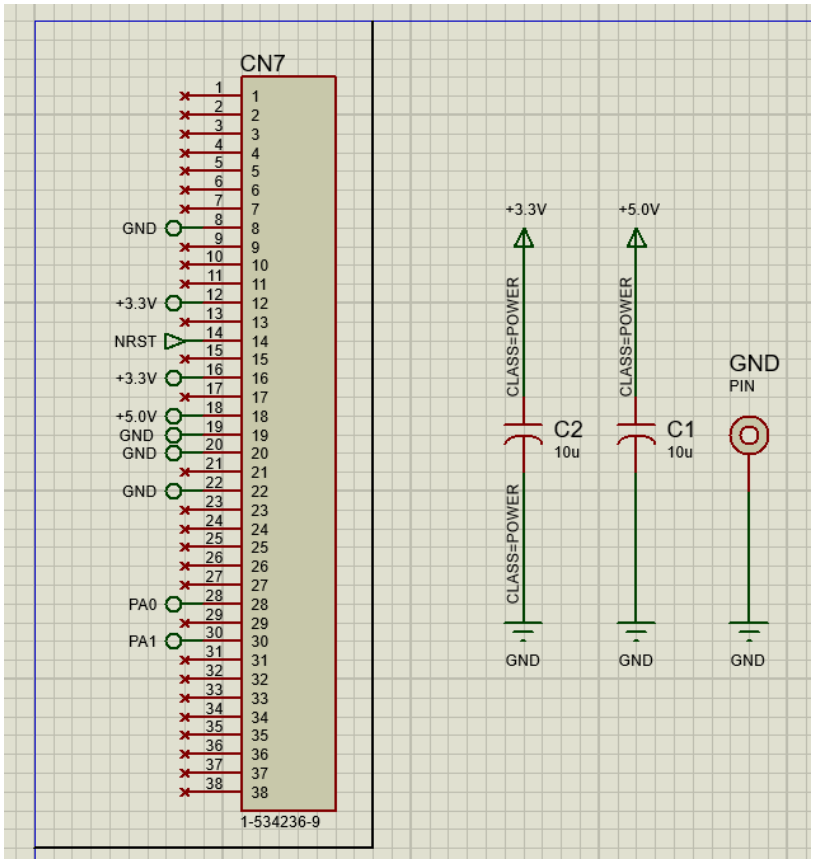
Capacitors are used in various ways on a typical PCB: Noise decoupling, power supply regulation, and signal processing.

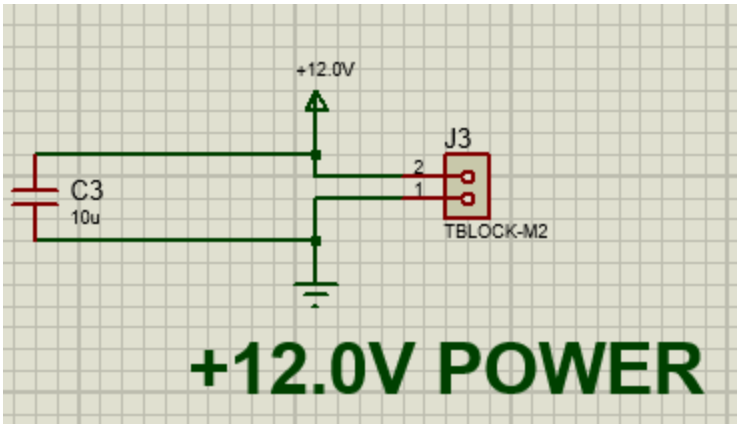
- **Add a decoupling cap to each IC power pin present on your schematic.** "Decoupling Capacitors" are low-value (0.01 to 0.1 µF) capacitors located close to every IC. Recall that as frequency goes up, the impedance of a capacitor goes down. So, decoupling caps provide a low-impedance bypass path for high-frequency noise away from the power pins of your ICs. In essence, they clean up the high-frequency noise coupled to the PCB power traces (copper wires) from the environment and other circuits.
- **Add a 10 µF bulk cap to each power pin on your PCB (any power pin on ICs and devices).** "Bulk Capacitors" are high-value (>= 10 µF) capacitors added wherever power first enters or is converted on a PCB. They act as charge reservoirs, sourcing and sinking current as the applied voltage fluctuates. Think of them as adding mass to a system to reduce a mechanical vibration – it takes time to charge and discharge a big capacitor (and therefore to change its voltage), so it smoothes out the voltage rails during changing supply and demand.

  Here are a few tips for real-world design – for Lab 4, use 10 µF caps only:
  - Use bigger capacitors when you must supply more current. For example, use 100 µF next to batteries and motors, and even bigger when significant current peaks are expected. Failure to do so will result in the voltage rails dropping during periods of high current demand.
  - Aluminum electrolytic capacitors provide high capacitance for a given size and price. However, they are usually polarized, so be sure to connect them in the correct orientation. Otherwise, they blow up.

- Capacitors are usually specified in pF and µF, but not nF. So, if you needed a 100 nF cap, you would instead be looking for a 0.1 µF or 100,000 pF cap.



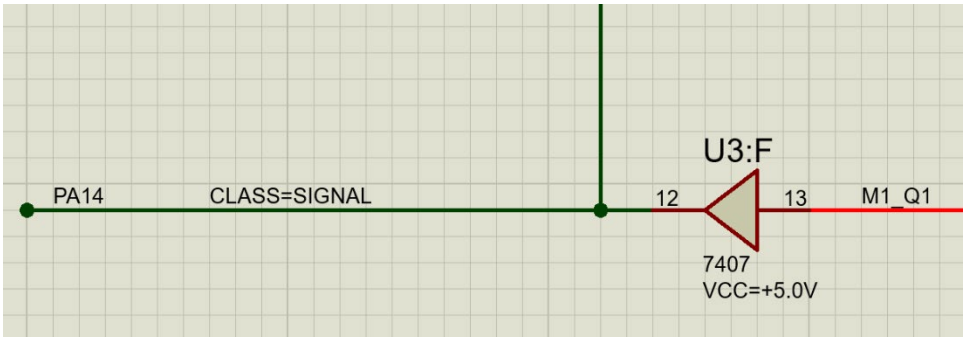




Step 5: Preparing Nets for Layout

Name Every Net

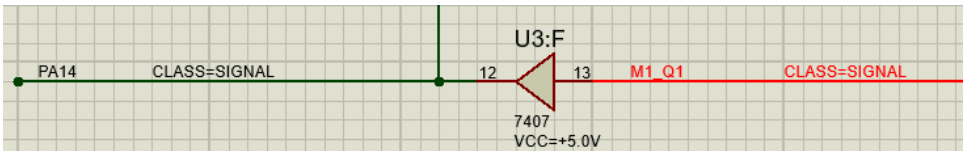
Name all nets so they can be easily identified during PCB signal trace routing. Use the Wire Label tool (LBL) or right-click on a selected net and choose the Place Wire Label option. Add the net name value in the String field.



Add Every Net to a Net Class

Add a net class property to each net in your schematic. A net class allows properties to be assigned to a group of similar kinds of nets. In this case, it will inform the PCB layout tool about which layers the signal can be routed on and how thick the trace should be. The POWER net class will have wider traces to lower the resistance, and the SIGNAL net class will have thinner traces to reduce the parasitic capacitance and inductance. You may further differentiate analog and digital signals, grounds, and voltages in a more complicated design. You may have slow signals, where you don't care about parasitics, and fast signals containing high-frequency components, where routing must follow special rules (like no 90° bends in the traces). It is common to have extra copper layers reserved for ground and voltage supplies, which can help alleviate noise from the system, and a net class would specify this connectivity.

Adding a net class property begins in the same way as adding a wire label. In the Edit Wire Label dialog box, select the Net Class tab and set the Net Class dropdown to either POWER or SIGNAL. Use POWER for high-current nets (motors, voltage rails, grounds), and use SIGNAL set for digital or analog signals. **Any nets left in the default net class will be penalized.**

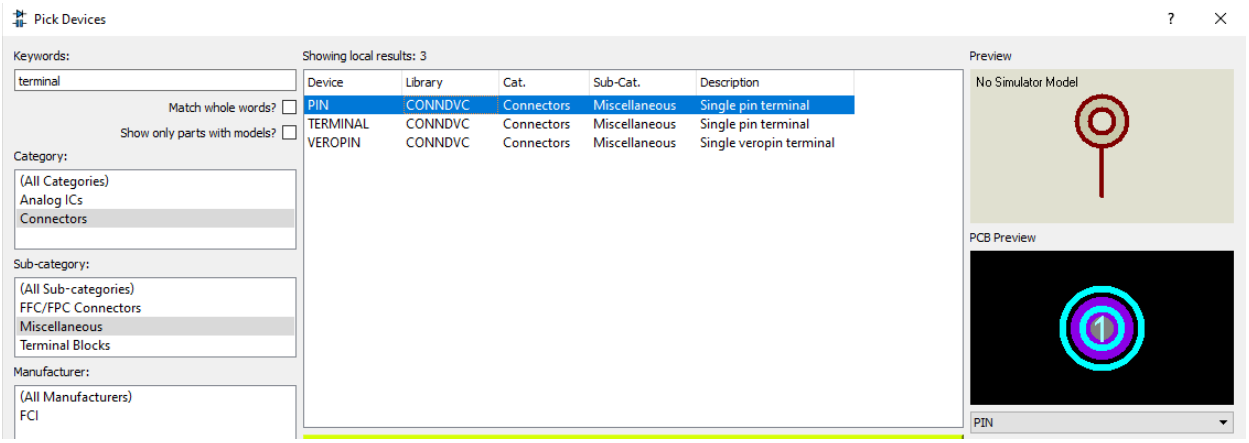


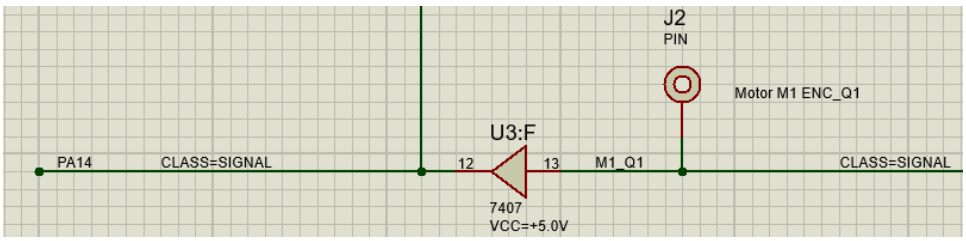
Step 6: Add Test Points

Add some Test Points to your schematic. These are pins added to the PCB for connecting to lab equipment or exposed metal pads that can be touched with a probe. Some PCB designs get very dense, and a test point is a **very safe** and **helpful** means of probing your circuit while it is operating. Test points prevent the probe from slipping and causing circuit damage. Your schematic's test points should have meaningful text descriptions that indicate their electrical functions to a user. Additional text could be written on the PCB silkscreen, so it's clear what the connection is, like how development boards label user pins.

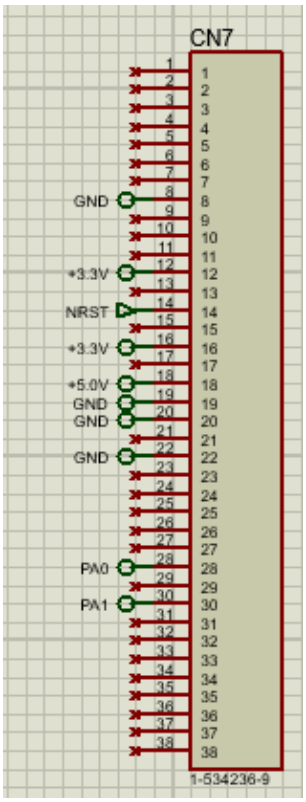
Here are some guidelines:

- A test point to GND is always required since all lab equipment must be connected to the same GND as the PCB under test.
- Test points to all voltage rails are recommended. One does not want to accidentally short VDD to GND when probing with a scope tip, and a test pin will help mitigate this risk.
- Digital and Analog signals of interest should have test points. Imagine needing to debug a non-functioning circuit and add test points to signals which might help you find the problem.
- As in Step 1, leave component reference designators as-is. You can add descriptive text on the schematic and PCB layout (place text on the top or bottom silkscreen layer next to the test point), but leave the reference designators to conform to the standard.





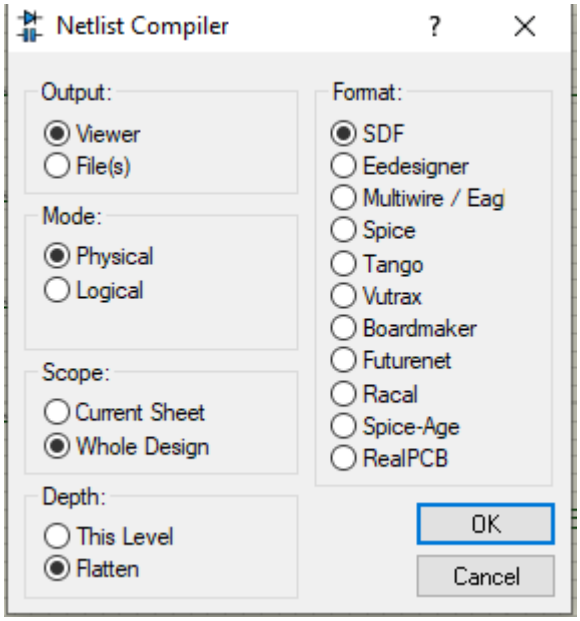
Step 7: Add No-Connects



Any CN7 and CN10 Connector pins (the headers that connect your PCB to the Nucleo-64) that don't go anywhere will have unused MCU pins that will become single-pin nets. **Place a "No Connect" (NC) termination on any unused header and IC pins. If they are not replaced by an NC termination, they will show up in your netlist report later as single pin nets and will be penalized. The CN7 NRST pin is exempt from this requirement.**

Step 8: Generate Netlist

Once the above changes have been made, you will compile your design. "Compiling" in this context means reducing the graphical schematic into a "netlist" that describes all the connections between parts. **Select Tool → Netlist Compiler**. Use the following default settings:



The resulting netlist is used in the PCB layout. Save the output for inclusion in project submission. **Any remaining single-pin nets will be penalized.** Use a No-Connect on the pin in question to fix it.

NETLIST - Schematic Capture

```
ISIS SCHEMATIC DESCRIPTION FORMAT 8.0
=====================================
Design:   ECE298_Lab4_testPCB_routed.pdsprj
Doc. no.: <NONE>
Revision: <NONE>
Author:   <NONE>
Created:  2021-03-08
Modified: 2021-03-10

*PROPERTIES,0

*MODELDEFS,0

*PARTLIST,25
C1,C2012Y5V1A106Z,10u,CODE="Digikey 445-1371-1-ND",EID=4,PACKAGE=CAPC2012X100
C2,C2012Y5V1A106Z,10u,CODE="Digikey 445-1371-1-ND",EID=3,PACKAGE=CAPC2012X100
C3,C0805N103K5XSH7189,10000pF,CODE="Digikey CDR31BX103AKUS TR-ND",EID=9,PACKAGE=CAPC2012X100
C4,C2012Y5V1A106Z,10u,CODE="Digikey 445-1371-1-ND",EID=D,PACKAGE=CAPC2012X100
C5,C0805N103K5XSH7189,10000pF,CODE="Digikey CDR31BX103AKUS TR-ND",EID=E,PACKAGE=CAPC2012X100
C6,C0805N103K5XSH7189,10000pF,CODE="Digikey CDR31BX103AKUS TR-ND",EID=F,PACKAGE=CAPC2012X100
C7,C0805N103K5XSH7189,10000pF,CODE="Digikey CDR31BX103AKUS TR-ND",EID=10,PACKAGE=CAPC2012X100
C8,C0805N103K5XSH7189,10000pF,CODE="Digikey CDR31BX103AKUS TR-ND",EID=1B,PACKAGE=CAPC2012X100
C9,C0805N103K5XSH7189,10000pF,CODE="Digikey CDR31BX103AKUS TR-ND",EID=1E,PACKAGE=CAPC2012X100
CN7,1-534236-9,1-534236-9,CODE=1-534236-9,EID=1,PACKAGE=ECE298_REVTRANS38DIL-1,SUPPLIER=TE_CONNECTIVITY
CN10,1-534236-9,1-534236-9,CODE=1-534236-9,EID=2,PACKAGE=ECE298_REVTRANS38DIL-1,SUPPLIER=TE_CONNECTIVITY
GND,PIN,PIN,EID=1D,PACKAGE=PIN
J1,25630701RP2,25630701RP2,CODE="NorComp 25630701RP2",EID=8,PACKAGE=CON7_1X7_U_2563
J2,PIN,PIN,EID=A,PACKAGE=PIN
J3,TBLOCK-M2,TBLOCK-M2,EID=6,PACKAGE=TBLOCK-M2
J4,25630701RP2,25630701RP2,CODE="NorComp 25630701RP2",EID=7,PACKAGE=CON7_1X7_U_2563
J5,PIN,PIN,EID=B,PACKAGE=PIN
J6,PIN,PIN,EID=C,PACKAGE=PIN
J7,PIN,PIN,EID=17,PACKAGE=PIN
J8,PIN,PIN,EID=18,PACKAGE=PIN
J9,PIN,PIN,EID=19,PACKAGE=PIN
RN1,RES10SIPB,10k,EID=1C,MODTYPE=ANALOG,PACKAGE=CONN-SIL10
U2,TB6612FNG,TB6612FNG,EID=5,PACKAGE=SOP65P760X120-24
U3,7407,7407,EID_A=11,EID_B=12,EID_C=13,EID_D=14,EID_E=15,EID_F=16,ITFMOD=TTL,MODFILE=74BUF.MDF,PACKAGE=SO14,VCC=+5.0V
U6,74HCT541,74HCT541,EID=1A,PACKAGE=SO20W,PINSWAP="1,19",VCC=+5.0V

*NETLIST,36
NRST,2
NRST,IT
CN7,PS,14
```

Instructions: PCB Layout

Developing a schematic and its PCB layout is an iterative process – changes can flow in both directions, from schematic to layout and vice versa. You can now move to the “PCB Layout” tab in Proteus.

PCB Layout Considerations

There are many things to consider during PCB design. Here are some of the most relevant:

- **Power entry:** AC or DC? Any DC-to-DC voltage conversion?
- **PCB Fabricator capabilities:** What are the Fab shop capabilities for “space and trace” (minimum spacing between traces and minimum trace thickness)? How many layers can their PCBs have? Here are some examples from commercial fabs:

  Domestic:
  - https://www.4pcb.com/pcb-manufacturing-custom-standard.html
  - https://www.7pcb.ca/pcb-fabrication/
  - https://www.customcircuitboards.com/pcb-capabilities/

  Overseas:
  - https://www.pcbcart.com/pcb-capability/multilayer-pcb-fabrication.html
  - https://www.allpcb.com/standard_pcb_manufacturing_capability.html

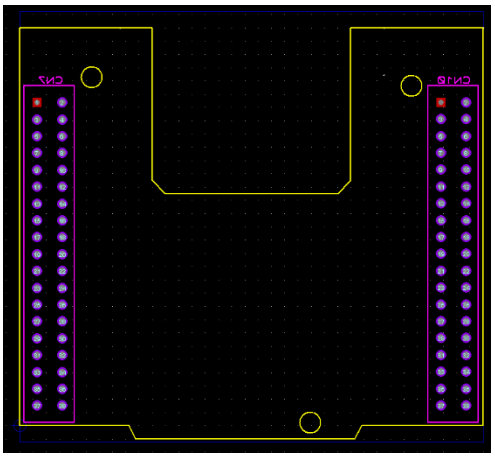
  - https://www.pcbway.com/capabilities.html
- **Design performance:** What are the maximum signal frequencies being used in the design? What is the "power budget"?
- **Thermal considerations:** Will there be airflow in the environment where the PCB assembly is located? Are there any PCB "hot spots" to mitigate?
- **Design time and cost:** How many layers can the PCB use? What conductor density is required?
- **Component packaging:** Through-hole or Surface Mount?
- **Environmental standards required:** Are there limitations on the components and materials your design may use or product end-of-life considerations?
- **Designing for Test (DfT):** Inclusion of test points, planning for automated test, etc.
- **Designing for Manufacturability (DfM):** Must consider device clearances during assembly, ease of automated and manual assembly steps, etc.
- **Design for Reliability (DfR):** Designing electrical, mechanical, and thermal robustness to reduce different types of failure modes.
- **Designing for Compliance (DfC):** Can include restriction to RoHS devices (Risk of Hazardous Substances) and EMC (Electro-Magnetic Compliance).

For this course, we will only consider the following the following features and limitations:

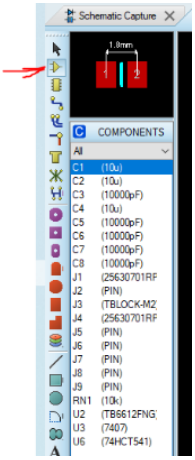
- The PCB will have **two layers**: Top Copper and Bottom Copper
- Minimum SPACE and TRACE setup of **8 mils** (1 mil = 0.001" = 0.0254 mm). This correlates to 0.203 mm space or trace widths. The unit "mil" is also called "thou" (short for "thousandth of an inch"). Note that you must work with both imperial and metric units when creating a PCB layout.

An initial PCB shape (usually referred to as its "form-factor" or "board cut-out") is provided in the Lab 4 Proteus Template. This file is the common PCB starting point for this course, and the PCB boundaries and placement of the Morpho connectors and mounting holes **must not be moved**. The connectors are called dual-row male-pin headers (100 mil spacing), and Morpho is the marketing name for the standardized Nucleo development board connector specification.

> Morpho connectors and mounting holes are placed so the PCB can attach to the Nucleo-64 Development Board. The "footprints" (the layout associated with a component) appear to be backwards because the connectors are on the bottom of the PCB.



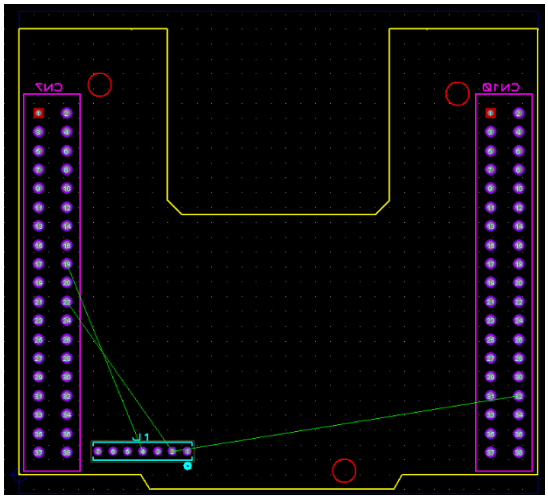
Component Placement



In the PCB Layout tool, select Component Mode ( ). The left-hand pane shows components from your design that still need to be placed onto the PCB.

The bottom left corner has a dropdown to choose which PCB layer you are working on: Component Side. Here, Component Side means the top layer, and Solder Side means the bottom layer. Select any component in the list and place it on the PCB. To take the component off the PCB, select it, press delete, and the component returns to the Component Pane.

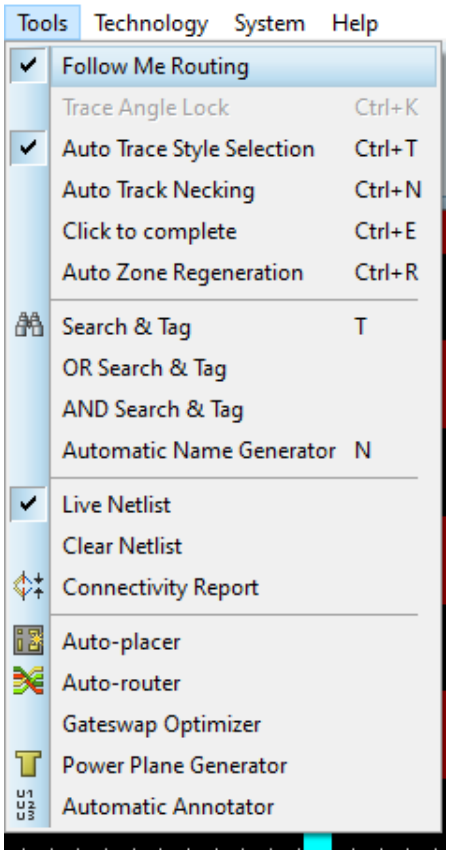
You can move components and change which side they are on as you work through your design. Begin with your off-board connectors (those going to motors, displays, etc.). The green lines connecting component pins show nets where copper traces (wire) must be drawn to connect them electrically.



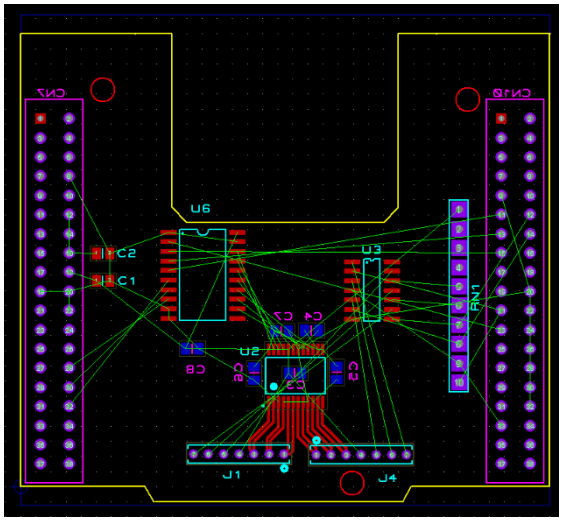
You may try the Tools → Auto-placer utility, but the quality is poor. However, it is a convenient way to get all the unplaced components onto the screen for manual placement.

Routing Traces

Before you begin routing your PCB design (drawing all the traces), ensure that the following options are set: Tools → Follow Me Routing, and Tools → Auto Trace Style Selection.



In the PCB Layout tool, select Track Mode ( ). You can click on a pin with an unrouted net (green line) to begin drawing a copper trace. Here is a design with some devices placed and some traces completely routed (red lines, which indicate they're on the Top Copper layer).

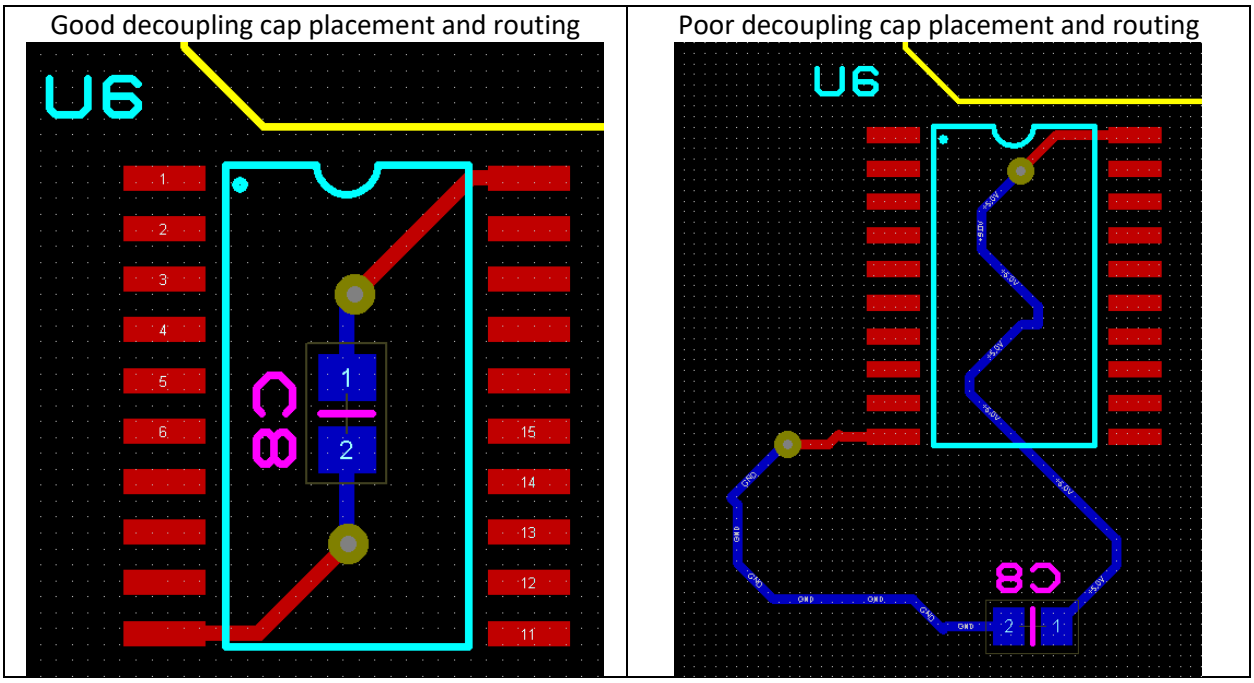


Top layer components are **cyan**, and **bottom layer components** are **magenta**.

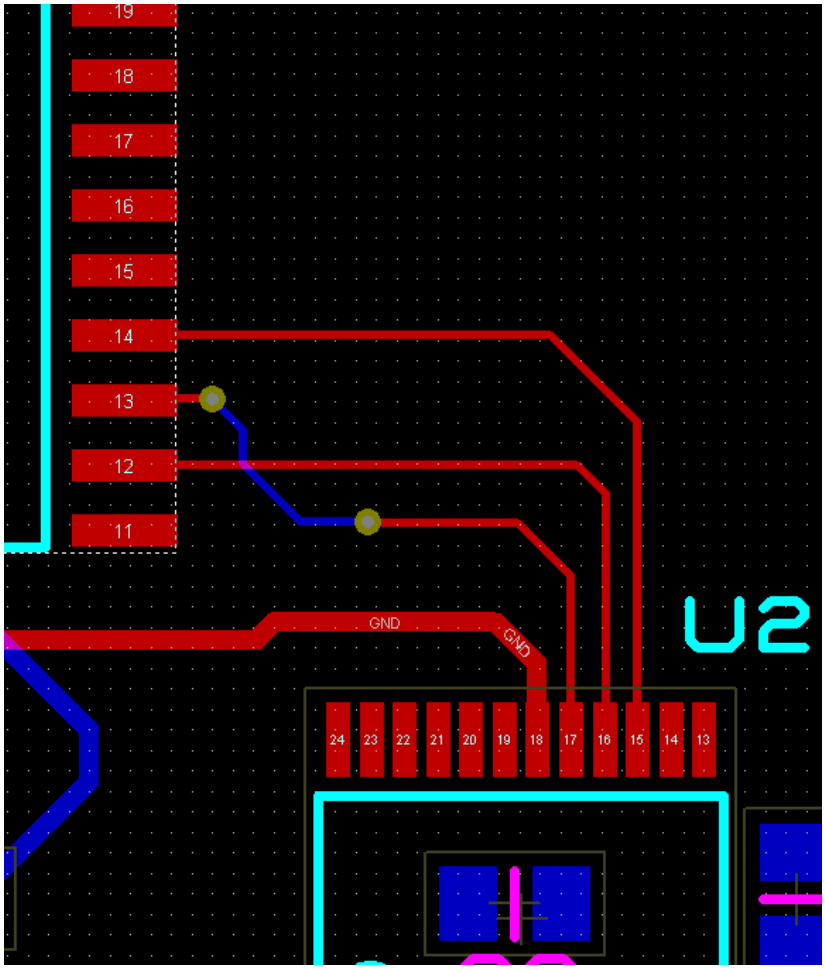
Top layer traces are **red**, and **bottom layer traces** are **blue**.

Notice that components also must have Reference Designators (e.g., C1, J2, CN7) placed on the PCB silkscreen (the graphical layers on the top and bottom of the PCB). In the above figure, the reference designator for U6 is off the PCB and must be moved.

Placement and routing of IC power connections and decoupling capacitors are essential. **Traces for power decoupling capacitors must be kept as short as possible** to reduce the trace parasitic inductance and resistance. An excellent place to put decoupling capacitors is underneath its associated component on the opposite layer of the PCB. If you want to switch layers while routing, double-click the mouse and a **via** hole is placed where the mouse pointer is located, and you continue routing on the opposite layer. Vias are metal-plated holes drilled through the PCB to connect all conducting layers at that location. It's a means of connecting from one layer to another.



The PCB layout must include the final placements of all components and traces. Each kind of trace uses its assigned net class to apply the appropriate trace width by default. Signal trace widths are set to 8 mil, and power trace widths are set to 15 mil. Here is an example that shows thinner signal traces and thicker power traces:



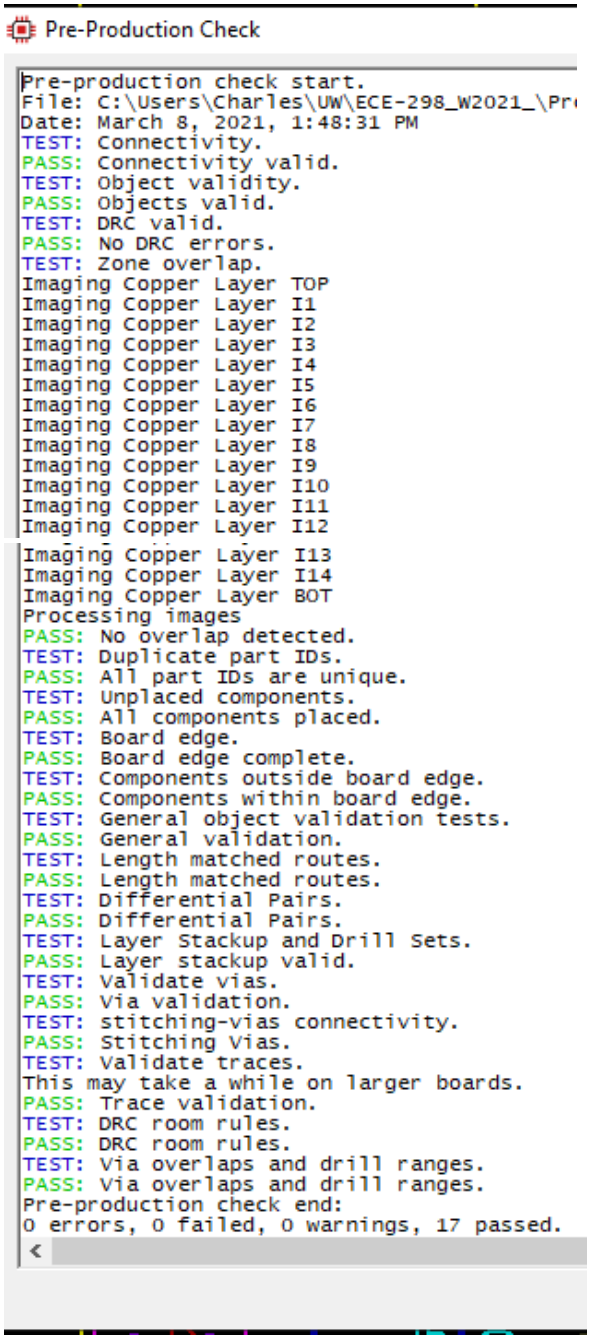
You may try the Tools → Auto-router utility, but sometimes the routing quality is poor. You will probably have to move some parts and traces.

Test Points

Place your test points in easily accessible locations, away from other devices. Test points are very important additions to your design, as discussed earlier when you added them to your schematic. On the PCB, they take the form of plated vias populated with a single pin or left as-is or are exposed pads on the top or bottom copper layer that can be probed. They connect to power rails or signals that can be used to verify that a design is working. Test points can be referred to in a Test Plan document using their reference designator, like "J7" or "TP12", so anyone can observe or measure circuit functionality. It can also make it safer to test the live circuit because test points can be placed away from devices with high-density pins. The test point can prevent a scope probe from slipping and shorting device pins. Add descriptive text on the appropriate silkscreen layer for important test points (e.g., "GND", "+12.0V", etc.). This is not required but is very handy for debugging a prototype.

Pre-Production Check

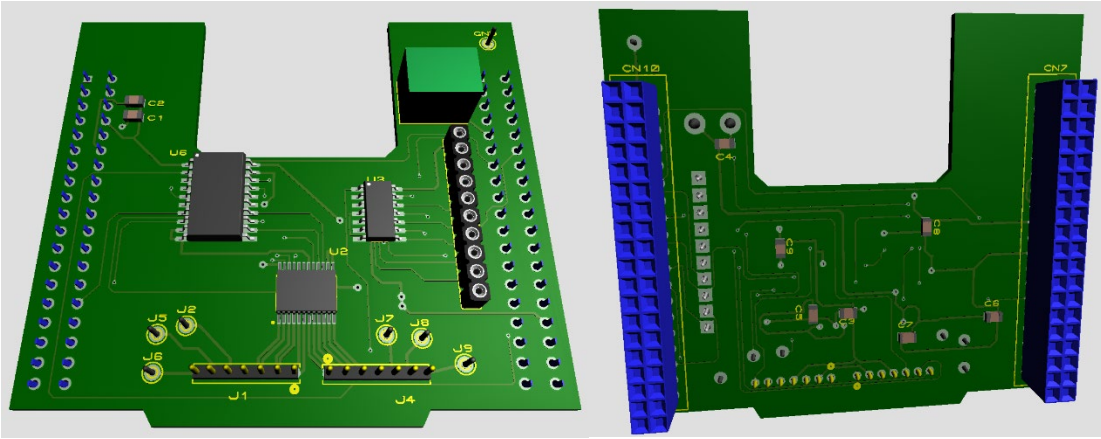
After your devices have been placed and routed, you will **run the Output → Pre-Production Check**. This step confirms proper layout electrical connectivity compared to the schematic netlist and checks if the design "passes DRC". The Design Rules Checks (DRC) compare your layout against the rules imposed by the fabrication target. For example, if the trace and space are set to 6 mil minimum but the layout has 4 mil traces, the DRC will identify this issue for you to correct.



Save the output (copy and paste into a.txt file) for inclusion in the submission.

3D Views

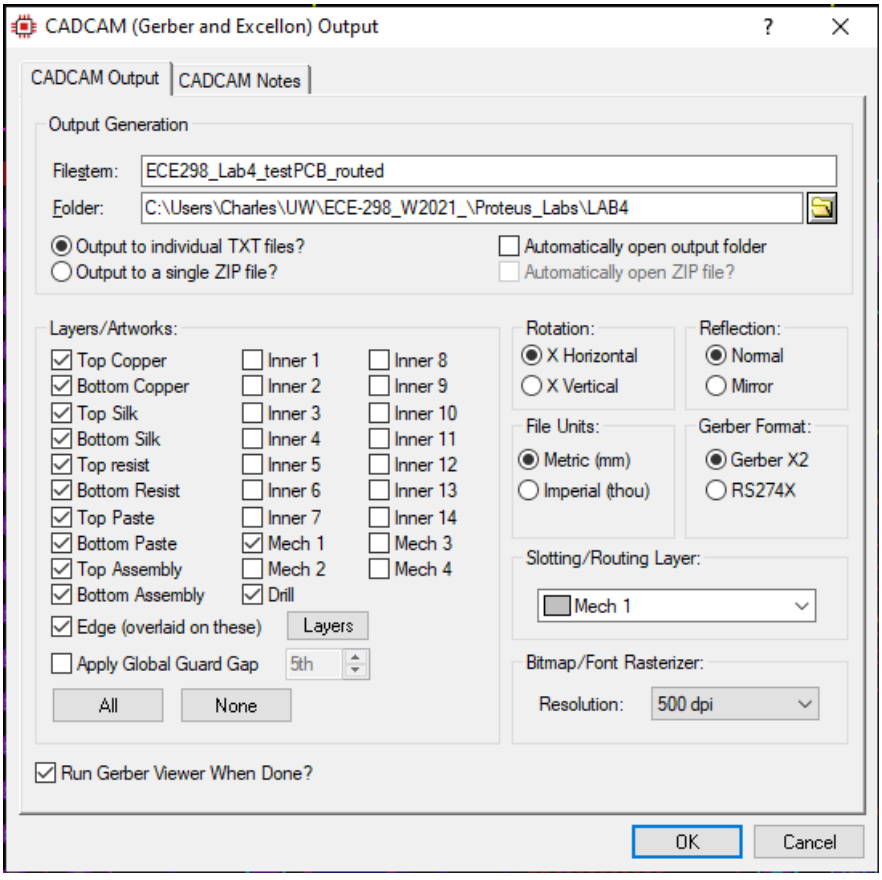
Create 3D views for the top and bottom assemblies. The Proteus 3D Visualizer (menu bar →) shows what the final assembly will look like. This view is handy for checking the "mechanical stack-up" – seeing how components and their connections off-board may interfere with one another. It also catches errors that pass all the rules check but are not what you intended, like devices being on the board's correct side and having adequate clearances from other parts.



Export a top and bottom views that capture the board's salient details, either as screenshots or PDFs (File → Print 3D View → Print to PDF), and place them into a "3D Views" subfolder.

Gerber Plots

Generate the Gerber-format CAD files necessary to fabricate your PCB. An industry-standard ASCII-format Gerber file is generated for each layer and specifies all the layout and drill hole geometry and coordinates. This step can be done in Proteus after a successful Pre-Production Check is run (Output → Generate Gerber/Excellon Files). Use the options as shown below. Be sure to enable "Run Gerber Viewer When Done".

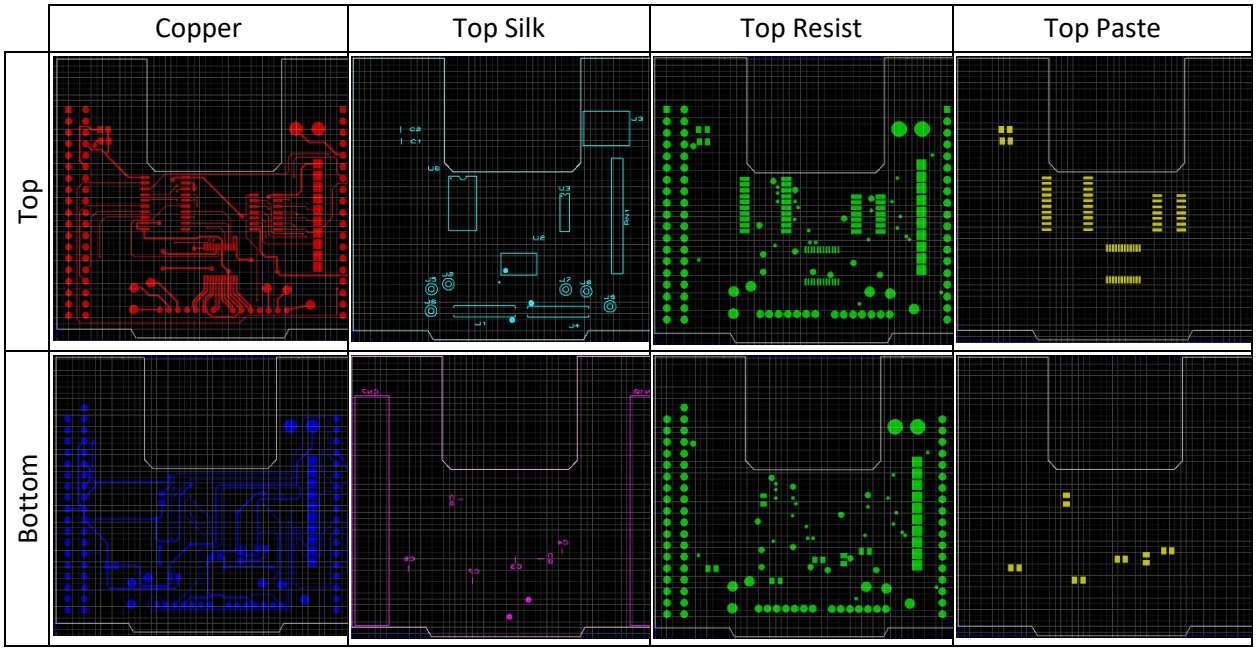


After generating the files, the Gerber viewer is launched with the following layers:

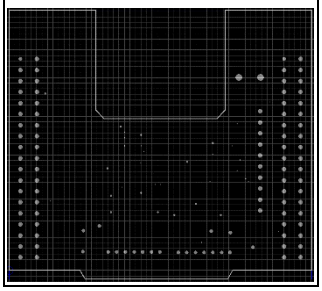
- **Top and Bottom Copper:** Traces, component pads, power plane areas for the top and bottom layers
- **Top and Bottom Silk:** The top and bottom silkscreened graphical layers that have reference designators and other notes
- **Top and Bottom Resist:** "Resist" is the coating used to cover and protect the top and bottom copper traces and plane areas but leaving the component pads exposed for soldering. This plot is a "negative", meaning that this layer's locations will be protected from the resist coating. This coating gives most PCBs their green colour, and you can often choose the resist coating colour.
- **Top and Bottom Paste:** "Paste" refers to solder paste, a gel of tiny solder balls suspended in flux paste. Solder is the metal that bonds a component to its solder pads or plated through-holes on a PCB. It is a combination of tin and lead (though increasingly lead-free) with a low melting point and good electrical and mechanical properties. Flux is a chemical that helps molten solder to flow into place. The paste layers are used to create thin stainless-steel solder-paste screens with holes where the paste is to be applied to the exposed solder pads on the top and bottom PCB surfaces. The screen is placed on the bare PCB, and solder-paste is dragged across it onto the component pads.
- **Various Mechanical Layers:** Additional layers have the board shape, component placement information, instructions for the fab, and anything else relevant to the PCB and its assembly.
- **Drill File:** Has PCB hole sizes and coordinates.

After the top and bottom layers are made in a fab process, they are aligned and formed into a layer stack. There can be numerous layers in a multi-layer board that are all aligned and bonded into one PCB. The layer alignment process is sometimes called PCB layer registration.

You can view each Gerber layer individually in the Gerber Viewer by going to the View → Edit Layer Colours/Visibility and enable the layer you wish to view. If the tab is closed, you need to regenerate the Gerber files to relaunch the viewer.



Drill Holes



PCB Assembly Information (Pick and Place File)

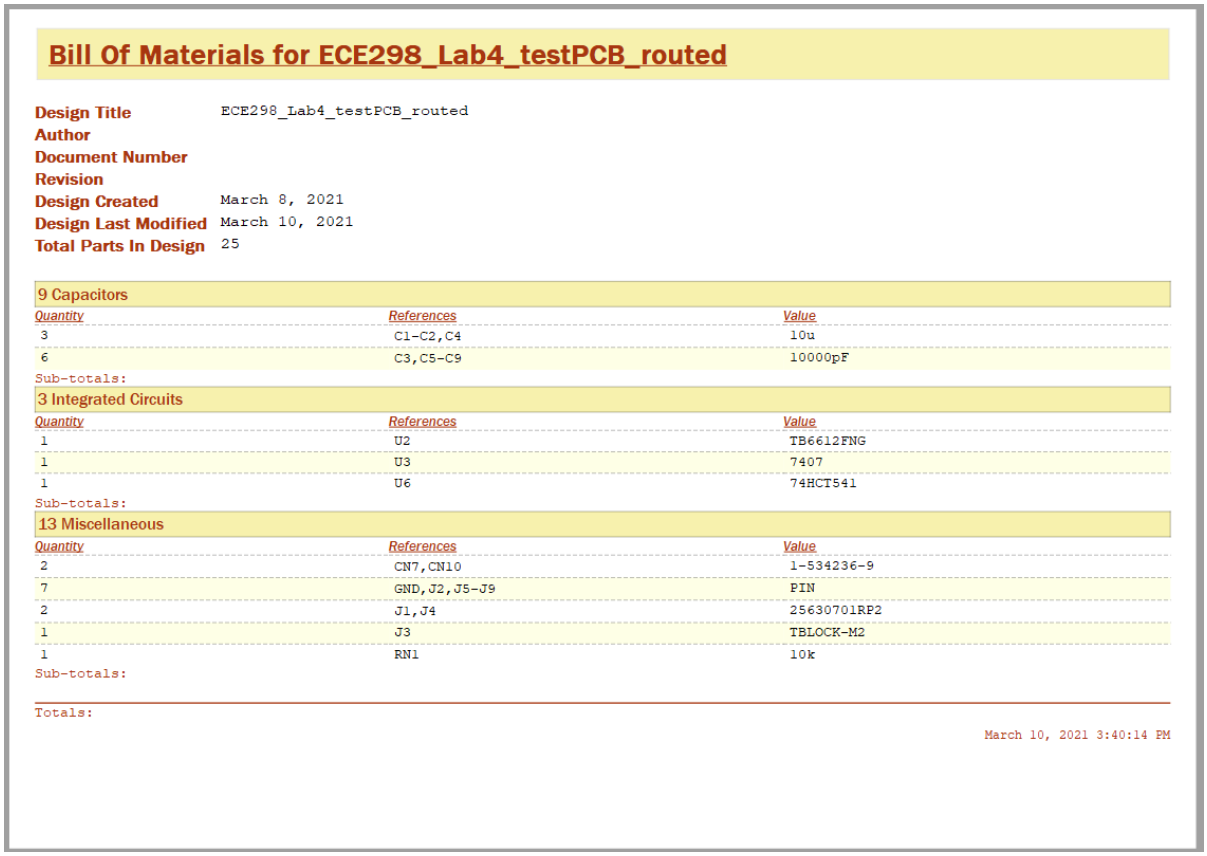
Generate the Pick and Place file (Output → Generate Pick and Place File)**.** During PCB assembly, after the solder paste is applied to the pads, the PCB goes into a pick and place machine (pick and place machine in action) that places parts onto the pads covered with solder paste. This generated file describes where to place the components and in what orientation. Then the assembly is placed in a "reflow oven" that melts the solder paste, forming electrically and mechanically strong joints between the devices and the PCB. First, either the top or bottom side is populated and reflowed, then the other side.

Part ID	Value	Package	Stock Code	Layer	Rotation	X	Y
CN7	1-534236-9	ECE298_REVTRANS38DIL-1	1-534236-9	BOT	0	177.362	1019.69
CN10	1-534236-9	ECE298_REVTRANS38DIL-1	1-534236-9	BOT	0	2577.36	1019.69
C1	10u	CAPC2012X100	Digikey 445-1371-1-ND	TOP	0	417.323	1641.73
C2	10u	CAPC2012X100	Digikey 445-1371-1-ND	TOP	0	413.386	1744.09
J1	25630701RP2	CON7_1X7_U_2563	NorComp 25630701RP2	TOP	0	1137.8	169.291
J4	25630701RP2	CON7_1X7_U_2563	NorComp 25630701RP2	TOP	-180	1775.59	165.354
U2	TB6612FNG	SOP65P760X120-24		TOP	90	1434.06	578.74
C3	10000pF	CAPC2012X100	Digikey CDR31BX103AKUS TR-ND	BOT	-180	1425.2	594.488
C5	10000pF	CAPC2012X100	Digikey CDR31BX103AKUS TR-ND	BOT	-270	1641.73	578.74
C6	10000pF	CAPC2012X100	Digikey CDR31BX103AKUS TR-ND	BOT	-270	1551.18	578.74
C7	10000pF	CAPC2012X100	Digikey CDR31BX103AKUS TR-ND	BOT	-270	1244.09	586.614
C8	10000pF	CAPC2012X100	Digikey CDR31BX103AKUS TR-ND	BOT	90	944.882	1114.17
C4	10u	CAPC2012X100	Digikey 445-1371-1-ND	BOT	0	2125.98	1637.8
U3	7407	SO14		TOP	0	1830.71	1023.62
RN1	10k	CONN-SIL10		TOP	-90	2149.61	1002.76
U6	74HCT541	SO20W		TOP	0	948.819	1102.36
J2	PIN	PIN		TOP	0	822.835	405.512
J5	PIN	PIN		TOP	0	677.165	362.205
J7	PIN	PIN		TOP	0	1838.58	358.268
J3	TBLOCK-M2	TBLOCK-M2		TOP	0	2189.05	1751.97
J6	PIN	PIN		TOP	0	673.228	173.228
J8	PIN	PIN		TOP	0	2015.75	342.52
J9	PIN	PIN		TOP	0	2220.47	212.598
GND	PIN	PIN		TOP	0	2582.68	2188.98
C9	10000pF	CAPC2012X100	Digikey CDR31BX103AKUS TR-ND	BOT	-270	1830.71	1015.75

Save the output as a .csv file for inclusion in the submission.

Bill of Materials

From the Proteus Menu Bar, select the "$" icon ( ) to create a Bill of Materials file (BOM) like the one shown below. Select the PDF icon ( ) to export it as a PDF to include in your submission.



Bill Of Materials for ECE298_Lab4_testPCB_routed

Design Title	ECE298_Lab4_testPCB_routed
Author	
Document Number	
Revision	
Design Created	March 8, 2021
Design Last Modified	March 10, 2021
Total Parts In Design	25

9 Capacitors

Quantity	References	Value
3	C1-C2,C4	10u
6	C3,C5-C9	10000pF

Sub-totals:

3 Integrated Circuits

Quantity	References	Value
1	U2	TB6612FNG
1	U3	7407
1	U6	74HCT541

Sub-totals:

13 Miscellaneous

Quantity	References	Value
2	CN7,CN10	1-534236-9
7	GND,J2,J5-J9	PIN
2	J1,J4	25630701RP2
1	J3	TBLOCK-M2
1	RN1	10k

Sub-totals:

Totals:

March 10, 2021 3:40:14 PM