



# EEE3017W: STM32F051 Reference Sheet

**AHB peripheral clock enable register (RCC\_AHBENR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	TSCEN	Res.	IOPF EN	IOPF EN	IOPD EN	IOPC EN	IOPB EN	IOPA EN	Res.	
							rw		rw	rw	rw	rw	rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	CRC EN	Res.	FLITF EN	Res.	SRAM EN	Res.	DMA EN							
									rw		rw		rw		

**TSCEN** Touch sensing controller clock enable  
**GPIOFEN** I/O port F clock enable  
**GPIOEEN** I/O port E clock enable  
**GPIODEN** I/O port D clock enable  
**GPIOCEN** I/O port C clock enable  
**GPIOBEN** I/O port B clock enable  
**GPIOAEN** I/O port A clock enable  
**CRCEN** CRC clock enable  
**FLITFEN** FLITF clock enable  
**SRAMEN** SRAM interface clock enable  
**DMAEN** DMA clock enable

0: Clock disabled  
 1: Clock enabled

Reset value: 0x0000 0014

**APB peripheral clock enable register 2 (RCC\_APB2ENR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DBGM CUEN	Res.	Res.	Res.
													rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	USART1 EN	Res.	SPI1 EN	TIM1 EN	Res.	ADC EN	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	SYSCFG COMP EN
		rw	rw	rw		rw									rw

**DBGMCUEN** MCU debug module clock enable  
**TIM17EN** TIM17 timer clock enable  
**TIM16EN** TIM16 timer clock enable  
**TIM15EN** TIM15 timer clock enable  
**USART1EN** USART1 clock enable  
**SPI1EN** SPI1 clock enable  
**TIM1EN** TIM1 timer clock enable  
**ADCEN** ADC interface clock enable  
**SYSCFGCOMPEN** SYSCFG & COMP clock enable

0: Clock disabled  
 1: Clock enabled

Reset value: 0x0000 0000

APB peripheral clock enable register 1 (RCC_APB1ENR)																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16																
Res.	CEC EN	DAC EN	PWR EN	CRS EN	Res.	CAN EN	Res.	USB EN	I2C2 EN	I2C1 EN	Res.	USART 4EN	USART 3EN	USART 2EN	Res.																
	rw	rw	rw	rw		rw		rw	rw	rw		rw	rw	rw																	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																
Res.	SPI2 EN	Res.	Res.	WWDG EN	Res.	Res.	TIM14 EN	Res.	Res.	TIM7 EN	TIM6 EN	Res.	Res.	TIM3 EN	TIM2 EN																
	rw			rw			rw			rw	rw			rw	rw																
CECEN	HDMI CEC clock enable																														
DACEN	DAC interface clock enable																														
PWREN	Power interface clock enable																														
CRSEN	Clock Recovery System interface clock enable																														
CANEN	CAN interface clock enable																														
USBEN	USB interface clock enable																														
I2C2EN	I2C2 clock enable																														
I2C1EN	I2C1 clock enable																														
USART4EN	USART4 clock enable																														
USART3EN	USART3 clock enable																														
USART2EN	USART2 clock enable																														
SPI2EN	SPI2 clock enable																														
WWDGEN	Window watchdog clock enable																														
TIM14EN	TIM14 timer clock enable																														
TIM7EN	TIM7 timer clock enable																														
TIM6EN	TIM6 timer clock enable																														
TIM3EN	TIM3 timer clock enable																														
TIM2EN	TIM2 timer clock enable																														
0: Clock disabled 1: Clock enabled																															
Reset value: 0x0000 0000																															

### Decimal to Binary to Hexadecimal conversions

Decimal	Binary	Hex	Decimal	Binary	Hex
0	0000	0	16	00010000	10
1	0001	1	17	00010001	11
2	0010	2	18	00010010	12
3	0011	3	19	00010011	13
4	0100	4	20	00010100	14
5	0101	5	21	00010101	15
6	0110	6	22	00010110	16
7	0111	7	23	00010111	17
8	1000	8	24	00011000	18
9	1001	9	25	00011001	19
10	1010	A	26	00011010	1A
11	1011	B	27	00011011	1B
12	1100	C	28	00011100	1C
13	1101	D	29	00011101	1D
14	1110	E	30	00011110	1E
15	1111	F	31	00011111	1F
255		FF	4095		FFF
65535		FFFF			

Power of 2	Decimal	Hex 16-bit	Power of 2	Decimal	Hex 16-bit
$2^0$	1	0001	$2^9$	512	0200
$2^1$	2	0002	$2^{10}$	1024	0400
$2^2$	4	0004	$2^{11}$	2048	0800
$2^3$	8	0008	$2^{12}$	4096	1000
$2^4$	16	0010	$2^{13}$	8192	2000
$2^5$	32	0020	$2^{14}$	16384	4000
$2^6$	64	0040	$2^{15}$	32768	8000
$2^7$	128	0080			
$2^8$	256	0100			

## GENERAL PURPOSE INPUT/OUTPUTS

### GPIO port mode register (GPIOx\_MODER) (x = A..F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODER15[1:0]	MODER14[1:0]		MODER13[1:0]	MODER12[1:0]		MODER11[1:0]	MODER10[1:0]		MODER9[1:0]	MODER8[1:0]					
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODER7[1:0]	MODER6[1:0]		MODER5[1:0]	MODER4[1:0]		MODER3[1:0]	MODER2[1:0]		MODER1[1:0]	MODER0[1:0]					
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

MODER<sub>y</sub>[1:0] Port x configuration bits (y = 0..15)

- 00: Input mode (reset state)
- 01: General purpose output mode
- 10: Alternate function mode
- 11: Analog mode

Reset value: 0x0C00 0000 (Port A)

0x0000 0000 (All other ports)

### GPIO port output type register (GPIOx\_OTYPER) (x = A..F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OSPEEDR15[1:0]	OSPEEDR14[1:0]		OSPEEDR13[1:0]	OSPEEDR12[1:0]		OSPEEDR11[1:0]	OSPEEDR10[1:0]		OSPEEDR9[1:0]	OSPEEDR8[1:0]					
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSPEEDR7[1:0]	OSPEEDR6[1:0]		OSPEEDR5[1:0]	OSPEEDR4[1:0]		OSPEEDR3[1:0]	OSPEEDR2[1:0]		OSPEEDR1[1:0]	OSPEEDR0[1:0]					
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

OSPEEDR<sub>y</sub>[1:0] Port x configuration bits (y = 0..15)

- x0: Low speed
- 01: Medium speed
- 11: High speed

Reset value: 0x0C00 0000 (Port A)

0x0000 0000 (All other ports)

### GPIO port output type register (GPIOx\_OTYPER) (x = A..F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OT15	OT14	OT13	OT12	OT11	OT10	OT9	OT8	OT7	OT6	OT5	OT4	OT3	OT2	OT1	OT0
rw															

OT<sub>y</sub> Port x configuration bits (y = 0..15)

- 0: Output push-pull (reset state)
- 1: Output open-drain

Reset value: 0x0000 0000

### GPIO port pull-up/pull-down register (GPIOx\_PUPDR) (x = A..F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PUPDR15[1:0]	PUPDR14[1:0]		PUPDR13[1:0]	PUPDR12[1:0]		PUPDR11[1:0]	PUPDR10[1:0]		PUPDR9[1:0]	PUPDR8[1:0]					
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PUPDR7[1:0]	PUPDR6[1:0]		PUPDR5[1:0]	PUPDR4[1:0]		PUPDR3[1:0]	PUPDR2[1:0]		PUPDR1[1:0]	PUPDR0[1:0]					
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

PUPDR<sub>y</sub>[1:0] Port x configuration bits (y = 0..15)

- 00: No pull-up, pull-down
- 01: Pull-up
- 10: Pull-down
- 11: Reserved

Reset value: 0x2400 0000 (Port A)

0x0000 0000 (All other ports)

## GENERAL PURPOSE INPUT/OUTPUTS CONT.

### GPIO port input data register (GPIOx\_IDR) (x = A..F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDR15	IDR14	IDR13	IDR12	IDR11	IDR10	IDR9	IDR8	IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Reset value: 0x0000 XXXX

### GPIO port bit set/reset register (GPIOx\_BSRR) (x = A..F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

BRy Port x Reset bit y (y= 0 .. 15)

- 0: No action on the corresponding ODRx bit
- 1: Reset the corresponding ODRx bit

BSy Port x set bit y (y= 0..15)

- 0: No action on the corresponding ODRx bit
- 1: Set the corresponding ODRx bit

Reset value: 0x0000 0000

### GPIO port output data register (GPIOx\_ODR) (x = A..F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ODR15	ODR14	ODR13	ODR12	ODR11	ODR10	ODR9	ODR8	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Reset value: 0x0000 0000

### GPIO port bit reset register (GPIOx\_BRR) (x = A..F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

BRy Port x Reset bit y (y= 0 .. 15)

- 0: No action on the corresponding ODRx bit
- 1: Reset the corresponding ODRx bit

Reset value: 0x0000 0000

## GENERAL PURPOSE INPUT/OUTPUTS CONT.

### GPIO port alternative function low register (GPIO<sub>x</sub>\_AFRL) (x = A..F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFR7[3:0]				AFR6[3:0]				AFR5[3:0]				AFR4[3:0]			
rw	rw	rw	rw												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFR3[3:0]				AFR2[3:0]				AFR1[3:0]				AFR0[3:0]			
rw	rw	rw	rw												

AFRL [ 3 : 0 ]

Alternate function selection for port x pin y  
(y=0..7)

0000: AF0  
0001: AF1  
0010: AF2  
0011: AF3  
0100: AF4  
0101: AF5  
0110: AF6  
0111: AF7  
1000 to 1111: Reserved

Reset value: 0x0000 0000

### GPIO port alternative function high register (GPIO<sub>x</sub>\_AFRH) (x = A..F)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFR15[3:0]				AFR14[3:0]				AFR13[3:0]				AFR12[3:0]			
rw	rw	rw	rw												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFR11[3:0]				AFR10[3:0]				AFR9[3:0]				AFR8[3:0]			
rw	rw	rw	rw												

AFRH [ 3 : 0 ]

Alternate function selection for port x pin y  
(y=8..15)

0000: AF0  
0001: AF1  
0010: AF2  
0011: AF3  
0100: AF4  
0101: AF5  
0110: AF6  
0111: AF7  
1000 to 1111: Reserved

Reset value: 0x0000 0000

## **ANALOGUE TO DIGITAL CONVERTOR**

## ADC interrupt and status register (ADC ISR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	AWD	Res.	Res.	OVR	EOSEQ	EOC	EOSMP	ADRDY							
							r_w1			r_w1	r_w1	rc_w1	r_w1	r_w1	

AWD	Analog watchdog flag
OVR	ADC overrun
EOSEQ	End of sequence flag
EOC	End of conversion flag
EOSMP	End of sampling flag
ADRDY	ADC ready

0: Flag clear  
1: Flag set

Reset value: 0x0000 0000

## **ADC data register (ADC\_DR)**

Reset value: 0x0000 0000

## ADC interrupt enable register (ADC\_IER)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	AWD IE	Res.	Res.	OVRIE	EOSEQ IE	EOCIE	EOSMP IE	ADRDY IE							
								rw			rw	rw	rw	rw	rw

AWDIE	Analog watchdog interrupt enable
OVRIE	Overrun interrupt enable
EOSEQIE	End of conversion sequence interrupt enable
EOCIE	End of conversion interrupt enable
EOSMPIE	End of sampling flag interrupt enable
ADRDYIE	ADC ready interrupt enable

0: Interrupt disabled  
1: Interrupt enabled

Reset value: 0x0000 0000

## ADC channel selection register (ADC\_CHSELr)

CHSELx	Channel-x selection
0	Input Channel-x is not selected for conversion
1	Input Channel-x is selected for conversion

Reset value: 0x0000 0000

### ADC control register (ADC\_CR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AD CAL	Res.	Res.	Res.	Res.	Res.	Res.									
rs															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ADSTP	Res.	ADSTA RT	ADDIS	ADEN	
										rs		rs	rs	rs	

ADCAL

ADC calibration

ADSTP

ADC stop conversion command

ADSTART

ADC start conversion command

ADDIS

ADC disable command

ADEN

ADC enable command

Reset value: 0x0000 0000

### ADC Data alignment

ALIGN	RES	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0x0	0x0															DR[11:0]
	0x1	0x00															DR[9:0]
	0x2	0x00															DR[7:0]
	0x3	0x00															DR[5:0]
1	0x0																DR[11:0] 0x0
	0x1																DR[9:0] 0x00
	0x2																DR[7:0] 0x00
	0x3																0x00 DR[5:0] 0x0

### ADC configuration register 1 (ADC\_CFGR1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Res.										Res.	Res.	AWDEN	AWDSGL	Res.	Res.	DISCEN
	rw	rw	rw	rw	rw					rw	rw					rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AUTOFF	WAIT	CONT	OVRMOD	EXTEN[1:0]	Res.					EXTSEL[2:0]	ALIGN	RES[1:0]	SCAND	DMAC	DMAEN	
rw	rw	rw	rw	rw						rw	rw	rw	rw	rw	rw	

AWDCH [ 4 : 0 ]

Analog watchdog channel selection

AWDEN

Analog watchdog enable

AWDSGL

Enable the watchdog on a single channel or on all channels

DISCEN

Discontinuous mode

AUTOFF

Auto-off mode

WAIT

Wait conversion mode

CONT

Single / continuous conversion mode

OVRMOD

Overrun management mode

EXTEN [ 1 : 0 ]

External trigger enable and polarity selection

00: Hardware trigger detection disabled

01: Hardware trigger detection on the rising edge

10: Hardware trigger detection on the falling edge

11: Hardware trigger detection on rising and falling edges

External trigger selection

000: TRG0 001: TRG1 010: TRG2 011: TRG3

100: TRG4 101: TRG5 110: TRG6 111: TRG7

ALIGN

Data alignment

0: Right alignment

1: Left alignment

RES [ 1 : 0 ]

Data resolution

00: 12 bits ; 01: 10 bits; 10: 8 bits ; 11: 6 bits

SCANDIR

Scan sequence direction

0: Upward scan (from CHSEL0 to CHSEL16)

1: Backward scan (from CHSEL16 to CHSEL0)

DMACFG

Direct memory access configuration

DMAEN

Direct memory access enable

Reset value: 0x0000 0000

## EXTERNAL INTERRUPTS

### Interrupt mask register (EXTI\_IMR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR31	MR30	MR29	MR28	MR27	MR26	MR25	MR24	MR23	MR22	MR21	MR20	MR19	MR18	MR17	MR16
rw															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
rw															

MRx

Interrupt mask on external/internal line x

0: Interrupt request from Line x is masked

1: Interrupt request from Line x is not masked

Reset value: 0x0F94 0000

### Falling trigger selection register (EXTI\_FTSR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	TR22	TR21	TR20	TR19	Res	TR17	TR16
									rw	rw	rw	rw		rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR15	TR14	TR13	TR12	TR11	TR10	TR9	TR8	TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

TRx

Rising trigger configuration bit of line x (x = 22 to 0)

0: Falling trigger disabled

1: Falling trigger enabled

Reset value: 0x0000 0000

### Rising trigger selection register (EXTI\_RTSR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR15	TR14	TR13	TR12	TR11	TR10	TR9	TR8	TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

TRx

Rising trigger configuration bit of line x (x = 22 to 0)

0: Rising trigger disabled

1: Rising trigger enabled

Reset value: 0x0000 0000

### Pending register (EXTI\_PR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PR15	PR14	PR13	PR12	PR11	PR10	PR9	PR8	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
rc_w1															

PRx

Pending bit on line x (x = 22 to 0)

0: No trigger request occurred

1: selected trigger request occurred

Reset value: Undefined

## SYSTEM CONFIGURATION CONTROLLER

### SYSCFG external interrupt configuration register 1 (SYSCFG\_EXTICR1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI3[3:0]				EXTI2[3:0]				EXTI1[3:0]				EXTI0[3:0]			
rw	rw	rw	rw												

EXIx [3:0]                    EXTI x configuration bits (x = 0 to 3)

- x000: PA[x] pin
- x001: PB[x] pin
- x010: PC[x] pin
- x011: PD[x] pin
- x100: PE[x] pin
- x101: PF[x] pin
- other configurations: reserved

Reset value: 0x0000 0000

EXI0, EXI1, EXI2, EXI3 selected in the in the SYSCFG\_EXTICR1 register

### SYSCFG external interrupt configuration register 3 (SYSCFG\_EXTICR3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI11[3:0]				EXTI10[3:0]				EXTI9[3:0]				EXTI8[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

EXIx [3:0]                    EXTI x configuration bits (x = 8 to 11)

- x000: PA[x] pin
- x001: PB[x] pin
- x010: PC[x] pin
- x011: PD[x] pin
- x100: PE[x] pin
- x101: PF[x] pin
- other configurations: reserved

Reset value: 0x0000 0000

EXI8, EXI9, EXI10, EXI11 selected in the in the SYSCFG\_EXTICR3 register

### SYSCFG external interrupt configuration register 2 (SYSCFG\_EXTICR2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI7[3:0]				EXTI6[3:0]				EXTI5[3:0]				EXTI4[3:0]			
rw	rw	rw	rw												

EXIx [3:0]                    EXTI x configuration bits (x = 4 to 7)

- x000: PA[x] pin
- x001: PB[x] pin
- x010: PC[x] pin
- x011: PD[x] pin
- x100: PE[x] pin
- x101: PF[x] pin
- other configurations: reserved

Reset value: 0x0000 0000

EXI4, EXI5, EXI6, EXI7 selected in the in the SYSCFG\_EXTICR2 register

### SYSCFG external interrupt configuration register 4 (SYSCFG\_EXTICR4)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI15[3:0]				EXTI14[3:0]				EXTI13[3:0]				EXTI12[3:0]			
rw	rw	rw	rw												

EXIx [3:0]                    EXTI x configuration bits (x = 12 to 15)

- x000: PA[x] pin
- x001: PB[x] pin
- x010: PC[x] pin
- x011: PD[x] pin
- x100: PE[x] pin
- x101: PF[x] pin
- other configurations: reserved

Reset value: 0x0000 0000

EXI12, EXI13, EXI14, EXI15 selected in the in the SYSCFG\_EXTICR4 reg.

## TIM14 (General-purpose timer)

### TIM14 control register 1 (TIM14\_CR1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	Res.	CKD[1:0]	ARPE	Res.	Res.	Res.	Res.	URS	UDIS	CEN	
						rw	rw	rw				rw	rw	rw	

CKD [1 : 0] Clock division

00:  $t_{DTS} = t_{CK\_INT}$

01:  $t_{DTS} = 2 \times t_{CK\_INT}$

10:  $t_{DTS} = 4 \times t_{CK\_INT}$

11: X

ARPE Auto-reload preload enable

0: TIMx\_ARR register is not buffered

1: TIMx\_ARR register is buffered

URS Update request source

0: A counter overflow or setting the UG bit generates a UEV event

1: Only counter overflow generates an UEV if enabled

UDIS Update disable

0: UEV enabled. An UEV is generated by counter overflow or setting UG bit

1: UEV disabled

CEN Counter enable

0: Counter disabled

1: Counter enabled

Reset value: 0x0000

### TIM14 interrupt enable register (TIM14\_DIER)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	CC1IE	UIE													
														rw	rw

CC1IE

Capture/Compare 1 interrupt enable

UIE

Update interrupt enable

0: Interrupt disabled

1: Interrupt enabled

Reset value: 0x0000

TIM14 status register (TIM14_SR)																TIM14 event generation register (TIM14_EGR)																																																																																	
<table border="1"> <tr> <td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>CC1OF</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>CC1F</td><td>UIF</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>Res.</td><td>CC1G</td><td>UG</td></tr> <tr> <td></td><td></td><td></td><td></td><td></td><td></td><td>rc_w0</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>rc_w0</td><td>rc_w0</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>w</td><td>w</td></tr> </table>																Res.	Res.	Res.	Res.	Res.	Res.	CC1OF	Res.	CC1F	UIF	Res.	CC1G	UG							rc_w0									rc_w0	rc_w0													w	w																																						
Res.	Res.	Res.	Res.	Res.	Res.	CC1OF	Res.	CC1F	UIF	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	CC1G	UG																																																																										
						rc_w0									rc_w0	rc_w0													w	w																																																																			
CC1OF																Capture/Compare 1 overcapture flag																																																																																	
CC1IF																Capture/Compare 1 interrupt flag																																																																																	
UIF																Update interrupt flag																																																																																	
0: Flag clear																0: Flag clear																																																																																	
1: Flag set																1: Flag set																																																																																	
Reset value:																0x0000																																																																																	
TIM14 auto-reload register (TIM14_ARR)																TIM14 prescaler (TIM14_PSC)																																																																																	
<table border="1"> <tr> <td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>PSC[15:0]</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr> <tr> <td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>ARR[15:0]</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td><td>rw</td></tr> </table>																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	PSC[15:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	ARR[15:0]	rw																															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	PSC[15:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																																																																	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	ARR[15:0]	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw																																																																	
ARR [15:0]																Auto-reload value (16-bit)																																																																																	
Reset value:																0x0000																																																																																	
TIM14 counter (TIM14_CNT)																TIM14 capture and compare register (TIM14_CCR1)																																																																																	
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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	CNT[15:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																																																																	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	CCR1[15:0]	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw																																																																	
CNT [15:0]																Counter value (16-bit)																																																																																	
Reset value:																0x0000																																																																																	

## TIM14 (General-purpose timer)

### TIM14 capture and compare mode register 1 (TIM14\_CCMR1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	OC1M[2:0]	OC1PE	OC1FE	CC1S[1:0]											
Res.	IC1F[3:0]	IC1PSC[1:0]													
									rw	rw	rw	rw	rw	rw	rw

### Output compare mode

OC1M[2:0] Output compare 1 mode

000: Frozen or no effect

001: Set channel 1 to inactive level on match

010: Set channel 1 to inactive level on match

011: Toggle

000: Force active level - OC1REF is forced high.

001: Force active level - OC1REF is forced high.

010: PWM mode 1

011: PWM mode 2

OC1PE Output compare 1 preload enable

0: Preload register on TIMx\_CCR1 disabled.

1: Preload register on TIMx\_CCR1 enabled

OC1FE Output compare 1 fast enable

0: CC1 behaves normally depending on counter and CCR1 values even when the trigger is ON.

1: An active edge on the trigger input acts like a compare match on CC1 output.

Capture/compare 1 selection

00: CC1 channel is configured as output.

01: CC1 channel is configured as input, IC1 is mapped on TI1

10: Reserved

11: Reserved

CC1S[1:0]

### TIM14 capture and compare enable register (TIM14\_CCER)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	CC1NP	Res.													
														rw	rw

CC1NP/TI1FP1 Capture/Compare 1 complementary output Polarity  
Channel as an output: CC1 channel configured as output: CC1NP must be kept cleared.

Channel as an input: CC1NP bit is used in conjunction with CC1P to define TI1FP1 polarity

CC1P Capture/Compare 1 output Polarity

Channel as an output

0: OC1 active high

1: OC1 active low

Channel as an input

00: noninverted/rising edge causes event

01: inverted/falling edge causes event

10: Reserved

11: noninverted/both edges cause event

CC1E Capture/Compare 1 output enable

0: Output capture/compare disabled

1: Output capture/compare enabled

Reset value: 0x0000

**Input capture mode**

IC1F[3:0]

Input capture 1 filter  
0000: no filter  
0001:  $f_{\text{SAMPLING}} = f_{\text{CK\_INT}}$ , N = 2  
0010:  $f_{\text{SAMPLING}} = f_{\text{CK\_INT}}$ , N = 4  
0011:  $f_{\text{SAMPLING}} = f_{\text{CK\_INT}}$ , N = 8  
0100:  $f_{\text{SAMPLING}} = f_{\text{CK\_DTS}}/2$ , N = 6  
0101:  $f_{\text{SAMPLING}} = f_{\text{CK\_DTS}}/2$ , N = 8  
0110:  $f_{\text{SAMPLING}} = f_{\text{CK\_DTS}}/4$ , N = 6  
0111:  $f_{\text{SAMPLING}} = f_{\text{CK\_DTS}}/4$ , N = 8  
1000:  $f_{\text{SAMPLING}} = f_{\text{CK\_DTS}}/8$ , N = 6  
1001:  $f_{\text{SAMPLING}} = f_{\text{CK\_DTS}}/8$ , N = 8  
1010:  $f_{\text{SAMPLING}} = f_{\text{CK\_DTS}}/16$ , N = 5  
1011:  $f_{\text{SAMPLING}} = f_{\text{CK\_DTS}}/16$ , N = 6  
1100:  $f_{\text{SAMPLING}} = f_{\text{CK\_DTS}}/16$ , N = 8  
1101:  $f_{\text{SAMPLING}} = f_{\text{CK\_DTS}}/32$ , N = 5  
1110:  $f_{\text{SAMPLING}} = f_{\text{CK\_DTS}}/32$ , N = 6  
1111:  $f_{\text{SAMPLING}} = f_{\text{CK\_DTS}}/32$ , N = 8

IC1PSC[1:0]

Input capture 1 prescaler  
00: no prescaler, capture is done every event  
01: capture is done once every 2 events

10: capture is done once every 4 events  
11: capture is done once every 8 events

CC1S[1:0]

Capture/compare 1 selection

00: CC1 channel is configured as output.  
01: CC1 channel is configured as input, IC1 is mapped on  
    TI1

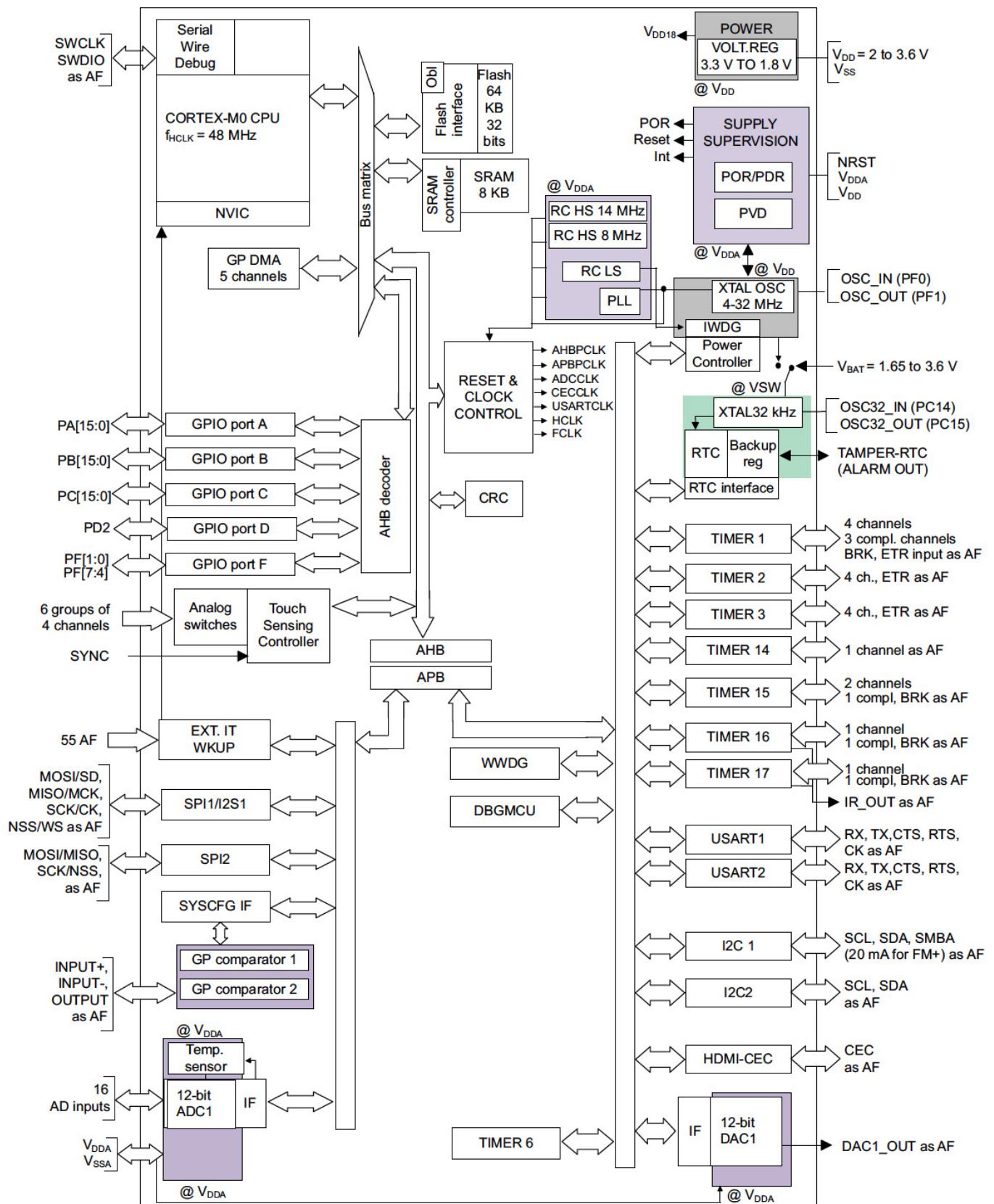
10: Reserved  
11: Reserved

Reset value: 0x0000

## INTERRUPT VECTOR TABLE

Position	Priority	Type of priority	Acronym	Description	Address
	-	-	-	Reserved	0x0000 0000
	-3	fixed	Reset	Reset	0x0000 0004
	-2	fixed	NMI	Non maskable interrupt. The RCC Clock Security System (CSS) is linked to the NMI vector.	0x0000 0008
	-1	fixed	HardFault	All class of fault	0x0000 000C
	3	settable	SVCall	System service call via SWI instruction	0x0000 002C
	5	settable	PendSV	Pendable request for system service	0x0000 0038
	6	settable	SysTick	System tick timer	0x0000 003C
0	7	settable	WWDG	Window watchdog interrupt	0x0000 0040
1	8	settable	PVD_VDDIO2	PVD and V <sub>DDIO2</sub> supply comparator interrupt (combined EXTI lines 16 and 31)	0x0000 0044
2	9	settable	RTC	RTC interrupts (combined EXTI lines 17, 19 and 20)	0x0000 0048
3	10	settable	FLASH	Flash global interrupt	0x0000 004C
4	11	settable	RCC_CRS	RCC and CRS global interrupts	0x0000 0050
5	12	settable	EXTI0_1	EXTI Line[1:0] interrupts	0x0000 0054
6	13	settable	EXTI2_3	EXTI Line[3:2] interrupts	0x0000 0058
7	14	settable	EXTI4_15	EXTI Line[15:4] interrupts	0x0000 005C
8	15	settable	TSC	Touch sensing interrupt	0x0000 0060
9	16	settable	DMA_CH1	DMA channel 1 interrupt	0x0000 0064
10	17	settable	DMA_CH2_3	DMA channel 2 and 3 interrupts	0x0000 0068
11	18	settable	DMA_CH4_5_6_7	DMA channel 4, 5, 6 and 7 interrupts	0x0000 006C
12	19	settable	ADC_COMP	ADC and COMP interrupts (ADC interrupt combined with EXTI lines 21 and 22)	0x0000 0070
13	20	settable	TIM1_BRK_UP_TRG_COM	TIM1 break, update, trigger and commutation interrupt	0x0000 0074
14	21	settable	TIM1_CC	TIM1 capture compare interrupt	0x0000 0078
15	22	settable	TIM2	TIM2 global interrupt	0x0000 007C
16	23	settable	TIM3	TIM3 global interrupt	0x0000 0080
17	24	settable	TIM6_DAC	TIM6 global interrupt and DAC underrun interrupt	0x0000 0084
18	25	settable	TIM7	TIM7 global interrupt	0x0000 0088
19	26	settable	TIM14	TIM14 global interrupt	0x0000 008C
20	27	settable	TIM15	TIM15 global interrupt	0x0000 0090
21	28	settable	TIM16	TIM16 global interrupt	0x0000 0094
22	29	settable	TIM17	TIM17 global interrupt	0x0000 0098
23	30	settable	I2C1	I <sup>2</sup> C1 global interrupt (combined with EXTI line 23)	0x0000 009C
24	31	settable	I2C2	I <sup>2</sup> C2 global interrupt	0x0000 00A0
25	32	settable	SPI1	SPI1 global interrupt	0x0000 00A4
26	33	settable	SPI2	SPI2 global interrupt	0x0000 00A8
27	34	settable	USART1	USART1 global interrupt (combined with EXTI line 25)	0x0000 00AC
28	35	settable	USART2	USART2 global interrupt (combined with EXTI line 26)	0x0000 00B0
29	36	settable	USART3_4	USART3 and USART4 global interrupts	0x0000 00B4
30	37	settable	CEC_CAN	CEC and CAN global interrupts (combined with EXTI line 27)	0x0000 00B8
31	38	settable	USB	USB global interrupt (combined with EXTI line 18)	0x0000 00BC

## STM32F0 SYSTEM OVERVIEW



## ALTERNATIVE FUNCTIONS

**Table 14. Alternate functions selected through GPIOA\_AFR registers for port A**

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0		USART2_CTS	TIM2_CH1_ETR	TSC_G1_IO1				COMP1_OUT
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	TSC_G1_IO2				
PA2	TIM15_CH1	USART2_TX	TIM2_CH3	TSC_G1_IO3				COMP2_OUT
PA3	TIM15_CH2	USART2_RX	TIM2_CH4	TSC_G1_IO4				
PA4	SPI1 NSS, I2S1_WS	USART2_CK		TSC_G2_IO1	TIM14_CH1			
PA5	SPI1_SCK, I2S1_CK	CEC	TIM2_CH1_ETR	TSC_G2_IO2				
PA6	SPI1_MISO, I2S1_MCK	TIM3_CH1	TIM1_BKIN	TSC_G2_IO3		TIM16_CH1	EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM1_CH1N	TSC_G2_IO4	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT				
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2	TSC_G4_IO1				
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	TSC_G4_IO2				
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	TSC_G4_IO3				COMP1_OUT
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	TSC_G4_IO4				COMP2_OUT
PA13	SWDIO	IR_OUT						
PA14	SWCLK	USART2_TX						
PA15	SPI1 NSS, I2S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT				

**Table 15. Alternate functions selected through GPIOB\_AFR registers for port B**

Pin name	AF0	AF1	AF2	AF3
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3
PB2				TSC_G3_IO4
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT
PB10	CEC	I2C2_SCL	TIM2_CH3	TSC_SYNC
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	TSC_G6_IO1
PB12	SPI2_NSS	EVENTOUT	TIM1_BKIN	TSC_G6_IO2
PB13	SPI2_SCK		TIM1_CH1N	TSC_G6_IO3
PB14	SPI2_MISO	TIM15_CH1	TIM1_CH2N	TSC_G6_IO4
PB15	SPI2_MOSI	TIM15_CH2	TIM1_CH3N	TIM15_CH1N

## STM32F051C6 LQFP48 PIN OUTS

