A Single-Stage High-Frequency Resonant AC/AC Converter

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***Abstract*—In many applications, such as large-scale LCD panel backlighting, street lighting, tunnel lighting, etc., an ac/dc light-emitting diode (LED) driver should realize the following three functions at least: power factor correction, multichannel constant current outputs, and galvanic isolation. A novel two-stage multichannel constant current ac/dc LED driver with a low cost and simple structure is proposed in this paper, which is composed of a high-frequency resonant ac/ac converter and as many passive LCL-T resonant rectifiers as the number of the output channels. The high frequency resonant ac/ac converter is focused on in this paper, which converts the ac-line input voltage into high frequency sinusoidal output voltage. First, topology derivation of the single-stage high-frequency resonant ac/ac converter is presented, also the operating principle of it. Then, the steady-state performance of it is completely analyzed, including its input power factor, voltage gain, total harmonic distortion of its output voltage, and its soft-switching condition. Finally, a 130 W prototype is built and the experimental results are given to verify the theoretical analysis.**

***Index Terms*—High-frequency resonant ac/ac converter, input power factor, light-emitting diode (LED) driver, voltage gain, zero-voltage-switching.**

I. Introduction

LIGHT-EMITTING-DIODE (LED) has become increasingly common in our daily lives for its high luminous efficacy, long lifetime, etc. [1]–[3]. The features of high luminous efficacy and long life make it use particularly attractive in applications such as street lighting, where costs associated with system maintenance and power consumption could be greatly decreased [4]–[9].

Commonly, input power for commercial LED street lamps lies between 60 and 240 W [10]; therefore, their drivers must employ power factor correction (PFC) techniques to achieve a high power factor to meet relevant harmonic standards, e.g., IEC 61000-3-2 [11]. Due to packaging technology and thermal management, connecting series LED strings in parallel has been a common practice to obtain sufficient luminance. Because of the exponential voltage–current characteristic and the negative temperature coefficient of the forward voltage drop of LEDs, the current sharing ability is poor in these strings. Thus, current balancing technique is needed for the driver [12]–[13]. Additionally, galvanic isolation is always necessary for safety consideration. All in all, an ac/dc driver for LED street lamps should realize the following three functions at least, which are PFC, multichannel constant current outputs, and galvanic isolation [14].

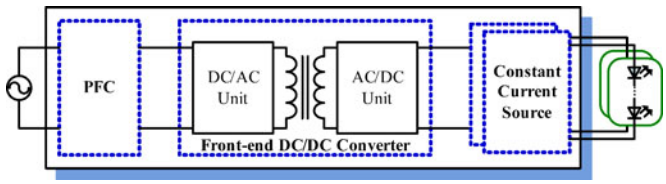

Fig. 1. Traditional three-stage multichannel constant current ac/dc LED driver.

Traditional three-stage multichannel constant current ac/dc LED driver for LED street lamps is shown in Fig. 1 [15]. High power factor is realized by the first PFC stage, and the ac input voltage is converted into stable dc-link voltage. The second front-end dc/dc converter stage is in the charge of providing galvanic isolation and converting the dc-link voltage into lower output dc voltage, moreover, the low-frequency voltage ripple of the dc-link voltage is greatly reduced. The third stage named constant current source stage makes the current through each LED string constant and current balancing among all LED strings is achieved. Since galvanic isolation is realized by employing a high-frequency isolation transformer in the second front-end dc/dc stage, a dc/ac unit (switching network) and an ac/dc unit (output rectifier and filter) are included. Therefore, in spite of its good performance, this three-stage solution is complicated and its efficiency is lowered to some extent; moreover, for the third stage to provide multiple constant current sources, each LED constant current source has its own power stage and controller, which increases the cost.

In order to simplify the circuit structure, boost efficiency, and reduce cost, many two-stage solutions are proposed by integrating the front-end dc/dc stage and constant current source stage into a second multichannel constant current source stage, as shown in Fig. 2 [16]–[20]. In [16], a multichannel constant current source is constructed by as many asymmetrical half bridges (AHBs) as LED strings. All the AHBs are galvanic isolated and the output current of each AHB is regulated to supply the LED string with constant current, since AHB can achieve soft switching in primary switches and high efficiency is achieved. However, the structure is still complicated and the cost is high because each AHB has its own power stage and controller. In [17], an LLC resonant converter with multitransformer and volt-

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Fig. 2. Two-stage multichannel constant current ac/dc LED driver.

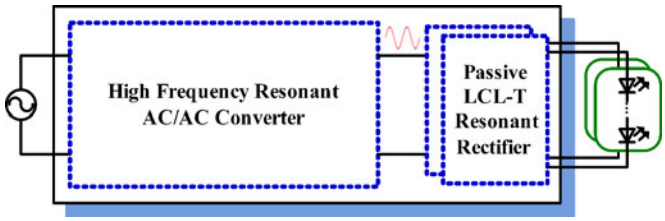

Fig. 3. Proposed two-stage multichannel constant current ac/dc LED driver.

age doubler configuration is adopted to serve as a multichannel constant current source. Because of the series connection of the primary side windings of the transformers and the charge balancing of the dc block capacitors, all output currents are automatically balanced. The structure is simplified and the cost is reduced when compared with the solution in [16], however, in order to implement a 2n-channels constant current source, n separated transformers are needed. In [18]–[20], a multichannel constant current source with only one transformer is proposed based on charge balancing principle of the dc block capacitors. The structure is further simplified and the cost is further reduced, thus it is a competitive solution. In [21], a multichannel constant current source with dynamic sinusoidal bus voltage regulation is proposed, which is composed of an *LCLC* series–parallel resonant inverter and as many passive LCL-T resonant rectifiers as output channels. It is a modular solution and can achieve multichannel constant current outputs as needed conveniently.

Inspired by this point that the passive LCL-T resonant rectifier analyzed in [21] can achieve constant output current without any control circuits provided that the amplitude of its input sinusoidal voltage is regulated to a constant value and the frequency of it is equal to the resonant frequency of the LCL-T resonant tank, another two-stage multichannel constant current ac/dc LED driver shown in Fig. 3 is proposed, which is composed of a high-frequency resonant ac/ac converter and as many passive LCL-T resonant rectifiers as the number of the LED strings needed. The high-frequency resonant ac/ac converter converts the ac-line voltage into high-frequency sinusoidal voltage with fixed amplitude and frequency, and implements PFC and galvanic isolation. The passive resonant rectifiers achieve multichannel constant current outputs inherently, since the resonant frequency of the LCL-T resonant network is equal to the frequency of its input sinusoidal voltage. The main advantage of the proposed two-stage solution is that it is a modular and cheap solution to realize multichannel outputs since only a passive resonant rectifier is needed to increase a constant current output channel, and only eight passive components are included to build a LCL-T resonant rectifier. The main disadvantage is that the output current of each output channel is not closed-loop regulated and the accuracy of it is affected by the tolerance of the passive components. The influence of the component tolerance on the output current is evaluated in [21] and it is possible to make the current difference among the output channels within 5% with proper design according to the experimental results.

Since the passive LCL-T resonant rectifier has been completely analyzed in [21], the main focus of this paper is the front high-frequency resonant ac/ac converter. There are two cascaded power conversion units included in the high-frequency resonant ac/ac converter, which are PFC unit and high-frequency resonant dc/ac unit. If the two units are independent, which means each unit has its own power stage and controller, the converter is called two-stage high-frequency resonant ac/ac converter. The two-stage solution has good performance, however, the component count is large and the cost is high, which can be used for high power applications. For the low-to-medium power applications, such as LED driver, single-stage solution is preferred because the component count and the cost can be obviously reduced by sharing the switches of the two power conversion units and adopting only one controller. In [22], a low-frequency ac to high-frequency ac inverter is presented, the cost is reduced when compared with the two-stage solution because only one unified controller is employed. However, the power stage of the inner two power conversion units is independent. In this paper, a true single-stage high-frequency resonant ac/ac converter is proposed by integrating the PFC unit and high-frequency resonant dc/ac unit into one power stage and adopting only one controller, thus the component count and cost are reduced further.

This paper is organized as follows. In Section II, the topology derivation of the single-stage high-frequency resonant ac/ac converter is described. The operating principle of the converter is presented in Section III and the performance of it is analyzed in Section IV in detail. The experimental results are given in Section IV and Section V summarizes the conclusions drawn from the investigation.

II. Topology Derivation

The main idea to derive the topology of a single-stage high-frequency resonant ac/ac converter is similar to that of a single-stage PFC ac/dc converter. A boost converter operating in discontinuous inductor current mode (DICM) with fixed duty cycle can achieve high power factor inherently, thus it is used as the PFC unit. Since an APWM *LCLC* series–parallel resonant inverter has the advantages of providing sinusoidal output voltage with extremely low total harmonic distortion (THD), achieving zero-voltage switching (ZVS) of the power switches and simple circuit structure [23], it is used as the high frequency resonant dc/ac unit. The topology of the proposed converter is derived by integrating the boost converter and the APWM *LCLC* series–parallel resonant inverter together in the following.

As shown in Fig. 4(a), the boost converter is composed of a boost inductor $L_{\rm B}$, a power switch $\rm S_B$, a diode $\rm D_B$, and a dc-link capacitor $C_{\rm B}$; the APWM *LCLC* series–parallel reso-

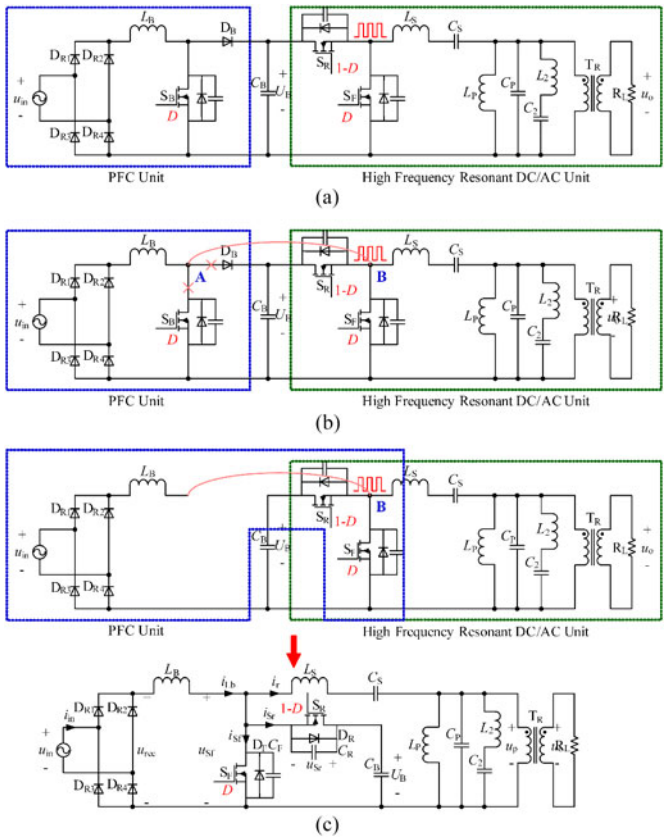

Fig. 4. Topology derivation of the single-stage high frequency resonant ac/ac converter.

nant inverter is composed of two power switches S_R and S_F, a *LCLC* series–parallel resonant tank, a second harmonic trap, a transformer T_R, along with the load resistor R_L. The resonant tank consists of a series branch and a parallel branch. The series branch composed by L_S and C_S is tuned around the operating frequency to achieve ZVS and maximum power transfer, however, the parallel branch composed by L_P and C_P is off-tuned to provide inductive impedance at the operating frequency. The second harmonic trap composed by L_2 and C_2 is adopted to eliminate the second harmonic component in the output voltage. It is noteworthy that S_R and S_F are complementarily operated. Additionally, in order to integrate the two units above together, S_B and S_R are turned ON and OFF at the same time. Since the voltage gain of the APWM *LCLC* series–parallel resonant inverter is centered on $D = 0.5$, where D is the duty cycle of S_R, gating signals of S_R and S_F can be exchanged, as shown in Fig. 4(b). From Fig. 4(b), when S_B and S_F are gated ON, node A and node B are connected together; when S_B and S_R are gated OFF, diode D_B is forced to conduct, simultaneously, S_R is gated ON, therefore, node A and node B are connected together too. In other words, the voltage between node A and node B is always zero and they can be directly shorted, thus, S_B and S_F are parallel-connected and one of them can be removed; D_B and S_R are parallel-connected too, however, the current through S_R is bidirectional, D_B should be removed accordingly. Finally, a single-stage high-frequency resonant ac/ac converter shown in Fig. 4(c) is derived.

From Fig. 4(c), it is clear that S_R and S_F are shared by the PFC unit and high-frequency resonant dc/ac unit, and only one controller is needed to control the amplitude of the high-frequency sinusoidal output voltage u_O, therefore, the circuit structure is simplified and the cost of it is low correspondingly when comparing with the two-stage solution shown in Fig. 4(a). However, the *LCLC* series–parallel resonant tank is quite complex and a second harmonic trap is included, which add the complexity of the topology and should be further simplified if possible in the future.

One of the biggest obstacles to putting the single-stage PFC ac/dc converter into use is the dc-link voltage varying with its input voltage amplitude and load, which is much higher at light load with maximum input voltage than at rated load with minimum input voltage, so is the proposed single-stage high-frequency resonant ac/ac converter. Fortunately, the specialty of LED applications happens to relieve the aforementioned problem for the proposed converter. With PWM enable dimming, the operating status of the converter can only be switched between shutdown and rated load [24]–[26]. Therefore, the maximum dc-link voltage is decided at the rated load with maximum input voltage.

III. Operating Principle

Fig. 5 shows the operating waveforms of the proposed converter and its equivalent circuits for each operating mode are presented in Fig. 6. The analysis and descriptions for every operating mode are listed as follows.

Mode 1 [$t_0 \le t < t_1$; see Fig. 6(a)]: At t_0, S_F is turned ON with zero voltage since the intrinsic diode is forced to conduct in the previous mode. The inductor current i_{Lb} increases linearly, simultaneously, the energy stored in the resonant tank freewheels through switch S_F and keeps supplying power to the load.

Mode 2 [$t_1 \le t < t_2$; see Fig. 6(b)]: At t_1, S_F is turned OFF, C_F is charged, and C_R is discharged at the same time. Since the increase rate of u_{Sf} is limited by C_F and C_R, SF is turned OFF at ZVS approximately and the turn-OFF losses of it can be reduced. Once u_{Sf} increases to U_B and u_{Sr} decreases to zero, this mode ends.

Mode 3 [$t_2 \le t < t3$; see Fig. 6(c)]: At t_2, u_{Sr} decreases to zero and the intrinsic diode D_R is forced to conduct. During this mode, L_B is discharged by $u_{in} - U_B$, and the energy stored in it releases to C_B and the resonant tank.

Mode 4 [$t_3 \le t < t_4$; see Fig. 6(d)]: At t_3, S_R is gated ON at ZVS because u_{Sr} is clamped to zero by the D_R. In this mode, the equivalent circuit is similar to mode 3.

Mode 5 [$t_4 \le t < t_5 \pm$; see Fig. 6(e)]: At t_4, inductor current i_{Lb} decreases to zero, simultaneously, diodes D_R1 and D_{R2} are reverse biased. In this mode, the energy stored in C_B releases to the resonant tank and keeps supplying power to the load.

Mode 6 [$t_5 \le t < t_6$; see Fig. 6(f)]: At t_5, S_R is turned OFF. Similarly, the increase rate of u_{Sr} is limited by C_F and C_R, S_R is turned OFF at ZVS approximately and its turn-OFF losses are reduced.

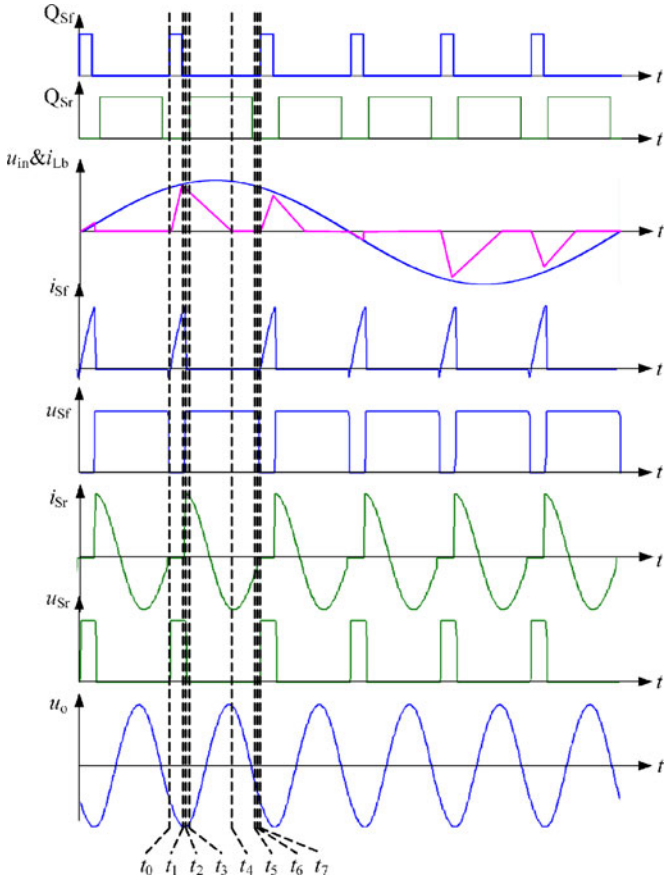

Fig. 5. Operational waveforms of the presented single-stage high frequency resonant ac/ac converter.

Mode 7 [$t_6 \le t < t_7$; see Fig. 6(g)]: At t_6,$u_{\rm Sf}$ decreases to zero and the intrinsic diode $\rm D_F$ starts to conduct, which creates a ZVS condition for turning ON $\rm S_F$. In this mode, diodes $\rm D_{R1}$ and $\rm D_{R4}$ are forced to conduct, the boost inductor $L_{\rm B}$ is charged by the ac-line voltage $u_{\rm in}$.

At t_7,$\rm S_F$ is turned ON at ZVS and the converter begins a new switching cycle.

Operational Modes 1–7 perform in the positive half-cycle of ac-line voltage. Since the operational modes which occur in the negative half-cycle is similar to those occurring in the positive half-cycle, they are omitted here.

IV. Performance Analysis

Before conducting the performance analysis of the presented single-stage high-frequency resonant ac/ac converter, the following assumptions are made:

1) the boost inductor $L_{\rm B}$ is designed to be operated in DCM;
2) the dc-link capacitor $C_{\rm B}$ is large enough that the ripple of the dc-link voltage $U_{\rm B}$ can be neglected;
3) the operating frequency of $\rm S_R$ and $\rm S_F$ is much higher than that of the ac-line voltage, thus, the ac-line voltage can be treated as a constant value in each switching period;
4) the losses are neglected and the efficiency of the converter is equal to one.

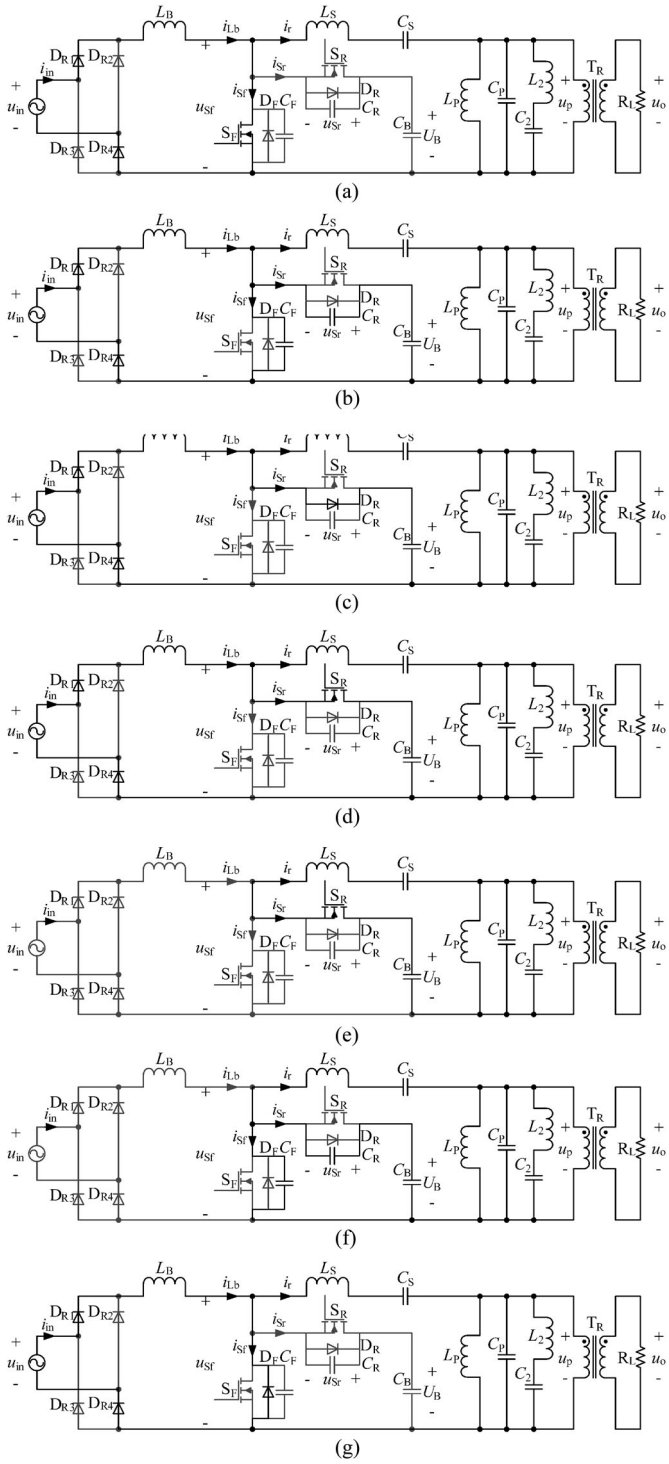

Fig. 6. Operational modes of the presented single-stage high frequency resonant ac/ac converter. (a) Mode 1 ($t_0 \le t < t_1$). (b) Mode 2 ($t_1 \le t < t_2$). (c) Mode 3 ($t_2 \le t < t_3$). (d) Mode 4 ($t_3 \le t < t_4$). (e) Mode 5 ($t_4 \le t < t_5$). (f) Mode 6 ($t_5 \le t < t_6$). (g) Mode 7 ($t_6 \le t < t_7$).

A. Input Factor

According to Fig. 4, the ac-line voltage is given as

$$u_{\rm in} = U_{\rm inm} \sin \omega t \tag{1}$$

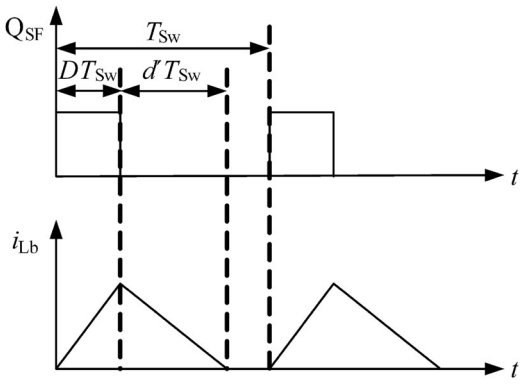

Fig. 7. Waveforms of $Q_{\rm Sf}$ and $i_{\rm Lb}$ during one switching period $T_{\rm SW}$.

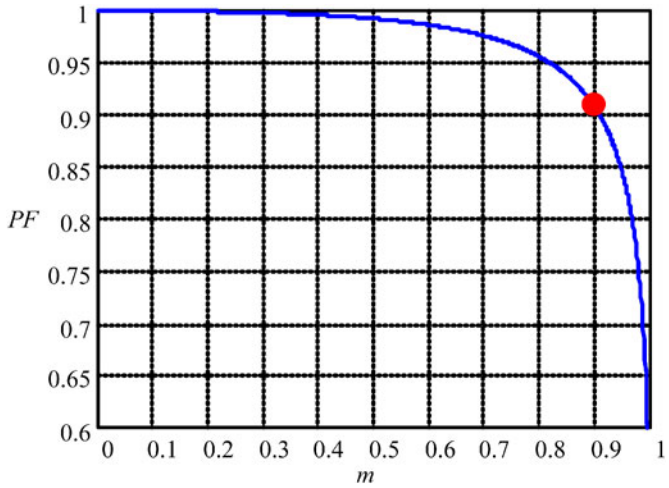

Fig. 8. Input power factor *PF* along with *m*.

where $U_{\rm inm}$ and ω is the amplitude and angular frequency of $u_{\rm in}$, respectively, and the phase angle is assumed to be zero.

Thus, the voltage appears after the diode bridge rectifier is derived as

$$u_{\rm rec} = U_{\rm inm} \left|\sin \omega t\right| \tag{2}$$

where $|\,|$ represents the modulus function.

The driving signal of switch S_F,Q_{Sf}, and the inductor current $i_{\rm Lb}$ are shown in Fig. 7. According to the volt-second balance principle to L_B in one switching period $T_{\rm Sw}$, the following equation is deduced

$$u_{\rm rec} D T_{\rm Sw} = (U_{\rm B} - u_{\rm rec}) d' T_{\rm Sw}. \tag{3}$$

The dc-link voltage U_B is assumed to be constant, moreover, only the amplitude of the high-frequency sinusoidal output voltage is closed-loop regulated, therefore, the duty cycle *D* of S_F can be treated to be constant during one period of the ac-line voltage, however, d' is variable with $u_{\rm rec}$.

According to Fig. 7, the average value of $i_{\rm Lb}$ in one switching period, $\bar{i}_{\rm LB}$, can be deduced as

$$\bar{i}_{\rm LB} = \frac{u_{\rm rec} D T_{\rm Sw} (D + d')}{2 L_{\rm B}}. \tag{4}$$

From (2) to (4), it is derived that

$$\bar{i}_{\rm LB} = \frac{km \left|\sin \omega t\right|}{1 - m \left|\sin \omega t\right|} \tag{5}$$

where

$$k = \frac{D^2 T_{\rm Sw} U_{\rm B}}{2 L_{\rm B}} \tag{6}$$

$$m = \frac{U_{\rm inm}}{U_{\rm B}}. \tag{7}$$

Since the RMS value of the input current $i_{\rm in}$,$I_{\rm in}$, is equal to that of the inductor current $i_{\rm Lb}$, $I_{\rm Lb}$, from (5), it is deduced that

$$I_{\rm in} = I_{\rm LB} = \sqrt{\frac{1}{\pi} \int_0^{\pi} \left[\frac{km \left|\sin \omega t\right|}{1 - m \left|\sin \omega t\right|}\right]^2 d(\omega t)} = k \sqrt{\frac{A}{\pi}} \tag{8}$$

where

$$\begin{aligned} A &= \int_0^{\pi} \left[\frac{m \left|\sin \omega t\right|}{1 - m \left|\sin \omega t\right|}\right]^2 d(\omega t) \\ &= \frac{2}{m(1-m^2)} + \frac{2}{m^2} + \frac{4m^2}{m^2 (1-m^2) \sqrt{1-m^2}} \\ &\quad \times \left[\frac{\pi}{2} - \text{arctg}\left(\frac{-m}{\sqrt{1-m^2}}\right)\right]. \end{aligned} \tag{9}$$

From (2) and (5), the average input power $P_{\rm in}$ is derived as

$$P_{\rm in} = \frac{kmBU_{\rm inm}}{\pi} \tag{10}$$

where

$$B = \int_0^{\pi} \frac{\left|\sin \omega t\right|^2}{1 - m \left|\sin \omega t\right|} d(\omega t). \tag{11}$$

The distortion of the input voltage is negligible, thus, the input power factor *PF* is can be deduced as

$$PF = \frac{P_{\rm in}}{U_{\rm in} I_{\rm in}} = B \sqrt{\frac{2}{\pi A}} \tag{12}$$

where $U_{\rm in}$ is the RMS value of $u_{\rm in}$.

From (9), (11), and (12), it is clear that the input power factor *PF* is only related with *m*, and the diagram *PF* along with *m* is plotted in Fig. 8. From Fig. 8, *m* should be smaller than 0.9 to ensure *PF* higher than 0.9 to qualify for Energy Star.

B. Voltage Gain

The voltage gain of the single-stage high-frequency resonant ac/ac converter $M_{\rm ac-ac}$ is defined as the ratio of the amplitude of the voltage across the primary winding of the transformer $T_R U_{\rm pm}$ to that of the input ac-line voltage $U_{\rm inm}$ for convenience, which is the product of the voltage gain of the PFC unit $M_{\rm PFC}$ and that of the high-frequency resonant dc/ac unit $M_{\rm dc-ac}$. The ratio of the amplitude of the output voltage $U_{\rm om}$ to $U_{\rm pm}$ is related with the turns ratio of the transformer n.$M_{\rm ac-ac}$,$M_{\rm PFC}$

and $M_{\mathrm{dc-ac}}$ are defined as follows:

$$M_{\mathrm{ac-ac}} = \frac{U_{\mathrm{Pm}}}{U_{\mathrm{inm}}} \tag{13}$$

$$M_{\mathrm{PFC}} = \frac{U_{\mathrm{B}}}{U_{\mathrm{inm}}} = \frac{1}{m} \tag{14}$$

$$M_{\mathrm{dc-ac}} = \frac{U_{\mathrm{pm}}}{U_{\mathrm{B}}}. \tag{15}$$

The efficiency of the converter is assumed to be equal to one, thus

$$P_{\mathrm{in}} = P_{\mathrm{out}} = P. \tag{16}$$

For the PFC unit, substitute (6), (11), (14), and (16) into (10), the following equation is deduced as

$$\frac{D^2 T_{\mathrm{Sw}} {U_{\mathrm{inm}}}^2}{2\pi L_{\mathrm{B}}} \int_0^{\pi} \frac{M_{\mathrm{PFC}} \sin^2 \omega t}{M_{\mathrm{PFC}} - \sin \omega t} = P. \tag{17}$$

The inductor L_{B} should be small enough to make the PFC unit operate in DICM. According to the operating principle of the PFC unit, if the PFC unit operates in DICM, when u_{in} is equal to its peak value U_{inm}, it is sure that the PFC unit can operate in DICM during the whole period of the ac-line voltage. Therefore, half of the maximum value of i_{Lb} during one switching period at $u_{\mathrm{in}} = U_{\mathrm{inm}}$, I_{Lbmax} should be larger than the maximum value of $\bar{i}_{\mathrm{LB}}$, $\bar{I}_{\mathrm{Lbmax}}$. I_{Lbmax} and $\bar{I}_{\mathrm{Lbmax}}$ are derived as

$$I_{\mathrm{Lbmax}} = \frac{U_{\mathrm{inm}} D T_{\mathrm{Sw}}}{2L_{\mathrm{B}}} = \frac{km}{D} \tag{18}$$

$$\bar{I}_{\mathrm{Lbmax}} = \frac{km}{1-m}. \tag{19}$$

Thus

$$D < 1 - m. \tag{20}$$

That is

$$D < 1 - \frac{1}{M_{\mathrm{PFC}}} \left(M_{\mathrm{PFC}} > \frac{1}{1-D} \right). \tag{21}$$

Commonly, electrolytic capacitor is adopted to realize C_{B} and the voltage stress of it is commonly limited to 450 V. When U_{inm}= 310 V, it is deduced that

$$M_{\mathrm{PFC}} < 1.45. \tag{22}$$

From (17), (21), and (22), the relationship between M_{PFC} and D is shown in Fig. 9 with $P = 130$ W, U_{inm}= 310 V, T_{Sw}= 10 μS(f_{Sw}= 100 kHz) and L_{B}= 150μH. It is shown that the expected range of D is about 0.128–0.177, the corresponding range of M_{PFC} is 1.15–1.45 and they are positive correlated. Here we choose D= 0.16 as an example and the corresponding voltage gain value $M_{\mathrm{PFC}} = 1.31$. Additionally, from (17), it is clear that the allowed range of D varies with the amplitude of the input voltage U_{inm}.

According to the operating principle of the proposed converter presented in Section III, switching voltage u_{Sf} during

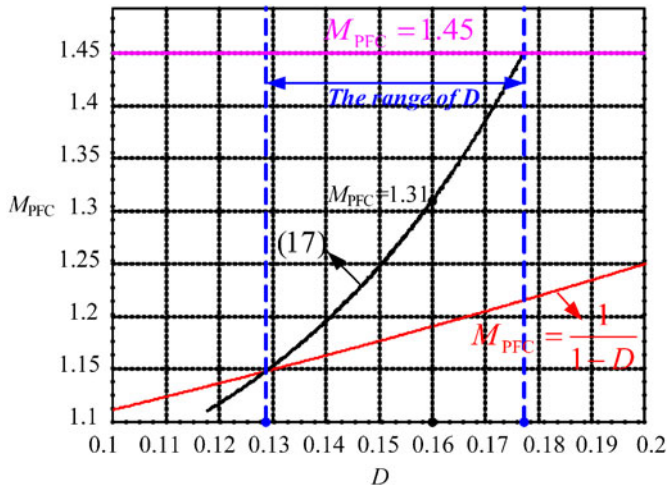

Fig. 9. Relationship between M_{PFC} and D.

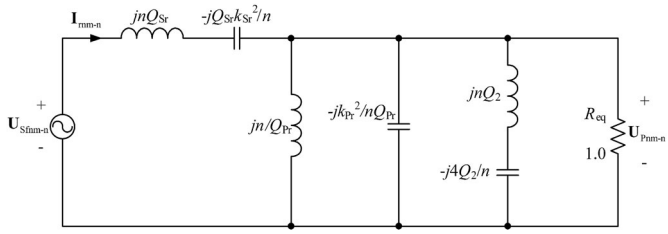

Fig. 10. Nth harmonic equivalent circuit of the high frequency resonant dc/ac unit.

one switching period is represented as

$$u_{\mathrm{Sf}}(t) = \begin{cases} 0, & 0 \le t < DT_{\mathrm{Sw}} \\ U_{\mathrm{B}}, & DT_{\mathrm{Sw}} \le t < T_{\mathrm{Sw}} \end{cases}. \tag{23}$$

Its Fourier series expansion is calculated as

$$u_{\mathrm{Sf}} = (1-D)U_{\mathrm{B}} + \sum_{n=1}^{\infty} \frac{\sqrt{2} U_{\mathrm{B}} \sqrt{1 - \cos 2n\pi D}}{n\pi} \times \sin(n\omega_{\mathrm{Sw}} t + \theta_n - \pi) \tag{24}$$

where

$$\omega_{\mathrm{Sw}} = 2\pi f_{\mathrm{Sw}} \tag{25}$$

$$\theta_n = \tan^{-1} \frac{\sin 2\pi n D}{1 - \cos 2\pi n D}. \tag{26}$$

Because of the dc-block capacitor C_{S}, only the ac components of u_{Sf} are considered in the following. The per unit nth harmonic equivalent circuit of the high-frequency resonant dc/ac unit is shown in Fig. 10. The minimum dc-link voltage U_{Bmin}, the equivalent resistance R_{eq}, and the switching angular frequency ω_{SW} are chosen as the base values. In Fig. 10, the following quantities are defined as follows.

Per unit switching voltage phasor

$$\mathbf{U}_{\mathrm{Sfnm-n}} = \frac{U_{\mathrm{B}} \sqrt{2 - 2\cos 2n\pi D}}{U_{\mathrm{B\,min}} n\pi} \angle(\theta_{\mathrm{n}} - \pi). \tag{27}$$

Per unit series and parallel resonant angular frequency

$$k_{\mathrm{Sr}} = \omega_{\mathrm{Sr}}/\omega_{\mathrm{Sw}} \tag{28}$$

$$k_{\mathrm{Pr}} = \omega_{\mathrm{Pr}}/\omega_{\mathrm{Sw}} > 1 \tag{29}$$

where ω_{Sr} and ω_{Pr} are defined as

$$\omega_{\mathrm{Sr}} = 1/\sqrt{L_{\mathrm{S}}C_{\mathrm{S}}} \tag{30}$$

$$\omega_{\mathrm{Pr}} = 1/\sqrt{L_{\mathrm{P}}C_{\mathrm{P}}}. \tag{31}$$

Quality factor of the series resonant network and the parallel resonant network, Q_{S} and Q_{P}

$$Q_{\mathrm{Sr}} = \frac{\omega_{\mathrm{Sw}}L_{\mathrm{S}}}{R_{\mathrm{eq}}} \tag{32}$$

$$Q_{\mathrm{pr}} = \frac{R_{\mathrm{eq}}}{\omega_{\mathrm{Sw}}L_{\mathrm{P}}} \tag{33}$$

where $R_{\mathrm{eq}} = N^2R_{\mathrm{L}}$ is equivalent load resistor seen at the primary side of the transformer, *N* is the turns ratio of the transformer T_{R} and R_{L} is the load resistor.

Quality factor of the second harmonic trap, Q_2

$$Q_2 = \frac{\omega_{\mathrm{Sw}}L_2}{R_{\mathrm{eq}}}. \tag{34}$$

From Fig. 10, the following equations are deduced as

$$\mathbf{U}_{\mathrm{Pnm-n}} = \frac{Z_{\mathrm{pn}}}{Z_{\mathrm{sn}}+Z_{\mathrm{pn}}}\mathbf{U}_{\mathrm{Sfnm-n}} \tag{35}$$

$$Z_{\mathrm{Sn}} = jQ_{\mathrm{Sr}}\left(n - \frac{k_{\mathrm{Sr}}^2}{n}\right) \tag{36}$$

$$Z_{\mathrm{Pn}} = \frac{1}{1 + jQ_{\mathrm{Pr}}\left(\frac{n}{k_{\mathrm{Pr}}^2} - \frac{1}{n}\right) + \frac{1}{j\left(nQ_2 - \frac{4Q_2}{n}\right)}}. \tag{37}$$

From (27), (35)–(37), the ratio of the peak value of the *n*th harmonic voltage across the primary winding of the transformer $T_{\mathrm{R}}U_{\mathrm{Pnm}}$ and the dc-link voltage U_{B} is derived as

$$M_{\mathrm{dc-acn}} = \frac{U_{\mathrm{Pnm}}}{U_{\mathrm{B}}}U_{\mathrm{Bmin}} = \frac{\sqrt{2-2\cos 2n\pi D}\,|Z_{\mathrm{pn}}|}{n\pi\,|Z_{\mathrm{sn}}+Z_{\mathrm{pn}}|}. \tag{38}$$

For the high-frequency resonant dc/ac unit, first harmonic approximation approach can be adopted because of the perfect filtering performance of the *LCLC* series–parallel resonant circuit, therefore

$$M_{\mathrm{dc-ac}} = \frac{\sqrt{2-2\cos 2\pi D}\,|Z_{\mathrm{p1}}|}{\pi\,|Z_{\mathrm{s1}}+Z_{\mathrm{p1}}|}. \tag{39}$$

From (36), (37), and (39), $M_{\mathrm{dc-ac}}$ as a function of the duty cycle *D* is shown in Fig. 11 with $k_{\mathrm{Sr}} = 0.9$, $k_{\mathrm{Pr}} = 1.2$, $Q_{\mathrm{Sr}} = 2.5$, $Q_{\mathrm{Pr}} = Q_2 = 2.0$. It is shown that the curve is centered on $D = 0.5$ where $M_{\mathrm{dc-ac}}$ gets its maximum value 0.43.

Finally, the voltage gain of the high-frequency resonant ac/ac converter $M_{\mathrm{ac-ac}}$ varying with duty cycle *D* is shown in Fig. 12. It is showed that the range of $M_{\mathrm{ac-ac}}$ is 0.195–0.328 within the duty cycle range of 0.128–0.177 and also they have a positive relationship. It can be concluded that the duty cycle should be chosen between 0.128 and 0.177 at this operating point. When

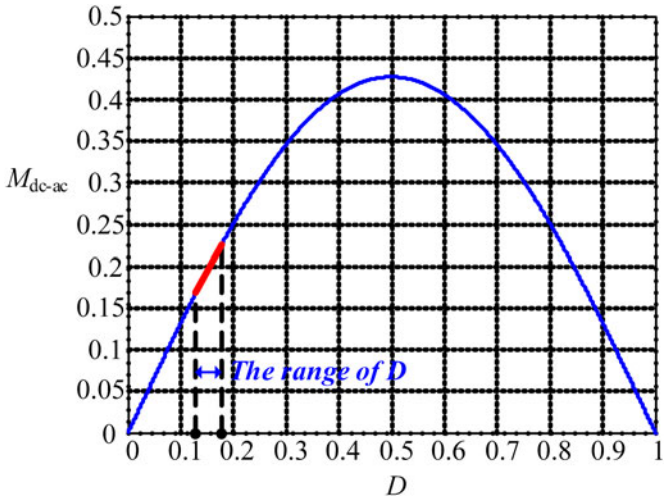

Fig. 11. Relationship between $M_{\mathrm{dc-ac}}$ and *D*.

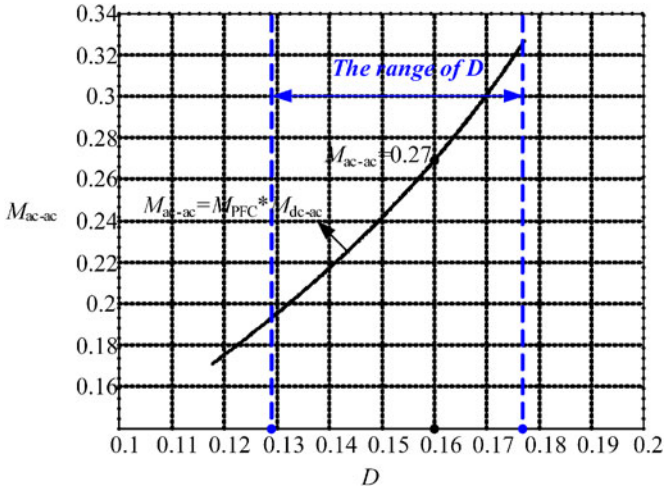

Fig. 12. Relationship between $M_{\mathrm{ac-ac}}$ and *D*.

$D = 0.16$ is chosen, the gain of the converter $M_{\mathrm{ac-ac}}$ is equal to 0.27.

C. THD of the Output Voltage

It is preferred that the THD of the sinusoidal output voltage u_{o} is as small as possible. From (38), if the second harmonic trap is not included, the harmonic profile of u_{p} is shown in Fig. 13 with $k_{\mathrm{Sr}} = 0.9$, $k_{\mathrm{Pr}} = 1.2$, $Q_{\mathrm{Sr}} = 2.5$, and $Q_{\mathrm{Pr}} = 2.0$. It can be seen that the most dominant harmonic is the second harmonic; therefore, a second harmonic trap with a quality factor $Q_2 = 2$ is adopted in the proposed converter.

Commonly, higher quality factor of the series and parallel resonant branch means better filtering performance and lower THD of the output voltage. However, high quality factor means high voltage and current stress of the resonant components. Thus, Q_{Sr} and Q_{Pr} should be as small as possible on the condition that THD of the output voltage qualify the requirement. From (38), THD of the output voltage as a function of Q_{Sr} and

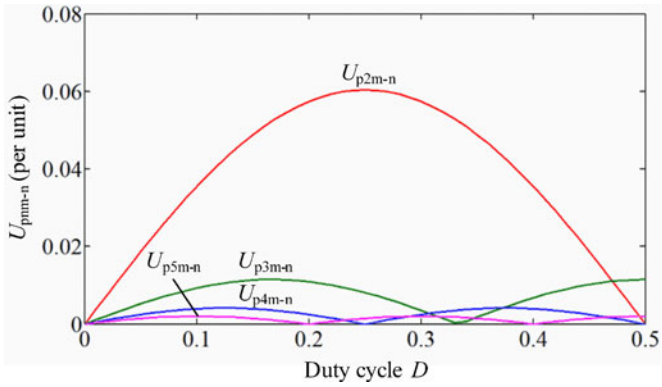

Fig. 13. Harmonic profile of $u_{\rm p}$ without the second harmonic trap.

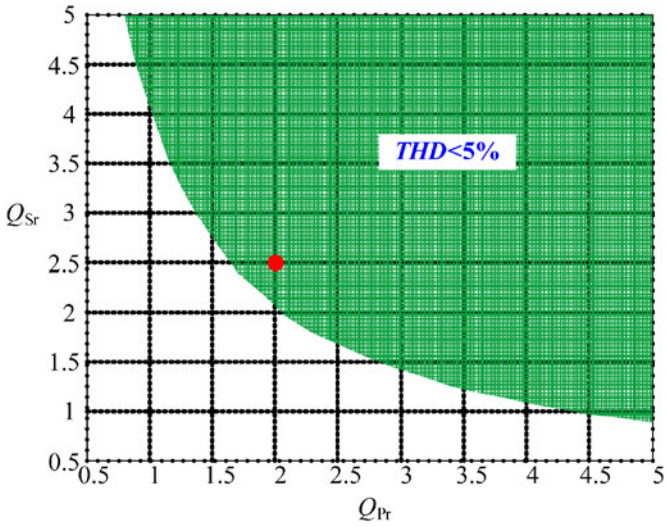

Fig. 14. THD along with $Q_{\rm Sr}$ and $Q_{\rm Pr}$.

$Q_{\rm Pr}$ with $D = 0.16$ and $Q_2 = 2.0$ is shown in Fig. 14. From Fig. 14, $Q_{\rm Sr} = 2.5, Q_{\rm Pr} = 2.0$ is a preferable choice to ensure THD $< 5\%$.

D. Soft Switching Condition

To provide information on the region of ZVS for the two switches $\rm S_R$ and $\rm S_F$, it is necessary to calculate the currents at turn-OFF of them.

When $\rm S_F$ is turned OFF and $\rm S_R$ is turned ON, switch current $i_{\rm Sf}$ is equal to the difference between $i_{\rm Lb}$ and $i_{\rm r}$. At the moment when $\rm S_F$ is turned OFF, $i_{\rm Lb}$ can be derived as

$$i_{\rm Lb}(DT_{\rm Sw}) = \frac{U_{\rm inm}\,|\sin\omega t|}{L_{\rm B}} DT_{\rm Sw}. \tag{40}$$

From Fig. 10, the value of $i_{\rm r}$ is deduced as

$$i_{\rm r}(t) = \sum_{n=1}^{\infty} \frac{U_{\rm B}\sqrt{2-2\cos(2n\pi D)}}{n\pi\,|Z_{\rm sn}+Z_{\rm pn}|\cdot R_{eq}} \sin(n\omega_{Sw}t + \theta_{\rm n} - \pi - \varphi_{\rm n}) \tag{41}$$

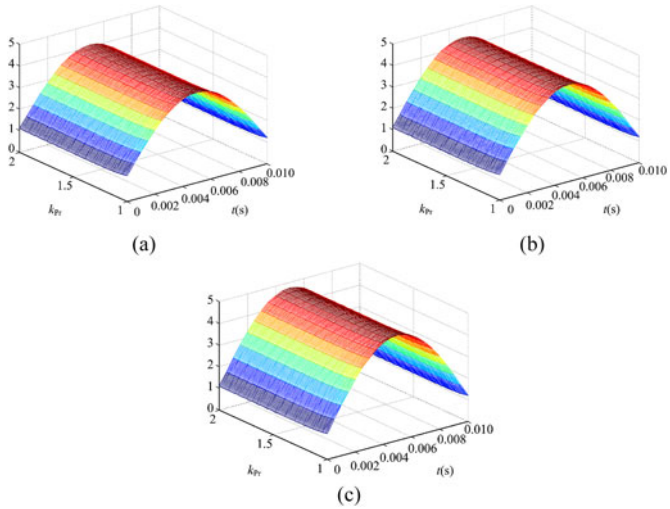

Fig. 15. $I_{\rm Sf-turn-off}$ along with $k_{\rm Pr}$ and t. (a) $U_{\rm inm} = 280$ V. (b) $U_{\rm inm} = 311$ V. (c) $U_{\rm inm} = 342$ V.

where

$$\varphi_n = tan^{-1}\left(|Z_{\rm Sn}| - |Z_{\rm PYn}| + |Z_{\rm Sn}|\cdot|Z_{\rm PYn}|^2\right) \tag{42}$$

$$|Z_{\rm PYn}| = Q_{\rm Pr}\left(\frac{n}{k_{\rm Pr}^2} - \frac{1}{n}\right) - \frac{1}{Q_2\left(n-\frac{4}{n}\right)}. \tag{43}$$

As described in Section III, to achieve ZVS for $\rm S_R$, the intrinsic diode $\rm D_R$ should be forced to conduct prior to the turn-ON of $\rm S_R$, therefore, switch current $i_{\rm Sf}$ at the turn-OFF of it, $I_{\rm Sf-turn-off}$, should be positive. $I_{\rm Sf-turn-off}$ can be deduced as

$$I_{\rm Sf-turn-off} = i_{\rm Lb}(DT_{\rm Sw}) - i_{\rm r}(DT_{\rm Sw}). \tag{44}$$

From (40)–(44), $I_{\rm Sf-turn-off}$ along with $k_{\rm pr}$ and t within half of the ac-line period is plotted with $P_{\rm o} = 130$ W, $f_{\rm Sw} = 100$ kHz, $L_{\rm B} = 150\ \mu$H, $k_{\rm Sr} = 0.9, Q_{\rm Sr} = 2.5, Q_{\rm Pr} = 2.0, Q_2 = 2.0, D = 0.16$ and three input voltages of $U_{\rm inm} = 280$ V, $U_{\rm inm} = 311$ V and $U_{\rm inm} = 342$, as showed in Fig. 15(a), (b), and (c), respectively. It is shown that when $k_{\rm Pr}$ varies from 1.0 to 2.0, $I_{\rm Sf-turn-off}$ is always positive, that is to say that $\rm S_R$ can realize ZVS when $\rm S_F$ is turned OFF within half of the ac-line period easily.

To achieve ZVS for $\rm S_F$, the intrinsic diode $\rm D_F$ should be forced to conduct prior to the turn-ON of $\rm S_F$, therefore, switch current $i_{\rm Sr}$ at the turn-OFF of it, $I_{\rm Sr-turn-off}$, should be negative. Since the PFC unit operates in DICM and $i_{\rm Lb}$ has decreased to zero before turning OFF $S_{\rm R}$, $I_{\rm Sr-turn-off}$ can be derived as

$$I_{\rm Sr-turn-off} = -i_{\rm r}(T_{\rm Sw}). \tag{45}$$

From (41) to (43) and (45), the relationship between $I_{\rm Sr-turn-off}$ and $k_{\rm Pr}$ can be obtained with $P_{\rm o} = 130$ W, $f_{\rm Sw} = 100$ kHz, $k_{\rm Sr} = 0.9$, $Q_{\rm Sr} = 2.5, Q_{\rm Pr} = 2.0, Q_2 = 2.0, D = 0.16$ and three input voltages of $U_{\rm inm} = 280$ V, $U_{\rm inm} = 311$ V, and $U_{\rm inm} = 342$ V, as shown in Fig. 16. It can be concluded that there is a negative correlation between $k_{\rm Pr}$ and $I_{\rm Sr-turn-off}$. On one hand, $k_{\rm Pr}$ should be larger than 1.18 to achieve ZVS for $\rm S_F$, on the other hand, it should be

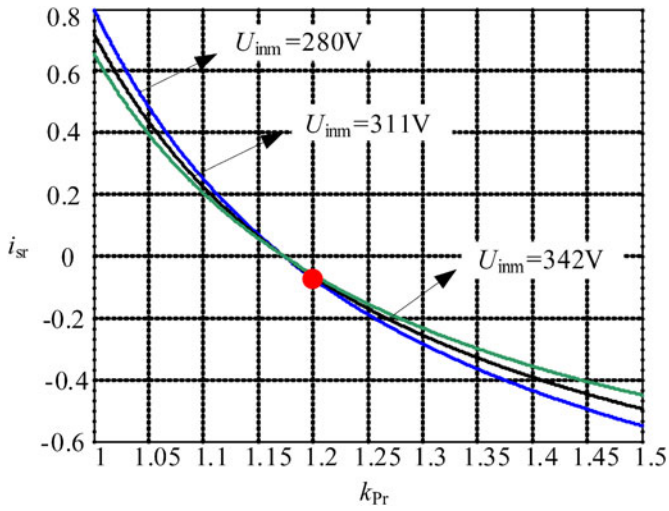

Fig. 16. Relationship between $I_{\mathrm{Sr-turn-off}}$ and k_{Pr}.

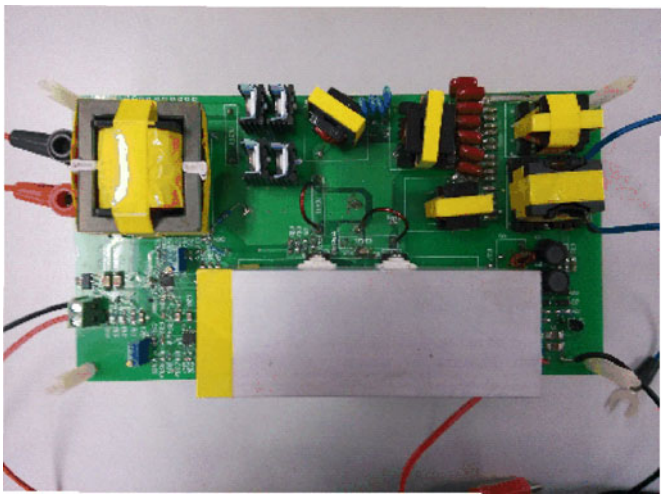

Fig. 17. Experimental prototype.

close to 1 to achieve low THD of the output sinusoidal voltage, therefore, $k_{\mathrm{Pr}} = 1.2$ is chosen as an example.

V. Experimental Results

A 130 W prototype shown in Fig. 17 has been built and tested to verify the theoretical analysis. The controller used in the prototype is LM5025 from Texas Instruments and its specifications are listed as follows:

1) input voltage: $u_{\mathrm{in}} = 220\ \mathrm{V_{ac}}/50\ \mathrm{Hz} \pm 10\%$;
2) output voltage: $u_{\mathrm{o}} = 45\ \mathrm{V_{ac}}/100\ \mathrm{kHz}$;
3) output power: $P_{\mathrm{o}} = 130\ \mathrm{W}$;
4) switching frequency: $f_{\mathrm{SW}} = 100\ \mathrm{kHz}$.

According to the performance analysis results above, $k_{\mathrm{Sr}} = 0.9, k_{\mathrm{Pr}} = 1.2, Q_{\mathrm{Sr}} = 2.5, Q_{\mathrm{Pr}} = 2.0, Q_2 = 2.0,$ and $D = 0.16$ are chosen when the RMS value of u_{in} is 220 V, and the parameters of the prototype are calculated as follows.

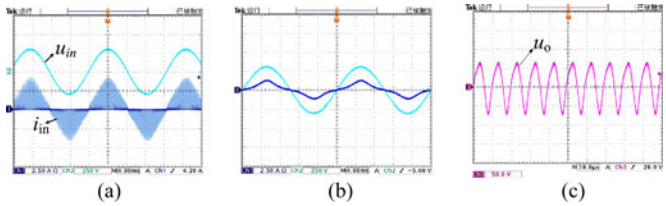

Fig. 18. Experimental waveforms at $u_{\mathrm{in}} = 220\ \mathrm{V_{ac}}$. (a) The input voltage u_{in} and input current i_{in} before filtered. (b) The input voltage and input current after filtered. (c) The output voltage u_{o} in detail.

Since $D = 0.16$, according to Fig. 12, $M_{\mathrm{ac-ac}} = 0.27$, and the turns-ratio of the transformer N can be calculated as

$$N = \frac{U_{\mathrm{pm}}}{U_{\mathrm{om}}} = \frac{M_{\mathrm{ac-ac}} U_{\mathrm{inm}}}{U_{\mathrm{om}}} = 1.32. \tag{46}$$

The equivalent load resistor seen at the primary side of the transformer R_{eq} is deduced as

$$R_{\mathrm{eq}} = N^2 R_L = 27.14\ \Omega. \tag{47}$$

As $Q_{\mathrm{Sr}} = 2.5, Q_{\mathrm{Pr}} = 2.0$, and $f_{\mathrm{SW}} = 100$ kHz, from (32), (33), and (47), the series resonant inductor L_{S} and parallel resonant inductor L_{P} is calculated as

$$L_{\mathrm{S}} = \frac{Q_{\mathrm{Sr}} R_{\mathrm{eq}}}{\omega_{\mathrm{Sw}}} = 108.99\ \mu\mathrm{H} \tag{48}$$

$$L_{\mathrm{P}} = \frac{R_{\mathrm{eq}}}{Q_{\mathrm{pr}} \omega_{\mathrm{Sw}}} = 21.61\ \mu\mathrm{H}. \tag{49}$$

Since $k_{Sr} = 0.9, k_{\mathrm{Pr}} = 1.2$, and $f_{\mathrm{SW}} = 100$ kHz, the series resonant angular frequency ω_{Sr} and parallel resonant angular frequency ω_{Pr} can be calculated out from (28) and (29). And then, the series resonant capacitor C_{S} and parallel resonant capacitor C_{P} can be calculated out from (30), (31), (48), and (49)

$$C_{\mathrm{S}} = \frac{1}{{\omega_{\mathrm{Sr}}}^2 L_{\mathrm{S}}} = 28.69\ \mathrm{nF} \tag{50}$$

$$C_{\mathrm{P}} = \frac{1}{{\omega_{\mathrm{Pr}}}^2 L_{\mathrm{P}}} = 0.08\ \mu\mathrm{F}. \tag{51}$$

Additionally, since $Q_2 = 2.0$ is chosen, the second harmonic trap inductor L_2 and capacitor C_2 can be calculated as

$$L_2 = \frac{Q_2 R_{\mathrm{eq}}}{\omega_{\mathrm{Sw}}} = 83.39\ \mu\mathrm{H} \tag{52}$$

$$C_2 = \frac{1}{4{\omega_{\mathrm{Sw}}}^2 L_2} = 7.59\ \mathrm{nF}. \tag{53}$$

A small *LC* filter is added at the input side to attenuate the high-frequency current ripple and make the fundamental component of the input current after filtered be in phase with the ac-line voltage. The input filter inductor L_{F} and capacitor C_{F} of the *LC* filter can be calculated out to be 63 nF and 8.73 mH, respectively, which will be introduced in another paper in future. Moreover, the dc-link capacitor C_{B} can be calculated to be 100 μF according to the second-harmonic ripple requirement of the dc-link voltage U_{B}.

Fig. 18 shows the experimental waveforms of input voltage u_{in}, input current i_{in} before and after filtered, and the output

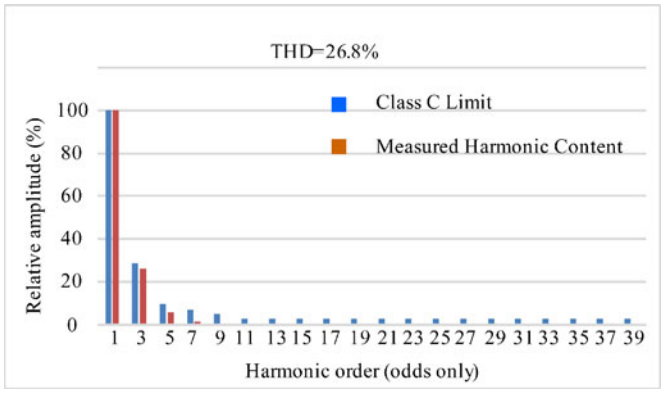

Fig. 19. Harmonic content of input current compared to IEC limits.

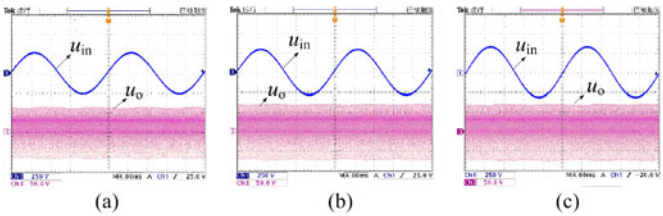

Fig. 20. Experimental waveforms of u_o at different input voltage. (a) $u_{in} = 198\ V_{ac}$. (b) $u_{in} = 220\ V_{ac}$. (c) $u_{in} = 242\ V_{ac}$.

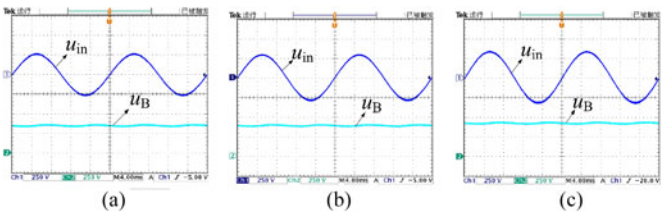

Fig. 21. Experimental waveforms of u_B at different input voltage. (a) $u_{in} = 198\ V_{ac}$. (b) $u_{in} = 220\ V_{ac}$. (c) $u_{in} = 242\ V_{ac}$.

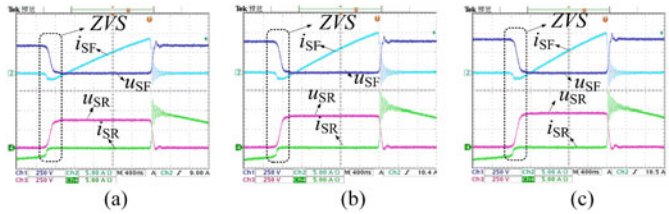

Fig. 22. Drain-source voltages of S_F and S_R and the currents through them at different input voltage. (a) $u_{in} = 198\ V_{ac}$. (b) $u_{in} = 220\ V_{ac}$. (c) $u_{in} = 242\ V_{ac}$.

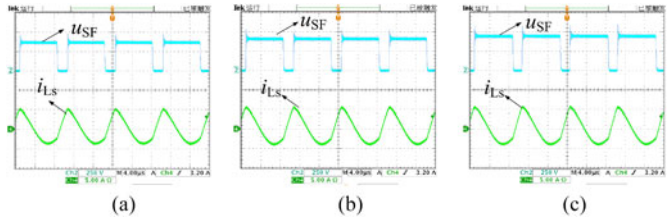

Fig. 23. Drain-source voltages of S_F and the current through L_s at different input voltage. (a) $u_{in} = 198\ V_{ac}$. (b) $u_{in} = 220\ V_{ac}$. (c) $u_{in} = 242\ V_{ac}$.

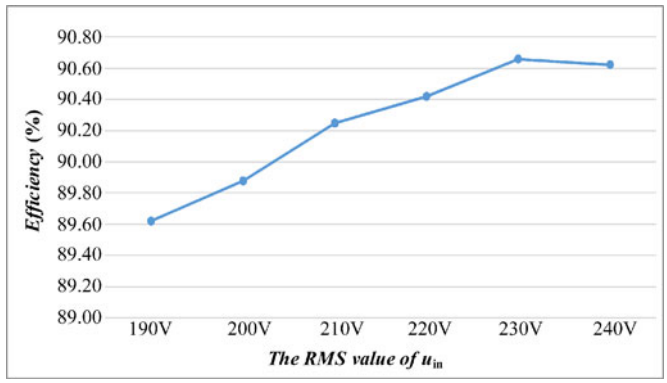

Fig. 24. Measured efficiency curve versus input voltage.

voltage u_o at $u_{in} = 220\ V_{ac}$. From Fig. 18(a), the current i_{LB} works in DCM at the peak value of u_{in}. Fig. 18(b) shows that the input current i_{in} after filtered is in phase with u_{in} and the measured input power factor are 0.95. From Fig. 18(c), the measured THD of the output voltage u_o is about 4.6%, which is smaller than 5% and the measured RMS value of u_o is about 45.7 V as expected.

In Fig. 19, the measured harmonic spectrum of the input current after filtered at $u_{in} = 220\ V_{ac}$ is compared to the limits imposed by IEC 61000-3-2 (all odd harmonics covered by IEC). It can be seen that the input current harmonics are below the IEC 61000-3-2 class C limits.

Fig. 20 shows the waveforms of the output voltage u_o at $u_{in} = 198\ V_{ac}$,$u_{in} = 220\ V_{ac}$ and $u_{in} = 242\ V_{ac}$, respectively. It is shown that the RMS value of u_o is 45.5, 45.7, and 45.9 V, respectively, thus the RMS value of the output voltage keeps almost constant throughout the whole range of u_{in}.

Fig. 21 shows the waveforms of the dc-link voltage u_B at $u_{in} = 198\ V_{ac}, u_{in} = 220\ V_{ac}$, and $u_{in} = 242\ V_{ac}$, respectively. The maximum values of u_B are 373, 410, and 441 V correspondingly, which are less than 450 V as expected.

Fig. 22(a), (b), and (c) show the drain-source voltages of S_R and S_F, and the currents through them at $u_{in} = 198, 220, 242\ V_{ac}$, respectively. The results indicate that the two power switches are turned ON under the ZVS condition at different input voltage, which are helpful to reduce the switching losses. Additionally, the drain-source voltage of S_F and current through L_S at $u_{in} = 198, 220, 242\ V_{ac}$, respectively, are shown in Fig. 23, and the ZVS turn ON of the switches is further verified.

The measured efficiency curve of the proposed single-stage high-frequency ac/ac converter versus input voltage is shown in Fig. 24. It is shown that the efficiency is around 90% in the whole range of input voltage and the maximum efficiency is about 90.6%. When the efficiency of the passive LCL-T resonant rectifier is included, the efficiency of the proposed LED driver shown in Fig. 3 is below 90%, which is lower than the carefully designed two-stage driver in [16]. The switching loss of it is

small because of its ZVS operation, thus its efficiency can be improved by reducing the conduction loss on the following two aspects: First, the bridgeless scheme can be adopted to reduce the conduction loss of the diode bridge rectifier; second, the resonant tank can be simplified and optimum designed to reduce the reactive power.

VI. Conclusion

A single-stage high-frequency resonant ac/ac converter has been proposed in this paper for a two-stage multichannel constant current ac/dc LED driver with high-frequency sinusoidal voltage bus. The performance of the converter was completely analyzed, including input power factor, voltage gain, THD of its output voltage, and the soft switching condition of the switches. A 130 W prototype was built and the experimental results have proven the correction of the theory analysis. The measured input power factor, the THD of the output voltage, and the efficiency at $u_{\rm in} = 220\ {\rm V_{ac}}$ are 0.95%, 4.6%, and 90.4%, respectively.

References

[1] A. Laubsch, M. Sabathil, J. Baur, M. Peter, and B. Hahn, "High-power and high-efficiency InGaN-based light emitters," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 79–87, Jan. 2010.

[2] H.-L. Cheng and C.-W. Lin, "Design and implementation of a high-power-factor LED driver with zero-voltage switching-on characteristics," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4949–4958, Sep. 2014.

[3] C. S. Wong, K. H. Loo, Y. M. Lai, Martin H. L. Chow, and C. K. Tse, "An alternative approach to LED driver design based on high-voltage driving," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2465–2475, Mar. 2016.

[4] R. A. Pinto, M. R. Cosetin, and A. Campos, M. A. Dalla Costa, and R. N. do Prado, "Compact emergency lamp using power LEDs," *IEEE Trans. Ind. Electron.*, vol. 59, no. 4, pp. 1728–1738, Apr. 2012.

[5] S. Y. R. Hui and Y. X.Qin, "A general photo-electro-thermal theory for light emitting diodes (LED) systems," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 1967–1976, Aug. 2009.

[6] Y. X. Qin and S. Y. R. Hui, "Comparative study on the structural designs of LED devices and systems based on the general photo-electro-thermal theory," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 507–513, Feb. 2010.

[7] S. Choi and T. Kim, "Symmetric current-balancing circuit for LED backlight with dimming," *IEEE Trans. Ind. Electron.*, vol. 59, no. 4, pp. 1698–1707, Apr. 2012.

[8] M. Arias, D. G. Lamar, J. Sebastián, D. Balocco, and A. A. Diallo, "High-efficiency LED driver without electrolytic capacitor for street lighting," *IEEE Trans. Ind. Appl.*, vol. 49, no. 1, pp. 127–137, Jan./Feb. 2013.

[9] C.-A. Cheng, H.-L. Cheng, and T.-Y. Chung, "A novel single-stage high-power-factor LED street-lighting driver with coupled inductors," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3037–3045, Sep./Oct. 2014.

[10] K. I. Hwu and Y. T. Yau, "Applying one-comparator counter-based sampling to current sharing control of multichannel LED strings," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2413–2421, Nov. 2011.

[11] *Electromagnetic compatibility, Part 3, Section 2. Limits for Harmonic Current Emissions (Equipment Input Current ≤ 16a Per Phase)*, IEC 61000-3-2, 2005.

[12] R. Zhang and H. S.-H. Chung, "Use of daisy-chained transformers for current-balancing multiple LED strings," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1418–1433, Mar. 2014.

[13] X. Wu, C. Hu, J. Zhang, and Z. Qian, "Analysis and design considerations of LLCC resonant multioutput DC/DC LED driver with charge balancing and exchanging of secondary series resonant capacitors," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 780–789, Feb. 2015.

[14] S. Li, S.-C. Tan, C. K. Lee, E. Waffenschmidt, S. Y. Hui, and C. K. Tse, "A survey, classification, and critical review of light-emitting diode drivers," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1503–1516, Feb. 2016.

[15] Texas Instruments User's Guide, "UCC28810EVM-003 110-W multiple string LED driver with universal line input and PFC," Nov. 2009.

[16] M. Arias, D. G. Lamar, F. F. Linera, D. Balocco, A. A. Diallo, and J. Sebasti, "Design of a soft-switching asymmetrical half-bridge converter as second stage of an LED driver for street lighting application," *IEEE Trans. Power Electron*., vol. 27, no. 3, pp. 1608–1621, Mar. 2012.

[17] W. Feng, F. C. Lee, and P. Mattavelli, "Optimal trajectory control of LLC resonant converters for LED PWM dimming," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 979–987, Feb. 2014.

[18] J. Zhang, L. Xu, X.Wu, and Z. Qian, "A precise passive current balancing method for multi-output LED drivers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2149–2159, Aug. 2011.

[19] J. Zhang, J. Wang, and X. Wu, "A capacitor-isolated LED driver with inherent current balance capability," *IEEE Trans. Ind. Electron.*, vol. 59, no. 4, pp. 1708–1716, Apr. 2012.

[20] C. Zhao, X. Xie, and S. Liu, "Multioutput LED drivers with precise passive current balancing," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1438–1448, Mar. 2013.

[21] Q. Luo, S. Zhi, C. Zou, W. Lu, and L. Zhou, "A LED driver with dynamic high-frequency sinusoidal bus voltage regulation for multistring applications," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1438–1448, Mar. 2013.

[22] W. Guo, P. K. Jain, "A power-factor-corrected AC–AC inverter topology using a unified controller for high-frequency power distribution architecture," *IEEE Trans. Ind. Electron.*, vol. 4, no. 51, pp. 874–883, Mar. 2004.

[23] M. Qiu, P. K. Jain, H. Zhang, "An APWM resonant inverter topology for high frequency AC power distribution systems," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 121–129, Jan. 2004.

[24] J. Garcia, A. J. Calleja, E. L´opez Corominas, D. G. Vaquero, and L. Campa, "Interleaved buck converter for fast PWM dimming of high-brightness LEDs," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2627–2636, Sep. 2011.

[25] D. Gacio, J. M. Alonso, J. Garcia, L. Campa, M. J. Crespo, and M. Rico-Secades, "PWM series dimming for slow-dynamics HPF LED drivers: The high-frequency approach," *IEEE Trans. Ind. Electron*, vol. 59, no. 4, pp. 1717–1727, Apr. 2012.

[26] C.-S. Moo, Y.-J. Chen, and W.-C. Yang, "An efficient driver for dimmable LED lighting," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4613–4618, Nov. 2012.

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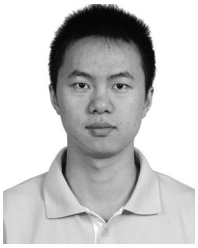

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