```
1   -- Kevin Miller
2   -- CMPT-281
3   -- HW7 - One Bit ALU
4   -- 2013-04-18
5
6   -- Op Codes:
7   -- a PLUS b  - 000
8   -- a AND b   - 001
9   -- a OR b    - 010
10  -- NOT B     - 011
11  -- a MINUS b - 100
12
13  Entity OneBitALU IS
14      PORT(
15          -- inputs and outputs
16          a, b            : IN BIT;   -- data inputs
17          output          : OUT BIT;  -- data output
18          ct0, ct1, ct2   : IN BIT;   -- control signals; ct2 is Add'/Subtract signal only
19          cout            : OUT BIT   -- carry out
20
21      );
22
23      --aliases
24      ALIAS cin IS ct2;   -- cin input to adder is same signal as ct2
25
26  END OneBitALU;
27
28  ARCHITECTURE Behaivior OF OneBitALU IS
29      -- internal signals
30
31      -- control
32      SIGNAL ct0N     : BIT;  -- NOT ct0
33      SIGNAL ct1N     : BIT;  -- NOT ct1
34      SIGNAL ct2N     : BIT;  -- NOT ct2
35
36      -- adder signals
37      SIGNAL aPb      : BIT;  -- a PLUS b
38      SIGNAL g0, p0   : BIT;  -- adder look-ahead sub-values
39      SIGNAL bXOcin   : BIT;  -- b XOR ct2(cin)
40
41      -- other operations
42      SIGNAL bN       : BIT;  -- NOT b
43      SIGNAL aAb      : BIT;  -- a AND b
44      SIGNAL aOb      : BIT;  -- a OR b
45
46      -- output selectors
47      SIGNAL addSel   : BIT;  -- output from adder/subtractor
48      SIGNAL andSel   : BIT;  -- output from AND function
49      SIGNAL orSel    : BIT;  -- output from OR function
50      SIGNAL bNSel    : BIT;  -- output from b NOT function
51
52
53  BEGIN
```

```
54      -- control signals
55      ct0N <= NOT ct0;
56      ct1N <= NOT ct1;
57      ct2N <= NOT ct2;
58
59      -- adder/subtractor signals
60      bXOcin <= b XOR cin;
61      g0     <= (a AND bXOcin);
62      p0     <= (a XOR bXOcin);
63      aPb    <= (cin XOR p0);
64      cout   <= ((cin AND p0) OR g0);
65
66      -- other opcode signals
67      bN  <= NOT b;
68      aAb <= a AND b;
69      aOb <= a OR b;
70
71      -- function select signals
72      addSel <= (aPb AND          ct1N AND ct0N); -- results of add/subtract
73      andSel <= (aAb AND ct2N AND ct1N AND ct0);  -- a AND b
74      orSel  <= (aOb AND ct2N AND ct1  AND ct0N); -- a OR b
75      bNSel  <= (bN  AND ct2N AND ct1  AND ct0);  -- NOT b
76
77      output <=
78          addSel OR -- results of add/subtract
79          andSel OR -- a AND b
80          orSel  OR -- a OR b
81          bNSel;    -- NOT b
82
83  END Behaivior;
84
85
```