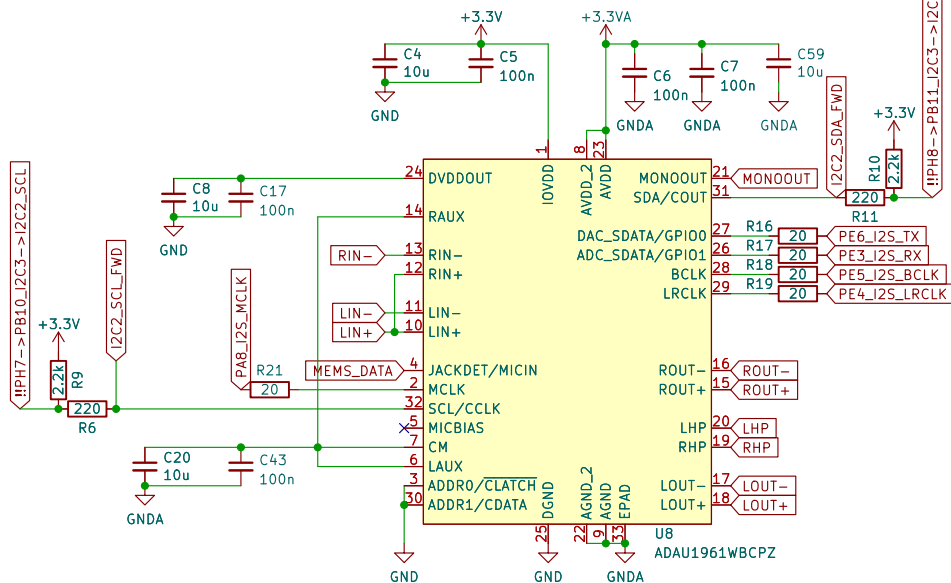
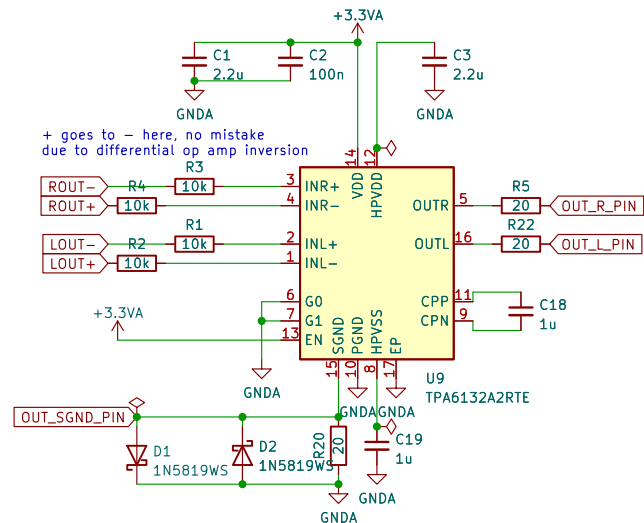


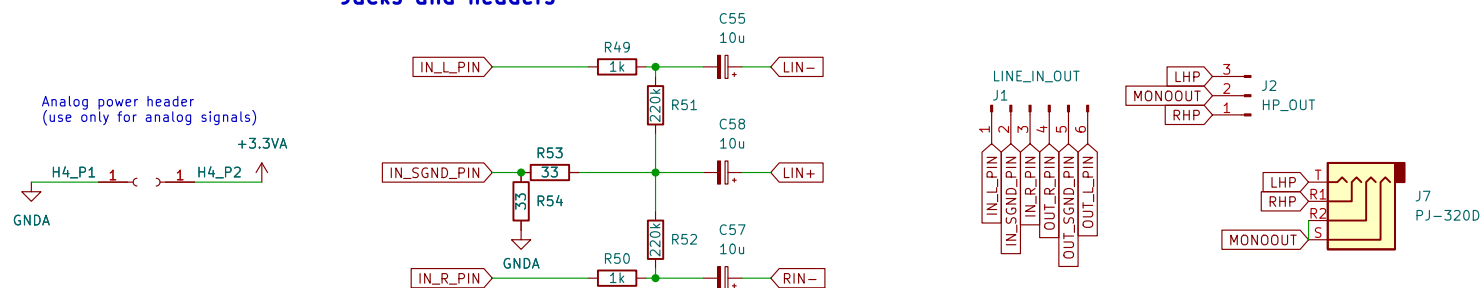
## Codec



## Output Opamp



## Jacks and headers



Sheet: /codec\_adau1961/  
File: codec\_adau1961.kicad\_sch

**Title: Ksoloti Core**

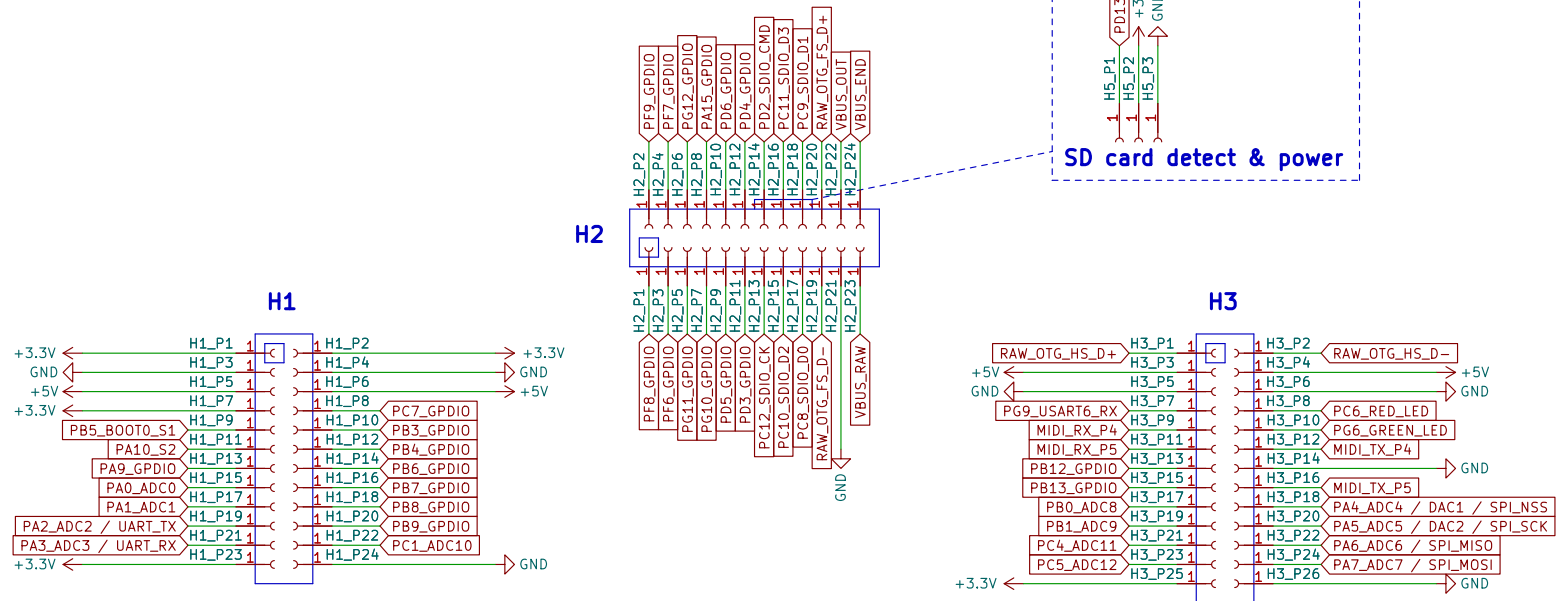
Size: A4 Date: 2024-10-07

KiCad E.D.A. kicad (6.0.11)

**Rev: v0.6**

Id: 2/8

# GPIO and function headers (PCB component side view)



SD card detect & power

RESERVED for SPILINK implementation  
Leave as is for regular use.



Digital microphone header



Sheet: /headers/  
File: headers.kicad\_sch

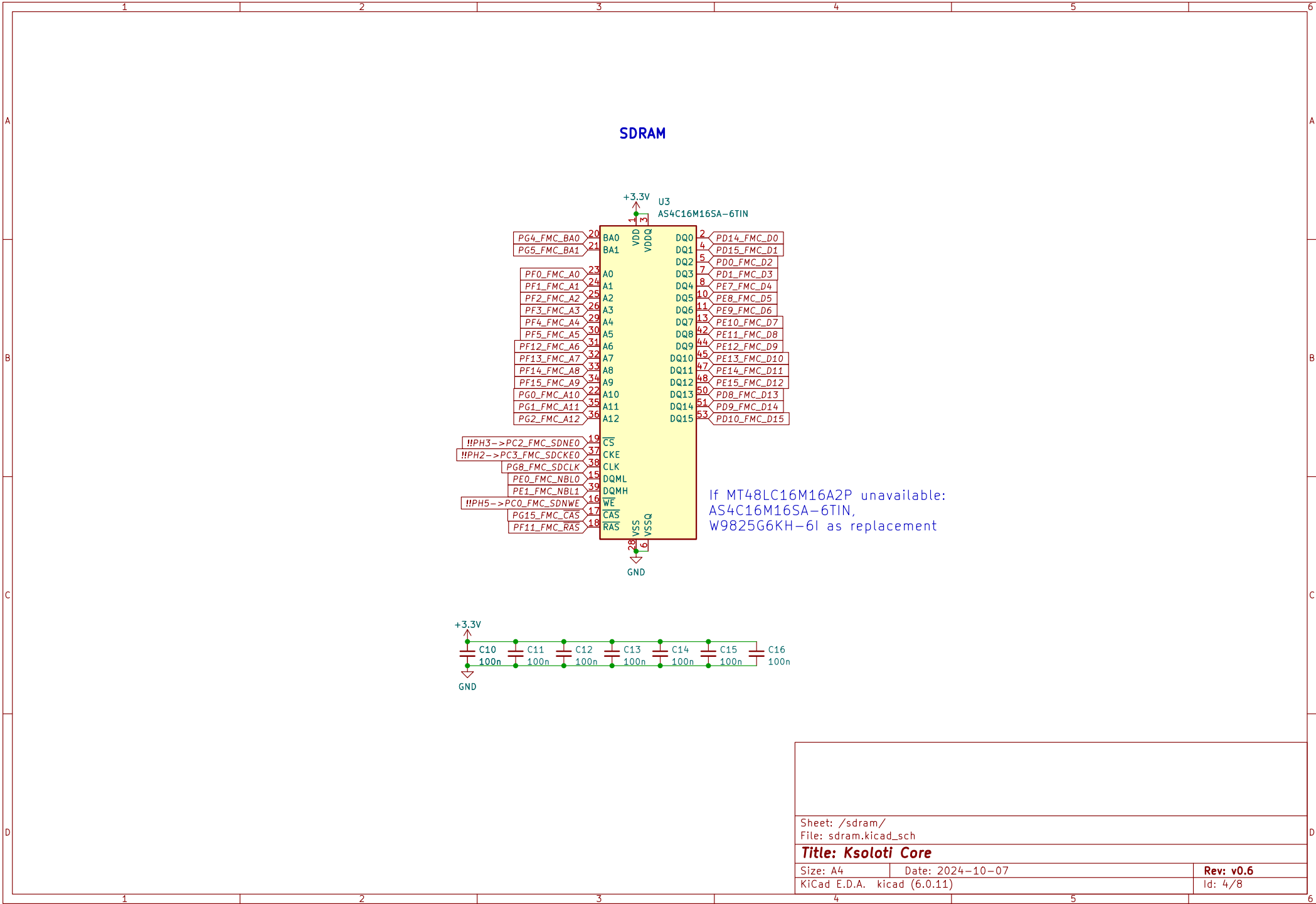
**Title: Ksoloti Core**

Size: A4 Date: 2024-10-07

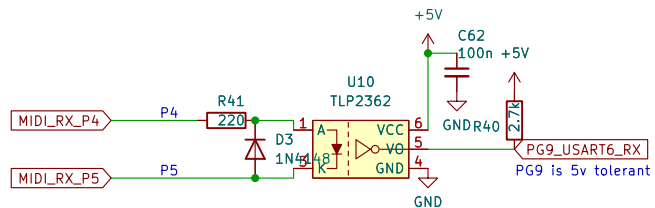
KiCad E.D.A. kicad (6.0.11)

**Rev: v0.6**

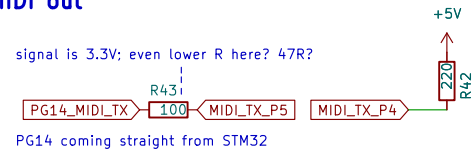
Id: 3/8



### MIDI in (OPTIONAL footprints on the bottom side of the PCB – not placed by default)



### MIDI out



GND = Shield  
M04 = Source  
M05 = Sink

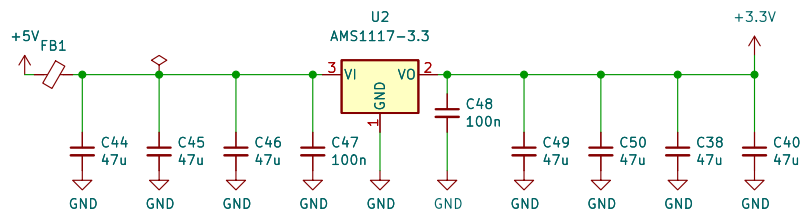
You can connect a DIN MIDI jack directly:

GND → DIN pin 2  
M04 → DIN pin 4  
M05 → DIN pin 5

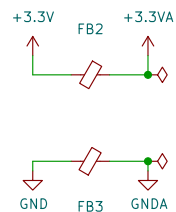
Or for TRS MIDI jacks:

GND → TRS sleeve  
M04 → TRS ring  
M05 → TRS tip

### 3.3V digital power supply

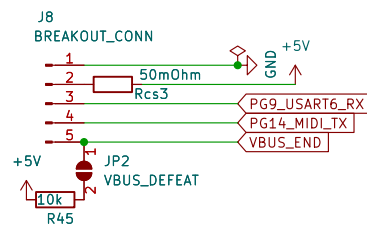


### Analog power (audio path only)



### To optional power/MIDI board

WARNING: J8 pinout inconsistent with Axoloti Core



Sheet: /power\_midi/  
File: power.kicad\_sch

**Title: Ksoloti Core**

Size: A4 Date: 2024-10-07

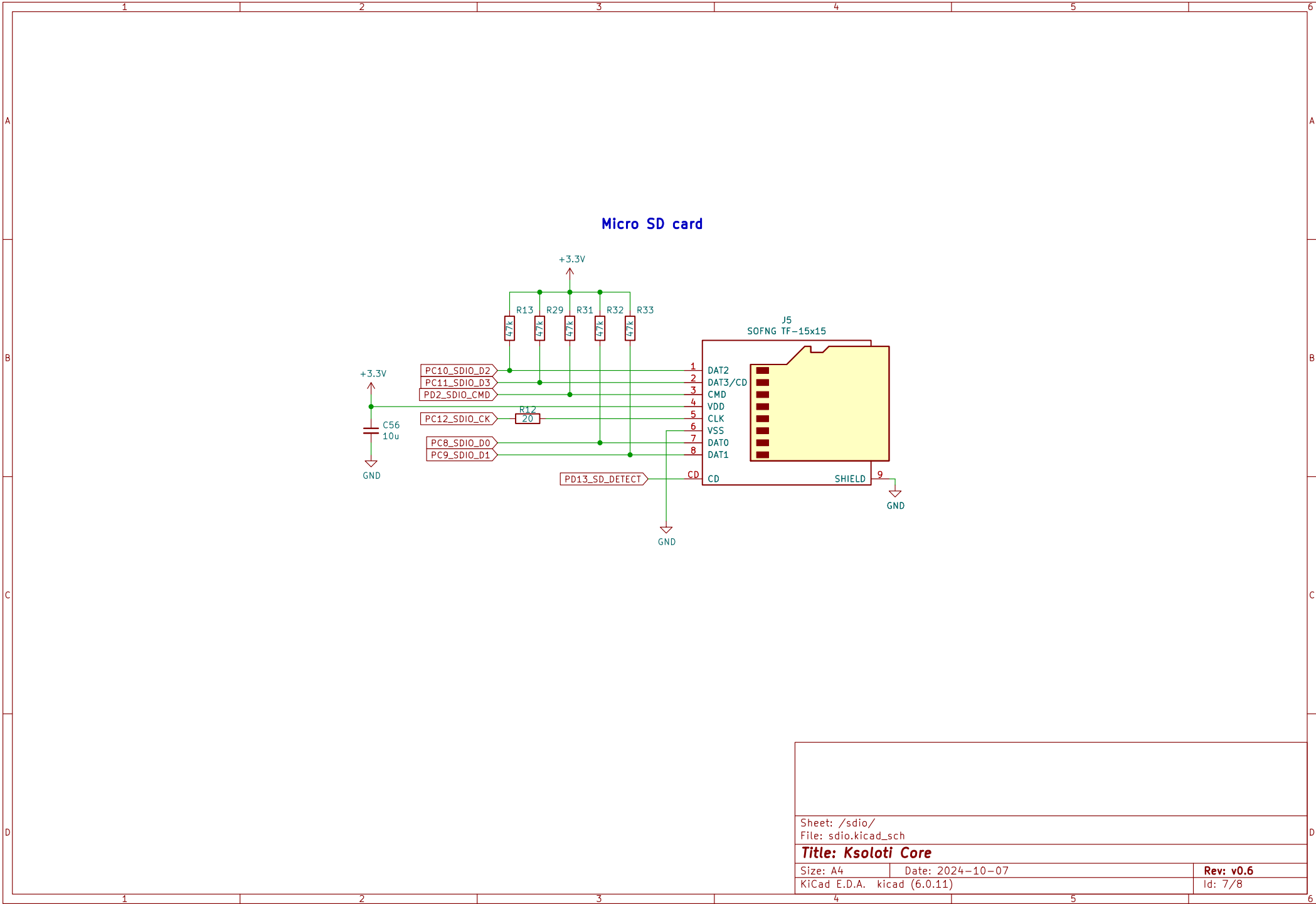
KiCad E.D.A. kicad (6.0.11)

**Rev: v0.6**

Id: 5/8

The schematic diagram illustrates the USB HOST interface circuit. It begins with a +5V power source connected to the IN pin of the AP2161 (U5) voltage regulator. The EN pin of U5 is controlled by PD7\_2141\_EN, and its output (OUT) provides VBUS\_OUT. The FLG pin of U5 is connected to PG13\_2141\_FLG. A 50mΩ resistor (Rcs2) and a 47μF capacitor (C52) are used for output filtering. The VBUS signal is then connected to the VBUS pin of the GT-USB-7010AW (J4). The CC1 and CC2 pins of J4 are pulled up to VBUS via 5.1k resistors (R35, R36). The D- and D+ pins of J4 are connected to the corresponding pins of the USBLC6-2SC6 (U6) level shifter. The SBU1 and SBU2 pins of J4 are left unconnected, as indicated by the 'X' marks. The USBLC6-2SC6 (U6) is configured with its input pins (1, 2, 3, 4) connected to ground and its output pins (5, 6) connected to the PB14\_OTG\_HS\_D- and PB15\_OTG\_HS\_D+ signals. These signals are also connected to the RAW\_OTG\_HS\_D- and RAW\_OTG\_HS\_D+ pins through 20Ω resistors (R34, R37). The shield pin of J4 is connected to ground via a series combination of two 100nF capacitors (C61, C51).

Id: 6/8



**A**

B

- C

## D

Sheet: /changelog/		D
File: changelog.kicad_sch		
<b>Title: Ksoloti Core</b>		
Size: A4	Date: 2024-10-07	
KiCad E.D.A. kicad (6.0.11)		Rev: v0.6
		Id: 8/8