

## SIC ARCHITECTURE

### ① memory

- Byte addressable
- There are  $2^{15}$  bytes in mem.  
3 consec. bytes = 1 word (24 bits)

### ② Registers

5. Each has a reg. number.

A - Accumulator - 0 - mathem. operations

X - Index - 1 - addressing

L - Linkage - 2 - stores the return addr.  
in case of subroutines

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PC - Program Counter - 8 - addr. of the next instr.

SW - Status word - 9 - contains a variety of info

mode	state	id	cc	mask	x	lcode
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### ③ Data Format

- Integers - 24 bit
- -ve no's - 2's complement
- char. - ASCII value (8 bit)
- No floating pt representation.

### ④ Instruction Format

opcode	x	Address
8	1	15

x = 0, direct addr. mode

x = 1, indexed " "

### ⑤ Instr. Set

- Load & Store - LDA, STA, LDCH, STCH
- Comparison - comp. <sup>(mem)</sup> w/ accum. COMP data
- Arithmetic - ADD, SUB, DIV
- Jump cond. - JLT, JEQ
- Subroutine linkage - JSUB.

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## ⑥ Input & Output

Perf. by transferring 1 byte at a time from or to 8 rightmost bits of accumulator.

3 I/O Instr:

- Test Device (TD) - - ready or not. cc in status word is used for this.  
if cc is < then device is ready.
- Read Data (RD) - Reads a byte from device & stores it in acc.
- Write Data (WD) - writes a byte from acc. to the device.

## SIC / XE ARCHITECTURE

### ① memory

- mem. size is  $2^{20}$  bytes
- 3 consec. bytes  $\rightarrow$  1 word

### ② Registers

9  $\rightarrow$  5 (SIC) + 4 add<sup>n</sup> :

B - Base reg.

S } General

T }

F - Floating pt. acc.

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### ③ Data Format

- Integer - <sup>by</sup> Binary no's.
- Char. - " " ASCII codes
- Floating pt. - 48 bits

### ④ Instruction Format

#### • Format 1

8 opcode

#### • Format 2

8 opcode 4 reg1 4 reg2

#### • Format 3

6 opcode 1 n 1 x 1 b 1 p 1 e 12 displ.

#### • Format 4

6 opcode 1 n 1 x 1 b 1 p 1 e 20 addr

n - indirect

x - index

p - progr. counter

i - immediate

b - base

e - exponential

### ⑤ Addressing Modes

Base Relative  $b=1, p=0$   $TA = (B) + displ.$

Program .c. rel  $b=0, p=1$   $TA = (PC) + displ.$

### ⑥ Instr. Format Set

(same as SLIC)

but extra for Floating pt with op's:

ADDF, SUBF, MULF, DIVF

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⑤ i/p & o/p

- <sup>ixc</sup> includes i/o channels that allow to perform i/o operations while CPU is executing other tasks.
- Allows overlapping of computing & I/O.

SIO	- start op.	} I/O channels
TIO	- Test op.	
HIO	- Halt op.	