CIE TEST - (2)

MICROPROCESSORS

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CODE - IS4S

1MS17IS051

1. Ans

(a) Prerequisits for using string instructions:-

• => DS & ES are to be defined: Initializing and using these segment makes DS as the source and ES as the destination segment.

=> SI and DI act as pointers: SI to point to DS & DI top point to ES, means SI should contain the address of the first location in the DS & DI should contain the address of the first location in ES

=> DF should be set/reset: Control flag called as direction flag, used exclusively for string operations. Purpose in string operation is, if flag is set, the pointers get automatically decremented, and if reset, the reverse occurs. So, during string instructions are used, DF should be set/reset depending on the direction.

=> CX should act as a counter: CX should be loaded with the count of number of operations required.

To compare 2 string the CMPS instruction is used. The instruction is for the comparasion, byte by byte or word by word as the case may be.
The conditional flags are modified according to the result of the Comparasion.

String comparasion has to be accompanied by the use of the conditional REP prefix.

Since string comparasion checks only for equality, the zero flag is made use of automatically.

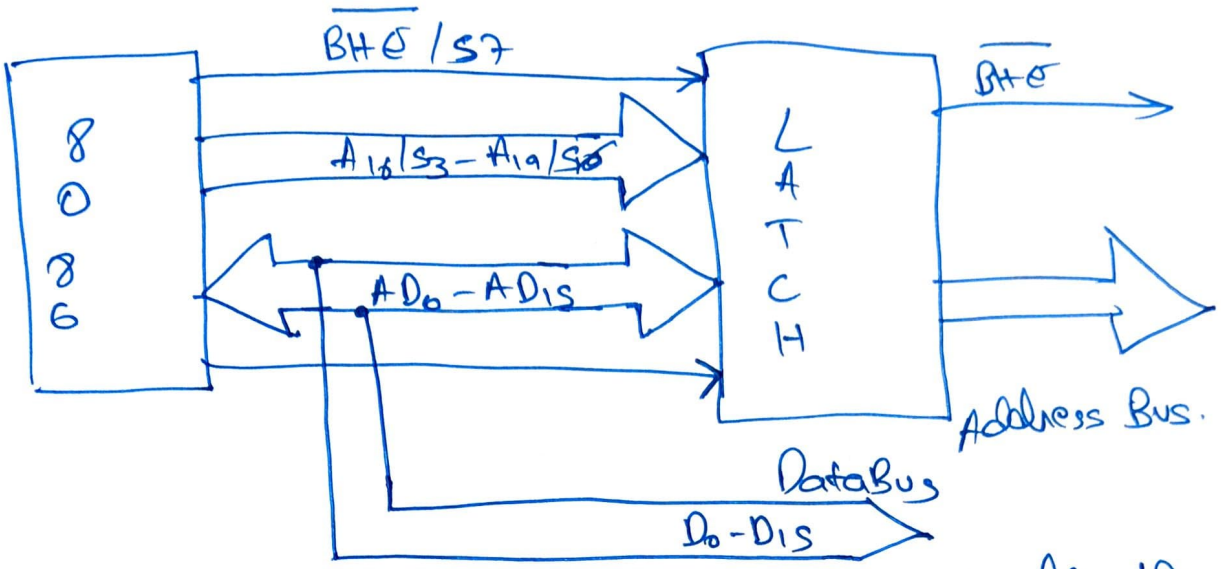
1. Ans (b).

The action of seperating address and data is called de-multiplexing

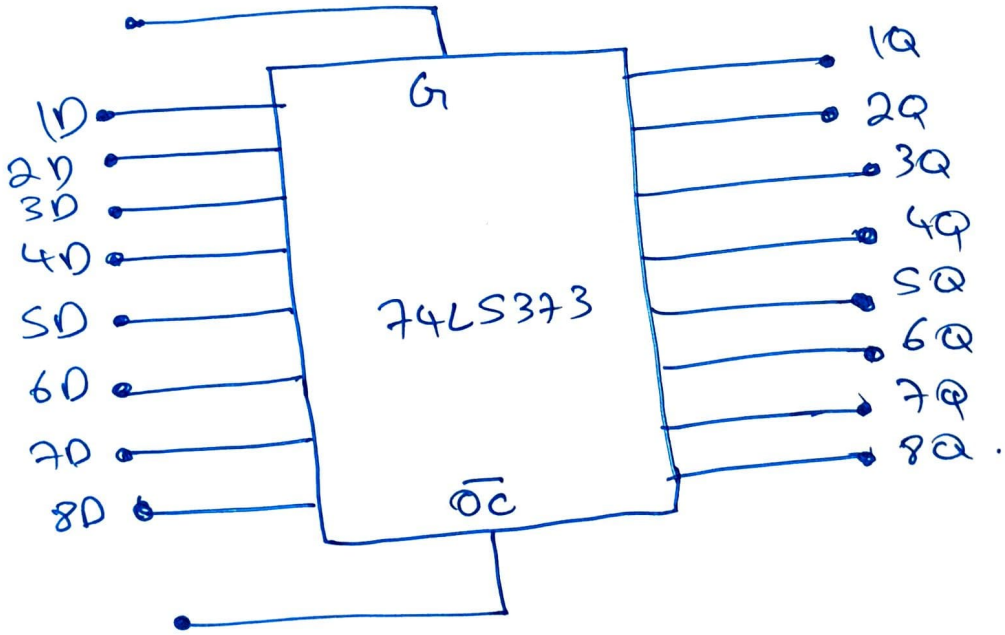
first step memory is placing the address on the address bus.

Need to appear on the data bus, means the bus must be made free to carry data. and for demultiplexing during the time that the address is in the address/data bus, it is to be latched on to a 'Latch IC' whose clock is ALE signal supplied to 8086.

Signal ALE goes high & functions as a clock for a latch that is available throughout the bus cycle. Once the address is latched on to the latches, it can be removed from the AD lines, then lines then are free to carry data



The data sheet of this IC specifies that, all the 8 latches of this 74LS373 is D-type latch.



Here the AE is connected to the G pin of the IC The $\overline{OC}$ (output control) is grounded for normal operation.

1. Ans

(c) for 2ms

```
MAIN: MOV   R6, #2D
LOOP: ACALL DELAY
      DJN2  R6,LOOP
      SJMP  MAIN

DELAY: MOV  TMOD, # 00000001B
       MOV  TH0, # 0FCH
       MOV  TL0, #018H
       SETB TR0
HERE: JNB   TF0, HERE
      CLR   TR0
      CLR   TF0
      RET:
```

for 1ms.

```
      MOV CX, N
HERE: NOP
      LOOP HERE.
```

2. Ans

(a) Intersegment for far call

Direct far call is a far call which means that the destination address is in a different code segement.

This will be a 5 byte instruction, the first byte being the opcode, the second and third bytes being the new value of IP, and the fourth & 5th the new values of CS.

This is not a relative call

when the procedure is called, the IP and CS values are replaced by the corresponding values in the call instruction

The RET instruction.

The execution of RET causes the returns addresses to be popped from the stack to IP or IP & CS.

When ever a procedure is defined, it is known wether it is a far or near procedure. From this, it is determined wether the stack has saved just the old IP value or both IP and CS.

(2 Ans)

(b)

```
.MODEL SMALL
.DATA
TMPS DB 20 DUP(0)
MAX DB 80
.CODE
.STARTUP
```

```
        MOV  CX,20
         MOV BX, 0
        MOV DX, ABOOH
         IN AL, DX
TAKE_IN: MOV TMPS[BX], AL      ;Transfer data into memory,
                               increament port address
         INC DX
          INC BX
          LOOP TAKE-IN         ;repeat until CX=0.
         MOV AH, MAX
         MOV DX, CDOSH
        MOV AL, 01
         MOV CX,20
         MOV BX,0
AGAIN :  CMP, TMPS[BX], Alt    ; compare data in memory with MAX.
         JA ALARM
OTHER :  INC DX
         INC BX
         LOOP AGAIN
         JMP EXEET             ;jump to exit point.
ALARM :  OUT DX, AL            ; output alarm data to o/p port
         JMP OTHER
EXEET :
          . EXIT
          END.
```