The Hardware structure of 8086

i) List out the differences b/w 8086 & 8088. (4M)

→ Differences b/w 8086 & 8088 are:

i) 8088 has an external data bus of 8 bits, while 8086 has a 16 bit data bus.

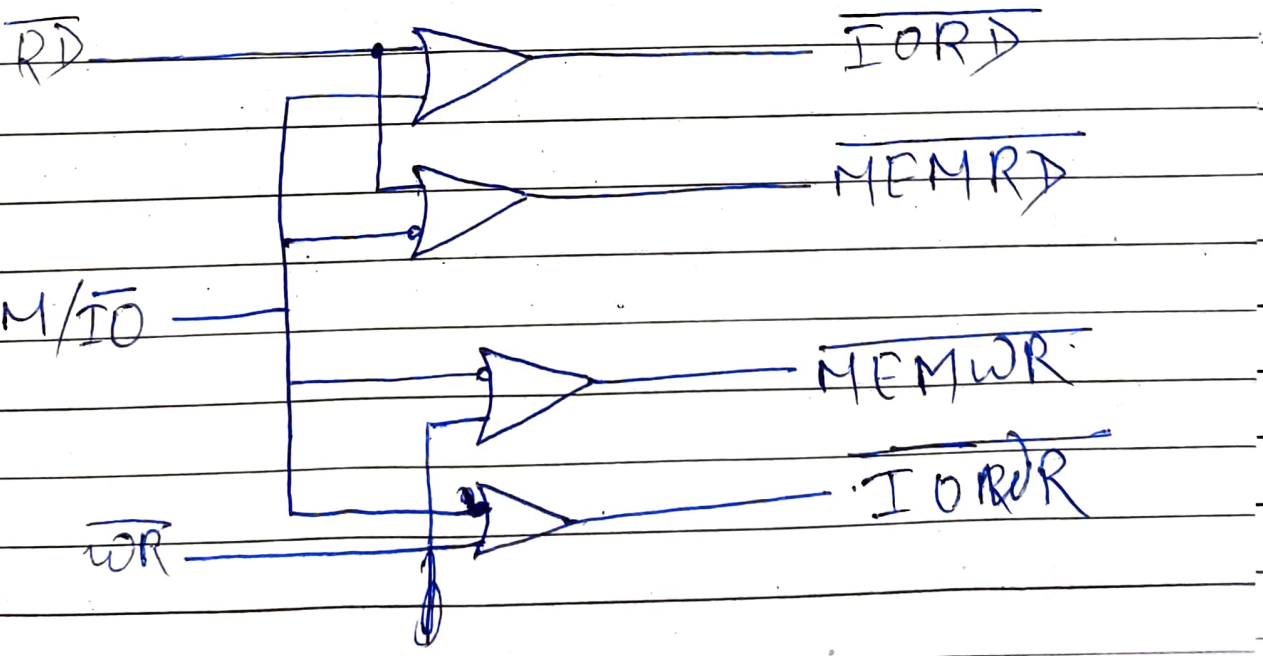
ii) The instruction queue of 8088 is 4 bytes, while 8086 has a 6 Byte queue.

iii) For 8088, pin NO. 28 (in min. mode) is an $\overline{M}/IO$ pin, while for 8086, the polarity of the pin is $M/\overline{IO}$.

iv) Pin No 34 is $\overline{SSO}$ for 8088, while it is $\overline{BHE}/S7$ for 8086.

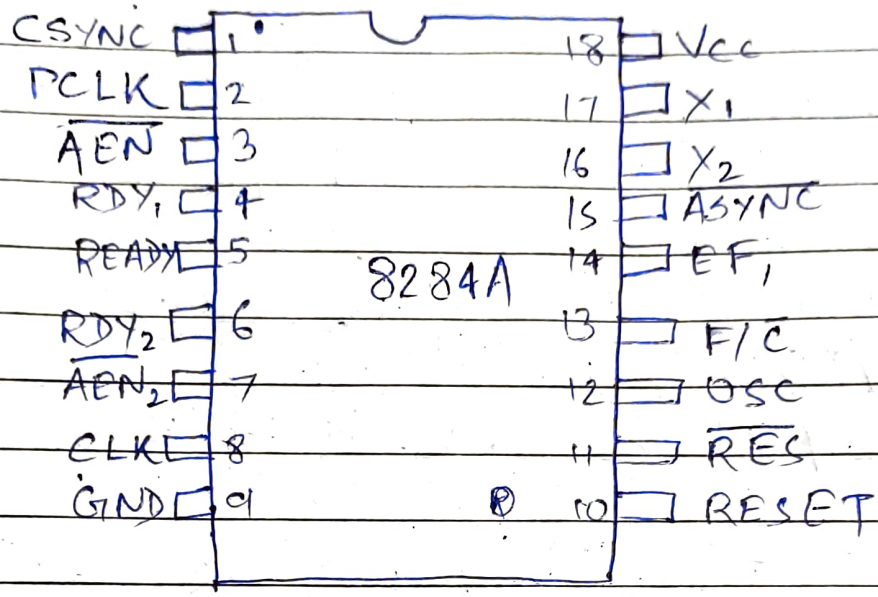
ii) Draw a memory write machine cycle showing the state of all important signals.

→



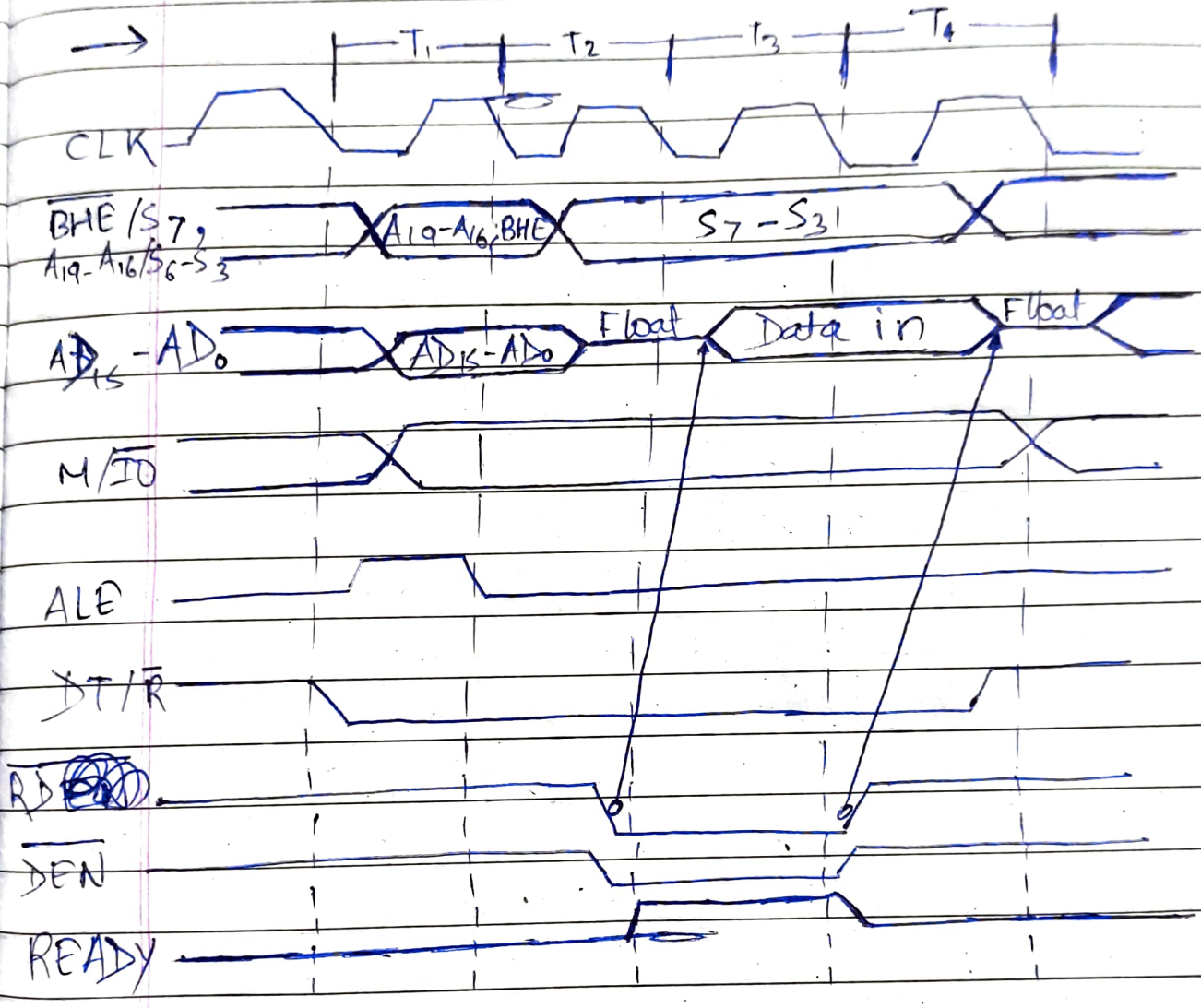
(III.) With a pin configuration, explain the different pins of clock generator IC 8284A.

→



Pin configuration of the clock gen. 8284A

Q) Draw the timing diagram of the 8086 MP Read machine cycle and explain the operation of the Address/data, M/IO, ALE, DT/R, RD, DEN and ready lines.



Read machine cycle timing diagram

i) Address/Data:

In T_1, the address of the location to be accessed is placed on the lines AD_0 to AD_{15} & $A_{16}/S_3 - A_{19}/S_6$.

i) In T_1, the ADS

ii) ALE:

In T_1, the ALE signal goes high for one clock cycle, and on it's trailing edge, the address information is latched and available at the output of the latches.

iii) M/$\overline{IO}$:

If it is 'memory read', the M/$\overline{IO}$ signal is high from T_1 to T_4. If it is 'I/O read', this signal is low.

iv) DT/$\overline{R}$:

DT/$\overline{R}$ is low from T_1 to T_4 indicating that data is to 'received' by the processor (since it is read cycle)

v) In T_2, the $\overline{RD}$ signal is made low.

vi) The line shown to the data bus is indicative of a 'cause-effect' relationship.

vi) $\overline{DEN}$:

In T_2, $\overline{DEN}$ goes low to enable the data bus buffer point.

vii) At the end of T_2, READY signal is sampled & if it is high, the bus cycle proceeds normally.

Q.) What is the duration of the bus cycle in a 8086 based microcomputer, if the clock frequency is 12 MHz & the three wait states are inserted?

→ The period of a 12 MHz mp, $T = 1/f = 83$ ns

The duration of the bus cycle without any wait-states is given by

$= T_{bus\text{-}cycle} = 4 \times T = 4 \times 83 = 332$ ns

Duration of the wait states is $= T_w = 3 \times T$
$= 249$ ns

So, extended bus cyle, $T_{bus\text{-}cycle} + T_w = 581$ ns

Q.) Write a program for delay of 5 msec

→

	Instruction	No. of cycles
	MOV CX, N	4
HERE:	NOP	3
	LOOP HERE	17/5

As most delay occurs in loop, the total cycles of delay is $[(3+17) \times N] - 12^{\circ}$

Total delay time $= 5$ msec $= 20N \times 0.033$ us

$N = \dfrac{5 \text{ msec}}{20 \times 0.033 \text{ usec}} = 3010$