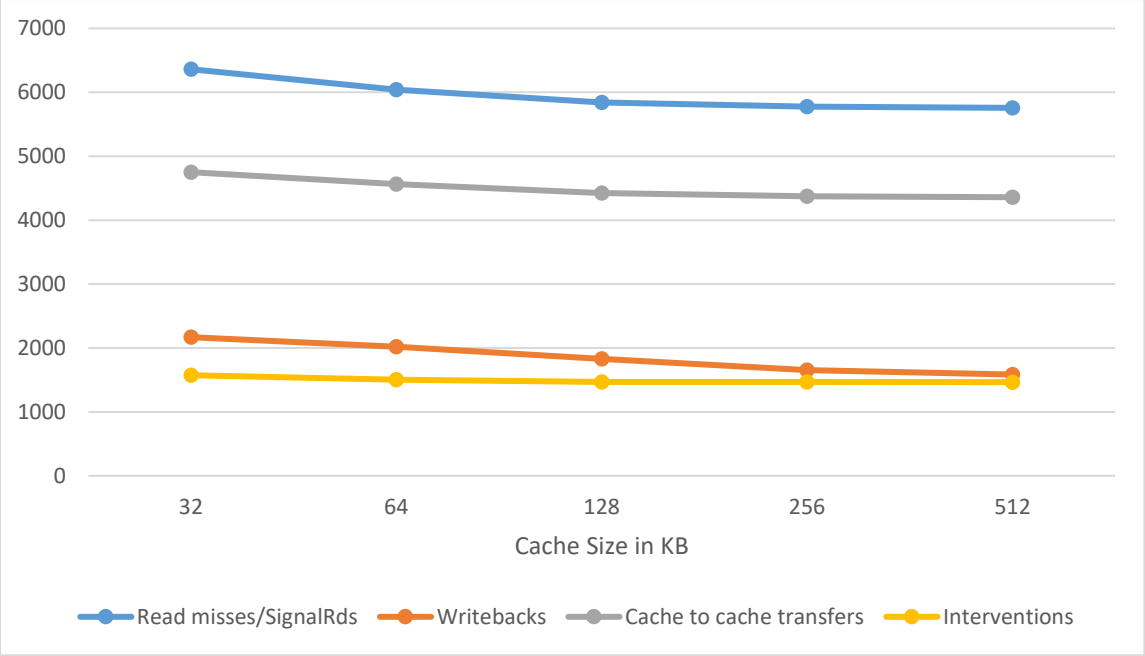
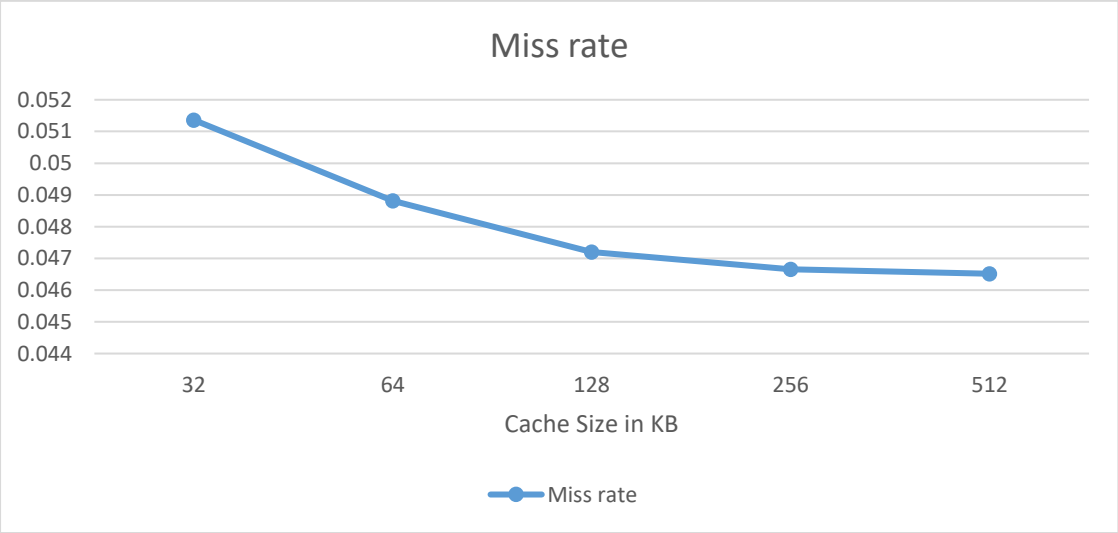
Report for Program 3

For increasing Cache Size (FBV and SSCI) (For canneal.04t.longTrace)

MESI Protocol	32 KB	64 KB	128 KB	256 KB	512 KB	Trend
number of reads	112661	112661	112661	112661	112661	Constant
number of read misses	6361	6044	5842	5775	5757	Decrease
number of writes	11942	11942	11942	11942	11942	Constant
number of write misses	39	39	39	39	39	Constant
total miss rate	0.051363	0.048819	0.047198	0.046660	0.046516	Decrease
number of writebacks	2169	2021	1831	1654	1585	Decrease
number of cache-to-cache transfers	4751	4564	4424	4372	4359	Decrease
number of SignalRds	6361	6044	5842	5775	5757	Decrease
number of SignalRdXs	39	39	39	39	39	Constant
number of SignalUpgrs	674	674	674	674	674	Constant
number of invalidations	2014	2014	2014	2014	2014	Constant
number of interventions	1574	1505	1471	1468	1466	Decrease



Based on the above table and graph, it can be concluded that, as we increase the size of the cache, the number of read misses, SignalRds, Writebacks, Cache to Cache transfers and Interventions undergone by the system, reduces.

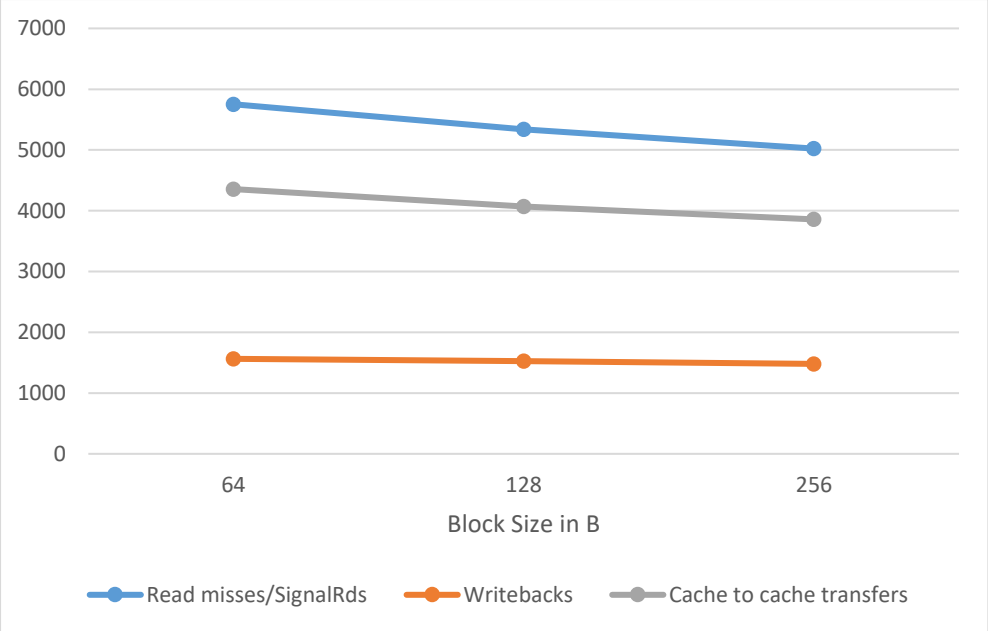


The miss rate associated tends to decrease as we increase the cache size. This is because, an increase in the cache size causes an increase in the capacity of the cache, thereby, allowing more memory blocks to be accommodated in the cache. This leads to decrease in the number of misses, and therefore the miss rate.

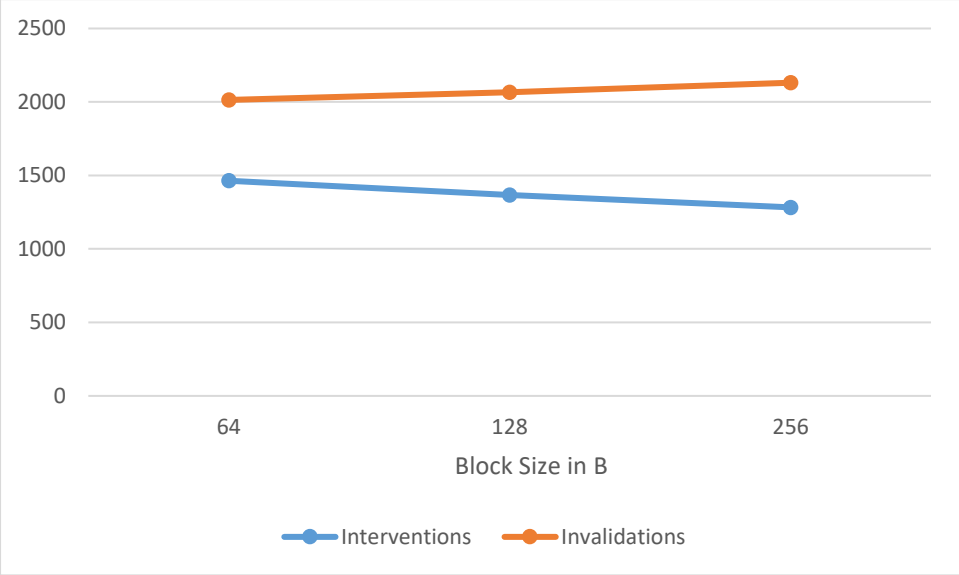
On the other hand, all the other parameters associated with the system remain constant as we increase the size of the cache.

For increasing Block Size (FBV and SSCI) (For canneal.04t.longTrace)

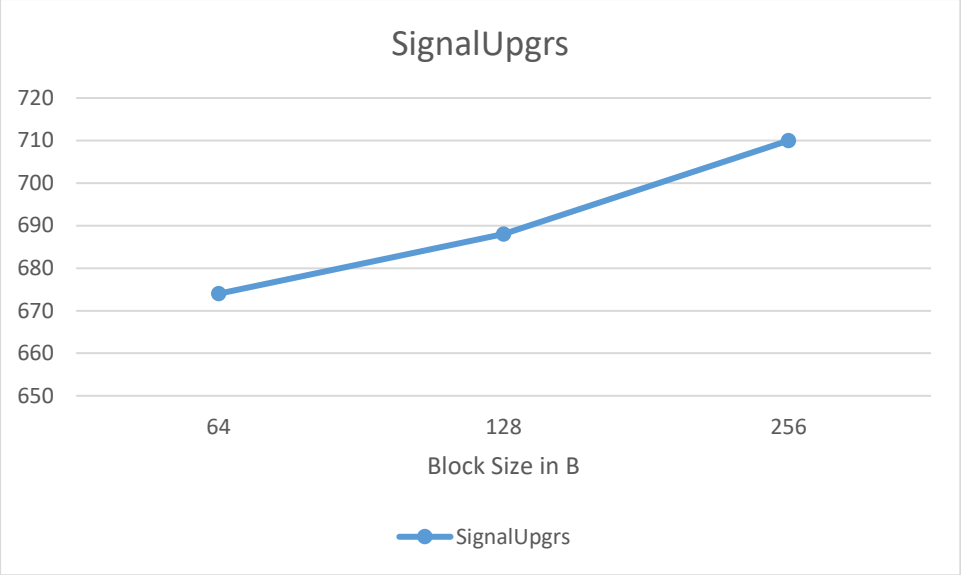
MESI Protocol	64 B	128 B	256 B	Trend
number of reads	112661	112661	112661	Constant
number of read misses	5752	5340	5023	Decrease
number of writes	11942	11942	11942	Constant
number of write misses	39	39	39	Constant
total miss rate	0.046476	0.043169	0.040625	Decrease
number of writebacks	1563	1523	1480	Decrease
number of cache-to-cache transfers	4356	4071	3858	Decrease
number of SignalRds	5752	5340	5023	Decrease
number of SignalRdXs	39	39	39	Constant
number of SignalUpgrs	674	688	710	Increase
number of invalidations	2014	2066	2131	Increase
number of interventions	1464	1367	1283	Decrease



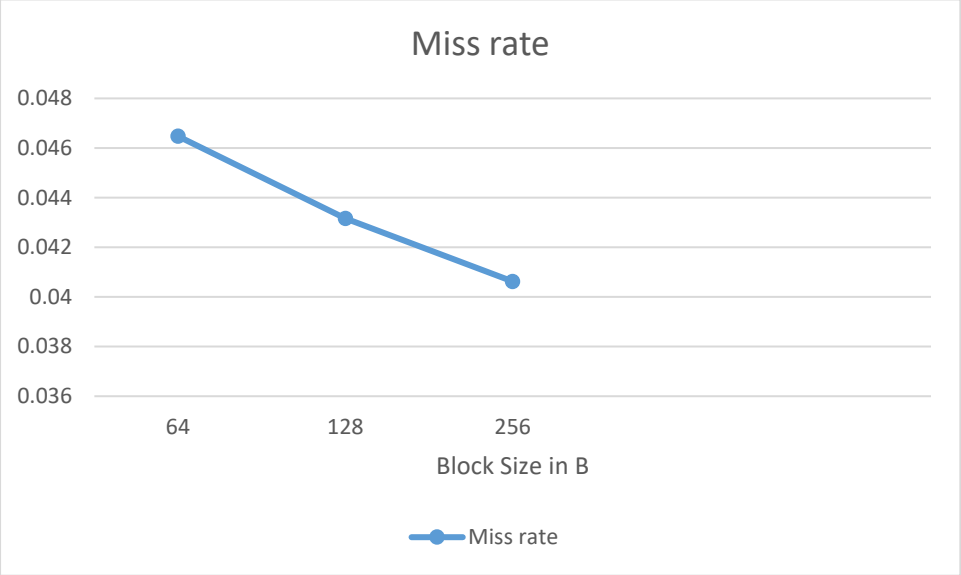
As it can be seen from the above table and the graph, as we increase the size of the block, the number of read misses, SignalRds, Writebacks, and the Cache to cache transfers, reduces.



The increase in the block size causes a decrease in the Interventions, while the Invalidations tend to increase.



The SignalUpgrs tend to increase while we increase the block size of the cache.



On the other hand, the miss rate of the system decrease on an increase in the block size of the cache.

Also, all the other parameters associated with the system remain constant with increase in the block size.