Kramer Straube

http://kstraube.github.io
kstraube@gmail.com | (650) 861-4409

EDUCATION

UNIVERSITY OF CALIFORNIA, DAVIS
MS & PhD in Computer Engineering
Expected June 2016 | Davis, CA
Cum. GPA:' 3.81 / 4.0

HARVEY MUDD COLLEGE
BS in Engineering
May 2011 | Claremont, CA
Cum. GPA: 3.2 / 4.0

LINKS

Github:// **kstraube**
LinkedIn:// **kstraube**

COURSEWORK

GRADUATE
Computer Architecture
Graphics Architecture
Embedded Computer Systems
Fault-Tolerant Systems
VLSI Design

UNDERGRADUATE
Introduction to CMOS VLSI
Microprocessor System: Design and Application
Advanced System Engineering

SKILLS

PROGRAMMING
Very Strong:
Java • Shell • LabView • Matlab
Python • LaTeX
Familiar:
Rails • Android • Assembly
C • C++

HDL AND HARDWARE DESIGN TOOLS
Very Strong:
Verilog • Cadence Design Suite (Synthesis, Simulation, Layout)
SystemVerilog • Xilinx ISE
Quartus Design Tools
Synplify Compiler Tools
Familiar:
VHDL

EXPERIENCE

INTEL | Graphics Architecture Lab Power Intern
6/2012 – 9/2012, 6/2013 - 9/2013
6/2014 - 9/2014, 6/2015 - 2/2016 | Folsom, CA

- Investigated high accuracy, high speed power measurement setup across many voltages
- Investigated maximum current measurement methodologies
- Created a Labview VI to automate measurement setup and easily change configurations
- Aided with architectural investigations into power characteristics of various devices

INTUITIVE SURGICAL | Several Intern Positions
Electrical Engineering Intern | 5/2011 - 8/2011 | Sunnyvale, CA

- Designed, tested and implemented link error testing module
- All work was done on FPGAs in Verilog

System Test Intern | 5/2010 - 7/2010 | Sunnyvale, CA

- Performed in-house system-level testing of daVinci robot
- Did formal verification of bugfixes

Platform Eng. Intern | 5/2009 - 7/2009, 12/2009 - 1/2010 | Sunnyvale, CA

- Researched new products for integration into the robot system
- Oversaw formal UL EMC testing of the daVinci robotic system

RESEARCH

UC DAVIS COMPUTER ARCHITECTURE LAB | Graduate Student Researcher
Dec 2011 – Present | Davis, CA
Several projects were completed in areas related to computer system simulation and asynchronous processor system architecture in conjuction with **Prof Venkatesh Akella**, **Prof Matthew Farrens** and **Prof Christopher Nitta**.

Designed and implemented **HySIM** - a hybrid computer system simulator design that uses a PC for memory and network simulation while the processor cores are emulated on an FPGA.

Designed and implemented **ATSim** - an asynchronous timing simulator using core-emulation on and FPGA with a decoupled functional and timing model. ATSim can model temperature, voltage, process variation and data-dependent delay effects.

Currently working on an asynchronous processor architecture for many-core machines with dynamic performance control to optimize for performance and energy efficiency.

INTERESTS

Participated in 2007 FIRST Robotics Team as Captain on newly formed team
Team got Highest Seeded Rookie Award at San Jose Regional Competition
Claremont-Mudd-Scripps NCAA Cross Country for 4 years, 2-time Nat'l competitor
Claremont-Mudd-Scripps NCAA Track for 4 years
University of California, Davis Ultimate Frisbee Team for 4 years
Team reached Nat'l Quarter-finals in 2012