1. You should see led3 blinking (one to zero). Take note when led3 blinks for the first time and also the time difference from the first to the second blink

243150 – Starts Blinking

243400 – Ends Blinking

485250 ns – Start of the second

485500ns – End of Second

Time Difference = 241850 ns is the time difference between the first and second blink

11110000 11110000 11110000 11110000

11110000 11110000 11110000 11110000

00000000000000001110011111101110

How many LUTs are used by the processor implementation?. •

How many flip-flops are used by the processor implementation?

What is the length in ns of the critical path of the processor?. •

Time distribution of the critical path between routing and logic?. •

Number of logic levels in the critical path ? •

Time for blinking in led3 blinking for the first time, time from the first to the second blink ? .

0000011000000110

How many clock cycles does it take for the LED to blink for the first time ( from start to negative edge when triggered ?

2.5 clock cycles

What is the number of lut’s and flipflops used by the design ?,

3131 Lut’s

842 Flip Flops

considering only the two main components in a logic cell, how many logic cells are fully occupied ?

607 are fully used

What are the data combinations visible on the BUS that make the LED from Detectorbus blink ?

F0F0F0F0 - Negative Edge and AAAA5555 – Positive Edge

How many logic levels are in the critical path ?

They are 14 levels

What is the distribution of logic and routing delay in percentages ?

22.1% logic / 21.7

77.9% Route / 78.3

14 Level

What is the length of critical path in nanoseconds ?

19.008 second – 14 Level

19.428 Ns

What is the maximum frequency of the design ?

52.6Mhz / 51.5Mhz

How many ns is the delay between the first led blink to the second led blink ( from negative edge to negative edge ) ?

242100 ns

10)