Sumesh Kumar

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RESEARCH INTERESTS

Hardware Accelerator Design, Computer Architecture, System Design

EDUCATION

School of Computing and Information Sciences, Florida International University   Miami, FL, USA
Ph.D. Computer Science   Aug 2019 − May 2024 (Expected), GPA: 3.95/4.0
Relevant Coursework: Parallel Computing Architectures, Advanced Machine Learning, Analysis of Algorithms

School of Electronics and Computer Science, University of Southampton   Southampton, United Kingdom
M.Sc. Systems, Control and Signal Processing   Sep 2017 − Oct 2018, Equiv. GPA: 3.33/4.0
Relevant Coursework: Advanced Signal Processing, Applied Control Systems, Machine Learning

School of Electrical Engineering and Computer Science, National University of Sciences and Technology
Islamabad, Pakistan
B.E. Electrical Engineering   Aug 2011 − June 2015, GPA: 3.24/4.0
Relevant Coursework: Digital System Design, Embedded Systems Design, Data Structures and Algorithms, Object Oriented
Programming

RESEARCH PROJECTS

Florida International University   Miami, FL, USA, Aug, 2018 − Present
PhD Researcher

- **Hardware Accelerator Design for Cross-Correlation Score Computation.** (Patent applied)
  - Designed accelerator architecture for Intel Stratix-10 FPGAs to speed-up correlation score computation by 24 times compared with state-of-the-art software tool. (VHDL, Verilog, Quartus, QSys 2+ Years)
  - Improved communication overhead of the design by 600 times by utilizing adaptive caching technique.
  - Awarded Intel Stratix-10 FPGA (worth 8000 USD) under the Intel University Program.
- **Data Restructuring for Improving Communication Patterns in Peptide Identification Algorithm**
  - Improve cache performance by 30% by restructuring mass-spectrometry data in database search problem for peptide identification. (Python, C/C++, Linux 2+ Years)

WORK EXPERIENCE

Hewlett Packard Enterprise   Durham, NC, USA, May 2022 - Aug 2022
Software Engineer Intern (QAOPS)

- Developed build-tests automation tool to improve engineer productivity by automatically gathering test-data from multiple databases. (Python, Celery, Flask 3+ Months)
- Enabled 20-fold speed-up in query search time by instantiating multiple celery workers.

Florida International University   Miami, FL, USA, Aug 2019 − Present
Graduate Teaching Assistant

- Mentored undergrad students in managing Senior Design Project using scrum development process
- Designed coursework assignments and exams for computer design and architecture course
- Conducted laboratory sessions for undergraduate Java programming course

Mentor Graphics Corporation (Now Siemens EDA)   Lahore, Punjab, Pakistan, August 2015 − June 2017
Embedded Software Engineer

- Improved code-performance analysis process by implementing code-tracing support in embedded multi-core framework. (C, Nucleus RTOS)
- Ported Mentor Embedded Multi-core Framework (MEMF) library for ARMv8 and ARMv7 architectures. (ARM, C)
- Improved the communication speed between master and remote processors by 42% by implementing zero-copy feature in shared-memory communication library.

SKILLS

FPGA Design, Embedded System Design, VHDL, Verilog, Intel Quartus, Intel QSys, Xilinx Vivado, PCIe interface, Hardware accelerator design, Re-confguerable architectures, Coarse-grained Re-configurable accelerator, Linux Pthreads, Real time operating system, Operating System Design, Avalon memory-mapped bus protocol, AXI-lite bus protocol, High-Performance

Computing, Parallel Computing, Algorithm Design and Analysis, Object Oriented Programming, Data Structures, Machine Learning, Deep Learning, Convolutional Neural Networks, LSTM, Generative Adversarial Networks, Python/Python3, NumPy, Pandas, Cuda, OpenCL, MPI, OpenMP, C, C++, Docker, Git, GitHub, GitLab, CMake, Jira

PUBLICATIONS

- Kumar, Sumesh, and Fahad Saeed. "Real-time peptide identification from high-throughput mass-spectrometry data." In Proceedings of the 12th ACM Conference on Bioinformatics, Computational Biology, and Health Informatics, pp. 1-1. 2021.
- S. Kumar and F. Saeed, "Communication-avoiding micro-architecture to compute Xcorr scores for peptide identification," 2021 31st International Conference on Field-Programmable Logic and Applications (FPL), 2021, pp. 99-103, doi: 10.1109/FPL53798.2021.00024.

PRESENTATIONS/AWARDS

- Presented "Communication-avoiding micro-architecture to compute Xcorr scores for peptide identification." at 2021 International Conference on Field Programmable Logic and Applications.
- Awarded Intel Stratix-10 FPGA (worth 8000 USD) under the Intel University Program.
- Awarded Xliinx Versal AI Core Series VCK190 Evaluation Kit (worth 14000 USD) under the Xilinx University Program.
- Selected as one of the 800 students worldwide for the Commonwealth Master's Scholarship program to undertake post-graduate studies in United Kingdom.

VOLUNTEER WORK/EXTRA-CURRICULAR ACTIVITIES

- Member Upsilon Pi Epsilon (UPE), UPE Leap, UPE SparkDev, and UPE Code.
- Regular participant in local official chess tournaments and registered with United States Chess Federation.