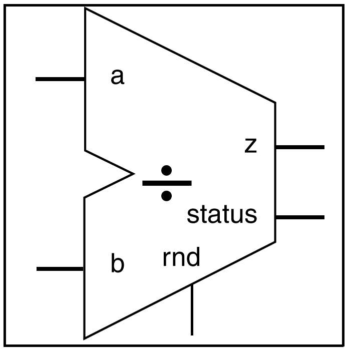
DW_fp_div

Floating-Point Divider

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

Revision History



- The precision format is parameterizable for either IEEE single, double precision, or a user-defined custom format
- Hardware for denormal numbers of IEEE 754 standard is provided.
- Fully compatible with the IEEE 754 Floating-point standard[1] with proper set of parameters
- Faithful rounding with 1 ulp error is supported by parameter
- DesignWare datapath generator is employed for better timing and area

Description

DW_fp_div is a floating-point divider that divides two floating-point operands: `a` by `b` to produce a floating-point quotient, `z`.

The input `rnd` is a 3-bit rounding mode (see Rounding Modes in the *Datapath Floating-Point Overview*) and the output `status` is an 8-bit status flag.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
a	*exp_width* + *sig_width* + 1 bits	Input	Dividend
b	*exp_width* + *sig_width* + 1 bits	Input	Divisor
rnd	3 bits	Input	Rounding mode
z	*exp_width* + *sig_width* + 1 bits	Output	Quotient of A/B
status	8 bits	Output	■ Status flags corresponding to `z`; for details, see STATUS Flags in the *Datapath Floating-Point Overview* ■ status[7]: Indicates divide-by-zero operation

Table 1-2 Parameter Description

Parameter	Values	Description
sig_width	4 to 253 bits Default: 23	Word length of fraction field of floating-point numbers `a`, `b`, and `z`

[1] For more information, see IEEE 754 Compatibility in the *Datapath Floating-Point Overview.*

Table 1-2 Parameter Description (Continued)

Parameter	Values	Description
exp_width	3 to 31 bits Default: 8	Word length of biased exponent of floating-point numbers a, b, and z
ieee_compliance	0 or 1 Default: 0	When 1, the generated architecture includes the use of denormals and NaNs
faithful_round	0 or 1 Default: 0	Select the faithful rounding that admits maximum 1 ulp error. 0: Support all rounding modes described in the *Datapath Floating-Point Overview*. 1: Results have 1 *ulp* error (see Table 1-5 on page 3).

Table 1-3 Synthesis Implementations[a]

Implementation Name	Function	License Feature Required
rtl	Synthesis model (Digit-recurrence Method)	DesignWare
str	Synthesis model (Multiplicative Method) NOTE: This implementation is disabled when sig_width ≤ 10. In this scenario, use the rtl implementation because it provides better QoR.	DesignWare

[a] During synthesis, Design Compiler will select the appropriate architecture for your constraints. However, you may force Design Compiler to use any architectures described in this table. For more, see *DesignWare Building Block IP User Guide*

Table 1-4 Simulation Models

Model	Function
DW02.DW_FP_DIV_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW_fp_div_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_fp_div.v	Verilog simulation model source code

Table 1-5 summarizes the error ranges with the rounding modes supported by DW_fp_div. The output of DW_fp_div, z, is a rounded value from the internal calculated value, so there exists a numerical error between z and the actual value of a/b. Depending on the rounding modes, the error ranges are slightly different, but the absolute error range of less than 1 *ulp* is guaranteed.

Table 1-5 Error Ranges ($\varepsilon = z - a/b$)

faithful_round	RND	Mode	Error (ε)	Absolute Error $\lvert\varepsilon\rvert$
0	0	Round to Nearest Even	$-0.5\ ulp \le \varepsilon \le 0.5\ ulp$[a]	$\lvert\varepsilon\rvert \le 0.5\ ulp$
	1	Round to Zero	$-1\ \mathrm{ulp} < \varepsilon \le 0$ if $z > 0$ $0 \le \varepsilon < 1\ ulp$ if $z < 0$	$\lvert\varepsilon\rvert < 1\ ulp$
	2	Round to +Inf.	$0 \le \varepsilon < 1\ ulp$	$\lvert\varepsilon\rvert < 1\ ulp$
	3	Round to -Inf.	$-1\ ulp < \varepsilon \le 0$	$\lvert\varepsilon\rvert < 1\ ulp$
	4	Round to Nearest Up	$-0.5\ ulp < \varepsilon \le 0.5\ ulp$	$\lvert\varepsilon\rvert \le 0.5\ ulp$
	5	Round Away from Zero	$0 \le \varepsilon < 1\ ulp$ if $z > 0$ $-1\ ulp < \varepsilon \le 0$ if $z < 0$	$\lvert\varepsilon\rvert < 1\ ulp$
1	-		$-1\ ulp < \varepsilon < 0.5\ ulp$	$\lvert\varepsilon\rvert < 1\ ulp$

[a] $\varepsilon = \pm 0.5\ ulp$ depends on the position of the nearest even floating-point number.

DW_fp_div provides the hardware for denormal numbers and NaNs of IEEE 754 standard. If the parameter `ieee_compliance` is turned off, denormal numbers are considered as zeros, and NaNs are considered as Infinity. Otherwise, denormal numbers and NaNs become effective and additional hardware for the division of denormal numbers is integrated.

For more information about the floating-point system defined for all the DW_fp components, including `status` flag bits, and integer and floating-point formats, refer to the *Datapath Floating-Point Overview*.

Related Topics

- Datapath Floating-Point Overview
- DesignWare Building Block IP Documentation Overview

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DW_Foundation_comp.all;
-- If using numeric types from std_logic_arith package,
-- comment the preceding line and uncomment the following line:
-- use DWARE.DW_Foundation_comp_arith.all;

entity DW_fp_div_inst is

  generic (
    inst_sig_width       : POSITIVE := 23;
    inst_exp_width       : POSITIVE := 8;
    inst_ieee_compliance : INTEGER := 0
  );
  port (
    inst_a      : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
    inst_b      : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
    inst_rnd    : in std_logic_vector(2 downto 0);
    z_inst      : out std_logic_vector(inst_sig_width+inst_exp_width downto 0);
    status_inst : out std_logic_vector(7 downto 0)
  );

end DW_fp_div_inst;


architecture inst of DW_fp_div_inst is

begin

  -- Instance of DW_fp_div
  U1 : DW_fp_div
  generic map (
    sig_width => inst_sig_width,
    exp_width => inst_exp_width,
    ieee_compliance => inst_ieee_compliance
  )
  port map (
    a => inst_a,
    b => inst_b,
    rnd => inst_rnd,
    z => z_inst,
    status => status_inst
  );

end inst;
```

```
-- pragma translate_off
configuration DW_fp_div_inst_cfg_inst of DW_fp_div_inst is
   for inst
   end for;
end DW_fp_div_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_fp_div_inst( inst_a, inst_b, inst_rnd, z_inst, status_inst );

parameter sig_width = 23;
parameter exp_width = 8;
parameter ieee_compliance = 0;


input [sig_width+exp_width : 0] inst_a;
input [sig_width+exp_width : 0] inst_b;
input [2 : 0] inst_rnd;
output [sig_width+exp_width : 0] z_inst;
output [7 : 0] status_inst;

  // Instance of DW_fp_div
DW_fp_div #(sig_width, exp_width, ieee_compliance) U1
( .a(inst_a), .b(inst_b), .rnd(inst_rnd), .z(z_inst), .status(status_inst)
);

endmodule
```

Revision History

Date	Release	Updates
July 2017	M-2016.12-SP5	■ For STAR 9001189734, added Note to description of str implementation in Table 1-3 on page 2 ■ Added this Revision History table

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