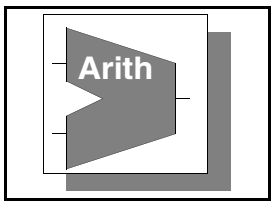
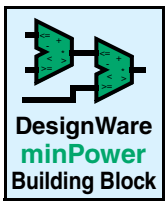


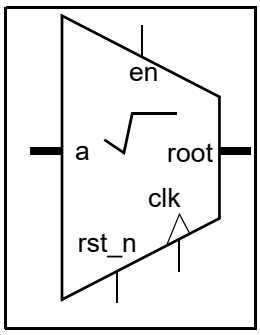


DW_sqrt_pipe

Stallable Pipelined Square Root

Version, STAR and Download Information: IP Directory

Features and Benefits



- Parameterized word length
- Unsigned and signed (two's complement) data operation
- Parameterized number of pipeline stages
- Parameterized stall mode (stallable or non-stallable)
- Parameterized reset mode (no reset, asynchronous or synchronous reset)
- Automatic pipeline retiming
- Provides minPower benefits with the DesignWare-LP license.

Description

DW_sqrt_pipe is a universal stallable pipelined square root generator. DW_sqrt_pipe computes the square root of operand a with a latency of *num_stages* – 1 clock cycles.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
clk	1 bit	Input	Input clock
rst_n	1 bit	Input	Reset, active-low (not used if parameter *rst_mode* = 0)
en	1 bit	Input	Register enable, active high (used only if parameter *stall_mode* = 1) 0 = stall 1 = enable register
a	*width* bit(s)	Input	Radicand
root	(*width*+1)/2 bit(s)	Output	Square root

Table 1-2 Parameter Description

Parameter	Values	Description
width	≥ 2	Word length of a. Default: None
num_stages	≥ 2	Number of pipeline stages. Default: 2

Table 1-2 Parameter Description (Continued)

Parameter	Values	Description
stall_mode	0 or 1 Default: 1	Stall mode 0 = non-stallable, 1 = stallable
rst_mode	0 to 2 Default: 1	Reset mode 0 = no reset, 1 = asynchronous reset, 2 = synchronous reset)
tc_mode	0 or 1 Default: 0	Two's Complement mode 0 = unsigned number, 1 = signed number
op_iso_mode	0 to 4 Default: 0	Operand Isolation Mode (controls datapath gating for minPower flow) If *stall_mode* is 0, this parameter is ignored and no isolation is applied. 0 = DC variable (DW_lp_op_iso_mode) can control the op iso mode 1 = 'none' 2 = 'and' 3 = 'or' 4 = preferred isolation style: 'and'

Table 1-3 Synthesis Implementations

Implementation Name	Implementation	License Feature Required
str[a]	Pipelined str synthesis model	DesignWare

a. One of rpl or cla implementation is selected based the constraints of the design.

Table 1-4 Simulation Models

Model	Function
DW02.DW_SQRT_PIPE_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW_sqrt_pipe_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_sqrt_pipe.v	Verilog simulation model source code

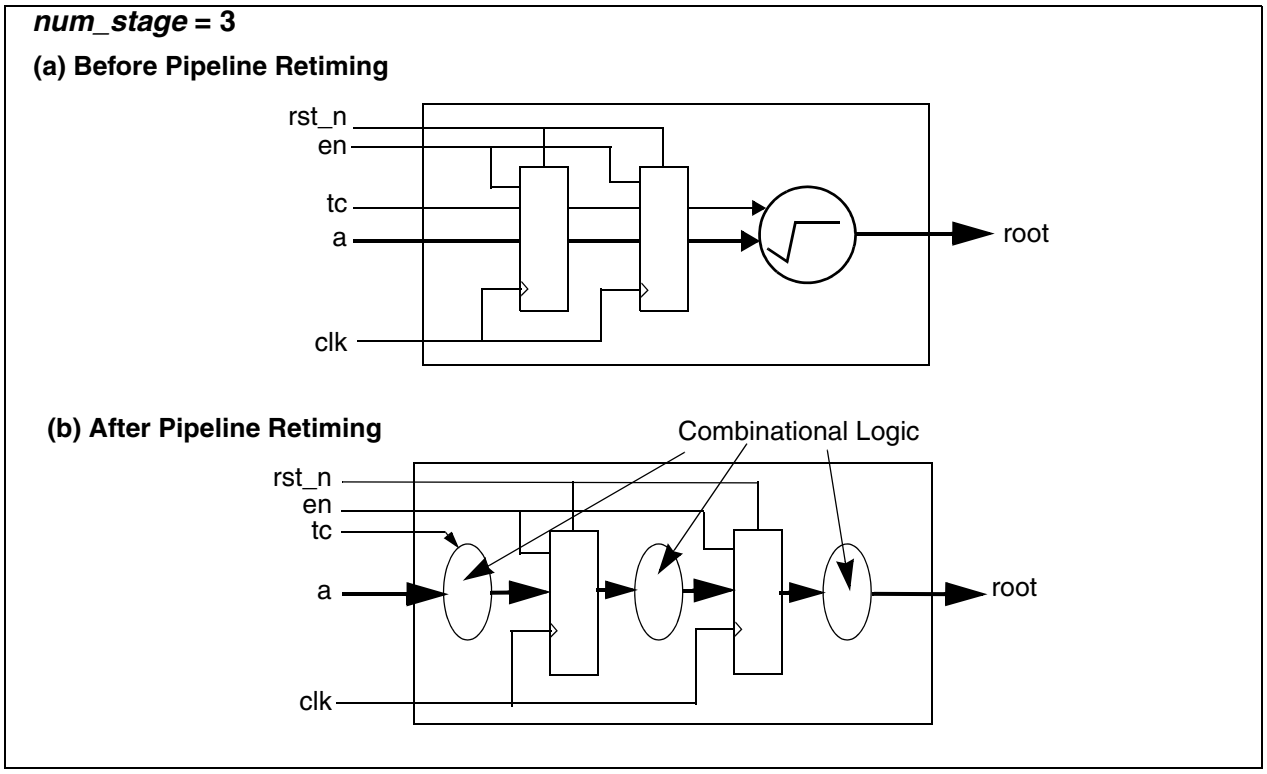
Functional Description

The parameter *tc_mode* determines whether the input and output data is interpreted as unsigned (*tc_mode*=0) or signed (*tc_mode*=1) numbers.

Automatic pipeline retiming ensures optimal placement of pipeline registers within the square root generator to achieve maximum throughput. The pipeline can be stalled by setting the load enable signal

en=0 (when *stall_mode*=1). The pipeline registers can either have no reset (*rst_mode*=0) or an asynchronous (*rst_mode*=1) or synchronous reset (*rst_mode*=2) connected to the reset signal rst_n.

Figure 1-1 Pipeline Retiming



Timing Waveform

Figure 1-2 Waveform 1

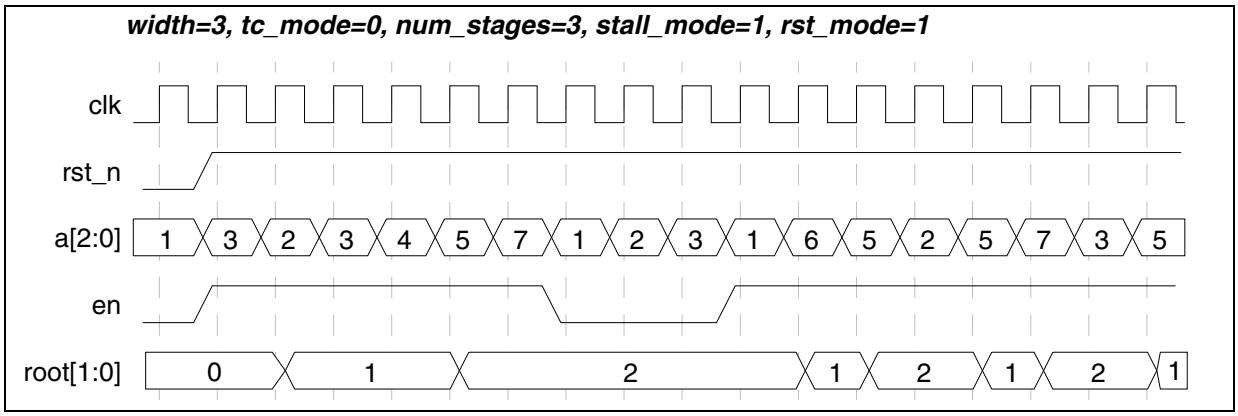
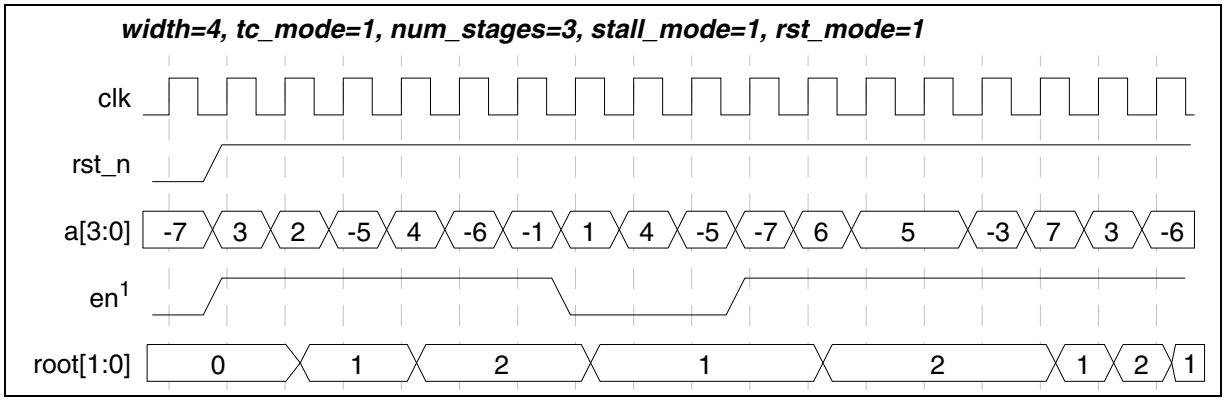


Figure 1-3 Waveform 2



[1]If parameter stall_mode=0, then pin en has no effect.

Figure 1-4 Waveform 3

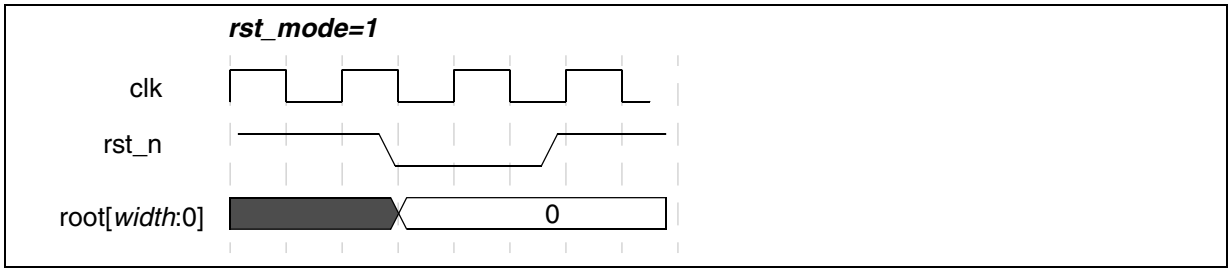
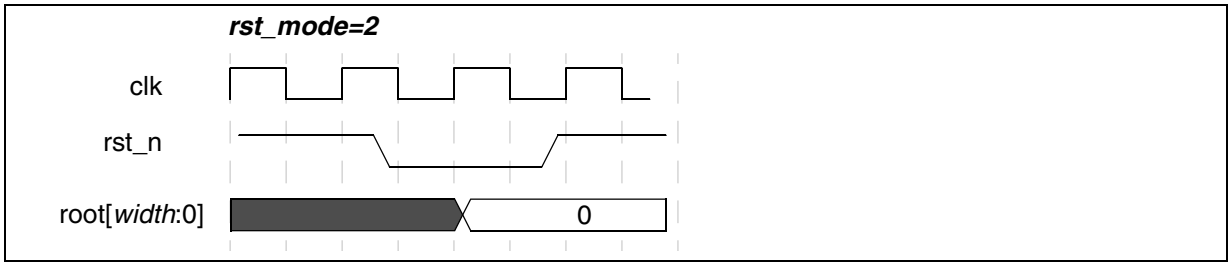


Figure 1-5 Waveform 4



Related Topics

- Math – Arithmetic Overview
- DesignWare Building Block IP Documentation Overview

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DW_Foundation_comp_arith.all;

entity DW_sqrt_pipe_inst is
  generic (inst_width      : POSITIVE := 2; inst_tc_mode     : NATURAL := 0;
           inst_num_stages : POSITIVE := 2; inst_stall_mode  : NATURAL := 1;
           inst_rst_mode   : NATURAL := 1;  inst_op_iso_mode : NATURAL := 0 );
  port (inst_clk   : in std_logic;
        inst_rst_n : in std_logic;
        inst_en    : in std_logic;
        inst_a     : in std_logic_vector(inst_width-1 downto 0);
        root_inst  : out std_logic_vector((inst_width+1)/2-1 downto 0)  );
end DW_sqrt_pipe_inst;

architecture inst of DW_sqrt_pipe_inst is
begin
  -- Instance of DW_sqrt_pipe
  U1 : DW_sqrt_pipe
    generic map (width => inst_width,   tc_mode => inst_tc_mode,
                 num_stages => inst_num_stages,  stall_mode => inst_stall_mode,
                 rst_mode => inst_rst_mode,   op_iso_mode => inst_op_iso_mode )
    port map (clk => inst_clk,   rst_n => inst_rst_n,   en => inst_en,
              a => inst_a,  root => root_inst );
end inst;

-- Configuration for use with VSS simulator
-- pragma translate_off
configuration DW_sqrt_pipe_inst_cfg_inst of DW_sqrt_pipe_inst is
  for inst
  end for; -- inst
end DW_sqrt_pipe_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_sqrt_pipe_inst( inst_clk, inst_rst_n, inst_en, inst_a, root_inst );
  parameter inst_width = 2;
  parameter inst_tc_mode = 0;
  parameter inst_num_stages = 2;
  parameter inst_stall_mode = 1;
  parameter inst_rst_mode = 1;
  parameter inst_op_iso_mode = 0;

  input inst_clk;
  input inst_rst_n;
  input inst_en;
  input [inst_width-1 : 0] inst_a;
  output [(inst_width+1)/2-1 : 0] root_inst;

  // Instance of DW_sqrt_pipe
  DW_sqrt_pipe #(inst_width, inst_tc_mode, inst_num_stages,
                 inst_stall_mode, inst_rst_mode, inst_op_iso_mode)
    U1 (.clk(inst_clk),   .rst_n(inst_rst_n),
        .en(inst_en),   .a(inst_a),   .root(root_inst) );
endmodule
```

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