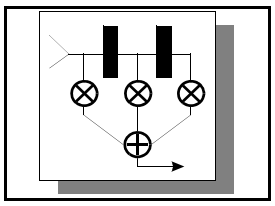
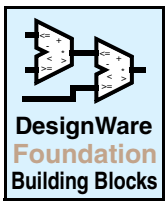




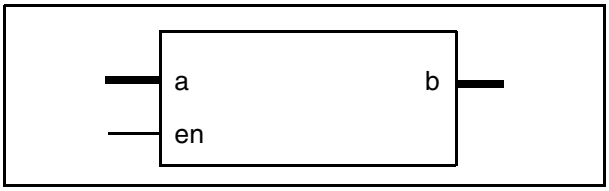
DW_decode_en

Binary Decoder with Enable

Version, STAR and Download Information: IP Directory

Features and Benefits

- Parameterized word length
- Integrates enable control



Description

DW_decode_en decodes an address on input port `a` to a single bit-line on output port `b`. A decoder with *width* = *n* bits has 2^n bits at the output, where each output with index *i* becomes active when *en* = *1* (enable input) and input *a* = *i*. The selected output bit is active high. When *en* = *0* none of the output bits are active.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
en	1 bit	Input	Enable input (active high)
a	*width*	Input	Binary input data
b	2^{width}	Output	Decoded output data

Table 1-2 Parameter Description

Parameter	Values	Description
width[a]	1 to 16	Word length of input a is *width*. Word length of output b is 2^{width}

a. The `width` parameter value causes the size of output B to grow exponentially. Therefore, a `width` value greater than 12 will result in abnormally long compile times.

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
str	Synthesis model	DesignWare
cgen	Datapath generator-based Implementation	DesignWare

Table 1-4 Simulation Models

Model	Function
DW01.DW_DECODE_EN_CFG_SIM	Design unit name for VHDL simulation
dw/dw01/src/DW_decode_en_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_decode_en.v	Verilog simulation model source code

Table 1-5 Truth Table (width = 3)

A(2:0)	en	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	B(0)
000	1	0	0	0	0	0	0	0	1
001	1	0	0	0	0	0	0	1	0
010	1	0	0	0	0	0	1	0	0
011	1	0	0	0	0	1	0	0	0
100	1	0	0	0	1	0	0	0	0
101	1	0	0	1	0	0	0	0	0
110	1	0	1	0	0	0	0	0	0
111	1	1	0	0	0	0	0	0	0
xxx	0	0	0	0	0	0	0	0	0

Related Topics

- Logic – Combinational Overview
- DesignWare Building Block IP Documentation Overview

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_Foundation_comp_arith.all;

entity DW_decode_en_inst is
      generic (
        inst_width : NATURAL := 8
        );
      port (
        inst_en : in std_logic;
        inst_a : in std_logic_vector(inst_width-1 downto 0);
        b_inst : out std_logic_vector(2**inst_width-1 downto 0)
        );
    end DW_decode_en_inst;


architecture inst of DW_decode_en_inst is

begin

    -- Instance of DW_decode_en
    U1 : DW_decode_en
    generic map (
          width => inst_width
          )
    port map (
          en => inst_en,
          a => inst_a,
          b => b_inst
          );


end inst;

-- pragma translate_off
configuration DW_decode_en_inst_cfg_inst of DW_decode_en_inst is
  for inst
  end for; -- inst
end DW_decode_en_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_decode_en_inst( inst_en, inst_a, b_inst );

parameter inst_width = 8;


input inst_en;
input [inst_width-1 : 0] inst_a;
output [(1<<inst_width)-1 : 0] b_inst;

    // Instance of DW_decode_en
    DW_decode_en #(inst_width) U1 (
                .en(inst_en),
                .a(inst_a),
                .b(b_inst) );

endmodule
```

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