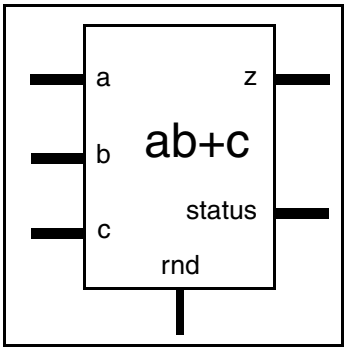
DW_fp_mac

Floating-Point Multiply-and-Add

Version, STAR and Download Information: IP Directory

Features and Benefits



- The precision format is parameterizable for either IEEE single, double precision, or a user-defined custom format
- Hardware for denormal numbers of IEEE 754 standard is selectively provided
- Accuracy conforms to IEEE 754 Floating-point standard[1]

Description

DW_fp_mac is a floating-point component that performs the multiply and add operation. It sums up a floating-point product of input a and b to input `c`: `ab + c` to produce a floating-point multiply and add result, `z`. The input `rnd` is a 3-bit rounding mode (see Rounding Modes in the *Datapath Floating-Point Overview*).

The output of this component has accuracy consistent with the IEEE Standard 754, where the computation happens as it was done using infinite precision, and rounding is executed as a last step to obtain the final result. As a consequence, the accuracy of DW_fp_mac is much better than the accuracy of an implementation using DW_fp_mult and DW_fp_add.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
a	*exp_width* + *sig_width* + 1 bits	Input	Multiplier
b	*exp_width* + *sig_width* + 1 bits	Input	Multiplicand
c	*exp_width* + *sig_width* + 1 bits	Input	Addend
rnd	3 bits	Input	Rounding mode
z	*exp_width* + *sig_width* + 1 bits	Output	MAC result (`a` x `b` + `c`)
status	8 bits	Output	See STATUS Flags in the *Datapath Floating-Point Overview*

1. For more information, see IEEE 754 Compatibility in the *Datapath Floating-point Overview*.

Table 1-2 Parameter Description

Parameter	Values	Description
sig_width	2 to 253 bits Default: 23	Word length of fraction field of floating-point numbers `a`, `b`, c, and `z`
exp_width	3 to 31 bits Default: 8	Word length of biased exponent of floating-point numbers `a`, `b`, c and `z`
ieee_compliance	0 or 1 Default: 0	When 1, the generated architecture includes the use of denormals and NaNs.

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
rtl	Area-optimized synthesis model	DesignWare
str	Delay-optimized synthesis model	DesignWare

Table 1-4 Simulation Models

Model	Function
DW02.DW_FP_MAC_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW_fp_mac_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_fp_mac.v	Verilog simulation model source code

DW_fp_mac has the ability to handle denormal numbers and NaNs of IEEE 754 standard. If the parameter *ieee_compliance* is turned off, denormal numbers are considered as zeros, and NaNs are considered as Infinity. Otherwise, denormal numbers and NaNs become effective and additional hardware for the multiply-and-addition of denormal numbers is integrated.

For more information on floating-point, including status flag bits, and integer and floating-point formats, refer to the *Datapath Floating-Point Overview*.

```
sc_uint< sig_width+exp_width+1 >
    DW_fp_mac< sig_width, exp_width, ieee_compliance >::implement  (
        sc_uint< sig_width+exp_width+1 >  a,
        sc_uint< sig_width+exp_width+1 >  b,
        sc_uint< sig_width+exp_width+1 >  c,
        sc_uint< 3 >  rnd,
        sc_uint< 8 > *  status )
```

Related Topics

- Datapath Floating-Point Overview
- DesignWare Building Block IP Documentation Overview

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_Foundation_comp_arith.all;

entity DW_fp_mac_inst is
     generic (
      inst_sig_width : POSITIVE := 23;
      inst_exp_width : POSITIVE := 8;
      inst_ieee_compliance : INTEGER := 0
      );
     port (
      inst_a : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
      inst_b : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
      inst_c : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
      inst_rnd : in std_logic_vector(2 downto 0);
      z_inst : out std_logic_vector(inst_sig_width+inst_exp_width downto 0);
      status_inst : out std_logic_vector(7 downto 0)
      );
    end DW_fp_mac_inst;

architecture inst of DW_fp_mac_inst is
begin

    -- Instance of DW_fp_mac
    U1 : DW_fp_mac
    generic map (
          sig_width => inst_sig_width,
          exp_width => inst_exp_width,
          ieee_compliance => inst_ieee_compliance
          )
    port map (
          a => inst_a,
          b => inst_b,
          c => inst_c,
          rnd => inst_rnd,
          z => z_inst,
          status => status_inst
          );

end inst;

-- pragma translate_off
configuration DW_fp_mac_inst_cfg_inst of DW_fp_mac_inst is
for inst
end for; -- inst
end DW_fp_mac_inst_cfg_inst;
```

```
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_fp_mac_inst( inst_a, inst_b, inst_c, inst_rnd, z_inst, status_inst );

parameter inst_sig_width = 23;
parameter inst_exp_width = 8;
parameter inst_ieee_compliance = 0;

input [inst_sig_width+inst_exp_width : 0] inst_a;
input [inst_sig_width+inst_exp_width : 0] inst_b;
input [inst_sig_width+inst_exp_width : 0] inst_c;
input [2 : 0] inst_rnd;
output [inst_sig_width+inst_exp_width : 0] z_inst;
output [7 : 0] status_inst;

    // Instance of DW_fp_mac
    DW_fp_mac #(inst_sig_width, inst_exp_width, inst_ieee_compliance) U1 (
                .a(inst_a),
                .b(inst_b),
                .c(inst_c),
                .rnd(inst_rnd),
                .z(z_inst),
                .status(status_inst) );

endmodule
```

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