



# DWF\_dp\_mult\_comb function

## Combined Unsigned/Signed Multiply

Version, STAR and Download Information: [IP Directory](#)

### Description

The DWF\_dp\_mult\_comb function performs combined (switchable) unsigned/signed multiplication of the two arguments a and b. Argument a (b) is interpreted as signed if argument a\_tc (b\_tc) is 1, otherwise as unsigned. The result must be interpreted as signed if argument a\_tc or b\_tc (or both) is 1 (= signed multiplication), otherwise as unsigned (= unsigned multiplication).

Table 1-1 Function Names

Function Name	Description
DWF_dp_mult_comb	VHDL combined multiply (std_logic_vector/unsigned/signed arguments)
DWF_dp_mult_comb	Verilog combined multiply
DWF_dp_mult_comb_tc	Verilog combined multiply (signed arguments)

Table 1-2 Argument Description

Name	Type	Width / Values	Description
a	Vector	<i>a_width</i>	Input multiplier
a_tc	Bit	1	Two's complement control for multiplier 0 = unsigned, 1 = signed
b	Vector	<i>b_width</i>	Input multiplicand
b_tc	Bit	1	Two's complement control for multiplicand 0 = unsigned, 1 = signed
DWF_dp_mult_comb	Vector	<i>a_width+b_width</i>	Returned value

Table 1-3 Parameter Description (Verilog)

Parameter	Values	Description
a_width	$\geq 1$	Word length of input a
b_width	$\geq 1$	Word length of input b

Verilog Include File: DW\_dp\_mult\_comb\_function.inc

## Functional Description

```
z[a_width+b_width-1:0] = DWF_dp_mult_comb (a[a_width-1:0], a_tc,  
                                           b[b_width-1:0], b_tc)
```

```
z (unsigned)  = a (unsigned) * b (unsigned)      if a_tc = 0 and b_tc = 0
```

```
z (signed)    = a (signed)   * b (unsigned)     if a_tc = 1 and b_tc = 0  
               = a (unsigned) * b (signed)      if a_tc = 0 and b_tc = 1  
               = a (signed)   * b (signed)      if a_tc = 1 and b_tc = 1
```

For more information about the DesignWare datapath functions, refer to the topic titled [DesignWare Datapath Functions Overview](#).

## Related Topics

- [DesignWare Datapath Functions Overview](#)
- [DesignWare Building Block IP Documentation Overview](#)

## VHDL Example

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

entity DWF_dp_mult_comb_test is
  port (a, b, c      : in  unsigned(7 downto 0);
        a_tc, b_tc  : in  std_logic;
        z           : out unsigned(15 downto 0));
end DWF_dp_mult_comb_test;

architecture rtl of DWF_dp_mult_comb_test is
begin
  z <= DWF_dp_mult_comb (a, a_tc, b, b_tc) + c;
end rtl;
```

---

## Verilog Example

```
module DWF_dp_mult_comb_test (a, b, c, a_tc, b_tc, z);

    input    [7:0] a, b, c;
    input          a_tc, b_tc;
    output [15:0] z;

    // Passes the parameters to the function
    parameter a_width = 8;
    parameter b_width = 8;

    // add "$SYNOPSISYS/dw/sim_ver" to the search path for simulation
    `include "DW_dp_mult_comb_function.inc"

    assign z = DWF_dp_mult_comb (a, a_tc, b, b_tc) + c;

endmodule
```

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Synopsys, Inc.  
690 E. Middlefield Road  
Mountain View, CA 94043  
[www.synopsys.com](http://www.synopsys.com)

