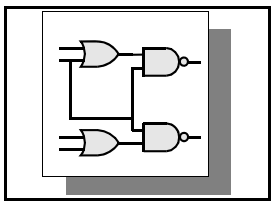
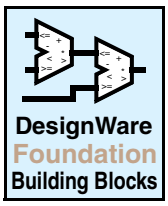




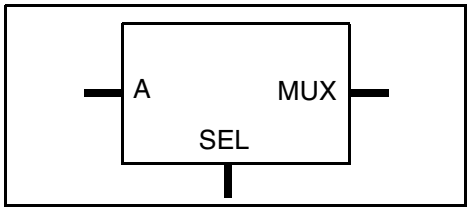
DW01_mux_any

Universal Multiplexer

Version, STAR and Download Information: IP Directory

Features and Benefits

- Parameterized word lengths
- Saves coding time by eliminating the need to code muxes explicitly
- Increases design abstraction
- Uses 8-to-1 muxes where possible



Description

DW01_mux_any is an universal multiplexer. This component selects a subrange of the input `A`, and places it on the output `MUX`. The select input, `SEL`, multiplexes the subrange of `A` to `MUX`. If necessary, `A` is padded with high order bits of zero. The widths of the inputs and outputs are fixed by the parameters *A_width*, *SEL_width*, and *MUX_width*.

DW01_mux_any uses 8-to-1 MUXes whenever possible to get the fastest possible implementation with the lowest gate count.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
A	*A_width*	Input	Data input bus
SEL	*SEL_width*	Input	Select input
MUX	*MUX_width*	Output	Multiplexed data out

Table 1-2 Parameter Description

Parameter	Values	Description
A_width	≥ 1	Word length of A
SEL_width	≥ 1	Word length of SEL
MUX_width	≥ 1	A((SEL + 1) × *MUX_width* – 1 downto SEL**MUX_width*)
bal_str[a]	0 or 1 Default: 0	Controls the symmetric structure of the ‘str’ implementation. 1 = use symmetric structure with ‘str” implementation.

a. Prior to release 2007.12-SP2, this parameter is ignored.

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
str	Synthesis model	DesignWare

Table 1-4 Simulation Models

Model	Function
DW01.DW01_MUX_ANY_CFG_SIM	Design unit name for VHDL simulation
dw/dw01/src/DW01_mux_any_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW01_mux_any.v	Verilog simulation model source code

Related Topics

- Logic – Combinational Overview
- DesignWare Building Block IP Documentation Overview

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW01_mux_any_inst is
  generic (inst_A_width : POSITIVE := 8;
           inst_SEL_width : POSITIVE := 8;
           inst_MUX_width : POSITIVE := 8);
  port (inst_A : in std_logic_vector(inst_A_width-1 downto 0);
        inst_SEL : in std_logic_vector(inst_SEL_width-1 downto 0);
        MUX_inst : out std_logic_vector(inst_MUX_width-1 downto 0));
end DW01_mux_any_inst;

architecture inst of DW01_mux_any_inst is
begin
  -- Instance of DW01_mux_any
  U1 : DW01_mux_any
    generic map ( A_width => inst_A_width, SEL_width => inst_SEL_width,
                  MUX_width => inst_MUX_width )
    port map ( A => inst_A, SEL => inst_SEL, MUX => MUX_inst );
end inst;

-- pragma translate_off
configuration DW01_mux_any_inst_cfg_inst of DW01_mux_any_inst is
  for inst
  end for; -- inst
end DW01_mux_any_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW01_mux_any_inst( inst_A, inst_SEL, MUX_inst );

  parameter A_width = 8;
  parameter SEL_width = 8;
parameter MUX_width = 8;

  input [A_width-1 : 0] inst_A;
  input [SEL_width-1 : 0] inst_SEL;
  output [MUX_width-1 : 0] MUX_inst;

    // Instance of DW01_mux_any
    DW01_mux_any #(A_width, SEL_width, MUX_width)
      U1 ( .A(inst_A), .SEL(inst_SEL), .MUX(MUX_inst) );

endmodule
```

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