

DW01_sub

Subtractor

Version, STAR and Download Information: [IP Directory](#)

Features and Benefits

- Parameterized word length
- Carry-in and carry-out signals

Description

DW01_sub is a two-input subtractor. DW01_sub subtracts two operands A and B with a carry-in (CI) to produce the output DIFF with a carry-out (CO).

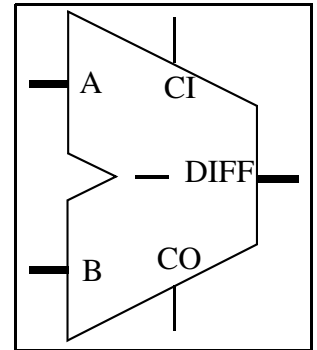


Table 1-1 Pin Description

Pin Name	Width	Direction	Function
A	<i>width</i> bit(s)	Input	Input data
B	<i>width</i> bit(s)	Input	Input data
CI	1 bit	Input	Carry-in
DIFF	<i>width</i> bit(s)	Output	Difference of $A - B - CI$
CO	1 bit	Output	Carry-out

Table 1-2 Parameter Description

Parameter	Values	Description
width	≥ 1	Word length of A, B, and DIFF

Table 1-3 Synthesis Implementations^a

Implementation Name	Function	License Feature Required
rpl	Ripple-carry synthesis model	none
cla	Carry-look-ahead synthesis model	none
pparch	Delay-optimized flexible parallel-prefix	DesignWare

Table 1-3 Synthesis Implementations^a (Continued)

Implementation Name	Function	License Feature Required
apparch	Area-optimized flexible architecture that can be optimized for area, for speed, or for area, speed	DesignWare

a. During synthesis, Design Compiler will select the appropriate architecture for your constraints. However, you may force Design Compiler to use any architectures described in this table. For more, see [DesignWare Building Block IP User Guide](#)

Table 1-4 Obsolete Synthesis Implementations^a

Implementation	Function	Replacement Implementation
clf	Fast carry-look-ahead synthesis model	pparch
bk	Brent-Kung architecture synthesis model	pparch
csm	Conditional-sum synthesis model	pparch
rpcs	Ripple-carry-select architecture	pparch

a. DC versions and DesignWare EST releases linked to DC versions prior to 2007.03 will still include these implementations.

Table 1-5 Simulation Models

Model	Function
DW01.DW01_SUB_CFG_SIM	Design unit name for VHDL simulation
dw/dw01/src/DW01_sub_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW01_sub.v	Verilog simulation model source code

Related Topics

- [Math – Arithmetic Overview](#)
- [DesignWare Building Block IP Documentation Overview](#)

HDL Usage Through Operator Inferencing - VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;

entity DW01_sub_oper is
    generic(wordlength: integer := 8);
    port(in1,in2 : in STD_LOGIC_VECTOR(wordlength-1 downto 0);
         diff : out STD_LOGIC_VECTOR(wordlength-1 downto 0));
end DW01_sub_oper;

architecture oper of DW01_sub_oper is
    signal in1_signed, in2_signed, diff_signed: SIGNED(wordlength-1 downto 0);
begin
    in1_signed <= SIGNED(in1);
    in2_signed <= SIGNED(in2);
    -- infer the "-" subtraction operator
    diff_signed <= in1_signed - in2_signed;
    diff <= STD_LOGIC_VECTOR(diff_signed);
end oper;
```

HDL Usage Through Operator Inferencing - Verilog

```
module DW01_sub_oper(in1,in2,diff);  
    parameter wordlength = 8;  
  
    input [wordlength-1:0] in1,in2;  
    output [wordlength-1:0] diff;  
  
    assign diff = in1 - in2;  
endmodule
```

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW01_sub_inst is
  generic ( inst_width : NATURAL := 8 );
  port ( inst_A      : in std_logic_vector(inst_width-1 downto 0);
        inst_B      : in std_logic_vector(inst_width-1 downto 0);
        inst_CI     : in std_logic;
        DIFF_inst   : out std_logic_vector(inst_width-1 downto 0);
        CO_inst     : out std_logic );
end DW01_sub_inst;

architecture inst of DW01_sub_inst is
begin
  -- Instance of DW01_sub
  U1 : DW01_sub
    generic map ( width => inst_width )
    port map ( A => inst_A,  B => inst_B,  CI => inst_CI,
              DIFF => DIFF_inst,  CO => CO_inst );
end inst;

-- pragma translate_off
configuration DW01_sub_inst_cfg_inst of DW01_sub_inst is
  for inst
    end for; -- inst
end DW01_sub_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW01_sub_inst( inst_A, inst_B, inst_CI, DIFF_inst, CO_inst );

    parameter width = 8;

    input [width-1 : 0] inst_A;
    input [width-1 : 0] inst_B;
    input inst_CI;
    output [width-1 : 0] DIFF_inst;
    output CO_inst;

    // Instance of DW01_sub
    DW01_sub #(width)
        U1 ( .A(inst_A),    .B(inst_B),    .CI(inst_CI),
            .DIFF(DIFF_inst),    .CO(CO_inst) );

endmodule
```

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