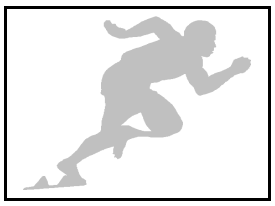

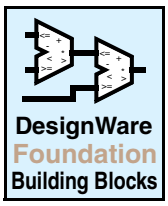

DesignWare Building Block IP QuickStart

The DesignWare Building Block IP product was formally known as DesignWare Foundation Library. The two different terms are still being used interchangeably.

Setting Up DesignWare Building Block IP

Include the following lines in your .synopsys_dc.setup file and ensure that you have a valid DesignWare license.

```
set synthetic_library [list dw_foundation.sldb]
set link_library [concat $target_library $synthetic_library]
set search_path [concat $search_path [list \
   [format "%s%s" $synopsys_root "/dw/sim_ver"]]]
set synlib_wait_for_design_license [list "DesignWare"]
```

Accessing DesignWare Building Block IP

You can access Building Block IP either by operator or functional inference, in some cases, or by instantiating the component directly. The example below shows how to access IP.

```
Verilog
assign PROD = IN1 * IN2; // Operator Inference
assign PROD = mult_tc(IN1, IN2); // Function Inference
DW01_mult #(8, 8) U1 (A, B, TC, PRODUCT); // Instantiation
```

Details about inference and instantiation in VHDL and Verilog are in the following directory: $SYNOPSYS/dw/examples.

Synthesizing DesignWare Building Block IP

Design Compiler automatically selects the best implementation for combinational DesignWare Building Block IP. You can also force Design Compiler to select the implementation of your choice either by adding Synopsys Compiler directives or by using the following commands:

```
dc_shell-t> set_dont_use standard.sldb/DW01_add/rpl
dc_shell-t> set_implementation clf [list add_68]
```

Simulating DesignWare Building Block IP

Synopsys VCS MX simulator uses the default setup file while simulating DesignWare Building Block IP. Use the following options to simulate IP with a Verilog simulator:

```
-y $SYNOPSYS/dw/sim_ver +libext+.v+
```

Technical Support

☎ (800) 245-8005 (toll free in the United States) - support_center@synopsys.com

Further Information

Visit t http://www.synopsys.com/designware

Related Topics

- DesignWare Building Block IP Documentation Overview

Building Block IP in DC FPGA QuickStart

The following topics provide the basic information to get started using the DesignWare Building Block IP with DC FPGA.

Updating Building Block IP for DC FPGA

To get the latest version and receive the best performance, install the Electronic Software Transfer (EST) release of DesignWare Building Block IP from the following location:

http://www.synopsys.com/designware/dwest

If you prefer, you may also send an e-mail to dw_EST@synopsys.com with EST in subject line. In that e-mail, send the following information in the body of the message, in the following format:

<Site Id> <Synopsys Release#>

For example, if your site id is 555 and you want to install the EST for use with the 2004.12 version of the Synopsys Synthesis CD, write the following two fields in the body of the message separated by a few blank spaces:

```
555   2004.12
```

Setting Up DesignWare Building Block IP for DC FPGA

Include the following lines in your .synopsys_dc.setup file and ensure that you have a valid DesignWare Library license:

```
target_library = your_library.db
synthetic_library = {dw_foundation.sldb tmg.sldb}
link_library = target_library + synthetic_library
search_path = search_path + {synopsys_root + "/dw/sim_ver"} \
+ {synopsys_root + "/libraries/syn/"} + { your_library path}
```

Accessing DesignWare Building Block IP in DC FPGA

You can access DesignWare Building Block IP either by operator or functional inference, or by instantiating the component directly. The example below shows how to access these IP:

```
Verilog
assign PROD = IN1 * IN2; // Operator Inference
assign PROD = DWF_mult_tc(IN1, IN2); // Function Inference
DW02_mult #(8, 8) U1 (A, B, TC, PRODUCT); // Instantiation
```

Details about inference and instantiation in VHDL and Verilog are in the following directory: $SYNOPSYS/dw/examples.

Synthesizing DesignWare Building Block IP in DC FPGA

DC FPGA automatically selects the best implementation for combinational DesignWare Building Block IP. You can also force DC FPGA to select the implementation of your choice either by adding Synopsys Compiler directives or by using the following commands:

```
dc_shell> set_dont_use standard.sldb/DW01_add/rpl
dc_shell> set_implementation clf {add_68}
```

Simulating DesignWare Building Block IP

Synopsys VCS simulator uses the default setup file while simulating DesignWare Building Block IP. Use the following options to simulate DesignWare Building Block IP with a Verilog simulator:

```
-y $SYNOPSYS/dw/sim_ver +libext+.v+
```

Related Topics

- DesignWare Building Block IP Documentation Overview

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