

DW02_mult_6_stage

Six-Stage Pipelined Multiplier

Version, STAR and Download Information: [IP Directory](#)

Features and Benefits

- Parameterized word length
- Unsigned and signed (two's-complement) data operation
- Six-stage pipelined architecture
- Automatic pipeline retiming

Description

DW02_mult_6_stage is a six-stage pipelined multiplier. DW02_mult_6_stage multiplies the operand A by B to produce a product (PRODUCT) with a latency of five clock (CLK) cycles.

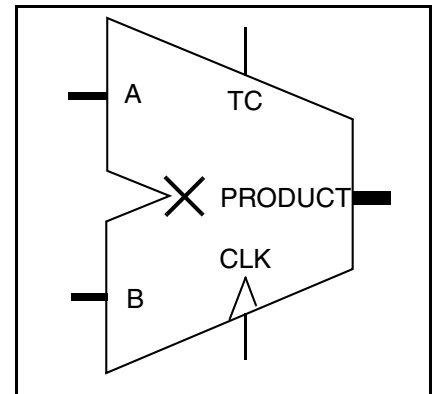


Table 1-1 Pin Description

Pin Name	Width	Direction	Function
A	<i>A_width</i> bit(s)	Input	Multiplier
B	<i>B_width</i> bit(s)	Input	Multiplicand
TC	1 bit	Input	Two's complement 0 = unsigned 1 = signed
CLK	1 bit	Input	Clock
PRODUCT	<i>A_width</i> + <i>B_width</i> bit(s)	Output	Product ($A \times B$)

Table 1-2 Parameter Description

Parameter	Values	Description
<i>A_width</i>	≥ 1	Word length of A
<i>B_width</i>	≥ 1	Word length of B

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
str	Booth-recoded Wallace-tree synthesis model	DesignWare

Table 1-4 Simulation Models

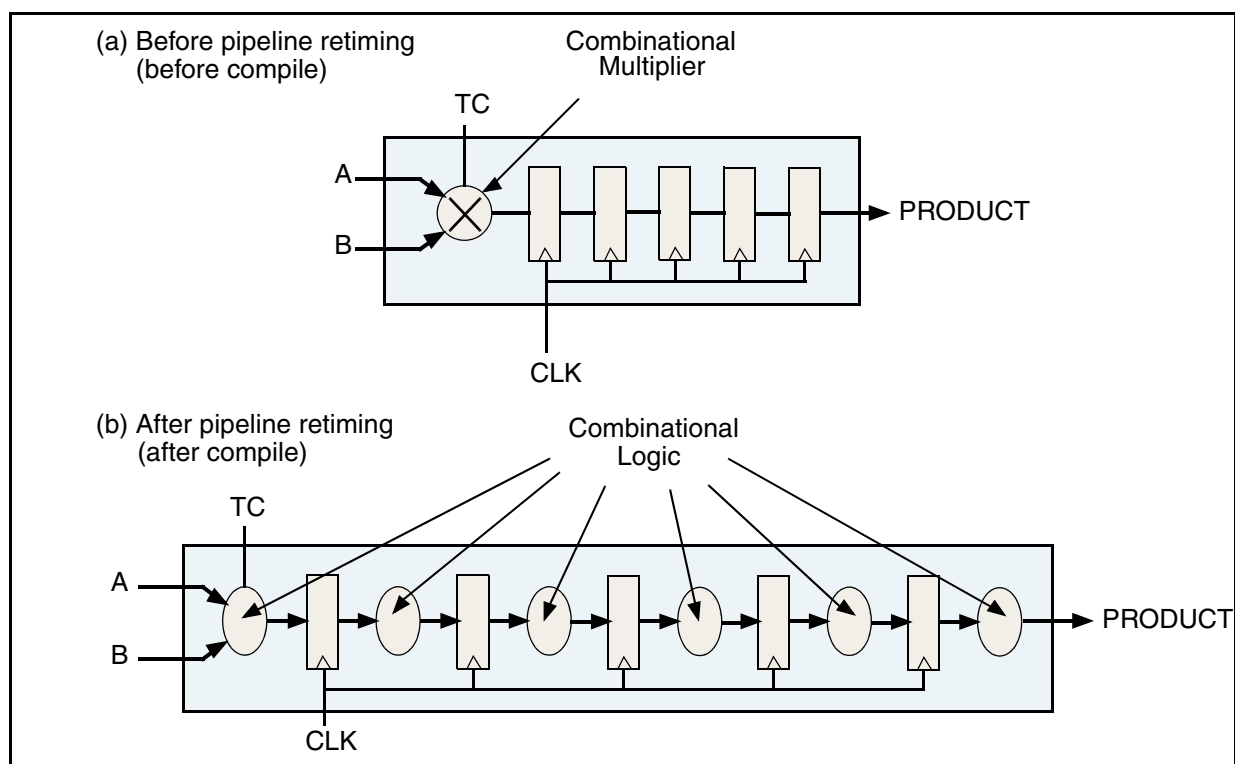
Model	Function
DW02.DW02_MULT_6_STAGE_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW02_mult_6_stage_sim.vhd	VHDL simulation model source code
dw/dw02/src_ver/DW02_mult_6_stage.v	Verilog simulation model source code

The control signal TC determines whether the input and output data is interpreted as unsigned (TC=0) or signed (TC=1) numbers.

Automatic pipeline retiming ensures optimal placement of pipeline registers within the multiplier to achieve maximum throughput.

For more information about DesignWare Building Blocks pipelined multipliers, refer to Application Note [AN 96-002](#).

Figure 1-1 Block Diagram



Related Topics

- [Math – Arithmetic Overview](#)
- [DesignWare Building Block IP Documentation Overview](#)

HDL Usage Through Component Instantiation - VHDL

```

library IEEE,DWARE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW02_mult_6_stage_inst is
  generic ( inst_A_width : POSITIVE := 8;
            inst_B_width : POSITIVE := 8 );
  port ( inst_A : in std_logic_vector(inst_A_width-1 downto 0);
        inst_B : in std_logic_vector(inst_B_width-1 downto 0);
        inst_TC : in std_logic;
        inst_CLK : in std_logic;
        PRODUCT_inst : out std_logic_vector(inst_A_width+inst_B_width-1 downto 0)
        );
end DW02_mult_6_stage_inst;

architecture inst of DW02_mult_6_stage_inst is
begin

  -- Instance of DW02_mult_6_stage
  U1 : DW02_mult_6_stage
    generic map ( A_width => inst_A_width, B_width => inst_B_width )
    port map ( A => inst_A,   B => inst_B,   TC => inst_TC,
              CLK => inst_CLK,   PRODUCT => PRODUCT_inst );
end inst;

-- pragma translate_off
configuration DW02_mult_6_stage_inst_cfg_inst of DW02_mult_6_stage_inst is
  for inst
    end for; -- inst
end DW02_mult_6_stage_inst_cfg_inst;
-- pragma translate_on

```

HDL Usage Through Component Instantiation - Verilog

```
module DW02_mult_6_stage_inst( inst_A, inst_B, inst_TC,
                              inst_CLK, PRODUCT_inst );

    parameter A_width = 8;
    parameter B_width = 8;

    input [A_width-1 : 0] inst_A;
    input [B_width-1 : 0] inst_B;
    input inst_TC;
    input inst_CLK;
    output [A_width+B_width-1 : 0] PRODUCT_inst;

    // Instance of DW02_mult_6_stage
    DW02_mult_6_stage #(A_width, B_width)
        U1 ( .A(inst_A),    .B(inst_B),    .TC(inst_TC),
            .CLK(inst_CLK),    .PRODUCT(PRODUCT_inst) );

endmodule
```

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