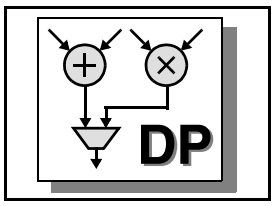

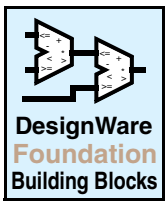

DWF_dp_mult_comb_sat function

Combined Unsigned/Signed Multiply and Saturate

Version, STAR and Download Information: IP Directory

Description

The DWF_dp_mult_comb_sat function performs combined (switchable) unsigned/signed multiplication of the two arguments `a` and `b`, truncates the upper bits of the result to the width specified by argument *p_width* and returns a saturated value if an overflow (or underflow) occurs. Argument `a` (`b`) is interpreted as signed if argument `a_tc` (`b_tc`) is 1, otherwise as unsigned. The result must be interpreted as signed if argument **`a_tc`** or `b_tc` (or both) is 1 (= signed multiplication), otherwise as unsigned (= unsigned multiplication). A dedicated overflow detection (needed for saturation) is used to improve QoR of the multiplier.

Table 1-1 Function Names

Function Name	Description
DWF_dp_mult_comb_sat	VHDL combined multiply and saturate (std_logic_vector/unsigned/signed arguments)
DWF_dp_mult_comb_sat	Verilog combined multiply and saturate
DWF_dp_mult_comb_sat_tc	Verilog combined multiply and saturate (signed arguments)

Table 1-2 Argument Description

Name	Type	Direction	Width / Values	Description
a	Vector	Input	*a_width*	Input multiplier
a_tc	Bit	Input	1	Two's complement control for multiplier 0 = unsigned, 1 = signed
b	Vector	Input	*b_width*	Input multiplicand
b_tc	Bit	Input	1	Two's complement control for multiplicand 0 = unsigned, 1 = signed
p_width	Integer	Input	≥ 2	Word length of return value (VHDL only, constant)
DWF_dp_mult_comb_sat	Vector	Output	*p_width*	Returned value

Table 1-3 Parameter Description (Verilog)

Parameter	Values	Description
a_width	≥ 2	Word length of input `a`
b_width	≥ 2	Word length of input `b`
p_width	≥ 2	Word length of returned value

Verilog Include File: DW_dp_mult_comb_sat_function.inc

Functional Description

```
z[p_width-1:0] = DWF_dp_mult_comb_sat (a[a_width-1:0], a_tc, b[b_width-1:0], b_tc, p_width)

p[a_width+b_width-1:0] (unsigned)  = a (unsigned) * b (unsigned)    if a_tc = 0 and b_tc = 0

p[a_width+b_width-1:0] (signed)    = a (signed)   * b (unsigned)    if a_tc = 1 and b_tc = 0
                                   = a (unsigned) * b (signed)      if a_tc = 0 and b_tc = 1
                                   = a (signed)   * b (signed)      if a_tc = 1 and b_tc = 1

z[p_width-1:0] = 2p_width-1         if      (a_tc = 0 and b_tc = 0) and
                                         (p[a_width+b_width-1:0] > 2p_width-1)
               = 2p_width-1-1        else if (a_tc = 1 or b_tc = 1) and
                                         (p[a_width+b_width-1:0] > 2p_width-1-1)
               = -2p_width-1         else if (a_tc = 1 or b_tc = 1) and
                                         (p[a_width+b_width-1:0] < -2p_width-1)
               = p[p_width-1:0]  else
```

For more information about the DesignWare datapath functions, refer to the topic titled DesignWare Datapath Functions Overview.

Related Topics

- DesignWare Datapath Functions Overview
- DesignWare Building Block IP Documentation Overview

VHDL Example

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

entity DWF_dp_mult_comb_sat_test is
  port (a, b, c    : in  unsigned(7 downto 0);
        a_tc, b_tc : in  std_logic;
        z          : out unsigned(7 downto 0));
end DWF_dp_mult_comb_sat_test;

architecture rtl of DWF_dp_mult_comb_sat_test is
begin
  z <= DWF_dp_mult_comb_sat (a, a_tc, b, b_tc, 8) + c;
end rtl;
```

Verilog Example

```
module DWF_dp_mult_comb_sat_test (a, a_tc, b, b_tc, c, z);

  input  signed [7:0] a, b, c;
  input               a_tc, b_tc;
  output signed [7:0] z;

  // Passes the parameters to the function
  parameter a_width = 8;
  parameter b_width = 8;
  parameter p_width = 8;

  // add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
  `include "DW_dp_mult_comb_sat_function.inc"

  assign z = DWF_dp_mult_comb_sat (a, a_tc, b, b_tc) + c;

endmodule
```

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