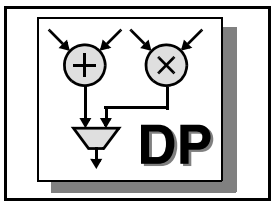

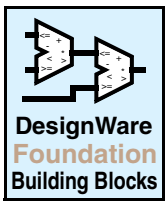

DWF_dp_sat functions

Arithmetic Saturation

Version, STAR and Download Information: IP Directory

Description

The DWF_dp_sat functions truncate the upper bits of argument `a` to the width specified by argument `size` and returns a saturated value if an overflow (or underflow) occurs. Argument `a` and the return value are both either signed (two's complement) or unsigned.

The DWF_dp_sati functions have the same functionality, except that all output bits are inverted.

Table 1-1 Function Names

Function Name	Description
DWF_dp_sat	VHDL unsigned saturate
DWF_dp_sat	VHDL signed (two's complement) saturate
DWF_dp_sat_uns	Verilog unsigned saturate
DWF_dp_sat_tc	Verilog signed (two's complement) saturate
DWF_dp_sati	VHDL unsigned saturate, inverted output
DWF_dp_sati	VHDL signed (two's complement) saturate, inverted output
DWF_dp_sati_uns	Verilog unsigned saturate, inverted output
DWF_dp_sati_tc	Verilog signed (two's complement) saturate, inverted output

Table 1-2 Argument Description

Argument Name	Type	Width / Values	Description
a	Vector	width	Input data
size	Integer	> 1, < width	Word length of return value (VHDL only, constant)
DWF_dp_sat DWF_dp_sati	Vector	size	Return value

Table 1-3 Parameter Description (Verilog)

Parameter	Values	Description
width	≥ 1	Word length of input `a`
size	> 1, < width	Word length of return value

Verilog Include File: DW_dp_sat_function.inc

Functional Description

```
z[size-1:0] = DWF_dp_sat (a[width-1:0], size)
```

Unsigned Saturate

$$z[size-1:0] = \begin{cases} 2^{size}-1 & \text{if } a[width-1:0] > 2^{size}-1 \\ a[size-1:0] & \text{else} \end{cases}$$

Signed Saturate

$$z[size-1:0] = \begin{cases} 2^{size-1}-1 & \text{if } a[width-1:0] > 2^{size-1}-1 \\ -2^{size-1} & \text{else if } a[width-1:0] < -2^{size-1} \\ a[size-1:0] & \text{else} \end{cases}$$

Unsigned Saturate, inverted output

```
z[size-1:0] = ~ DWF_dp_sat (a[width-1:0], size)
```

Signed Saturate, inverted output

```
z[size-1:0] = ~ DWF_dp_sat (a[width-1:0], size)
```

For more information about the DesignWare datapath functions, refer to the topic titled DesignWare Datapath Functions Overview.

Related Topics

- DesignWare Datapath Functions Overview
- DesignWare Building Block IP Documentation Overview

VHDL Example

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

entity DWF_dp_sat_test is
  port (a, b, c : in  signed(7 downto 0);
        z       : out signed(7 downto 0));
end DWF_dp_sat_test;

architecture rtl of DWF_dp_sat_test is
begin
  z <= DWF_dp_sat (a * b, 8) + c;
end rtl;
```

Verilog Example

```
module DWF_dp_sat_test (a, b, c, z);

  input  signed [7:0] a, b, c;
  output signed [7:0] z;

  // Passes the parameters to the function
  parameter width = 16;
  parameter size  = 8;

  // add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
  `include "DW_dp_sat_function.inc"

  assign z = DWF_dp_sat_tc (a * b) + c;

endmodule
```

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