



# Memory – Registers Overview

This section documents the following memory registers found in the DesignWare Building Block IP:

**Table 1-1**      **Memory Registers**

IP	Description
<a href="#">DW03_pipe_reg</a>	Pipeline Register
<a href="#">DW03_reg_s_pl</a>	Register with Synchronous Enable Reset
<a href="#">DW03_shftreg</a>	Shift Register
<a href="#">DW04_shad_reg</a>	Shadow and Multibit Register
<a href="#">DW_pl_reg</a>	Pipeline Register

## Related Topics

For a listing of Building Block components and associated datasheets, see:

- [DesignWare Building Block IP Documentation Overview](#)

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