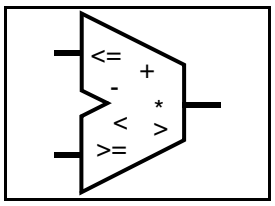

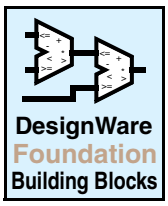

Basic IP Library Overview

Synopsys provides a collection of IP, referred to as the Basic IP Library, as part of the HDL Compiler products. Basic IP provide basic implementations of common arithmetic functions that can be referenced by HDL operators in your VHDL or Verilog source code.

In addition, Synopsys offers the DesignWare Building Block IP, which is sold as a separate product. The DesignWare Building Block IP provides 100 components and 160 architectures that are not available in the Basic IP Library, including higher performance implementations of most components offered in the Basic IP Library. The licensed, high-performance components in the DesignWare Building Block IP offer enhanced synthesis results, based on your design constraints.

Table 1-1 lists the Basic IP and their corresponding DesignWare Building Block IP implementations. For example, DW02_mult has three available implementations: the carry save array (csa) multiplier in the Basic IP Library; the high-performance Wallace tree (wall) multiplier; and the non-Booth-coded Wallace tree synthesis model (nbw) licensed in the Advanced Math Family DesignWare Building Block IP. Because each performs multiply operations, the same component name is used, and the same datasheet describes the implementations. For detailed information about each component, refer to the associated datasheet.

Table 1-1 Basic Library IP

IP	Basic Library Implementations	Operator / Function[a]	DesignWare Building Block Implementation
DW01_absval Absolute Value	Ripple (rpl)	DW_absval	Fast Carry Look-Ahead (clf)
	Carry Look-Ahead (cla)		
DW01_add Adder	Ripple (rpl)	+	Fast Carry Look-Ahead (clf), Brent-Kung architecture (bk), Conditional Sum (csm)
	Carry Look-Ahead (cla)		
DW01_addsub Adder-Subtractor	Ripple (rpl)	+, –	Fast Carry Look-Ahead (clf), Brent-Kung architecture (bk), Conditional Sum (csm)
	Carry Look-Ahead (cla)		
DW01_ash Arithmetic Shifter	2:1 multiplexer (mx2)	<<, >>	2:1 inverting mux (mx2i), 2:1 non-inverting mux (mx2n), 4:1 and 2:1 mux (mx4), 8:1, 4:1, and 2:1 mux (mx8), Synthesis model (str, astr)
DW01_cmp2 2-Function Comparator	Ripple (rpl)	<, >	Fast Carry Look-Ahead (clf), Brent-Kung architecture (bk)
DW01_cmp6 6-Function Comparator	Ripple (rpl)	<, >, <=, >=	Fast Carry Look-Ahead (clf), Brent-Kung architecture (bk)

Table 1-1 Basic Library IP (Continued)

IP	Basic Library Implementations	Operator / Function[a]	DesignWare Building Block Implementation
DW01_dec Decrementer	Ripple (rpl)	–	Fast Carry Look-Ahead (clf)
	Carry Look-Ahead (cla)		
DW01_decode Binary Decoder	Structural (str)	None	None
DW01_inc Incrementer	Ripple (rpl)	+	Fast Carry Look-Ahead (clf)
	Carry Look-Ahead (cla)		
DW01_incdec Incrementer-Decrementer	Ripple (rpl)	+, –	Fast Carry Look-Ahead (clf)
	Carry Look-Ahead (cla)		
DW01_sub Subtractor	Ripple (rpl)	–	Fast Carry Look-Ahead (clf), Brent-Kung architecture (bk), Conditional Sum (csm)
	Carry Look-Ahead (cla)		
DW02_mult Multiplier	Carry Save Array (csa)	*	Non-Booth-recoded Wallace (nbw), Wallace Tree (wall)

a. Operators, such as “+”, indicate the operator in both Verilog and VHDL from which this IP can be inferred. Function names, such as DW_absval, refer to VHDL functions from which this IP can be inferred.

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