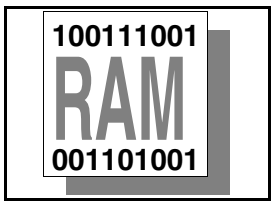

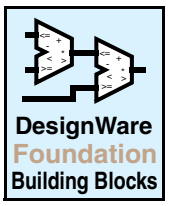

Memory – Synchronous RAMs

The following IP comprise the memory synchronous RAMs:

Table 1-1 Synchronous RAM Memory

IP	Description
DW_ram_r_w_s_dff	Synchronous Write-Port, Asynchronous Read-Port RAM (Flip-Flop-Based)
DW_ram_r_w_s_lat	Synchronous Write-Port, Asynchronous Read-Port RAM (Latch-Based)
DW_ram_2r_2w_s_dff	Synchronous Dual Write-Port, Asynchronous Dual Read-Port RAM (Flip-Flop-Based)
DW_ram_2r_w_s_dff	Synchronous Write-Port, Asynchronous Dual Read-Port RAM (Flip-Flop-Based)
DW_ram_2r_w_s_lat	Synchronous Write-Port, Asynchronous Dual Read-Port RAM (Latch-Based)
DW_ram_rw_s_dff	Synchronous Single-Port, Read/Write RAM (Flip-Flop-Based)
DW_ram_rw_s_lat	Synchronous Single-Port, Read/Write RAM (Latch-Based)
DW_ram_r_w_a_dff	Asynchronous Dual-Port RAM (Flip-Flop-Based)
DW_ram_r_w_a_lat	Asynchronous Dual-Port RAM (Latch-Based)
DW_ram_2r_w_a_dff	Write-Port, Dual-Read-Port RAM (Flip-Flop-Based)
DW_ram_2r_w_a_lat	Write-Port, Dual-Read-Port RAM (Latch-Based)
DW_ram_rw_a_dff	Asynchronous Single-Port RAM (Flip-Flop-Based)
DW_ram_rw_a_lat	Asynchronous Single-Port RAM (Latch-Based)

Related Topics

- DesignWare Building Block IP Documentation Overview

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