DesignWare

Building Block IP

Documentation Overview

DWBB_201806.0
O-2018.06
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Documentation Overview

DesignWare Building Block IP comprise a technology-independent, microarchitecture-level library that is tightly integrated into the Synopsys synthesis environment. This product was formally known as the DesignWare Foundation Library. A more complete introduction is available in *DesignWare Building Block IP Introduction*.

The following sections list the entire documentation set and datasheets that supports this library:

- "DesignWare Building Block IP Document List" on page 3
- "List of DesignWare Building Block IP" on page 5
- "Obsoleted IP for New Designs" on page 14
  Note: This information is now found in the Release Notes.

1.1 DesignWare Building Block IP Document List

Table 1-1 DesignWare Building Block IP Documentation

DesignWare Building Block IP Release Notes	Contains usage issues for DesignWare Building Block IP Library components (DWBB_201806.0) for Design Compiler O-2018.06.
DesignWare Building Block IP QuickStart	Provides a quick look-up list of things you need to know to get started with the library of DesignWare Building Block IP.
Basic Library Components Overview	Describes the Basic Library components, which provide basic implementations of common arithmetic and combinational logic functions that can be referenced by HDL operators in your VHDL or Verilog source code.
DesignWare Building Block IP User Guide	Explains the use of DesignWare Building Block IP.
DesignWare Building Block IP Application Notes	A compilation of Application Notes that support the DesignWare Building Block IP.
DesignWare Building Block IP Developer Guide	This manual is for silicon suppliers, systems companies, and third party macro and model developers who want to develop technology-specific designs or proprietary components.
Designware GTECH Library Databook	Provides detailed datasheets for the GTECH Library components.
DesignWare Interface and Standards IP Quick Reference Guide	Provides a catalog of information for most DesignWare IP products.

1.2 DesignWare minPower Components Documentation

NOTE: DesignWare minPower Components documentation is available on the Synopsys website, and requires access authentication.

Table 1-2 DesignWare minPower Components Documentation

DesignWare minPower Components Documentation Overview	Lists the minPower Components documentation, which provide Low Power implementations of common arithmetic functions.
DesignWare minPower Components DC Release Notes	Contains usage issues for DesignWare minPower Components (O-2018.06) for Design Compiler DWBB_201806.0.
DesignWare minPower Components User Guide	Explains the use of DesignWare minPower Components.
DesignWare minPower Components Overview	A listing and brief description of the DesignWare minPower Components. Use this document to access minPower Component datasheets.

1.3 Synopsys Common Licensing (SCL)

You can find general SCL information on the following page:

http://www.synopsys.com/keys

1.4 Additional Information

For additional Synopsys documentation, refer to the following location:

http://www.synopsys.com/dw/dwlibdocs.php

For up-to-date information about the latest verification models and synthesizable IP available from Synopsys, visit the DesignWare IP website:

http://www.synopsys.com/IP

1.4.1 List of DesignWare Building Block IP

The following table provides links to each datasheet. For information about DesignWare Building Block (DWBB) IP that are obsolete for new designs, see "Obsoleted IP for New Designs" on page 14.

Table 1-3 List of DesignWare Building Block IP

IP	Inference Supported?	Description
Application Specific: Control Logic (Overview)		
DW_arb_2t	No	Two-Tier Arbiter with Dynamic/Fair-Among-Equal Scheme
DW_arb_dp	No	Arbiter with Dynamic Priority Scheme
DW_arb_fcfs	No	Arbiter with First-Come-First-Served Priority Scheme
DW_arb_rr	No	Arbiter with Round Robin Priority Scheme
DW_arb_sp	No	Arbiter with Static Priority Scheme
Datapath: Arithmetic Components (Overview)		
DW01_absval	Function	Absolute Value
DW01_add	Operator	Adder
DW01_addsub	Operator	Adder-Subtractor
DW_addsub_dx	No	Duplex Adder/Subtractor with Saturation and Rounding
DW01_ash	Function	Arithmetic Shifter
DW_bin2gray	Function	Binary to Gray Converter
DW01_bsh	Function	Barrel Shifter
DW01_cmp2	Operator	2-Function Comparator
DW01_cmp6	No	6-Function Comparator

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Inference Supported?	Description
DW_cmp_dx	No	Duplex Comparator
DW_cntr_gray	No	Gray Code Counter
DW01_csa	No	Carry Save Adder
DW01_dec	Operator	Decrementer
DW_div	Function/Operator	Combinational Divider
DW_div_sat	Function	Combinational Divider with Saturation
DW_div_pipe	No	Stallable Pipelined Divider
DW_exp2	No	Base 2 Exponential (2a)
DW_gray2bin	No	Gray to Binary Converter
DW01_inc	Operator	Incrementer
DW01_incdec	Operator	Incrementer-Decrementer
DW_inc_gray	Function	Gray Incrementer
DW_inv_sqrt	No	Reciprocal of Square-Root
DW_lbsh	Function	Barrel Shifter with Preferred Left Direction
DW_ln	No	Natural Logarithm (ln(a))
DW_log2	No	Base 2 Logarithm ($\log_2$(a))
DW02_mac	Function	Multiplier-Accumulator
DW_minmax	Function	Minimum/Maximum Value
DW02_mult	Function*/Operator	Multiplier * Does not support function inference for VHDL
DW02_multp	No	Partial Product Multiplier
DW02_mult_2_stage	No	Two-Stage Pipelined Multiplier
DW02_mult_3_stage	No	Three-Stage Pipelined Multiplier
DW02_mult_4_stage	No	Four-Stage Pipelined Multiplier
DW02_mult_5_stage	No	Five-Stage Pipelined Multiplier
DW02_mult_6_stage	No	Six-Stage Pipelined Multiplier
DW_mult_dx	No	Duplex Multiplier
DW_mult_pipe	No	Stallable Pipelined Multiplier
DW_norm	No	Normalization for Fractional Input

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Inference Supported?	Description
DW_norm_rnd	No	Normalization and Rounding
DW_piped_mac	No	Pipelined Multiplier-Accumulator
DW02_prod_sum	No	Generalized Sum of Products
DW02_prod_sum1	No	Multiplier-Adder
DW_prod_sum_pipe	No	Stallable Pipelined Generalized Sum of Products
DW_rash	Function	Arithmetic Shifter with Preferred Right Direction
DW_rbsh	Function	Barrel Shifter with Preferred Right Direction
DW01_satrnd	No	Arithmetic Saturation and Rounding Logic
DW_shifter	Function	Combined Arithmetic and Barrel Shifter
DW_sla	No	Arithmetic Shifter with Preferred Left Direction (VHDL style)
DW_sra	No	Arithmetic Shifter with Preferred Right Direction (VHDL style)
DW_square	Function	Integer Squarer
DW_squarep	No	Partial Product Integer Squarer
DW_sqrt	Function/Operator*	Combinational Square Root * Does not support operator inference for Verilog
DW_sqrt_pipe	No	Stallable Pipelined Square Root
DW01_sub	Operator	Subtractor
DW02_sum	Function	Vector Adder
DW02_tree	No	Wallace Tree Compressor
Datapath: Floating Point (Overview)		
DW_fp_add	No	Floating Point Adder
DW_fp_addsub	No	Floating Point Adder/Subtractor
DW_fp_cmp	No	Floating Point Comparator
DW_fp_div	No	Floating Point Divider
DW_fp_div_seq	No	Floating Point Sequential Divider
DW_fp_dp2	No	2-Term Floating Point Dot-product
DW_fp_dp3	No	3-Term Floating Point Dot-product
DW_fp_dp4	No	4-Term Floating Point Dot-product
DW_fp_exp	No	Floating Point Exponential (e^a)

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Inference Supported?	Description
DW_fp_exp2	No	Floating Point Base-2 Exponential (2a)
DW_fp_flt2i	No	Floating Point to Integer Converter
DW_fp_i2flt	No	Integer to Floating Point Converter
DW_fp_invsqrt	No	Floating Point Reciprocal of Square Root
DW_fp_ln	No	Floating Point Natural Logarithm (ln(a))
DW_fp_log2	No	Floating Point Base 2 Logarithm ($\log_2$(a))
DW_fp_mac	No	Floating Point Multiply-and-Add
DW_fp_mult	No	Floating Point Multiplier
DW_fp_recip	No	Floating Point Reciprocal (1/a)
DW_fp_sincos	No	Floating Point Sine and Cosine
DW_fp_sqrt	No	Floating Point Square Root
DW_fp_square	No	Floating Point Square
DW_fp_sub	No	Floating Point Subtractor
DW_fp_sum3	No	3-input Floating Point Adder
DW_fp_sum4	No	4-input Floating Point Adder
Datapath: Sequential (Overview)		
DW_div_seq	No	Sequential Divider
DW_fp_div_seq	No	Floating Point Sequential Divider
DW_mult_seq	No	Sequential Multiplier
DW_sqrt_seq	No	Sequential Square Root
Datapath: Trigonometric (Overview)		
DW_sincos	No	Combinational Sine - Cosine
Data Integrity (Overview)		
DW_crc_p	No	Universal Parallel (Combinational) CRC Generator/Checker
DW_crc_s	No	Universal Synchronous (Clocked) CRC Generator/Checker
DW_ecc	No	Error Checking and Correction
DW04_par_gen	Function*	Parity Generator and Checker * Does not support function inference for Verilog

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Inference Supported?	Description
Data Integrity: Coding (Overview)		
DW_8b10b_dec	No	8b10b Decoder
DW_8b10b_enc	No	8b10b Encoder
DW_8b10b_unbal	No	8b10b Coding Balance Predictor
Digital Signal Processing (DSP) (Overview)		
DW_fir	No	High-Speed Digital FIR Filter
DW_fir_seq	No	Sequential Digital FIR Filter Processor
DW_iir_dc	No	High-Speed Digital IIR Filter with Dynamic Coefficients
DW_iir_sc	No	High-Speed Digital IIR Filter with Static Coefficients
DW_dct_2d	No	Two Dimensional Discreet Cosine Transform
DW_decode_en	No	Binary Decoder with Enable
DW_thermdec	No	Binary Thermometer Decoder and Enable
Interface: Clock Domain Crossing (Overview)		
DW_data_qsync_hl	No	Quasi-Synchronous Data Interface for H-to-L Frequency Clocks
DW_data_qsync_lh	No	Quasi-Synchronous Data Interface for L-to-H Frequency Clocks
DW_data_sync	No	Data Bus Synchronizer with Acknowledge
DW_data_sync_na	No	Data Bus Synchronizer without Acknowledge
DW_data_sync_1c	No	Single Clock Filtered Data Bus Synchronizer
DW_fifo_2c_df	No	Dual independent clock FIFO
DW_fifo_s2_sf	No	Synchronous (Dual-Clock) FIFO with Static Flags
DW_fifoctl_2c_df	No	Family of FIFO Controllers with Dynamic Flags
DW_fifoctl_s2_sf	No	Synchronous (Dual-Clock) FIFO Controller with Static Flags
DW_gray_sync	No	Gray Coded Synchronizer
DW_pulse_sync	No	Dual Clock Pulse Synchronizer
DW_pulseack_sync	No	Pulse Synchronizer with Acknowledge
DW_reset_sync	No	Reset Sequence Synchronizer
DW_stream_sync	No	Data Stream Synchronizer

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Inference Supported?	Description
DW_sync	No	Single Clock Data Bus Synchronizer
Logic: Combinational Components (Overview)		
DW01_binenc	Function	Binary Encoder
DW01_bsh	Function	Barrel Shifter
DW01_decode	Function	Decoder
DW_lod	Function	Leading One's Detector
DW_lsd	Function	Leading Signs Detector
DW_lza	Function	Leading Zero's Anticipator
DW_lzd	Function	Leading Zero's Detector
DW01_mux_any	No	Universal Multiplexer
DW_pricod	Function	Priority Coder
DW01_prienc	Function	Priority Encoder
Logic: Sequential Components (Overview)		
DW03_bictr_dcnto	No	Up/Down Binary Counter with Dynamic Count-to Flag
DW03_bictr_scnto	No	Up/Down Binary Counter with Static Count-to Flag
DW03_bictr_decode	No	Up/Down Binary Counter with Output Decode
DW_dpll_sd	No	Digital Phase Locked Loop
DW03_lfsr_dcnto	No	LFSR Counter with Dynamic Count-to Flag
DW03_lfsr_scnto	No	LFSR Counter with Static Count-to Flag
DW03_lfsr_load	No	LFSR Counter with Loadable Input
DW03_lfsr_updn	No	LFSR Up/Down Counter
DW03_updn_ctr	No	Up/Down Counter

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Inference Supported?	Description
Memory: FIFO (Overview)		
DW_asymdata_inbuf	No	Asymmetric Data Input Buffer
DW_asymdata_outbuf	No	Asymmetric Data Output Buffer
DW_asymfifo_s1_df	No	Asymmetric I/O Synchronous (Single Clock) FIFO with Dynamic Flags
DW_asymfifo_s1_sf	No	Asymmetric I/O Synchronous (Single Clock) FIFO with Static Flags
DW_asymfifo_s2_sf	No	Asymmetric Synchronous (Dual-Clock) FIFO with Static Flags
DW_fifo_2c_df	No	Dual independent clock FIFO
DW_fifo_s1_df	No	Synchronous (Single Clock) FIFO with Dynamic Flags
DW_fifo_s1_sf	No	Synchronous (Single Clock) FIFO with Static Flags
DW_fifo_s2_sf	No	Synchronous (Dual-Clock) FIFO with Static Flags
Memory: FIFO Controllers		
DW_asymfifoctl_s1_df	No	Asymmetric I/O Synchronous (Single Clock) FIFO Controller with Dynamic Flags
DW_asymfifoctl_s1_sf	No	Asymmetric I/O Synchronous (Single Clock) FIFO Controller with Static Flags
DW_asymfifoctl_s2_sf	No	Asymmetric Synchronous (Dual-Clock) FIFO Controller with Static Flags
DW_asymfifoctl_2c_df	No	Asymmetric Dual-Clock FIFO Controller with Dynamic Flags
DW_fifoctl_2c_df	No	Family of FIFO Controllers with Dynamic Flags
DW_fifoctl_s1_df	No	Synchronous (Single Clock) FIFO Controller with Dynamic Flags
DW_fifoctl_s1_sf	No	Synchronous (Single-Clock) FIFO Controller with Static Flags
DW_fifoctl_s2_sf	No	Synchronous (Dual-Clock) FIFO Controller with Static Flags

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Inference Supported?	Description
Memory: Registers (Overview)		
DW03_pipe_reg	No	Pipeline Register
DW_pl_reg	No	Pipeline Register
DW03_reg_s_pl	No	Register with Synchronous Enable Reset
DW03_shftreg	No	Shift Register
DW04_shad_reg	No	Shadow and Multi-bit Register
Memory: SRAMs		
DW_ram_r_w_s_dff	No	Synchronous Write-Port, Asynchronous Read-Port RAM (Flip-Flop-Based)
DW_ram_r_w_s_lat	No	Synchronous Write-Port, Asynchronous Read-Port RAM (Latch-Based)
DW_ram_2r_2w_s_dff	No	Synch. Dual Write-Port, Async Dual Read-Port RAM (Flip-Flop-Based)
DW_ram_2r_w_s_dff	No	Synchronous Write-Port, Async Dual Read-Port RAM (Flip-Flop-Based)
DW_ram_2r_w_s_lat	No	Synchronous Write-Port, Async Dual Read-Port RAM (Latch-Based)
DW_ram_rw_s_dff	No	Synchronous Single-Port, Read/Write RAM (Flip-Flop-Based)
DW_ram_rw_s_lat	No	Synchronous Single-Port, Read/Write RAM (Latch-Based)
DW_ram_r_w_a_dff	No	Asynchronous Dual-Port RAM (Flip-Flop-Based)
DW_ram_r_w_a_lat	No	Asynchronous Dual-Port RAM (Latch-Based)
DW_ram_2r_w_a_dff	No	Write-Port, Dual-Read-Port RAM (Flip-Flop-Based)
DW_ram_2r_w_a_lat	No	Write-Port, Dual-Read-Port RAM (Latch-Based)
DW_ram_rw_a_dff	No	Asynchronous Single-Port RAM (Flip-Flop-Based)
DW_ram_rw_a_lat	No	Asynchronous Single-Port RAM (Latch-Based)
Memory: Stacks		
DW_stack	No	Synchronous (Single-Clock) Stack
DW_stackctl	No	Synchronous (Single Clock) Stack Controller
Test: JTAG (Overview)		
DW_tap	No	TAP Controller

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Inference Supported?	Description
DW_tap_uc	No	TAP Controller with USERCODE Support
DW_bc_1	No	Boundary Scan Cell Type BC_1
DW_bc_2	No	Boundary Scan Cell Type BC_2
DW_bc_3	No	Boundary Scan Cell Type BC_3
DW_bc_4	No	Boundary Scan Cell Type BC_4
DW_bc_5	No	Boundary Scan Cell Type BC_5
DW_bc_7	No	Boundary Scan Cell Type BC_7
DW_bc_8	No	Boundary Scan Cell Type BC_8
DW_bc_9	No	Boundary Scan Cell Type BC_9
DW_bc_10	No	Boundary Scan Cell Type BC_10
Datapath Functions (Overview)		
DWF_dp_absval	Function	Returns the absolute value (magnitude) of an argument
DWF_dp_blend	Function	Implements an alpha blender or linear interpolator
DWF_dp_count_ones	Function	Performs ones count in argument
DWF_dp_mult_comb	Function	Performs a combined unsigned/signed multiply
DWF_dp_mult_comb_offldet	Function	Performs a combined unsigned/signed multiply and overflow detection
DWF_dp_mult_comb_sat	Function	Performs a combined unsigned/signed multiply and saturation
DWF_dp_mult_ovfldet	Function	Performs a multiplication with overflow detection
DWF_dp_mult_sat	Function	Performs a multiplication and saturation
DWF_dp_rnd	Function	Performs arithmetic rounding
DWF_dp_rndsat	Function	Performs arithmetic rounding and saturation
DWF_dp_sat	Function	Performs arithmetic saturation
DWF_dp_sign_select	Function	Performs sign selection / conditional two's complement

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Inference Supported?	Description
DWF_dp_simd_add	Function	Implements SIMD adder
DWF_dp_simd_addc	Function	Implements SIMD adder with carry
DWF_dp_simd_mult	Function	Implements SIMD multiplier
DWF_dp_sub_abs	Function	Performs a subtraction and returns its absolute value (magnitude)

1.4.2 Obsoleted IP for New Designs

For information on DesignWare Building Block IP that is in the process of being obsoleted, refer to "Obsoleted IP for New Designs" in the *DesignWare Building Block IP Release Notes*.