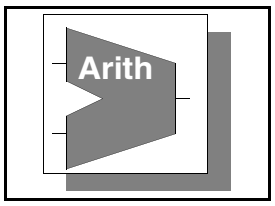
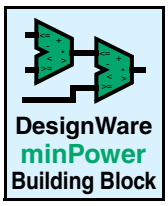




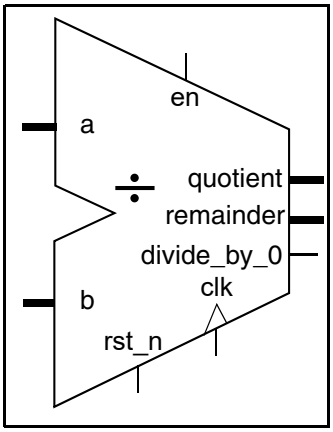
DW_div_pipe

Stallable Pipelined Divider

Version, STAR and Download Information: IP Directory

Features and Benefits

- Parameterized word length
- Parameterized unsigned and signed data operation
- Parameterized number of pipeline stages
- Parameterized stall mode (stallable or non-stallable)
- Parameterized reset mode (no reset, asynchronous or synchronous reset)
- Automatic pipeline retiming
- Provides minPower benefits with the DesignWare-LP license (Get the minPower version of this datasheet.)



Description

DW_div_pipe is a universal stallable pipelined divider with optional low-power benefits. It contains the DW_div component to perform the division, and additional pipelining register logic and timing.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
clk	1 bit	Input	Input clock
rst_n	1 bit	Input	Reset, active-low (not used if parameter *rst_mode*=0)
en	1 bit	Input	Register enable, active high (used only if parameter *stall_mode*=1) 0 = stall 1 = enable register
a	*a_width* bit(s)	Input	Dividend
b	*b_width* bit(s)	Input	Divisor
quotient	*a_width* bit(s)	Output	Quotient `a` / `b`
remainder	*b_width* bit(s)	Output	Remainder
divide_by_0	1 bit	Output	Indicates if `b` equals zero

Table 1-2 Parameter Description

Parameter	Values	Description
a_width	≥ 2 Default: None	Word length of `a`
b_width	≥ 2 Default: None	Word length of `b`
tc_mode	0 or 1 Default: 0	Two's complement control 0 = unsigned 1 = signed
rem_mode	0 or 1 Default: 1	Remainder output control 0 = modulus 1 = remainder
num_stages	≥ 2 Default: 2	Number of pipeline stages
stall_mode	0 or 1 Default: 1	Stall mode 0 = non-stallable 1 = stallable
rst_mode	0 to 2 Default: 1	Reset mode 0 = no reset 1 = asynchronous reset 2 = synchronous reset
op_iso_mode	0 to 4 Default: 0	Operand Isolation Mode (controls datapath gating for minPower flow) If *stall_mode* is '0', this parameter is ignored and no isolation is applied. 0 = DC variable (DW_lp_op_iso_mode) can control the op iso mode 1 = 'none' 2 = 'and' 3 = 'or' 4 = preferred isolation style: 'and'

Table 1-3 Synthesis Implementations

Implementation Name	Implementation	License Feature Required
str[a]	Pipelined str synthesis model	DesignWare

a. One of pparch or apparch implementation is selected based the constraints of the design.

Table 1-4 Simulation Models

Model	Function
DW02.DW_DIV_PIPE_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW_div_pipe_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_div_pipe.v	Verilog simulation model source code

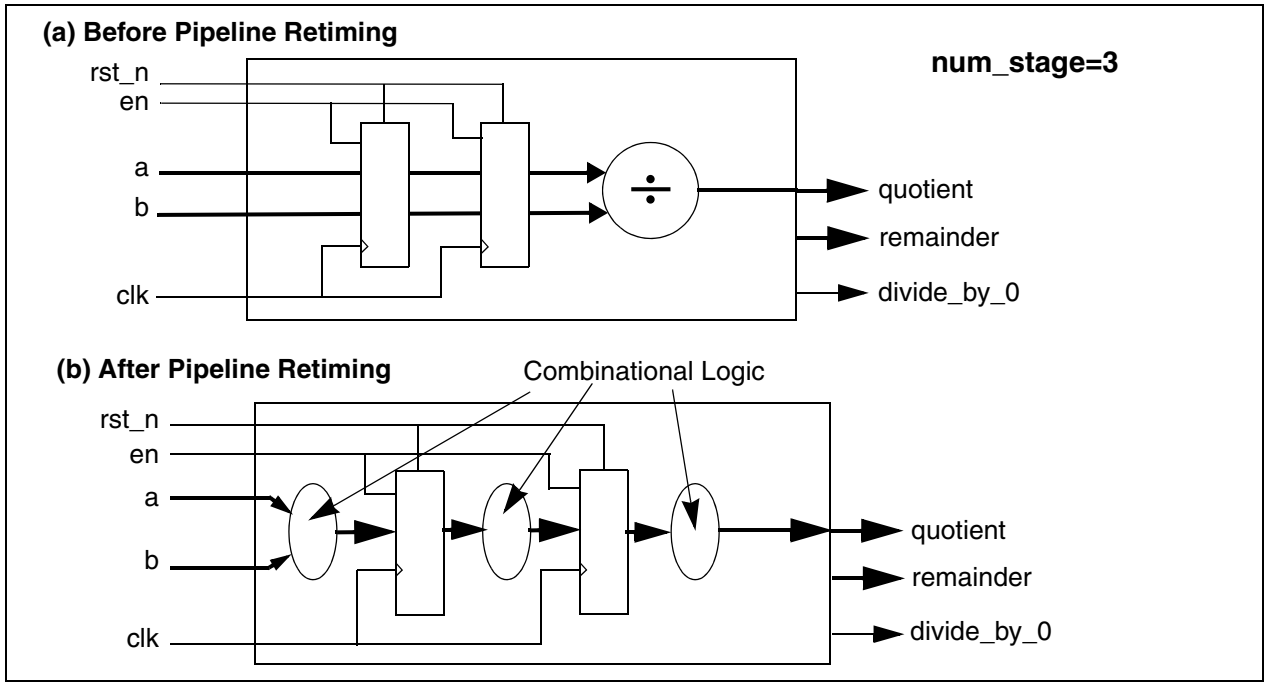
DW_div_pipe divides the operands `a` by `b` to produce a `quotient` and a `remainder`, if selected through a parameter, with a latency of *num_stages*–1 clock (`clk`) cycles. The parameter *tc_mode* determines whether the input and output data is interpreted as unsigned (*tc_mode=0*) or signed (*tc_mode=1*) numbers.

Attention A divide by zero warning message is generated each time the `b` input changes to the value zero. This warning can be disabled for Verilog simulations by defining the Verilog macro, DW_SUPPRESS_WARN, either in the test bench or on the simulator command line (such as, `+define+DW_SUPPRESS_WARN+`).

The DW_div_pipe incorporates the DW_div component to perform the division. For more information on the DW_div component, see *DW_div Combinational Divider*.

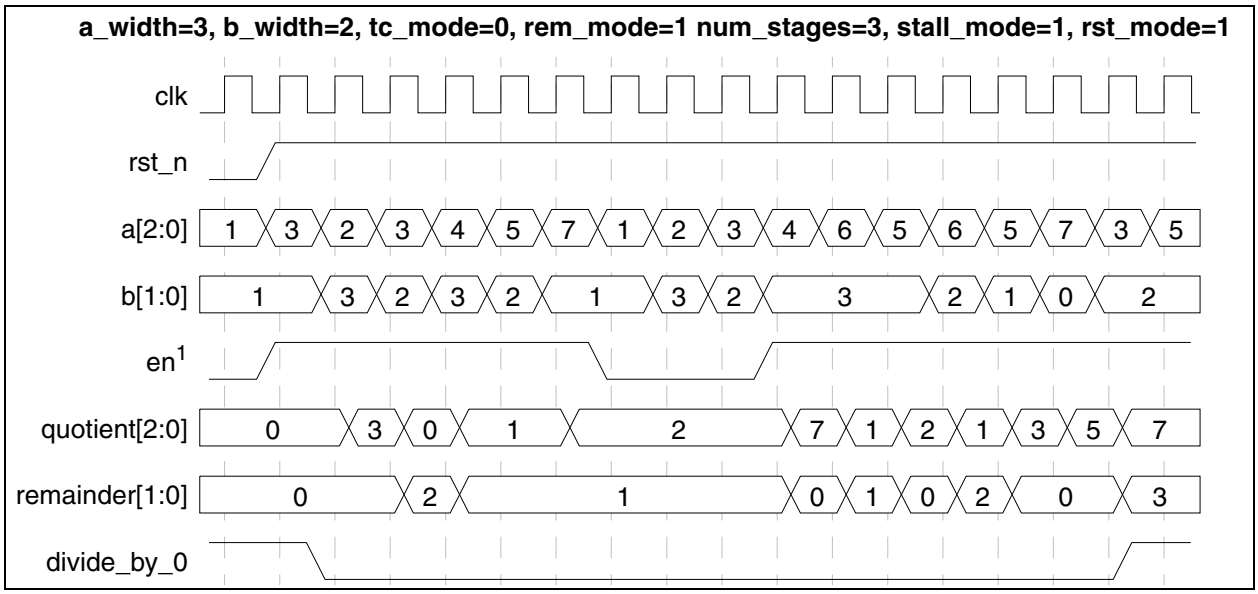
Automatic pipeline retiming ensures optimal placement of pipeline registers within the divider to achieve maximum throughput. The pipeline can be stalled by setting the load enable signal `en` low(*stall_mode*=1). The pipeline registers can either have no reset (*rst_mode*=0) or an asychronous (*rst_mode*=1) or synchronous reset (*rst_mode*=2) connected to the reset signal `rst_n`.

Figure 1-1 Pipeline Retiming



Timing Waveforms

Figure 1-2 Waveform 1



[1]If parameter stall_mode=0, then pin en has no effect.

Figure 1-3 Waveform 2

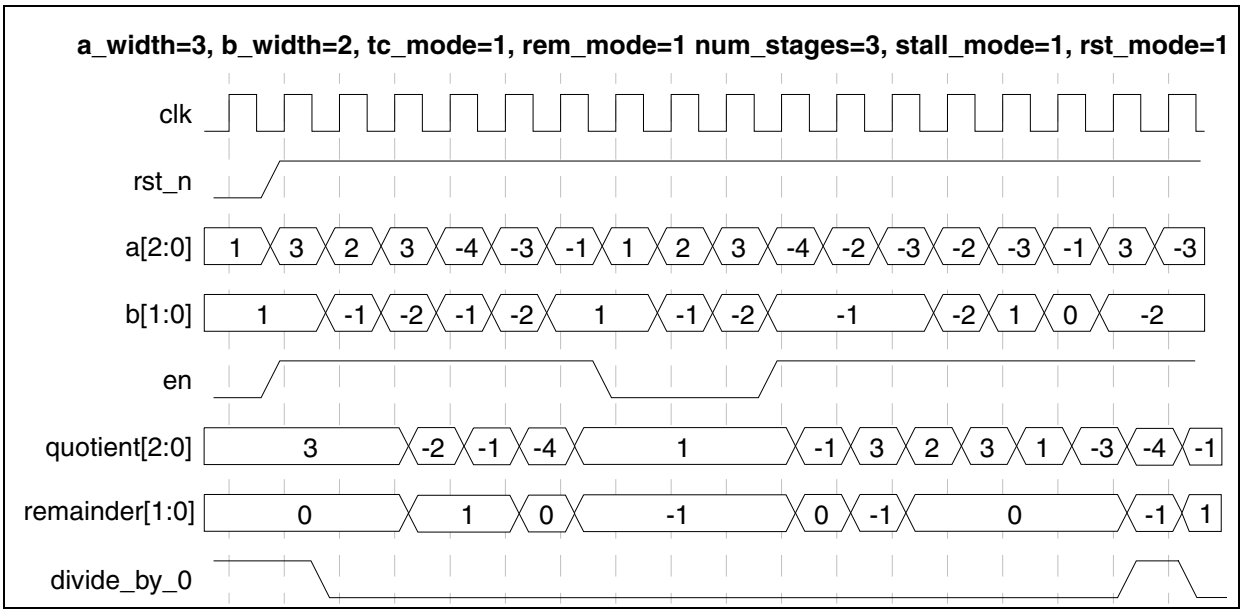


Figure 1-4 Waveform 3

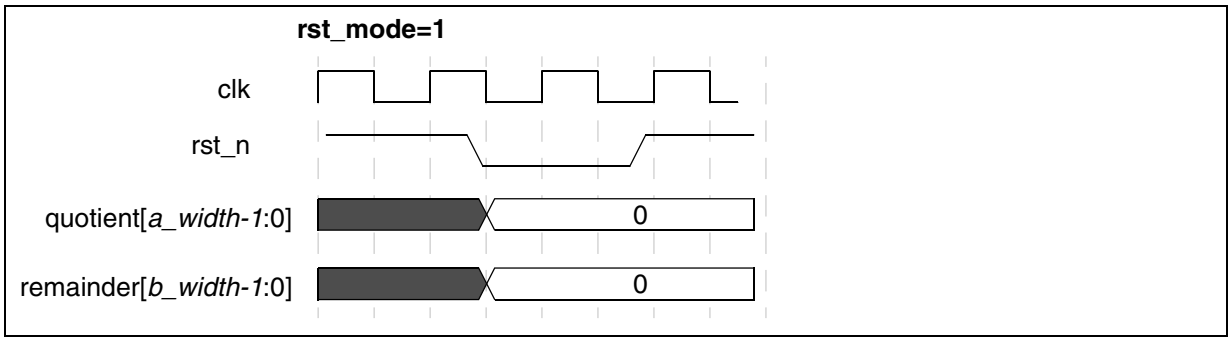
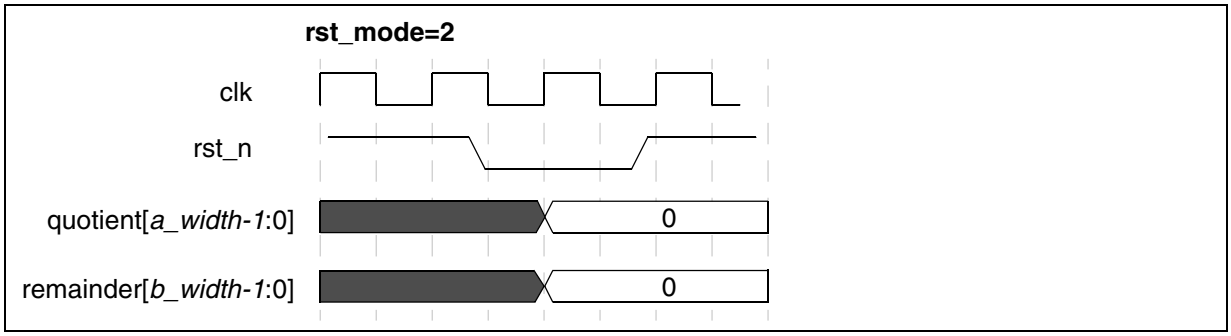


Figure 1-5 Waveform 4



Related Topics

- Math – Arithmetic Overview
- DesignWare Building Block IP Documentation Overview

HDL Usage Through Component Instantiation - VHDL

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DW_Foundation_comp_arith.all;

entity DW_div_pipe_inst is
  generic (inst_a_width    : POSITIVE := 8;  inst_b_width     : POSITIVE := 8;
           inst_tc_mode    : NATURAL := 0;   inst_rem_mode    : NATURAL := 1;
           inst_num_stages : POSITIVE := 2;  inst_stall_mode  : NATURAL := 1;
           inst_rst_mode   : NATURAL := 1;   inst_op_iso_mode : NATURAL := 0 );
  port (inst_clk         : in std_logic;
        inst_rst_n       : in std_logic;
        inst_en          : in std_logic;
        inst_a           : in std_logic_vector(inst_a_width-1 downto 0);
        inst_b           : in std_logic_vector(inst_b_width-1 downto 0);
        quotient_inst    : out std_logic_vector(inst_a_width-1 downto 0);
        remainder_inst   : out std_logic_vector(inst_b_width-1 downto 0);
        divide_by_0_inst : out std_logic );
end DW_div_pipe_inst;

architecture inst of DW_div_pipe_inst is
begin
  -- Instance of DW_div_pipe
  U1 : DW_div_pipe
    generic map (a_width => inst_a_width,   b_width => inst_b_width,
                 tc_mode => inst_tc_mode,   rem_mode => inst_rem_mode,
                 num_stages => inst_num_stages,  stall_mode => inst_stall_mode,
                 rst_mode => inst_rst_mode,   op_iso_mode => inst_op_iso_mode )
    port map (clk => inst_clk,   rst_n => inst_rst_n,   en => inst_en,
              a => inst_a,   b => inst_b,
              quotient => quotient_inst,   remainder => remainder_inst,
              divide_by_0 => divide_by_0_inst );
end inst;

-- Configuration for use with VSS simulator
-- pragma translate_off
configuration DW_div_pipe_inst_cfg_inst of DW_div_pipe_inst is
  for inst
  end for; -- inst
end DW_div_pipe_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_div_pipe_inst(inst_clk, inst_rst_n, inst_en, inst_a, inst_b,
                        quotient_inst, remainder_inst, divide_by_0_inst );

  parameter inst_a_width = 8;
  parameter inst_b_width = 8;
  parameter inst_tc_mode = 0;
  parameter inst_rem_mode = 1;
  parameter inst_num_stages = 2;
  parameter inst_stall_mode = 1;
  parameter inst_rst_mode = 1;
  parameter inst_op_iso_mode = 0;

  input inst_clk;
  input inst_rst_n;
  input inst_en;
  input [inst_a_width-1 : 0] inst_a;
  input [inst_b_width-1 : 0] inst_b;
  output [inst_a_width-1 : 0] quotient_inst;
  output [inst_b_width-1 : 0] remainder_inst;
  output divide_by_0_inst;

  // Instance of DW_div_pipe
  DW_div_pipe #(inst_a_width,   inst_b_width,   inst_tc_mode,  inst_rem_mode,
                inst_num_stages,   inst_stall_mode,   inst_rst_mode,
  inst_op_iso_mode)
    U1 (.clk(inst_clk),   .rst_n(inst_rst_n),   .en(inst_en),
        .a(inst_a),   .b(inst_b),   .quotient(quotient_inst),
        .remainder(remainder_inst),   .divide_by_0(divide_by_0_inst) );
endmodule
```

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