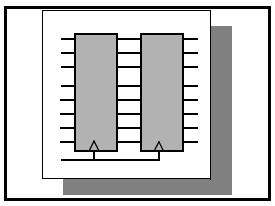
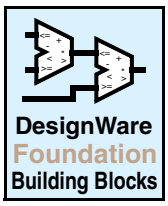


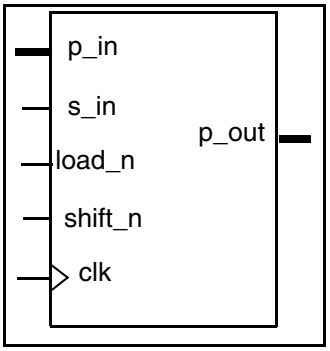



# DW03_shftreg

## Shift Register

Version, STAR and Download Information: IP Directory

## Features and Benefits




- Parameterized word length
- Active low shift enable
- Active low load enable
- Provides minPower benefits with the DesignWare-LP license.

## Description

DW03_shftreg is a shift register of parameterized length. The active LOW load enable, `load_n`, provides parallel load access and the active LOW shift enable, `shift_n`, shifts the data. If `load_n` is set to a constant HIGH value during synthesis, a serial shifter with no parallel access is built. The serial output of the shift register is computed as `p_out(`*length*`-1)`.

**Table 1-1 Pin Description**

| Pin Name | Width | Direction | Function |
|---|---|---|---|
| clk | 1 bit | Input | Clock |
| s_in | 1 bit | Input | Serial shift input |
| p_in | *length* bit(s) | Input | Parallel input |
| shift_n | 1 bit | Input | Shift enable, active low |
| load_n | 1 bit | Input | Parallel load enable, active low |
| p_out | *length* bit(s) | Output | Shift register parallel output |

**Table 1-2 Parameter Description**

| Parameter | Values | Description |
|---|---|---|
| length | ≥ 1 | Length of shifter |

**Table 1-3 Synthesis Implementations**

| Implementation Name | Function | License Feature Required |
|---|---|---|
| str | Synthesis model | DesignWare |

**Table 1-4 Simulation Models**

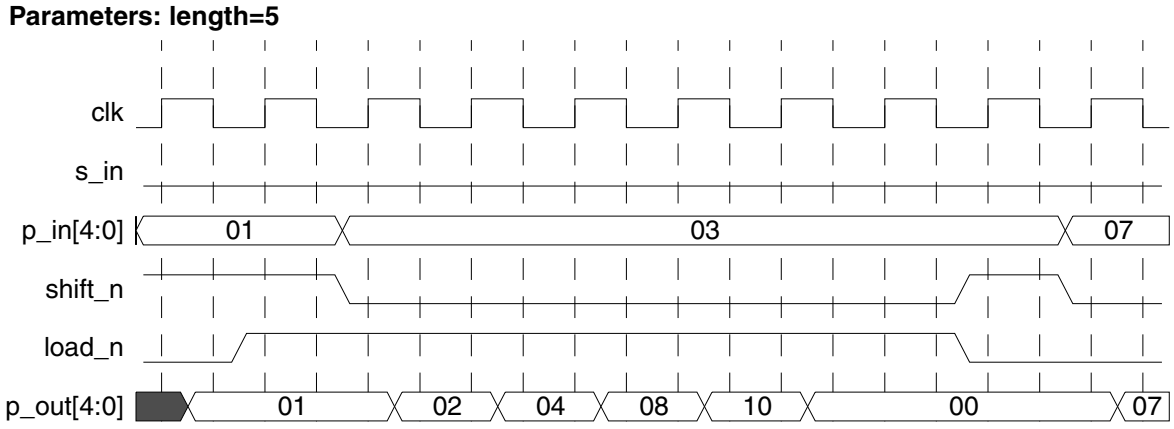
| Model | Function |
|---|---|
| DW03.DW03_SHFTREG_CFG_SIM | Design unit name for VHDL simulation |
| dw/dw03/src/DW03_shftreg_sim.vhd | VHDL simulation model source code |
| dw/sim_ver/DW03_shftreg.v | Verilog simulation model source code |

**Table 1-5 Shift Register Operation Truth Table**

| load_n | shift_n | Operation |
|---|---|---|
| 0 | X | Parallel load |
| 1 | 0 | Serial shift |
| 1 | 1 | Standby |

## Timing Diagram

**Figure 1-1 Functional Operation**




## Related Topics

- Memory – Registers Overview
- DesignWare Building Block IP Documentation Overview

## HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW03_shftreg_inst is
  generic ( inst_length : NATURAL := 4 );
  port ( inst_clk     : in std_logic;
         inst_s_in    : in std_logic;
         inst_p_in    : in std_logic_vector(inst_length-1 downto 0);
         inst_shift_n : in std_logic;
         inst_load_n  : in std_logic;
         p_out_inst   : out std_logic_vector(inst_length-1 downto 0) );
end DW03_shftreg_inst;

architecture inst of DW03_shftreg_inst is
begin

  -- Instance of DW03_shftreg
  U1 : DW03_shftreg
    generic map ( length => inst_length )
    port map ( clk => inst_clk,   s_in => inst_s_in,   p_in => inst_p_in,
               shift_n => inst_shift_n,    load_n => inst_load_n,
               p_out => p_out_inst );
end inst;

-- pragma translate_off
configuration DW03_shftreg_inst_cfg_inst of DW03_shftreg_inst is
  for inst
  end for; -- inst
end DW03_shftreg_inst_cfg_inst;
-- pragma translate_on
```

## HDL Usage Through Component Instantiation - Verilog

```
module DW03_shftreg_inst( inst_clk, inst_s_in, inst_p_in,
                          inst_shift_n, inst_load_n,  p_out_inst );

  parameter length = 4;

  input inst_clk;
  input inst_s_in;
  input [length-1 : 0] inst_p_in;
  input inst_shift_n;
  input inst_load_n;
  output [length-1 : 0] p_out_inst;

  // Instance of DW03_shftreg
  DW03_shftreg #(length)
    U1 (.clk(inst_clk),   .s_in(inst_s_in),   .p_in(inst_p_in),
        .shift_n(inst_shift_n),   .load_n(inst_load_n),  .p_out(p_out_inst));

endmodule
```

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