SYNOPSYS®

DesignWare® Building Block IP

Release Notes

DWBB_201806.3 Release for Design Compiler

Supported DC Synthesis Releases:
See Table 1-2 on page 5.

Supported Synplify FPGA Releases:
See Table 1-3 on page 6.

DWBB_201806.3
O-2018.06-SP3
October 2018

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Release Notes: Building Block IP

This document contains the latest information about the Synopsys DesignWare Building Block DWBB_201806.3 IP Release for Design Compiler (DC), Synplify Pro (FPGA) and VCS MX. This library of IP was previously called the DesignWare Foundation (DWF) Library. The older DWF nomenclature appears in licensing and file naming. This release is based on the O-2018.06-SP3 Synthesis release.

This document also contains release information for Building Block IP in FPGA synthesis (Synplify tools).

The following lists the topic described in this document:

1.1 Features and Changes in Version DWBB_201806.3 / O-2018.06-SP3

This section lists DWBB IP additions/updates for the current release. This section also describes the release information and issues related to using Building Block IP with Synopsys Synplify Premier and Synplify Premier with Design Planner tools.

This release contains the following bug fixes and enhancements.

Table 1-1 STARs Resolved in DWBB_201806.3 (O-2018.06-SP3)

Component	STAR ID	Type	Description
DW_ram_r_w_2c_dff	9001406396	Enhancement	Request to make DW_ram_r_w_2c_dff available as a main component
DW_fp_div_seq	[a]9001366623	Bug	Verilog simulation model has illegal register definition
DW_fir_seq DW_8b10b_dec	[a]9001396239	Bug	Verilog simulation models contain SV constructs
DW_asymfifo_s2_sf	[a]9001390667	Bug	Verilog simulation model has syntax error

a. Originally released in DWBB_201709.5.4 / N-2017.09-SP5-4 and included in O series releases from this point forward.

1.2 Known Problems and Limitations

Known problems (STARs) are listed in the following table. Any links in the table go to more information in the STARs on the Web system.

Component	STAR ID	Type	Description
DW_data_sync_na DW_pulseack_sync	9000756521	Bug	Simulation model does not allow parameter *tst_mode* to be set

To access the latest STAR information for all library components, see "STARs on the Web" on page 19.

1.3 DWBB Version Compatibility with Tool Versions

> **Note** View this document on the Synopsys website for the latest compatibility information: https://www.synopsys.com/dw/doc.php/doc/dwf/manuals/dwbb_relnotes.pdf

1.3.1 Design Compiler Compatibility

Table 1-2 shows which DWBB IP releases work with the supporting Design Compiler releases:

Table 1-2 DesignWare Building Block Release Compatibility

Building Block IP Release	2018.06 -SP3 D3	2017.09 -SP5-4 DC	2018.06 -SP2 DC	2018.06 -SP1 DC	2018.06 DC	2017.09 -SP5 DC	2017.09 -SP4 DC	2017.09 -SP3 DC	2017.09 -SP2 & 2016.12 -SP5-2 DC	2017.09 -SP1 & 2016.12 -SP5-1 DC	2017.09 DC	2016.12 -SP5 DC	2016.12 -SP4 DC	2016.12 -SP3 DC	2016.12 -SP2 DC
DWBB_201806.3	Bundled														
DWBB_201709.5.4		Bundled													
DWBB_201806.2			Bundled												
DWBB_201806.1				Bundled											
DWBB_201806.0					Bundled										
DWBB_201709.5						Bundled									
DWBB_201709.4							Bundled								
DWBB_201709.3								Bundled							
DWBB_201709.2 DWBB_201612.5.2									Bundled						
DWBB_201709.1 DWBB_201612.5.1										Bundled					
DWBB_201709.0											Bundled				
DWBB_201612.5												Bundled			
DWBB_201612.4													Bundled		
DWBB_201612.3														Bundled	
DWBB_201612.2															Bundled

1.3.2 Synplify FPGA Synthesis Tool Compatibility

Table 1-3 shows which DWBB IP releases work with the Synplify Premier releases:

Table 1-3 DesignWare Building Block / Synplify Premier Release Compatibility

Building Block IP Release / (DC Bundled)	Synplify Premier Release									
	2018.09	2018.09	2018.03 -SP1-1	2018.03 -SP1	2017.09 -SP1	2017.09 -SP1	2017.09 -SP1	2017.09 -SP1	2017.09	2017.03 -SP1-2
DWBB_201806.3/ O-2018.06-SP3	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201709.5.4/ N-2017.09-SP5-4	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201806.2/ O-2018.06-SP2	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201806.1/ O-2018.06-SP1	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201806.0/ O-2018.06	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201709.5/ N-2017.09-SP5	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201709.4/ N-2017.09-SP4	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201709.3/ N-2017.09-SP3	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201709.2/ N-2017.09-SP2 DWBB_201612.5.2/ M-2016.12-SP5-2	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201709.1/ N-2017.09-SP1 DWBB_201612.5.1/ M-2016.12-SP5-1	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201709.0/ N-2017.09	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201612.5/ M-2016.12-SP5	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201612.4/ M-2016.12-SP4	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201612.3/ M-2016.12-SP3	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
DWBB_201612.2/ M-2016.12-SP2	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔

1.3.3 VCS MX Compatibility

The DWBB_201806.3 Building Block IP release works with VCS MX.

1.4 Features and Changes in Previous Versions (History)

1.4.1 DWBB_201709.5.4 / N-2017.09-SP5-4

This release contains the following bug fixes and enhancements.

This release continues in the N sequence of releases and does not include fixes or enhancements that are in the O sequence of releases.

Table 1-4 STARs Resolved in DWBB_201709.5.4 (N-2017.09-SP5-4)

Component	STAR ID	Type	Description
DW_fp_div_seq	9001366623	Bug	Verilog simulation model has illegal register definition
DW_fir_seq DW_8b10b_dec	9001396239	Bug	Verilog simulation models contain SV constructs
DW_asymfifo_s2_sf	9001390667	Bug	Verilog simulation model has syntax error

1.4.2 DWBB_201806.2 / O-2018.06-SP2

This release contains no technical bug fixes or enhancements.

1.4.3 DWBB_201806.1 / O-2018.06-SP1

This release contains the following bug fixes and enhancements.

Table 1-5 STARs Resolved in DWBB_201806.1 (O-2018.06-SP1)

Component	STAR ID	Type	Description
DW_exp2 DW_ln DW_log2	9001341564	Bug	VHDL simulation model has variable that is never used
DW_fp_div_seq	9001366623	Bug	Verilog simulation model has a variable of type “reg” but is used as if it is of type “wire”, which causes a syntax error in a non-SystemVerilog context
DW_exp2 DW_fp_exp DW_fp_exp2	9001366625	Bug	Datasheet is missing width limits on simulation model for VHDL and non-VCS simulators

1.4.4 DWBB_201806.0 / O-2018.06

This release contains no technical bug fixes or enhancements.

1.4.5 DWBB_201709.5 / N-2017.09-SP5

This release contains the following bug fixes and enhancements.

Table 1-6 STARs Resolved in DWBB_201709.5 (N-2017.09-SP5)

Component	STAR ID	Type	Description
DW_asymdata_inbuf DW_asymdata_outbuf DW_asymfifo_s2_sf DW_fifo_s2_sf	9001317257	Bug	Expand the supported width (and depth, for the two FIFO components) to better fit related components
DW_fp_ln	9001308455	Bug	Upper bound of *extra_prec* is incorrect, both in the sldb and the datasheet

1.4.6 DWBB_201709.4 / N-2017.09-SP4

This release contains the following bug fixes and enhancements.

Table 1-7 STARs Resolved in DWBB_201709.4 (N-2017.09-SP4)

Component	STAR ID	Type	Description
DW_fp_mac DW_fp_dp2 DW_fp_sum3 DW_fp_sum4	9001298598	Bug	The “huge” status flag is not set for an overflow condition when the rounding mode is 1, 2, or 3.
DW_div_seq	9001296230	Bug	Register output is not recovered by async reset after UPF power up in an NLP simulation.
DW_lza	9001242906	Bug	In the datasheet, the example of functional inference is incorrect.
Library	9001214579	Bug	DC generates an empty netlist without any warnings or errors when you use set_implementation to force DC to use an illegal implementation.

1.4.7 DWBB_201709.3 / N-2017.09-SP3

This release contains the following bug fixes and enhancements.

Table 1-8 STARs Resolved in DWBB_201709.3 (N-2017.09-SP3)

Component	STAR ID	Type	Description
Library support scripts (Synthesis)	9001205061	Bug	Getting CMD- messages from DWBB designs when using UPF compatibility mode in DC

1.4.8 DWBB_201709.2 / N-2017.09-SP2 and DWBB_201612.5.2 / M-2016.12-SP5-2

These releases contain the following bug fixes and enhancements.

Table 1-9 STARs Resolved in DWBB_201709.2 (N-2017.09-SP2) and DWBB_201612.5.2 (M-2016.12-SP5-2)

Availability	Component	STAR ID	Type	Description
DWBB_201709.2 (N-2017.09-SP2)	DW_asymfifo_s2_sf DW_asymfifoctl_s2_sf DW_fifo_s2_sf DW_fifoctl_s2_sf	9001026675	Enhancement	Ability to inject random missamples for clock domain crossings NOTE: This enhancement applies to only Verilog simulation models at this time; for specifics, see the datasheets
DWBB_201709.2 (N-2017.09-SP2) DWBB_201612.5.2 (M-2016.12-SP5-2)	DW_fp_div_seq	9001121224	Bug	The `complete` signal is asserted 1 clock earlier (or de-asserted 1 clock later) than expected
		9001251699	Bug	For configurations that have *INTERNAL_REG* = 1 and *OUTPUT_MODE* = 1, a change on `rnd` affects rounding results 1 cycle earlier than normal during back-to-back operations.

1.4.9 DWBB_201709.1 / N-2017.09-SP1 and DWBB_201612.5.1 / M-2016.12-SP5-1

These releases contain the following bug fixes and enhancements.

Table 1-10 STARs Resolved in DWBB_201709.1 (N-2017.09-SP1) and DWBB_201612.5.1 (M-2016.12-SP5-1)

Component	STAR ID	Type	Description
DW_div_seq	9001112685	Bug	Incorrect synthesis results with an overflow condition when tc_mode = 1
	9001226703	Enhancement	Enhance timing behavior of `complete` and `divide_by_0` outputs (datasheet updated)
DW_ecc	9001217597	Bug	The Verilog simulation model causes an error in VCS NLP Low Power Simulation flow

1.4.10 DWBB_201709.0 / N-2017.09

This release contains no technical bug fixes or enhancements.

1.4.11 DWBB_201612.5 / M-2016.12-SP5

This release contains the following bug fixes and enhancements.

Table 1-11 STARs Resolved in DWBB_201612.5 (M-2016.12-SP5)

Component	STAR ID	Type	Description
DW_fp_div	9001189734	Bug	The str implementation produces incorrect results for some configurations (datasheet updated)
DW_fp_div	9001210054	Bug	Incorrect results when b is a denormal number for some configurations
DW_fp_exp	9001204304	Bug	VHDL simulation model for DW_fp_exp does not run due to array size mismatch
DWF_dp_mult_comb_ovfldet	9001204853	Bug	Missing port direction in DWF_dp_mult_comb_ovfldet VHDL simulation model
DW_fifoctl_2c_df	9001209980	Bug	Datasheet error with the size of the wr_addr_s port (datasheet updated)

1.4.12 DWBB_201612.4 / M-2016.12-SP4

This section lists DWBB IP additions/updates for the current release. This section also describes the release information and issues related to using Building Block IP with Synopsys Synplify Premier and Synplify Premier with Design Planner tools.

This release contains the following bug fixes and enhancements.

- In the following memory components, the “str” implementation has been obsoleted and replaced by the “rtl” implementation:
  - DW_ram_2r_w_a_dff
  - DW_ram_2r_w_s_dff
  - DW_ram_r_w_a_dff
  - DW_ram_rw_a_dff
  - DW_ram_r_w_s_dff
  - DW_ram_rw_s_dff

  The datasheet for each of these memory components contains the following explanation:

  The implementation, “rtl,” replaces the obsolete implementation, “str”. Existing designs that specify the obsolete implementation (“str”) will automatically have that implementation replaced by the new superseding implementation (“rtl”) as will be noted by an information message (SYNDB-36) generated during DC compilation.

Table 1-12 STARs Resolved in DWBB_201612.4 (M-2016.12-SP4)

Component	STAR ID	Type	Description
DW_data_sync	9001170509	Bug	Inaccurate timing waveforms in datasheet

1.4.13 DWBB_201612.3 / M-2016.12-SP3

This release contains the following bug fixes and enhancements.

Table 1-13 STARs Resolved in DWBB_201612.3 (M-2016.12-SP3)

Component	STAR ID	Type	Description
DW_fp_ln	9001116007	Enhancement	Does not support divide-by-zero status flag
DW_fp_div	9001121180	Bug	The str implementation with #(52, 11, 0/1) has larger than 1 ulp error
DW_fp_dp3	9001123397	Bug	Synthesis model provides incorrect results for certain configurations
DW_fp_div	9001167381	Bug	Produces tiny and huge status bit errors as well as an output z error at minnorm and maxnorm.

1.4.14 DWBB_201612.2 / M-2016.12-SP2

This release contains the following bug fixes and enhancements.

Table 1-14 STARs Resolved in DWBB_201612.2 (M-2016.12-SP2)

Component	STAR ID	Type	Description
DW_tap DW_tap_uc	9001134192	Bug	Redundant clock logic
DW_asymfifoctl_2c_df DW_fifo_2c_df DW_fifoctl_2c_df	9001152809	Enhancement	Support *clk_ratio* = 0 to allow arbitrary clock relationships

1.4.15 DWBB_201612.1 / M-2016.12-SP1

This release contains the following bug fixes and enhancements.

Table 1-15 STARs Resolved in DWBB_201612.1 (M-2016.12-SP1)

Component	STAR ID	Type	Description
DW_sync	9001106160	Bug	Preferred sync cells are not correctly mapped for multi-stage synchronizers
Documentation	9001120644	Enhancement	Floating-point Overview update needed to clarify NaN behavior
DW_fp_square	9001121118	Bug	Synthesis model sometimes shows an incorrect result when *sig_width* = 52
DW_squarep DW02_multp	9001128623	Enhancement	Change of the default value of *verif_en* parameter (from '1' to '2')

Table 1-15 STARs Resolved in DWBB_201612.1 (M-2016.12-SP1) (Continued)

Component	STAR ID	Type	Description
DW_ecc	9001134170	Enhancement	Reduce lower limit of *width* parameter from 8 to 4

1.4.16 DWBB_201612.0 / M-2016.12

This release contains no technical bug fixes or enhancements.

1.4.17 DWBB_201603.5 / L-2016.03-SP5

This release contains the following bug fixes and enhancements.

Table 1-16 STARs Resolved in DWBB_201603.5 (L-2016.03-SP5)

Component	STAR ID	Type	Description
DW_fp_log2	9001082385	Bug	Result for log2(-0) and log2(+0) incorrect
DW_ecc	9001097173	Bug	DW_ecc_function.inc unusable due to semantic error
DW_norm_rnd	9001102004	Bug	VCS warning/error when *a_width* = *b_width* (VHDL models)

1.4.18 DWBB_201603.4 / L-2016.03-SP4

This release contains the following bug fixes and enhancements.

Table 1-17 STARs Resolved in DWBB_201603.4 (L-2016.03-SP4)

Component	STAR ID	Type	Description
DW_norm_rnd	9000999112	Bug	Lint error in DW_norm_rnd
DW_fp_flt2i	9001069342	Enhancement	Datasheet needs info for input=-Inf
DW_tap DW_tap_uc	9001077028	Bug	Zero time race condition with sync_mod=1

1.4.19 DWBB_201603.3 / L-2016.03-SP3

This release contains the following bug fixes and enhancements.

Table 1-18 STARs Resolved in DWBB_201603.3 (L-2016.03-SP3)

Component	STAR ID	Type	Description
DW01_binenc	9001048364	Bug	False error message during DC elaboration of DW01_binenc 'cla' implementation when width=1
DW_fp_div	9001048917	Bug	The str implementation has a 1 ulp error when rnd = 1, 2, or 3

Table 1-18 STARs Resolved in DWBB_201603.3 (L-2016.03-SP3) (Continued)

Component	STAR ID	Type	Description
DW_fp_div	9001058879	Bug	Incorrect inexact status flag from str implementation when faithful_round = 0
DW_dct_2d	9001068856	Bug	When the 'enable' input is set low during calculation, data corruption occurs.

1.4.20 DWBB_201603.2 / L-2016.03-SP2

The Verilog simulation model for the following component has been enhanced to comply with enhancements in a planned release of the VCS NLP power modeling simulation flow:

- DW_stream_sync

This release contains the following bug fixes and enhancements.

Table 1-19 STARs Resolved in DWBB_201603.2 (L-2016.03-SP2)

STAR ID	Type	Description
9000896107	Bug	**DW_fifoctl_2c_df** encounters false errors during clearing sequence caused **DW_reset_sync** inside (defect also affects **DW_asymfifoctl_2c_df**, **DW_fifo_2c_df**, and **DW_stream_sync**)
9001047128	Bug	**DW_fp_sincos** simulation models are not properly ignoring err_range when pi_multiple = 0
9000948184	Bug	Design Compiler is unable to control multi-bit mapping and synchronous set/reset of F/Fs within DesignWare components when DesignWare cache is enabled; affects all sequential DWBB components.

1.4.21 DWBB_201603.1 / L-2016.03-SP1

The Verilog simulation models for the following components have been enhanced to comply with the VCS NLP power modeling simulation flow:

- DW_crc_s
- DW_fir_seq
- DW_fir
- DW_8b10b_dec
- DW_8b10b_enc
- DW_wc_d1_s
- DW_wc_s1_s
- DW_mult_seq
- DW_fifoctl_s2dr_sf
- DW_dct_2d
- DW_div_seq
- DW_sqrt_seq
- DW_stream_sync
- DW_bc_1
- DW_bc_2
- DW_bc_3
- DW_bc_4
- DW_bc_5
- DW_bc_7
- DW_asymfifoctl_s1_sf
- DW_asymfifoctl_s2_sf
- DW03_bictr_decode
- DW_fp_div_seq

This release contains the following bug fixes and enhancements.

Table 1-20 STARs Resolved in DWBB_201603.1 (L-2016.03-SP1)

STAR ID	Type	Description
9000999057	Bug	Verilog simulation model for **DW_tap_uc** (and **DW_tap**) not fully compatible with VCS-NLP
9001002086	Bug	Corrects corrupted FPGA IP file (which affects the ZeBu product as well as FPGA synthesis tools and FM for FPGA)

1.4.22 DWBB_201603.0 / L-2016.03

This release contains no technical bug fixes or enhancements.

1.4.23 DWBB_201506.5 / K-2015.06-SP5

This release contains the following bug fixes and enhancements.

Table 1-21 STARs Resolved in DWBB_201506.5 (K-2015.06-SP5)

STAR ID	Type	Description
9000854445	Bug	For **DW_fp_ln**, the value of log2(-0) is being delivered as 'invalid' (or NaN) when the correct output should be negative infinity
9000983334	Bug	The **DW_fp_mult** produces incorrect results without denormals for a few configurations
9000984209	Bug	For **DW_fp_log2**, the value of log2(-0) is being delivered as 'invalid' (or NaN) when the correct output should be negative infinity
9000986633	Bug	A large number of **DW03_updn_ctr** instances causes long runtime
9000609524	Enhancement	The datasheet for **DW_pulse_sync** needs to be updated (timing diagram)

1.4.24 DWBB_201506.4 / K-2015.06-SP4

This release contains the following bug fixes and enhancements.

Table 1-22 STARs Resolved in DWBB_201506.4 (K-2015.06-SP4)

STAR ID	Type	Description
9000972181	Bug	■ DC fails to elaborate **DW_fp_exp** when exp_width + sig_width + 1 > 62 ■ Upper bound of sig_width in datasheet should be 57

1.4.25 Update To DesignWare Developer

This optional section notes additions/updates for the current release of the DesignWare Developer, which is a tool that enables you to encapsulate your own designs as DesignWare components.

- License Queuing Support for Synopsys Encryptor (`synenc`)

  The `synenc` utility encrypts the RTL or Tcl source code. Using the utility requires either a DesignWare Developer license or a DesignWare license. When the required license is not available, the utility quits with an error message.

  Beginning with this release, the `synenc` utility supports license queuing functionality to wait for licenses to become available if all licenses are in use. To enable this functionality, set the `SNPSLMD_QUEUE` environment variable to `true` before you run the `synenc` utility.

  When you invoke `synenc` utility, it displays the following message:

  ```
  Information: License queuing is enabled. (SYNENC-12)
  ```

  Use the `SNPS_MAX_WAITTIME` variable to specify the maximum wait time in seconds for the license. The default wait time is 28800 (8 hours).

1.5 Obsoleted IP for New Designs

DesignWare Building Block IP components are occasionally removed from the library. The process of removing components occurs in three stages over a period of at least two years.

1.5.1 Stage 1: Notification of Obsoleted IP

The first stage in obsoleting IP is a notification that the IP will not be supported in the future. You can still simulate and synthesize the IP, but a warning is issued during simulation.

There is currently no DesignWare Building Block IP at this stage.

1.5.2 Stage 2: Notification of Obsoleted Simulation Models

The second stage of the IP obsolescence is to remove the simulation model from the library. This occurs approximately 1 year from the time of the announcement that a particular IP is being obsoleted for new designs. Simulation is not possible, but synthesis of old designs still is possible

There is currently no DesignWare Building Block IP at this stage.

1.5.3 Stage 3: Notification of Obsoleted Synthesis Models

The third and final stage of the IP obsolescence process is to remove the remaining synthesis model from the library. This occurs approximately 2 years from the time of the announcement that a particular IP is being obsoleted for new designs. Simulation and synthesis is not possible.

The following DWBB IP is at stage 3 of obsolescence: **DW02_sincos**, **DW02_sin**, and **DW02_cos**.

1.5.4 Notification of Obsoleted Synthesis Implementations

There are no recent obsoleted synthesis implementations.

1.6 Installation

DesignWare Building Block IP is installed with your DC synthesis release. If you install a patch to DC, refer to "When to Run the Reanalysis Scripts" on page 17.

1.6.1 How Can I Tell Which DWBB Version Is Installed?

One way to view which DesignWare Building Block IP library you currently have installed on your UNIX system is to issue the following command:

```
% cat $SYNOPSYS/dw/version
```

The string that is returned looks something like this:

```
O-2018.06-SP3-DWBB_201806.3
```

The "O-2018.06-SP3" portion indicates the Synthesis base release. The "DWBB_201806.3" portion indicates the DesignWare Building Block IP release, which uses the YYYYMM.S format. In this example, the year (YYYY) is 2014, the month (MM) is 09 (September) and the service pack release is 3 (SP3).

To determine which DWBB Library version is installed over VCS MX, issue the following command:

```
% cat $VCS_HOME/dw/version
```

The string that is returned is displayed similar to the following:

```
X-XXXXX-DWBB_201806.3 #(DC version scheme - O-2018.06-SP3)
```

1.6.2 Installation of Building Block IP for FPGA Synthesis

Building Block IP installation for FPGA synthesis is the same process as for DC. For details, refer to "Installation" on page 17. You can use an existing DC installation without modification for FPGA synthesis, as long as the version is compatible (see Table 1-2 for version compatibility).

1.6.3 Version Label for Technical Support

For future reference, a file exists under $SYNOPSYS/dw called 'version', which contains the release version label. You need to know this label when contacting Synopsys technical support.

1.6.4 When to Run the Reanalysis Scripts

There are two special script files included with each DWBB release that reanalyze your DWBB IP source files. When run, the dw_analyze_syn.csh or dw_analyze_sim.csh script reanalyzes all existing DC and VCS MX components in your $SYNOPSYS/dw/ or $VCS_HOME/dw/ tree to ensure compatibility with newer versions of Synopsys Synthesis releases.

You must run the appropriate script for either of the following situations:

- When you receive a patch to DC that does not include DWBB IP, or if you add another tool after DC installation, you must do the following:

```
setenv SYNOPSYS path
set path = (${SYNOPSYS}/platform/syn/bin $path)
setenv LM_LICENSE_FILE ${SYNOPSYS}/admin/license/key:$LM_LICENSE_FILE
cd $SYNOPSYS/dw/scripts
./dw_analyze_syn.csh
egrep -i 'warning|error' $SYNOPSYS/dw_analyze_syn.*.log
```

- When you receive a patch to VCS MX that does not include DWBB IP, or if you add another tool after VCS MX installation, you must do the following for every target platform:

```
set path = (${VCS_HOME}/platform/bin $path) # VCS MX
setenv LM_LICENSE_FILE ${VCS_HOME}/admin/license/key:$LM_LICENSE_FILE
cd $VCS_HOME/dw/scripts
./dw_analyze_sim.csh
egrep -i 'warning|error' $VCS_HOME/dw_analyze_sim.log
```

path is the directory location where DesignWare Building Block IP and Synopsys synthesis and simulation tools have been installed, (for, example, "/synopsys/H-2013.03" or "/synopsys/VCS_mxversion").

platform is one of the following: sparc64, sparcOS5, linux, or any supported platform.

The reanalyze_sim.csh script is also available, along with dw_analyze_sim.csh. It is a simple reanalyze script that is independent of versions and the installation location of DWBB IP.

1.7 Documentation

1.7.1 DesignWare Building Block IP Datasheets and Manuals

PDF files containing the complete set of current DesignWare Building Block IP datasheets and manuals exist in the directory, $SYNOPSYS/dw/doc. The latest documentation is also available on the Synopsys website at the following location:

http://www.synopsys.com/dw/buildingblock.php

You can also find the documentation for a specific Building Block component by:

1. Using "Search for IP" field to find your desired DWBB component
2. Click on the "More Information..." link provided
3. Click on the Documentation: "Show Documents..." link to view the document list
4. Click on the document title to display the specific document

1.7.2 FPGA Synthesis Documentation

For a "QuickStart" on using Building Block IP with Synplify Premier tools for FPGA synthesis, refer to "Using DesignWare Building Block IP in FPGA Synthesis" in the *DesignWare Building Block IP User Guide*.

For Synplify Premier tool and FPGA synthesis information, see the *Synopsys FPGA Synthesis User Guide.*

1.8 Getting Help

1.8.1 Web Resources

- Fast access to DWBB component instantiation code snippets, function inference snippets (where appropriate), and links to documentation:

  http://www.synopsys.com/dw/buildingblock.php

- To subscribe to receive proactive notifications on new product releases, information on Synopsys Technical Action Requests (STARs), product updates, and more (requires SolvNet login):

  https://www.synopsys.com/dw/mydesignware.php

- Up-to-date information about the latest DesignWare Library IP:

  http://www.designware.com

- General Synopsys Licensing (SCL) information:

  http://www.synopsys.com/Support/LI/Pages/default.aspx

1.8.2 STARs on the Web

You can view a complete list of problem reports (STARs) for this product, including problems identified after product release, by accessing the STAR report on the Web. Note that you must have a SolvNet ID to view STAR reports.

To see STAR reports, got to the following link and navigate to the desired component, which lists the link for the Open and/or Closed STARs reports:

https://www.synopsys.com/dw/buildingblock.php

1.8.3 Customer Support

- First, prepare the following debug information, if applicable:
  - The coreConsultant-dwfc tool can create a tar file with information that is useful to debug problems. First, select the component, then use the **File > Build Debug Tar-file** menu item.
  - In addition, it is useful to provide the Support Center with the following information:
    - Create a waveforms file (such as VPD or VCD)
    - Identify the hierarchy path to the DWBB instance
    - Identify the timestamp of any signals or locations in the waveforms that are not understood

- Then, contact Support Center, with a description of your question and supplying the above information, using one of the following methods:
  - *For fastest response*, use the SolvNet website. If you fill in your information as explained below, your issue is automatically routed to a support engineer who is experienced with your product. The **Sub Product 1** entry is critical for correct routing.

    Go to http://solvnet.synopsys.com/EnterACall and click on the link to enter a call. Provide the requested information, including:
    - **Product:** *DesignWare Building Blocks*
    - **Product Version:** *DWBB_201806.3*
    - **Problem Type:**
    - **Issue Severity:**
    - **Problem:** Provide a short title for the issue you have encountered.

      Describe the details to clarify your problem; include names and configurations of DWBB components you are using and any warning or error messages. For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood.

    After creating the case, attach any debug files you created in the previous step.
  - Or, send an e-mail message to support_center@synopsys.com (your e-mail will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
    - Include the information as identified above so your email can be routed correctly.
    - For simulation issues, include the timestamp of any signals or locations in waveforms
    - Attach any debug files you created in the previous step.
  - Or, telephone your local support center:
    - https://www.synopsys.com/support/global-support-centers.html