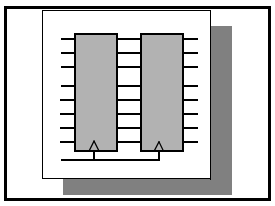
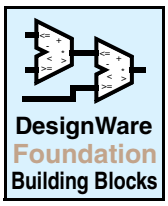




DW03_pipe_reg

Pipeline Register

Version, STAR and Download Information: IP Directory

Features and Benefits

- Parameterized data width and depth

Description

DW03_pipe_reg is a set of *width*-bit wide registers connected in series to form a pipeline shift register *depth* levels deep.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
A	*width* bit(s)	Input	Input data bus
clk	1 bit	Input	Clock
B	*width* bit(s)	Output	Output data bus

Table 1-2 Parameter Description

Parameter	Values	Description
depth	≥ 1	Depth of registers
width	≥ 1	Width of A and B buses

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
str	Synthesis model	DesignWare

Table 1-4 Simulation Models

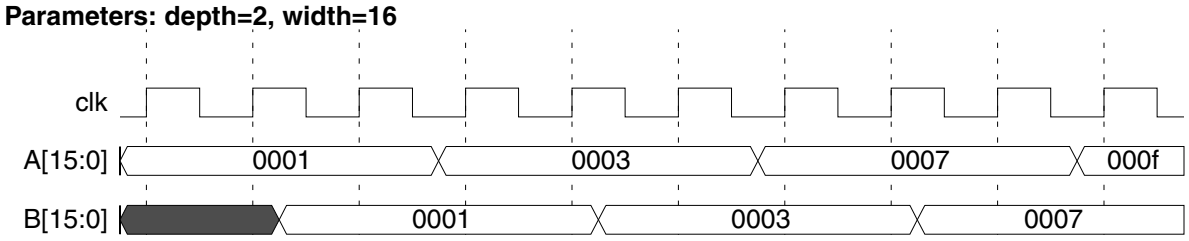
Model	Function
DW03.DW03_PIPE_REG_CFG_SIM	Design unit name for VHDL simulation
dw/dw03/src/DW03_pipe_reg_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW03_pipe_reg.v	Verilog simulation model source code

This component is composed of a simple array of D flip-flops connected in series by their `D` and `Q` pins. Setup and hold constraints are relative to the rising edge of clock signal `clk` and are technology dependent.

Because this pipeline register has no reset pin, data output `B` is unknown for the first *depth*–1 clock cycles after startup (the pipeline register's latency is *depth*–1 clock cycles).

Timing Diagram

Figure 1-1 Timing Waveforms for Pipeline Register



Related Topics

- Memory – Registers Overview
- DesignWare Building Block IP Documentation Overview

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW03_pipe_reg_inst is
  generic ( inst_depth : INTEGER := 8;
            inst_width : INTEGER := 8 );
  port ( inst_A   : in std_logic_vector(inst_width-1 downto 0);
         inst_clk : in std_logic;
         B_inst   : out std_logic_vector(inst_width-1 downto 0) );
end DW03_pipe_reg_inst;

architecture inst of DW03_pipe_reg_inst is
begin

  -- Instance of DW03_pipe_reg
 U1 : DW03_pipe_reg
    generic map ( depth => inst_depth, width => inst_width )
    port map ( A => inst_A, clk => inst_clk, B => B_inst );
end inst;

-- pragma translate_off
configuration DW03_pipe_reg_inst_cfg_inst of DW03_pipe_reg_inst is
  for inst
  end for; -- inst
end DW03_pipe_reg_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW03_pipe_reg_inst( inst_A, inst_clk, B_inst );

  parameter depth = 8;
  parameter width = 8;

  input [width-1 : 0] inst_A;
  input inst_clk;
  output [width-1 : 0] B_inst;

  // Instance of DW03_pipe_reg
  DW03_pipe_reg #(depth, width)
    U1 ( .A(inst_A), .clk(inst_clk), .B(B_inst) );
endmodule
```

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