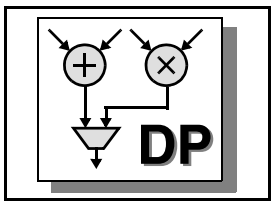

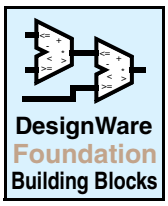

DWF_dp_mult_sat functions

Multiply and Saturate

Version, STAR and Download Information: IP Directory

Description

The DWF_dp_mult_sat function multiplies the two arguments a and b, truncates the upper bits of the result to the width specified by argument *p_width* and returns a saturated value if an overflow (or underflow) occurs. A dedicated overflow detection is used to improve QoR of the multiplier.

Table 1-1 Function Names

Function Name	Description
DWF_dp_mult_sat	VHDL unsigned multiply and saturate
DWF_dp_mult_sat	VHDL signed (two's complement) multiply and saturate
DWF_dp_mult_sat_uns	Verilog unsigned multiply and saturate
DWF_dp_mult_sat_tc	Verilog signed (two's complement) multiply and saturate

Table 1-2 Argument Description

Argument Name	Type	Width / Values	Description
a	Vector	*a_width*	Input multiplier
b	Vector	*b_width*	Input multiplicand
p_width	Integer	≥ 2	Word length of returned value (VHDL only, constant)
DWF_dp_mult_sat	Vector	*p_width*	Returned value

Table 1-3 Parameter Description (Verilog)

Parameter	Values	Description
a_width	≥ 2	Word length of input a
b_width	≥ 2	Word length of input b
p_width	≥ 2	Word length of returned value

Verilog Include File: DW_dp_mult_sat_function.inc

Functional Description

```
z[p_width-1:0] = DWF_dp_mult_sat (a[a_width-1:0], b[b_width-1:0], p_width)
```

Unsigned Multiply and Saturate

$$
\begin{aligned}
p[a\_width+b\_width-1:0] &= a[a\_width-1:0] * b[b\_width-1:0] \\
z[p\_width-1:0] &= 2^{p\_width}-1 \quad \text{if } p[a\_width+b\_width-1:0] > 2^{p\_width}-1 \\
&= p[p\_width-1:0] \quad \text{else}
\end{aligned}
$$

Signed Multiply and Saturate

$$
\begin{aligned}
p[a\_width+b\_width-1:0] &= a[a\_width-1:0] * b[b\_width-1:0] \\
z[p\_width-1:0] &= 2^{p\_width-1}-1 \quad \text{if } p[a\_width+b\_width-1:0] > 2^{p\_width-1}-1 \\
&= -2^{p\_width-1} \quad \text{else if } p[a\_width+b\_width-1:0] < -2^{p\_width-1} \\
&= p[p\_width-1:0] \quad \text{else}
\end{aligned}
$$

For more information about the DesignWare datapath functions, refer to the topic titled DesignWare Datapath Functions Overview.

Related Topics

- DesignWare Datapath Functions Overview
- DesignWare Building Block IP Documentation Overview

VHDL Example

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

entity DWF_dp_mult_sat_test is
  port (a, b, c : in  signed(7 downto 0);
        z       : out signed(7 downto 0));
end DWF_dp_mult_sat_test;

architecture rtl of DWF_dp_mult_sat_test is
begin
  z <= DWF_dp_mult_sat (a, b, 8) + c;
end rtl;
```

Verilog Example

```
module DWF_dp_mult_sat_test (a, b, c, z);

  input  signed [7:0] a, b, c;
  output signed [7:0] z;

  // Passes the parameters to the function
  parameter a_width = 8;
  parameter b_width = 8;
  parameter p_width = 8;

  // add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
  `include "DW_dp_mult_sat_function.inc"

  assign z = DWF_dp_mult_sat_tc (a, b) + c;

endmodule
```

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