

DW_fp_exp

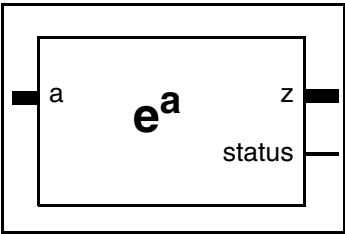
Floating-Point Exponential (e^a)

Version, STAR and Download Information: [IP Directory](#)

Features and Benefits

- The precision is controlled by parameters, and covers formats in the IEEE Standard 754
- Exponents can range from 3 to 31 bits
- Fractional part of the floating-point number can range from 2 to 57 bits
- A parameter controls the use of denormal values.

Revision History



Description

DW_fp_exp computes the exponential of a floating-point input a , delivering an output $z=e^a$, which is also a floating-point value.

A list of all the parameters used to configure this component is shown in [Table 1-2](#).

The parameter *ieee_compliance* controls the use of denormals and NaNs, as done for other FP operators in the DesignWare Library. When *ieee_compliance* = 0, the operator takes NaN values as infinities, and denormals as zeros. When *ieee_compliance* = 1, the component accepts and generates denormalized values, handles NaN inputs, and delivers NaN outputs when necessary.

Parameters *sig_width* (significand field size) and *exp_width* (exponent field size) define the floating-point format used by input and output operands. Some of these floating-point formats match the formats defined in the IEEE Standard 754.

Table 1-1 Pin Description

| Pin Name | Width | Direction | Function |
|----------|--|-----------|---|
| a | <i>sig_width</i> + <i>exp_width</i> + 1 bits | Input | Input data |
| z | <i>sig_width</i> + <i>exp_width</i> + 1 bits | Output | Exponential = e^a |
| status | 8 bits | Output | See STATUS Flags in the <i>Datapath Floating-Point Overview</i> |

Table 1-2 Parameter Description

| Parameter | Values | Description |
|------------------|----------------------|--|
| <i>sig_width</i> | 2 to 57 ^a | Word length of fraction field of floating-point numbers a and z . |
| <i>exp_width</i> | 3 to 31 | Word length of biased exponent of floating-point numbers a and z . |

Table 1-2 Parameter Description (Continued)

| Parameter | Values | Description |
|-----------------|----------------------|--|
| ieee_compliance | 0 or 1 Default: 0 | Controls the use of denormals and NaNs: 0: don't use denormals or NaNs 1: use denormals and NaNs |
| arch | 0 to 2 Default: 2 | Implementation selection. 0: area optimized 1: speed optimized 2: uses 2007.12 sub-components |

a. The synthesis model fully supports this range, as does the Verilog simulation model in VCS, but the VHDL simulation model (in all simulators) and the Verilog simulation model in non-VCS simulators are limited to a range of 2 - 35.

Table 1-3 Synthesis Implementations

| Implementation Name | Function | License Feature Required |
|---------------------|--|--------------------------|
| rtl | Implement using the Datapath Generator technology combined with static DesignWare components | DesignWare |

Table 1-4 Simulation Model

| Model | Function |
|-------------------------------|--------------------------------------|
| DW02.DW_FP_EXP_CFG_SIM | Design unit name for VHDL simulation |
| dw/dw02/src/DW_fp_exp_sim.vhd | VHDL simulation model source code |
| dw/sim_ver/DW_fp_exp.v | Verilog simulation model source code |

Given the properties of algorithms to compute the exponential function, and the goal to have a component with good QoR, this component does not have rounding mode control as other FP components in the library. The output is bounded to have 1ulp error.

The *arch* parameter controls implementation alternatives for this component. Different values result in different numerical behavior, but the error on the computed values is always bounded by 1 ulp. You should experiment with this parameter to find out which value provides the best QoR for your design constraints and technology. Using *arch* = 0 (area optimized implementation) usually provides the best QoR for most time constraints.

For information about the floating-point system defined for the floating-point components, including status flag bits and floating-point formats, refer to the [Datapath Floating-Point Overview](#).

Related Topics

- [Datapath Floating-Point Overview](#)
- [DesignWare Building Block IP Documentation Overview](#)

HDL Usage Through Component Instantiation - VHDL

```

library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DW_Foundation_comp_arith.all;

entity DW_fp_exp_inst is
    generic (
        inst_sig_width : POSITIVE := 10;
        inst_exp_width : POSITIVE := 5;
        inst_ieee_compliance : INTEGER := 0;
        inst_arch : INTEGER := 2
    );
    port (
        inst_a : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        z_inst : out std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        status_inst : out std_logic_vector(7 downto 0)
    );
end DW_fp_exp_inst;

architecture inst of DW_fp_exp_inst is

begin

    -- Instance of DW_fp_exp
    U1 : DW_fp_exp
    generic map (
        sig_width => inst_sig_width,
        exp_width => inst_exp_width,
        ieee_compliance => inst_ieee_compliance,
        arch => inst_arch
    )
    port map (
        a => inst_a,
        z => z_inst,
        status => status_inst
    );

end inst;

-- pragma translate_off
configuration DW_fp_exp_cfg_inst of DW_fp_exp_inst is
    for inst
    end for; -- inst
end DW_fp_exp_cfg_inst;
-- pragma translate_on

```

HDL Usage Through Component Instantiation - Verilog

```
module DW_fp_exp_inst( inst_a, z_inst, status_inst );

parameter inst_sig_width = 10;
parameter inst_exp_width = 5;
parameter inst_ieee_compliance = 0;
parameter inst_arch = 2;

input [inst_sig_width+inst_exp_width : 0] inst_a;
output [inst_sig_width+inst_exp_width : 0] z_inst;
output [7 : 0] status_inst;

// Instance of DW_fp_exp
DW_fp_exp #(inst_sig_width, inst_exp_width, inst_ieee_compliance, inst_arch) U1 (
    .a(inst_a),
    .z(z_inst),
    .status(status_inst) );

endmodule
```

Revision History

For notes about this release, see the [DesignWare Building Block IP Release Notes](#).

For lists of both known and fixed issues for this component, refer to the [STAR report](#).

For a version of this datasheet with visible change bars, click [here](#).

| Date | Release | Updates |
|-----------|---------------|---|
| July 2018 | O-2018.06-SP1 | <ul style="list-style-type: none">For STAR 9001366624, in Table 1-2 on page 1, clarified the range of <i>sig_width</i> for the VHDL simulation model (in all simulators) and the Verilog simulation model for non-VCS simulators.Added this Revision History table and the document links on this page |

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