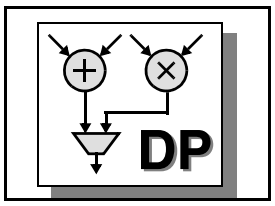

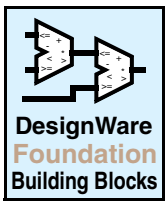

DesignWare Datapath Functions Overview

Introduction

The DesignWare Datapath Functions are a collection of HDL functions that can be called in a design's RTL code (Verilog or VHDL) in order to implement commonly used higher-level datapath functionality.

How Do DesignWare Datapath Functions Work?

DesignWare Datapath Functions are themselves written in HDL. They describe some dedicated datapath functionality in synthesizable RTL code. The functions are made available as follows:

- in VHDL through packages
- in Verilog through include files

During design elaboration, the function's HDL code is elaborated together with the design's HDL code. During compile, the elaborated design goes through regular synthesis. The sub-design described by the function is automatically optimized by datapath synthesis, together with surrounding datapath functionality.

Benefits of DesignWare Datapath Functions

Since the DesignWare Datapath Functions are written in HDL code and go through the regular synthesis flow, synthesis results are not different than directly describing the same functionality in the HDL code of the design. However, the DesignWare Datapath Functions offer the following benefits:

- **Ease-of-use:** The desired functionality can be included in the design with a simple function call instead of being written out in HDL code. This alleviates the sometimes cumbersome task of writing correct and synthesis-efficient datapath code.
- **Functional correctness:** The DesignWare Datapath Functions are pre-verified and therefore guarantee functional correctness.
- **Best QoR:** The DesignWare Datapath Functions guarantee best possible QoR because their code is optimized for datapath synthesis with Design Compiler.
- **Design integration:** The DesignWare Datapath Function's HDL code tightly integrates into surrounding datapath functionality. This allows high-level optimizations and datapath synthesis to work on larger design partitions, which helps improve QoR even further.
- **Flow integration:** The DesignWare Datapath Functions are tightly integrated into the Design Compiler's datapath synthesis flow. As a result, datapath optimization techniques, such as carry-save representations, can be fully exploited.

Differences to DesignWare Building Block IP

The DesignWare Building Block IP library has the following characteristics:

- Provides implementations for commonly used building blocks.
- Describes dedicated circuit structures that synthesis otherwise cannot generate.
- Complements synthesis.
- Building blocks are synthesized individually, not taking into account the broader design context.

In comparison, the DesignWare Datapath Functions library has the following characteristics:

- Provides easy-to-use code templates for commonly used datapath functionality.
- Describes higher-level functionality, not low-level circuit structures.
- Relies on datapath synthesis to implement the functionality efficiently.
- Functions are synthesized and optimized in a broader design context, together with surrounding datapath functionality.

DesignWare Datapath Functions Organization

The DesignWare Datapath Functions are organized in VHDL packages and Verilog include files. Two versions exist for each:

- Synthesis packages and include files are used for synthesis with Design Compiler. The code is optimized for best possible QoR. The source files are encrypted for IP protection.
- Simulation packages and include files are used for simulation, verification and third-party tools. The code is not optimized for QoR and is not intended for synthesis. The source files are not encrypted and therefore can be used as concise documentation of the functions behavior.

VHDL

The DesignWare Datapath Functions for VHDL are made available through VHDL packages. Table 1-1 summarizes the names of the packages and the corresponding source file names.

- Source files are relative to the installation path $SYNOPSYS/packages/dware/src/.
- Analyzed synthesis source files are in $SYNOPSYS/packages/dware/lib/.
- A different functions package needs to be used depending on the employed numeric package (ieee.numeric_std and ieee.std_logic_arith).

Table 1-1 VHDL Packages

Package / File Name	Numeric Package	Description
DW_dp_functions	ieee.numeric_std	Functions package
DW_dp_functions_arith	ieee.std_logic_arith	Functions package
DW_dp_functions_syn.vhd.e	ieee.numeric_std	Encrypted synthesis package file
DW_dp_functions_arith_syn.vhd.e	ieee.std_logic_arith	Encrypted synthesis package file
DW_dp_functions_sim.vhd	ieee.numeric_std	Simulation package file
DW_dp_functions_arith_sim.vhd	ieee.std_logic_arith	Simulation package file

No special setup is required for synthesis with Design Compiler (packages are automatically found). For simulation and third-party tools, the installation path has to be specified and the source files pre-analyzed accordingly.

Verilog

The DesignWare Datapath Functions for Verilog are made available through include files:

- Include files are named DW_dp_<name>_function.inc. For example, DW_dp_absval_function.inc.
- Encrypted include files for synthesis are in $SYNOPSYS/dw/syn_ver/.
- Include files for simulation are in $SYNOPSYS/dw/sim_ver/.

No special setup is required for synthesis with Design Compiler (include files are automatically found). For simulation and third-party tools, the installation path has to be specified accordingly. For verification with Formality, add `$SYNOPSYS/dw/syn_ver` to the search path.

Usage of DesignWare Datapath Functions

VHDL

DesignWare Datapath Functions are used in VHDL as follows:

- Declare the use of the DW_dp_functions package.
- Call the function in the HDL code.

Example:

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used

       entity DWF_dp_absval_test is
         port (a, b, c : in  signed(7 downto 0);
               z       : out signed(15 downto 0));
       end DWF_dp_absval_test;

       architecture rtl of DWF_dp_absval_test is
       begin
         z <= DWF_dp_absval (a * b) + c;
       end rtl;
```

Verilog

DesignWare Datapath Functions are used in Verilog as follows:

- Define the function parameters to be passed to the function.
- Include the function include file (“DW_dp_<name>_function.inc”).
- Call the function in the HDL code.

Example:

```
module DWF_dp_absval_test (a, b, c, z);

  input  signed  [7:0] a, b, c;
  output signed [15:0] z;

  // Passes the parameter to the function
  parameter width = 16;

  // add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
  `include "DW_dp_absval_function.inc"

  assign z = DWF_dp_absval (a * b) + c;

endmodule
```

Notes

- The function arguments can be arithmetic expressions themselves:

  ```
  assign z = DWF_dp_absval (a * b);
  ```

- The function call can be part of an arithmetic expression:

  ```
  assign z = DWF_dp_absval (a) + c;
  ```

- However, be careful when using functions and arithmetic expressions within the same statement to avoid unintended behavior, due to ambiguities between unsigned and signed types and expression widths. Use intermediate signals if necessary.

  ```
  assign t = a * b;
  assign z = DWF_dp_absval (t) + c;
  ```

  For more information, refer to the Coding Guidelines for Datapath Synthesis:

  http://www.synopsys.com/products/designware/dwtb/articles/coding_guidelines

- In any case (function and expression in same statement or use of intermediate signals), the function's functionality and the surrounding datapath functionality are extracted and optimized together as one large datapath partition. Typical datapath optimization techniques (such as carry-save representations) are used wherever possible and beneficial.
- Synthesis results of the DesignWare Datapath Functions are best if used in conjunction with DC Ultra, which provides the datapath optimizations referred to in this text.

Available Functions

Table 1-2 summarizes the currently available DesignWare Datapath Functions.

Table 1-2 DesignWare Datapath Functions

Function Name	Description
DWF_dp_absval DWF_dp_sub_abs	Absolute Value Subtract and Absolute Value
DWF_dp_blend DWF_dp_blend_exact DWF_dp_blend_exact2 DWF_dp_blend2 DWF_dp_blend2_exact2	Graphics Alpha Blend
DWF_dp_count_ones	Counts ones in the argument
DWF_dp_rnd DWF_dp_rndsat	Arithmetic Rounding
DWF_dp_sat DWF_dp_sati	Arithmetic Saturation
DWF_dp_mult_comb DWF_dp_mult_comb_ovfldet DWF_dp_mult_comb_sat DWF_dp_mult_ovfldet DWF_dp_mult_sat	Multiply Functions - Combined Unsigned/Signed Combined Unsigned/Signed with Overflow Detection Combined Unsigned/Signed with Saturation Multiply and Overflow Detection Multiply and Saturate
DWF_dp_sign_select	Sign Selection / Conditional Two's Complement
DWF_dp_simd_add DWF_dp_simd_addc DWF_dp_simd_mult	SIMD operations

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