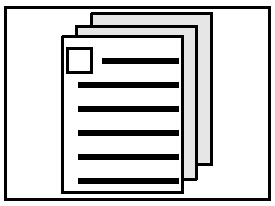
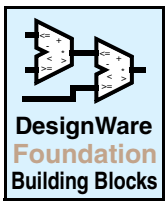




DesignWare Building Block IP Introduction

Overview of the DesignWare Library

The DesignWare Library provides designers with a comprehensive collection of synthesizable IP. The library contains the following principal ingredients for ASIC, SoC, and FPGA design and verification:

- Building Block IP (Datapath, Data Integrity, DSP, Test, and more)
- AMBA Bus Fabric and Peripherals
- Microcontrollers (8051 and 6811)

A single license gives you access to all the IP in the library. For more information on the DesignWare Library, refer to the following:

http://www.synopsys.com/IP/SoCInfrastructureIP/DesignWare/Pages/default.aspx

DesignWare Building Block IP

High-performance implementations of Basic Library components plus many components that implement more advanced arithmetic and sequential logic functions make up this library. The DesignWare Building Block IP library consists of:

- Basic Library - A set of components bundled with HDL Compiler that implements several common arithmetic and logic functions.
- Logic: Combinational and Sequential Components.
- Math: Arithmetic and Trigonometric Components.
- Memory: Registers, FIFOs, and FIFO Controllers, Synchronous and Asynchronous RAMs and Stack Components.
- Clock Domain Crossing: Synchronization Components
- Application Specific: Data Integrity, Interface, and JTAG Components.
- DSP Library - Digital filters for digital signal processing (DSP) applications.
- GTECH Library - (Genetic TECHnology Library). A technology-independent, gate-level library.

Overview of DesignWare Building Block IP

DesignWare Building Block IP is a collection of reusable intellectual property blocks that are tightly integrated into the Synopsys synthesis environment. Using these IP allows transparent, high-level optimization of performance during synthesis. With the large number of parts available, design reuse is enabled and significant productivity gains are possible.

Benefits of Using the DesignWare Building Block IP

Using these IP provides the following advantages:

- Better Quality of Results (QOR) in Synthesis – During synthesis, these IP are subject to arithmetic optimization, resource sharing, and implementation selection. Most of the IP in the Logic and Math categories include multiple synthesis implementations (architectures designed for the best speed or area results). You set the constraints, and Design Compiler automatically selects the implementation that best meets your design goals.
- Increased Productivity – Using parametrized, pre-verified DesignWare Building Block IP allows you to spend less time designing and debugging lower-level design blocks, leaving more time to evaluate higher-level design trade-offs.
- Decreased Design and Technology Risk - Design risk is greatly reduced using the Building Block pre-verified, zero defect IP. Since DesignWare Building Block IP are technology-independent, there is no technology risk.
- Increased Design Reusability - Using the DesignWare Building Block IP set of parameterized and technology independent IP allows you to re-use your proven design for subsequent projects, saving time and money, and eliminating the frustration of starting designs over from the beginning.

Characteristics

All DesignWare Building Block IP have the following characteristics:

- Pre-verified for quality
- Linked to high-level synthesis
- Parameterized in size and, for some IP, functionality
- Technology-independent

DesignWare Building Block IP supports the entire design flow by providing multiple views, including synthesizable models, simulation models, datasheets, and examples.

New and Obsoleted DesignWare Building Block IP

Refer to the current Release Notes for a list of new and obsoleted components and to the "Obsoleted DesignWare Building Block IP" topic.

The DesignWare Building Block IP library is continuously being updated with improved IP. As a result, older, inferior IP will be phased out of the libraries over two Synopsys releases and will become obsolete. These obsoleted IP are kept permanently available in the library, but are no longer recommended for use. Many obsoleted parts will have replacement IP that have upgraded functionality and usability. However, Synopsys does not make a commitment to provide direct replacement IP for every part that is obsoleted.

DesignWare Datapath and Building Block IP Documentation

The set of datasheets is intended for ASIC and systems designers who are using, or are considering using Synopsys Designware Building Block IP in conjunction with Synopsys tools. The most recent listing of DesignWare Datapath and Building Block IP documentation can be found at:

http://www.synopsys.com/dw/buildingblock.php

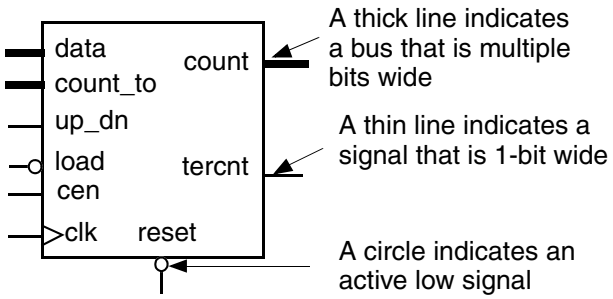
Documentation Conventions

The following conventions are used throughout the text of this document:

Table 1-1 Document Conventions

Convention	Description
italics	Indicates a place holder for some value rather than a literal string. For example, the width of bus `data` is determined by the parameter named A_width. Bus `data` is said to be *A_width* wide.
`monospace`	Used for code examples or code fragments that appear in a paragraph, command names, pin names and values.
[ ]	Denotes optional parameters. For example, `pin1 [pin2,.. pinN]` indicates that at least one pin name must be entered (`pin1`), but others are optional `[pin2,.. pinN]`.
|	Indicates a choice among alternatives, such as `low | medium | high`. This example indicates that you can enter one of three possible values for an option: `low`, `medium`, or `high`.
\	Indicates a continuation of a command line.
/	Indicates levels of directory structure.

The following diagram illustrates the conventions used in the symbol for each datasheet:



Related Publications

This document is part of a complete family of documents that are listed in the *DesignWare Building Block IP Documentation Overview*.

The following location contains all product manuals for the DesignWare Library:

https://www.synopsys.com/dw/dwlibdocs.php

More Information

For more information about DesignWare products:

- Contact your local Synopsys sales office
- To have a sales expert contact you:
  - Submit a request
  - Call: 800-388-9125
- For all Synopsys contact information, see:

  http://www.synopsys.com/Company/Pages/ContactUs.aspx

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