



# DWF\_dp\_absval function

### Absolute Value

Version, STAR and Download Information: IP Directory

### **Description**

The DWF\_dp\_absval function returns the absolute value (magnitude) of argument a. Argument a and the return value are signed (two's complement). The signed return value can be converted to an unsigned to prevent overflow. Overflow occurs for the value DWF\_dp\_absval  $(-2^{width-1}) = 2^{width-1}$ , which cannot be represented as a signed number of width bits.

#### **Table 1-1** Function Names

<b>Function Name</b>	Description	
DWF_dp_absval <sup>a</sup>	VHDL/Verilog signed (two's complement) absolute value	

a. A similar function DWF\_absval exists for DesignWare Building Blocks component DW01\_absval. However, function DWF\_dp\_absval is likely to give better QoR, especially if used inside a larger datapath context.

### Table 1-2 Argument Description

Argument Name	Туре	Width	Description
а	Vector	width	Input data
DWF_dp_absval	Vector	width	Return value

### Table 1-3 Parameter Description (Verilog)

Parameter	Values	Description
width	≥ 1	Word length of input a and return value

Verilog Include File: DW\_dp\_absval\_function.inc

# **Functional Description**

For more about DesignWare datapath functions, refer to Arithmetic - Datapath Functions Overview.

### **Related Topics**

- Arithmetic Datapath Functions Overview
- DesignWare Building Block IP Documentation Overview

### **VHDL Example**

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use DWARE.DW_dp_functions.all;
-- DWARE.DW_dp_functions_arith package if IEEE.std_logic_arith is used
entity DWF_dp_absval_test is
   port (a, b, c : in signed(7 downto 0);
        z : out signed(15 downto 0));
end DWF_dp_absval_test;
architecture rtl of DWF_dp_absval_test is
begin
   z <= DWF_dp_absval (a * b) + c;
end rtl;</pre>
```

## **Verilog Example**

```
module DWF_dp_absval_test (a, b, c, z);
input signed [7:0] a, b, c;
output signed [15:0] z;

// Passes the parameter to the function
parameter width = 16;

// add "$SYNOPSYS/dw/sim_ver" to the search path for simulation
'include "DW_dp_absval_function.inc"

assign z = DWF_dp_absval (a * b) + c;
endmodule
```

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