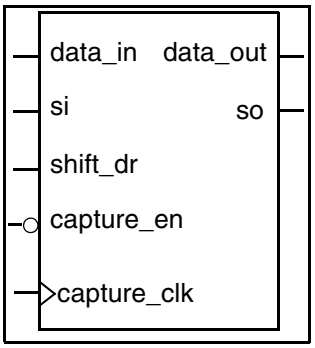
DW_bc_4

Boundary Scan Cell Type BC_4

Version, STAR and Download Information: IP Directory

Features and Benefits



- IEEE Standard 1149.1 compliant
- Synchronous or asynchronous scan cells with respect to `tck`
- Supports the standard instructions: EXTEST, SAMPLE/PRELOAD, and BYPASS

Description

DW_bc_4 is a boundary scan cell for performance-sensitive IC inputs such as clocks. It is an observe-only cell and does not support INTEST or RUNBIST instructions. The Boundary Scan Description Language (BSDL) description of this cell is of type BC_4 described in the BSDL package STD_1149_1_1990.

The cell may be synchronous or asynchronous with respect to `tck` (Test Clock system pin), depending on the port connections.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
capture_clk	1 bit	Input	Clocks data into the capture stage
capture_en	1 bit	Input	Enable for data clocked into the capture stage, active low
shift_dr	1 bit	Input	Enables the boundary scan chain to shift data one stage toward its serial output (tdo)
si	1 bit	Input	Serial path from the previous boundary scan cell
data_in	1 bit	Input	Input data from system input pin
so	1 bit	Output	Serial path to the next boundary scan cell
data_out	1 bit	Output	Output data

Table 1-2 Synthesis Implementations

Implementation Name	Function	License Feature Required
str	Synthesis model	DesignWare or Test-IEEE-STD-1149-1

Table 1-3 Simulation Models

Model	Function
DW04.DW_BC_4_CFG_SIM	Design unit name for VHDL simulation
dw/dw04/src/DW_bc_4_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_bc_4.v	Verilog simulation model source code

Table 1-4 lists the connections for asynchronous boundary scan chains.

Table 1-4 Port Connections for Asynchronous Boundary Scan Chains

DW_bc_4 Port Name	Connection
capture_clk	clock_dr from TAP controller
capture_en	Logic zero
shift_dr	shift_dr from TAP controller
si	so from previous boundary scan cell
data_in	System performance-sensitive input pin
so	si of next boundary scan cell

Table 1-5 lists the connections for synchronous boundary scan chains.

Table 1-5 Port Connections for Synchronous Boundary Scan Chains

DW_bc_4 Port Name	Connection
capture_clk	tck from system pin
capture_en	sync_capture_en from TAP controller
shift_dr	shift_dr from TAP controller
si	so from previous boundary scan cell
data_in	System performance-sensitive input pin
so	si of next boundary scan cell

Related Topics

- Application Specific – JTAG Overview
- DesignWare Building Block IP Documentation Overview

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW_bc_4_inst is
  port (inst_capture_clk : in std_logic;
        inst_capture_en  : in std_logic;
        inst_shift_dr    : in std_logic;
        inst_si          : in std_logic;
        inst_data_in     : in std_logic;
        so_inst          : out std_logic;
        data_out_inst    : out std_logic );
end DW_bc_4_inst;

architecture inst of DW_bc_4_inst is
begin

  -- Instance of DW_bc_4
  U1 : DW_bc_4
    port map (capture_clk => inst_capture_clk,
              capture_en => inst_capture_en,   shift_dr => inst_shift_dr,
              si => inst_si,   data_in => inst_data_in,   so => so_inst,
              data_out => data_out_inst );
end inst;

-- pragma translate_off
configuration DW_bc_4_inst_cfg_inst of DW_bc_4_inst is
  for inst
  end for; -- inst
end DW_bc_4_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_bc_4_inst(inst_capture_clk, inst_capture_en, inst_shift_dr,
                    inst_si, inst_data_in, so_inst, data_out_inst );

  input inst_capture_clk;
  input inst_capture_en;
  input inst_shift_dr;
  input inst_si;
  input inst_data_in;
  output so_inst;
  output data_out_inst;

  // Instance of DW_bc_4
  DW_bc_4
    U1 (.capture_clk(inst_capture_clk),   .capture_en(inst_capture_en),
        .shift_dr(inst_shift_dr),   .si(inst_si),   .data_in(inst_data_in),
        .so(so_inst),   .data_out(data_out_inst) );
endmodule
```

Copyright Notice and Proprietary Information

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the reader's responsibility to determine the applicable regulations and to comply with them.

Disclaimer

SYNOPSYS, INC., AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Trademarks

Synopsys and certain Synopsys product names are trademarks of Synopsys, as set forth at https://www.synopsys.com/company/legal/trademarks-brands.html.

All other product or company names may be trademarks of their respective owners.

Third-Party Links

Any links to third-party websites included in this document are for your convenience only. Synopsys does not endorse and is not responsible for such websites and their practices, including privacy practices, availability, and content.

Synopsys, Inc.
690 E. Middlefield Road
Mountain View, CA 94043

www.synopsys.com