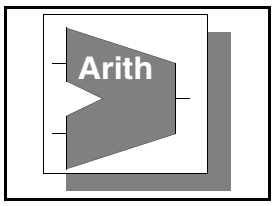
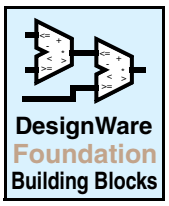




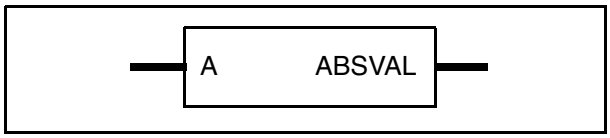
DW01_absval

Absolute Value

Version, STAR and Download Information: IP Directory

Features and Benefits

- Parameterized word length
- Inferable through a function call



Description

DW01_absval determines the absolute value of data from input port `A` and places this value on output port `ABSVAL`.

The input is assumed to be represented as a signed two's complement number. The output is represented as an unsigned number.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
A	*width* bit(s)	Input	Input data
ABSVAL	*width* bit(s)	Output	Absolute value of A

Table 1-2 Parameter Description

Parameter	Values	Function
width	≥ 1	Word length of A and ABSVAL

Table 1-3 Synthesis Implementations[a]

Implementation Name	Function	License Feature Required
rpl	Ripple-carry synthesis model	none
cla	Carry-look-ahead synthesis model	none
clf	Fast carry-look-ahead synthesis model	DesignWare

a. During synthesis, Design Compiler will select the appropriate architecture for your constraints. However, you may force Design Compiler to use any architectures described in this table. For more, see *DesignWare Building Block IP User Guide*

Table 1-4 Simulation Models

Model	Function
DW01.DW01_ABSVAL_CFG_SIM	Design unit name for VHDL simulation
dw/dw01/src/DW01_absval_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW01_absval.v	Verilog simulation model source code

Table 1-5 Truth Table (width = 3)

A(2:0)	Value of A	ABSVAL(2:0)	Value of ABSVAL
000	0	000	0
001	1	001	1
010	2	010	2
011	3	011	3
100	–4	100	4[a]
101	–3	011	3
110	–2	010	2
111	–1	001	1

a. Only correct if the result is interpreted as an unsigned number.

Related Topics

- Math – Arithmetic Overview
- DesignWare Building Block IP Documentation Overview

HDL Usage Through Function Inferencing - VHDL

```
library IEEE, DWARE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use DWARE.DW_foundation_arith.all;

entity DW01_absval_func is
  generic(width: integer:= 8);
  port( func_A : in std_logic_vector(width-1 downto 0);
        ABSVAL_func : out  std_logic_vector(width-1 downto 0) );
end DW01_absval_func;

architecture func of DW01_absval_func is
begin

  ABSVAL_func <= std_logic_vector(DWF_absval(SIGNED(func_A)));
end func;
```

HDL Usage Through Function Inferencing - Verilog

```
module DW01_absval_func (func_A, ABSVAL_func);
  parameter func_A_width = 8;

  // Passes the width to the absolute value function
  parameter width = func_A_width;

  // Please add search_path = search_path + {synopsys_root + "/dw/sim_ver"}
  // to your .synopsys_dc.setup file (for synthesis) and add
  // +incdir+$SYNOPSYS/dw/sim_ver+ to your verilog simulator command line
  // (for simulation).
  `include "DW01_absval_function.inc"

  input  [func_A_width-1 : 0] func_A;
  output [func_A_width-1 : 0] ABSVAL_func;
  assign ABSVAL_func = DWF_absval(func_A);

endmodule
```

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW01_absval_inst is
  generic ( inst_width : NATURAL := 8 );
  port ( inst_A : in std_logic_vector(inst_width-1 downto 0);
         ABSVAL_inst : out std_logic_vector(inst_width-1 downto 0) );
end DW01_absval_inst;

architecture inst of DW01_absval_inst is
begin

  -- Instance of DW01_absval
  U1 : DW01_absval
    generic map ( width => inst_width )
    port map ( A => inst_A, ABSVAL => ABSVAL_inst );
end inst;

-- pragma translate_off
configuration DW01_absval_inst_cfg_inst of DW01_absval_inst is
  for inst
  end for; -- inst
end DW01_absval_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW01_absval_inst( inst_A, ABSVAL_inst );
  parameter width = 8;

  input [width-1 : 0] inst_A;
  output [width-1 : 0] ABSVAL_inst;

  // Instance of DW01_absval
  DW01_absval #(width)
    U1 ( .A(inst_A), .ABSVAL(ABSVAL_inst) );

endmodule
```

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