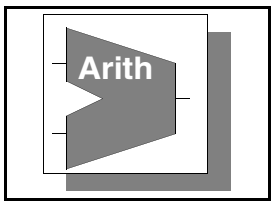
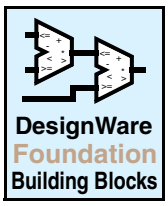




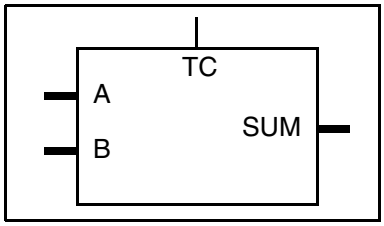
DW02_prod_sum

Generalized Sum of Products

Version, STAR and Download Information: IP Directory

Features and Benefits

- Parameterized number of inputs
- Parameterized word length



Applications

- Digital filtering
- Matrix multiplication
- Graphics

Description

DW02_prod_sum performs a summation of a set of products ($A(i) \times B(i)$).

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
A	*A_width* × *num_inputs* bit(s)	Input	Concatenated input data
B	*B_width* × *num_inputs* bit(s)	Input	Concatenated input data
TC	1 bit	Input	Two's complement 0 = unsigned 1 = signed
SUM	*SUM_width* bit(s)	Output	Sum of products

Table 1-2 Parameter Description

Parameter	Values	Description
A_width	≥ 1	Word length of A
B_width	≥ 1[a]	Word length of B
num_inputs	≥ 1	Number of inputs
SUM_width	≥ 1	Word length of SUM

a. For nbw implementation, *A_width* + *B_width* ≤ 36. Due to concern of implementation selection run time, a limitation is set for *A_width* and *B_width*.

Table 1-3 Synthesis Implementations[a]

Implementation	Function	License Feature Required
pparch	Delay-optimized flexible Booth Wallace	DesignWare
apparch	Area-optimized flexible architecture that can be optimized for area, for speed, or for area, speed	DesignWare

a. During synthesis, Design Compiler will select the appropriate architecture for your constraints. However, you may force Design Compiler to use any architectures described in this table. For more, see *DesignWare Building Block IP User Guide*

Table 1-4 Obsolete Synthesis Implementations[a]

Implementation	Function	Replacement Implementation
csa	Carry-save array synthesis model	pparch
wall	Booth-recoded Wallace-tree synthesis model[b]	pparch
nbw	Either a non-Booth (*A_width* + *B_width* ≤ 41) or a Booth Wallace-tree (*A_width* + *B_width* > 41) synthesis model[c]	pparch

a. DC versions and DesignWare EST releases linked to DC versions prior to 2007.03 will still incude these implementations.
b. In most cases the wall implementation generates both faster and smaller circuits for medium- to large-sized multipliers.
c. In cases where *A_width* + *B_width* ≤ 41, the nbw implementation generates a non-Booth recoded Wallace-tree multiplier. For multipliers having products larger than 41 bits (such as, *A_width* + *B_width* > 41) the nbw implementation produces a Booth-recoded multiplier identical to the wall implementation.

Table 1-5 Simulation Models

Model	Function
DW02.DW02_PROD_SUM_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW02_prod_sum_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW02_prod_sum.v	Verilog simulation model source code

The equation for SUM is:

$$\mathrm{SUM}(k\text{-}1{:}0) = \sum_{j=0}^{N-1} \mathrm{A}[(j+1)\times m\text{-}1{:}j\times m]\times \mathrm{B}[(j+1)\times n\text{-}1{:}j\times n]$$

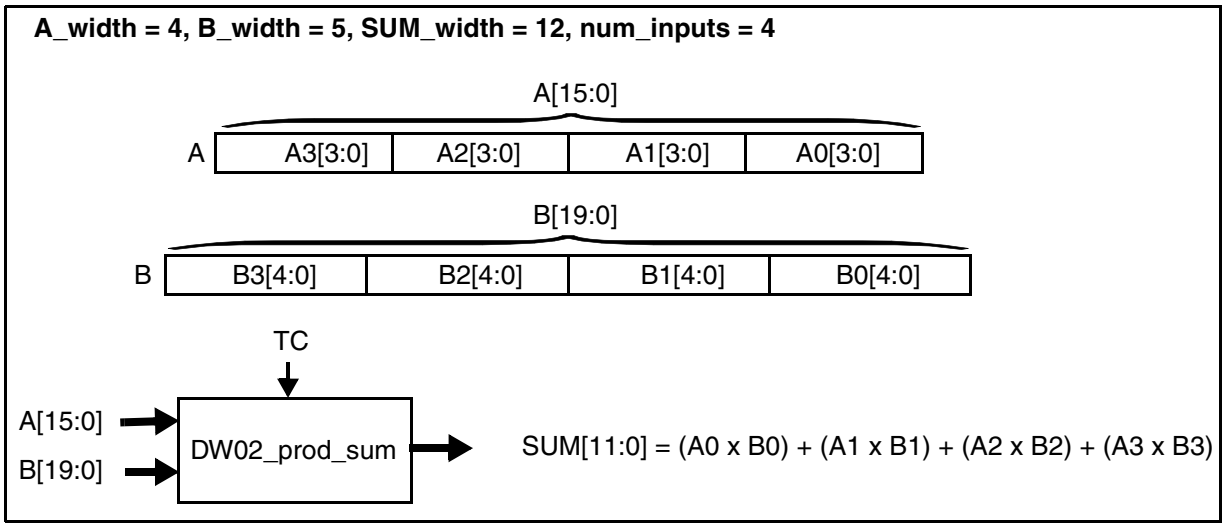
where:

m = A_width n = B_width
N = num_inputs k = SUM_width

The set of coefficients to be multiplied and summed must be concatenated into two vectors, each with a length of *num_inputs* × *A_width* and *num_inputs* × *B_width*. These two vectors are connected to the A and B pins.

Internally, DW02_prod_sum disassembles the individual words from A and B and then performs the sum of products. The control signal TC determines whether the input and output data is interpreted as unsigned numbers (TC=0) or signed (TC=1).

Figure 1-1 Functional Operation



Related Topics

- Math – Arithmetic Overview
- DesignWare Building Block IP Documentation Overview

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_foundation_comp.all;

entity DW02_prod_sum_inst is
  generic ( inst_A_width : NATURAL := 5;
            inst_B_width : NATURAL := 5;
            inst_num_inputs : POSITIVE := 3;
            inst_SUM_width : NATURAL := 12 );
  port (inst_A   : in std_logic_vector
                                  (inst_num_inputs*inst_A_width-1 downto 0);
        inst_B   : in std_logic_vector
                                  (inst_num_inputs*inst_B_width-1 downto 0);
        inst_TC  : in std_logic;
        SUM_inst : out std_logic_vector(inst_SUM_width-1 downto 0) );
end DW02_prod_sum_inst;

architecture inst of DW02_prod_sum_inst is
begin

  -- Instance of DW02_prod_sum
  U1 : DW02_prod_sum
    generic map (A_width => inst_A_width,  B_width => inst_B_width,
                 num_inputs => inst_num_inputs, SUM_width => inst_SUM_width )
    port map ( A => inst_A,  B => inst_B,  TC => inst_TC,  SUM => SUM_inst );
end inst;

-- pragma translate_off
configuration DW02_prod_sum_inst_cfg_inst of DW02_prod_sum_inst is
  for inst
  end for; -- inst
end DW02_prod_sum_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW02_prod_sum_inst( inst_A, inst_B, inst_TC, SUM_inst );

  parameter A_width = 5;
  parameter B_width = 5;
  parameter num_inputs = 3;
  parameter SUM_width = 12;

  input [num_inputs*A_width-1 : 0] inst_A;
  input [num_inputs*B_width-1 : 0] inst_B;
  input inst_TC;
  output [SUM_width-1 : 0] SUM_inst;

  // Instance of DW02_prod_sum
  DW02_prod_sum #(A_width, B_width, num_inputs, SUM_width)
    U1 ( .A(inst_A), .B(inst_B), .TC(inst_TC), .SUM(SUM_inst) );

endmodule
```

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