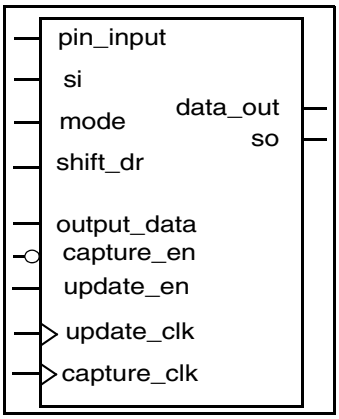
DW_bc_10

Boundary Scan Cell Type BC_10

Version, STAR and Download Information: IP Directory

Features and Benefits



- IEEE Standard 1149.1-2001 compliant
- Synchronous or asynchronous scan cells with respect to `tck`
- Supports the standard instructions: EXTEST, SAMPLE/PRELOAD, and BYPASS
- Supports the optional instructions RUNBIST, CLAMP, and HIGHZ

Description

DW_bc_10 is a boundary scan cell, lacking INTEST support, that can be used to monitor a signal at the corresponding pin instead of the signal driven from the system logic.

The Boundary Scan Description Language (BSDL) description of this cell is of type bc_10 described in the BSDL package STD_1149_1_2001.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
capture_clk	1 bit	Input	Clocks data into the capture stage
update_clk	1 bit	Input	Clocks data into the update stage
capture_en	1 bit	Input	Enable for data clocked into the capture stage, active low
update_en	1 bit	Input	Enable for data clocked into the update stage, active high
shift_dr	1 bit	Input	Enables the boundary scan chain to shift data one stage toward its serial output (tdo)
mode	1 bit	Input	Determines whether `data_out` is controlled by the boundary scan cell or by the `data_in` signal
si	1 bit	Input	Serial path from the previous boundary scan cell
pin_input	1 bit	Input	IC system input pin
output_data	1 bit	Input	IC output logic signal
data_out	1 bit	Output	Output data
so	1 bit	Output	Serial path to the next boundary scan cell

Table 1-2 Synthesis Implementations

Implementation Name	Function	License Feature Required
str	Synthesis model	DesignWare or Test-IEEE-STD-1149-1

The DW_bc_10 cell may be synchronous or asynchronous with respect to `tck` (Test Clock system pin), depending on the port connections. Table 1-4 on page 2 lists the connections for asynchronous boundary scan chains. Table 1-5 on page 3 lists the connections for synchronous boundary scan chains.

The `mode` signal gives the Test Access Port (TAP) instructions control of the boundary scan cell. Table 1-3 lists the required values of the `mode` signal for each of the TAP instructions that DW_bc_10 supports. The INTEST instruction is not supported if the cell is used as an output cell.

Table 1-3 Mode Signal Generation for DW_bc_10

Instruction	Mode for Input Cell
EXTEST	1
SAMPLE/PRELOAD	0
CLAMP	1
RUNBIST	1
BYPASS	0

Table 1-4 lists the connections for asynchronous boundary scan chains.

Table 1-4 Port Connections for Asynchronous Boundary Scan Chains

DW_bc_10 Port Name	Connection
capture_clk	clock_dr from TAP controller
update_clk	update_dr from TAP controller
capture_en	Logic zero
update_en	Logic one
shift_dr	shift_dr from TAP controller
mode	Mode generation logic
si	so from previous boundary scan cell
pin_input	System input pin for input cells or IC output logic for output cells
output_data	IC output logic
data_out	System output pin
so	si of next boundary scan cell

Table 1-5 lists the connections for synchronous boundary scan chains.

Table 1-5 Port Connections for Synchronous Boundary Scan Chains

DW_bc_10 Port Name	Connection
capture_clk	tck from system pin
update_clk	tck_n from system pin
capture_en	sync_capture_en from TAP controller
update_en	sync_update_dr from TAP controller
shift_dr	shift_dr from TAP controller
mode	Mode generation logic
si	so from previous boundary scan cell
pin_input	System input pin for input cells or IC output logic for output cells
output_data	IC output logic
data_out	System output pin
so	si of next boundary scan cell

Related Topics

- Application Specific – JTAG Overview
- DesignWare Building Block IP Documentation Overview

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DW_Foundation_comp_arith.all;

entity DW_bc_10_inst is
  port (inst_capture_clk : in  std_logic;
        inst_update_clk  : in  std_logic;
        inst_capture_en  : in  std_logic;
        inst_update_en   : in  std_logic;
        inst_shift_dr    : in  std_logic;
        inst_mode        : in  std_logic;
        inst_si          : in  std_logic;
        inst_pin_input   : in  std_logic;
        inst_output_data : in  std_logic;
        data_out_inst    : out std_logic;
        so_inst          : out std_logic );
end DW_bc_10_inst;

architecture inst of DW_bc_10_inst is
begin
  -- Instance of DW_bc_10
  U1 : DW_bc_10
    port map (capture_clk => inst_capture_clk,
              update_clk  => inst_update_clk,
              capture_en  => inst_capture_en,
              update_en   => inst_update_en,
              shift_dr    => inst_shift_dr,
              mode        => inst_mode,
              si          => inst_si,
              pin_input   => inst_pin_input,
              output_data => inst_output_data,
              data_out    => data_out_inst,
              so          => so_inst );
end inst;

-- pragma translate_off
configuration DW_bc_10_inst_cfg_inst of DW_bc_10_inst is
  for inst
  end for; -- inst
end DW_bc_10_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - VHDL

```
module DW_bc_10_inst(inst_capture_clk, inst_update_clk, inst_capture_en,
                     inst_update_en, inst_shift_dr, inst_mode, inst_si,
                     inst_pin_input, inst_output_data, data_out_inst,
                     so_inst );

  input inst_capture_clk;
  input inst_update_clk;
  input inst_capture_en;
  input inst_update_en;
  input inst_shift_dr;
  input inst_mode;
  input inst_si;
  input inst_pin_input;
  input inst_output_data;
  output data_out_inst;
  output so_inst;

  // Instance of DW_bc_10
  DW_bc_10
    U1 (.capture_clk(inst_capture_clk),
        .update_clk(inst_update_clk),
        .capture_en(inst_capture_en),
        .update_en(inst_update_en),
        .shift_dr(inst_shift_dr),
        .mode(inst_mode),
        .si(inst_si),
        .pin_input(inst_pin_input),
        .output_data(inst_output_data),
        .data_out(data_out_inst),
        .so(so_inst) );
endmodule
```

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