



# Datapath–Arithmetic Overview

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The Datapath arithmetic DesignWare Building Block IP, many of which are inferred, are applicable to ASIC or SoC designs. These IP are high-performance arithmetic implementations (based on a fast carry look-ahead architecture) to augment those in the Basic IP Library. The Basic IP Library is included in your (V)HDL Compiler product.

Most IP in this category have multiple architectures for each function (architecturally optimized for either performance or area). This provides you with the best architecture for your design goals. All IP have a parameterized word length.

## Related Topics

For a listing of Building Block components and associated datasheets, see:

- [DesignWare Building Block IP Documentation Overview](#)

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