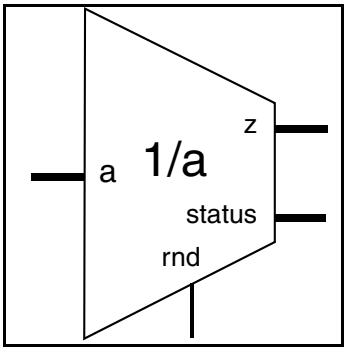
DW_fp_recip

Floating-Point Reciprocal

Version, STAR and Download Information: IP Directory

Features and Benefits

- The precision format is parameterizable for either IEEE single, double precision, or a user-defined custom format
- Hardware for denormal numbers of IEEE 754 standard is selectively provided
- Both IEEE 754 standard rounding modes and the faithful rounding with 1 ulp error are supported
- Accuracy conforms to IEEE 754 Floating-point standard



Description

DW_fp_recip is a floating-point reciprocal unit that calculates `z = 1/a` where `a` is a floating-point value. DW_fp_recip supports the IEEE 754 compatible rounding modes as well as the faithful rounding that admits maximum 1 ulp error. The input `rnd` is valid only when the parameter *faithful_round* = 0. The output `status` is an 8-bit vector of status flags.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
a	*exp_width* + *sig_width* + 1 bits	Input	Divisor
rnd	3 bits	Input	Rounding mode (rnd takes effect only when *faithful_round* = 0)
z	*exp_width* + *sig_width* + 1 bits	Output	Quotient of 1/a
status	8 bits	Output	See STATUS Flags in the *Datapath Floating-Point Overview*

Table 1-2 Parameter Description

Parameter	Values	Description
sig_width	2 to 60 bits	Word length of fraction field of floating-point numbers `a`, and `z`
exp_width	3 to 31 bits	Word length of biased exponent of floating-point numbers `a`, and `z`
ieee_compliance	0 or 1 Default: 0	When 1, the generated architecture includes the use of denormals and NaNs.

Table 1-2 Parameter Description (Continued)

Parameter	Values	Description
faithful_round	0 or 1 Default: 0	Select the faithful rounding that admits maximum 1 ulp error. 0: Support all rounding modes described in *Datapath Floating-point Overview* 1: Results have 1 ulp error

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
rtl	Synthesis model	DesignWare

Table 1-4 Simulation Models

Model	Function
DW02.DW_FP_RECIP_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW_fp_recip_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_fp_recip.v	Verilog simulation model source code

Table 1-5 summarizes the error ranges with the rounding modes supported by DW_fp_recip. The output of DW_fp_recip, z, is a rounded value from the internal calculated value, so there exists a numerical error between z and the actual value of 1/a. Depending on the rounding modes, the error ranges are slightly different, but the absolute error ranges of less than 1 *ulp* are guaranteed.

Table 1-5 Error Ranges ($\varepsilon = z - 1/a$)

faithful_round	RND	Mode	Error (ε)	Absolute Error $\lvert\varepsilon\rvert$
0	0	Round to Nearest Even	$-0.5\ ulp \le \varepsilon \le 0.5\ ulp$[a]	$\lvert\varepsilon\rvert \le 0.5\ ulp$
	1	Round to Zero	$-1\ ulp < \varepsilon \le 0$ if $z > 0$ $0 \le \varepsilon < 1\ ulp$ if $z < 0$	$\lvert\varepsilon\rvert \le 1\ ulp$
	2	Round to +Inf.	$0 \le \varepsilon < 1\ ulp$	$\lvert\varepsilon\rvert \le 1\ ulp$
	3	Round to -Inf.	$-1\ ulp < \varepsilon \le 0$	$\lvert\varepsilon\rvert \le 1\ ulp$
	4	Round to Nearest Up	$-0.5\ ulp < \varepsilon \le 0.5\ ulp$	$\lvert\varepsilon\rvert \le 0.5\ ulp$
	5	Round Away from Zero	$0 \le \varepsilon < 1\ ulp$ if $z > 0$ $-1\ ulp < \varepsilon \le 0$ if $z < 0$	$\lvert\varepsilon\rvert \le 1\ ulp$
1	-		$-1\ ulp < \varepsilon < 0.5\ ulp$	$\lvert\varepsilon\rvert \le 1\ ulp$

a. $\varepsilon = \pm 0.5\ ulp$ depends on the position of the nearest even floating-point number.

DW_fp_recip provides the hardware for denormal numbers and NaNs of IEEE 754 standard. If the parameter *ieee_compliance* is turned off, denormal numbers are considered as zeros, and NaNs are considered as infinity. Otherwise, denormal numbers and NaNs become effective and additional hardware to manipulate denormal numbers is integrated.

For more information about the floating-point system defined for all the DW_fp components, including `status` flag bits, and integer and floating-point formats, refer to the *Datapath Floating-Point Overview*.

Alternative Implementation of Floating-point Reciprocal using DW_lp_fp_multifunc

The floating-point reciprocal operation can also be implemented by DW_lp_fp_multifunc component (a member of the minPower Library, licensed separately), which evaluates the value of floating-point reciprocal with 1 ulp error bound. There will be 1 ulp difference between the value from DW_lp_fp_multifunc and the value from DW_fp_recip. Performance and area of the synthesis results are different between the DW_fp_recip and reciprocal implementation of the DW_lp_fp_multifunc, depending on synthesis constraints, library cells and synthesis environments. By comparing performance and area between the reciprocal implementation of DW_lp_fp_multifunc and DW_fp_recip component, the DW_lp_fp_multifunc provides more choices for the better synthesis results. Below is an example of the Verilog description for the floating-point reciprocal of the DW_lp_fp_multifunc. For more detailed information, see the DW_lp_fp_multifunc datasheet.

```
DW_lp_fp_multifunc #(sig_width, exp_width, ieee_compliance, 1, 1, faithful_round) U1 (
    .A(A),
    .FUNC(16'h0001),
    .RND(RND),
    .Z(Z),
    .STATUS(STATUS)
);
```

Related Topics

- Datapath Floating-Point Overview
- DesignWare Building Block IP Documentation Overview

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DWpackages.all;
use DWARE.DW_Foundation_comp_arith.all;

entity DW_fp_recip_inst is
      generic (
        inst_sig_width : POSITIVE := 23;
        inst_exp_width : POSITIVE := 8;
        inst_ieee_compliance : INTEGER := 0;
        inst_faithful_round : INTEGER := 0
        );
      port (
        inst_a : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        inst_rnd : in std_logic_vector(2 downto 0);
        z_inst : out std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        status_inst : out std_logic_vector(7 downto 0)
        );
    end DW_fp_recip_inst;


architecture inst of DW_fp_recip_inst is

begin

    -- Instance of DW_fp_recip
    U1 : DW_fp_recip
    generic map (
          sig_width => inst_sig_width,
          exp_width => inst_exp_width,
          ieee_compliance => inst_ieee_compliance,
          faithful_round => inst_faithful_round
          )
    port map (
          a => inst_a,
          rnd => inst_rnd,
          z => z_inst,
          status => status_inst
          );


end inst;
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_fp_recip_inst( inst_a, inst_rnd, z_inst, status_inst );

parameter inst_sig_width = 23;
parameter inst_exp_width = 8;
parameter inst_ieee_compliance = 0;
parameter inst_faithful_round = 0;


input [inst_sig_width+inst_exp_width : 0] inst_a;
input [2 : 0] inst_rnd;
output [inst_sig_width+inst_exp_width : 0] z_inst;
output [7 : 0] status_inst;

    // Instance of DW_fp_recip
    DW_fp_recip #(inst_sig_width, inst_exp_width, inst_ieee_compliance,
inst_faithful_round) U1 (
                .a(inst_a),
                .rnd(inst_rnd),
                .z(z_inst),
                .status(status_inst) );

endmodule
```

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