**Robert Karmazin**

rob@csl.cornell.edu

100 Graham Road, Apt 7H

Ithaca, NY 14850

631-258-8961

Research Interests

Asynchronous circuits and systems, Computer Architecture, VLSI methodology, Computer-aided design, Hardware security, Memory systems, Optimization

Education

**Cornell University** May 2015

Ph.D. in Electrical and Computer Engineering

Advisor: Dr. Rajit Manohar

Thesis: Automating the Physical Design of Asynchronous Circuits

**The Johns Hopkins University** May 2006

B.S. in Electrical and Computer Engineering

Advisor: Dr. Ralph Etienne-Cummings

Professional Experience

**Cornell University** August 2006 – Present

*Graduate Research Assistant Ithaca, NY*

Developed CAD software to automate the physical implementation of DRC clean custom asynchronous digital logic. Designed configuration memory subsystems for multiple iterations of an asynchronous FPGA at multiple technology nodes. Integrated asynchronous circuits with acoustic MEMS devices for IARPA TIC program.

**Cornell University** 2013-2015

*Professional Reviewer Ithaca, NY*

Reviewed paper submissions for: ASP-DAC 2015, HPCA 2014, ASYNC 2013, 2014

**ZMD-A** June 2006 – August 2006

*Intern Melville, NY*

Ported existing two-stage high-accuracy ADC design to new technology node. Simulated various components to determine bandwidth and power improvements over original design.

**Johns Hopkins Applied Physics Laboratory** June 2005 – August 2005

*Undergraduate Intern Laurel, MD*

Implemented various MATLAB functions and procedures in C to optimize execution time. Included additional type checking and interfacing to MATLAB programming environment.

Teaching Experience

**Cornell University** August 2006 – December 2007

*Student Mentor Ithaca, NY*

Guided M.Eng. student who developed hardware and software testing infrastructure for split-foundry asynchronous FPGA. Work included designing PCB to interface test chip to Raspberry Pi and writing low level software drivers for Raspberry Pi.

**Cornell University** May 2011 – July 2011

*Student Advisor Ithaca, NY*

Advised M.S. student who wrote a channel router used for connecting multiple pipeline stages, optimizing for total required routing area. Capable of handling obstacles within routing channel.

**Cornell University** August 2006 – December 2007

*Teaching Assistant Ithaca, NY*

Lead laboratory sessions for introductory digital logic and design course. Held regular office hours and graded homeworks, reports, and exams.

Chips

1. Split Foundry Asynchronous FPGA, 65nm 2014

Implemented three asynchronous FPGAs, each with unique transistor-level obfuscation strategies, as part of the IARPA TIC program. Achieved 550 MHz throughput.

1. Split Foundry Asynchronous FPGA, 130nm 2013

Implemented asynchronous FPGA as part of the IARPA TIC program. Demonstrated usability of custom layout flow. Achieved 270MHz throughput.

1. Ultra Low-Power Sensor Network Asynchronous Processor, 90nm 2011

Designed and implemented chip IO for ULSNAP processor. Implemented full custom layout for processor core and periphery. Achieved 97 MIPS at 4mW.

1. SyNAPSE, 45nm 2011

Validated and implemented various components for address demux unit in the SyNAPSE chip.

1. Hybrid FPGA, 65nm 2010

Designed, validated, and implemented configuration memory for FPGA-Processor hybrid as part of an AFRL collaboration. Achieved 700MHz throughput in extracted simulation.

Publications

1. Timing Driven Placement for Quasi Delay-Insensitive Circuits

**Robert Karmazin**, Stephen Longfield, Carlos Tadeo Ortega Otero, and Rajit Manohar

International Symposium on Asynchronous Circuits and Systems, (In Review)

1. Automatic Obfuscated Cell Layout for Trusted Split-Foundry Design

Carlos Tadeo Ortega Otero, Jonathan Tse, **Robert Karmazin**, and Rajit Manohar

International Symposium on Hardware-Oriented Security and Trust, (In Review)

1. ULSNAP: An Ultra-Low Power Event-Driven Microcontroller for Sensor Network Nodes

Carlos Tadeo Ortega Otero, Jonathan Tse, **Robert Karmazin**, and Rajit Manohar

Proceedings of the International Symposium on Quality Electronic Design, March 2014

1. A Split-Foundry Asynchronous FPGA

Benjamin Hill, **Robert Karmazin**, Carlos Tadeo Ortega Otero, Jonathan Tse, and Rajit Manohar

Cusom Integrated Circuits Conference, September 2013

1. cellTK: Automated Layout for Asynchronous Circuits with Nonstandard Cells

**Robert Karmazin**, Carlos Tadeo Ortega Otero, and Rajit Manohar

International Symposium on Asynchronous Circuits and Systems, May 2013

1. Neural Spiking Dynamics in Asynchronous Digital Circuits

Nabil Imam, Kyle Wecker, Jonathan Tse, **Robert Karmazin**, Carlos Tadeo Ortega Otero, and Rajit Manohar

International Joint Conference on Neural Networks, August 2013

1. Overcoming Single-Thread Performance Hurdles in the Core Fusion Reconfigurable Multicore Architecture

Janani Mukundan, Saugata Ghose, **Robert Karmazin**, Engin Ipek, and José Martínez

International Joint Conference on Neural Networks, August 2013

Patents

1. Automated Layout for Integrated Circuits with Nonstandard Cells

Rajit Manohar, **Robert Karmazin**, Carlos Tadeo Ortega Otero

WIPO Patent Published WO 2014/186803 A1, 20 Nov 2014

Skills

Programming: C, C++, Python, MATLAB, Verilog, VHDL, Java, TCL

Design: Micromagic, Cadence Virtuoso, HSPICE, Calibre, Quartus, Encounter, Eagle PCB

Platforms: Windows, Linux, Raspberry Pi, Arduino, PIC