Khayle Torres

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EDUCATION

09/2019 – present — **MEng Electrical and Information Engineering** — London, United Kingdom
Imperial College London
- Currently average a 1st in Second Year
- Modules of Interest (Y2): Information Processing, Discrete Maths (Complexity Theory in Programming), Control Engineering
- Modules of Interest (Y1): Digital Electronics and Computer Architecture, Programming for Engineers (C++)

09/2017 – 06/2019 — **A Levels** — London, United Kingdom
St Pauls Catholic College
- Further Maths - A
- Maths - A*
- Physics - A

SKILLS

Technical Skills
- C++/ Matlab / Python / Verilog (Advanced)
- C / C# / MIPS & MU0 Assembly / Flex / Bison / Yacc / Lex / Quartus Prime Lite (Intermediate)
- SQL / Python / AWS (Beginner)
- Experienced Working with Github & Bash Scripts

Other Skills
- Good with Physics scripting, Animation, UI in Unity
- Fluent in English and Tagalog

PROFESSIONAL EXPERIENCE

10/2020 – present — **Remote Academic Tutoring** — London, United Kingdom
Mytutor
- Tutored multiple students in STEM related subjects. Primarily focused on Maths in both A level and GCSEs

07/2018 – 08/2018 — **Internship** — Surrey, United Kingdom
OTM Servo (
- Used CAD software to model a specific part of an actuator to get a better idea of model design
- Helped with the machinery and assembly of components

PROJECTS

05/2021 – 06/2021 — **MARS Rover Project**
- Combines multiple subsystems in order to make a fully autonomous Rover that can detect objects, send encrypted data to and from a server, and be controlled remotely using distance calculations or remote control
- https://github.com/sts219/Debonair

02/2021 – 03/2021 — **Intel DE10-Lite FPGA Game**
- Created a game that can be played remotely using a DE10-Lite board as the controller
- Uses TCP/IP, Unity, Quartus, AWS and multiple languages to allow the game to work.
- https://github.com/sts219/World_of_DE10s

11/2020 – 12/2020 — **MIPS CPU**
- Created two CPUs that follows the MIPS architecture specification (Revision 3.2). Asynchronous and Synchronous
- Avalon compatible memory interface
- the Synchronous CPU is built using the Asynchronous CPU and a wrapper
- https://github.com/xw2519/ISA-MIPS-coursework

02/2021 – 03/2021 — **C to MIPS Compiler**
- Lexer designed from scratch, Parser heavily influenced by ANSI C Parser
- Uses Flex, Bison, Make and C++ for the contents
- https://github.com/kt1719/C-to-MIPS

05/2020 – 06/2020 — **CPU Architecture**
- Created a fully functional CPU in Quartus with its own architecture that is efficient for the specific tasks given in the specification
- The CPU has its own Fibonacci, Multiply, Divide and Linked List function on top of the base instruction set created