ECE 425 VLSI Circuit Design Lab 4 prelab

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Truth table

Operation	op6	op5	op4	op3	op2	op1	op0
AND	0	0	0	1	–	0	0
OR	0	0	0	1	–	0	1
NOR	1	0	0	0	–	0	0
XOR	0	0	0	0	–	0	0
ADD	0	1	0	1	0	0	0
SUB	1	0	1	0	1	0	0
SLT	0	0	0	0	–	0	0

Table 1 – Partial Function Table for Alternative ALU

Slicing plan