ECE 425 VLSI Circuit Design Lab 1

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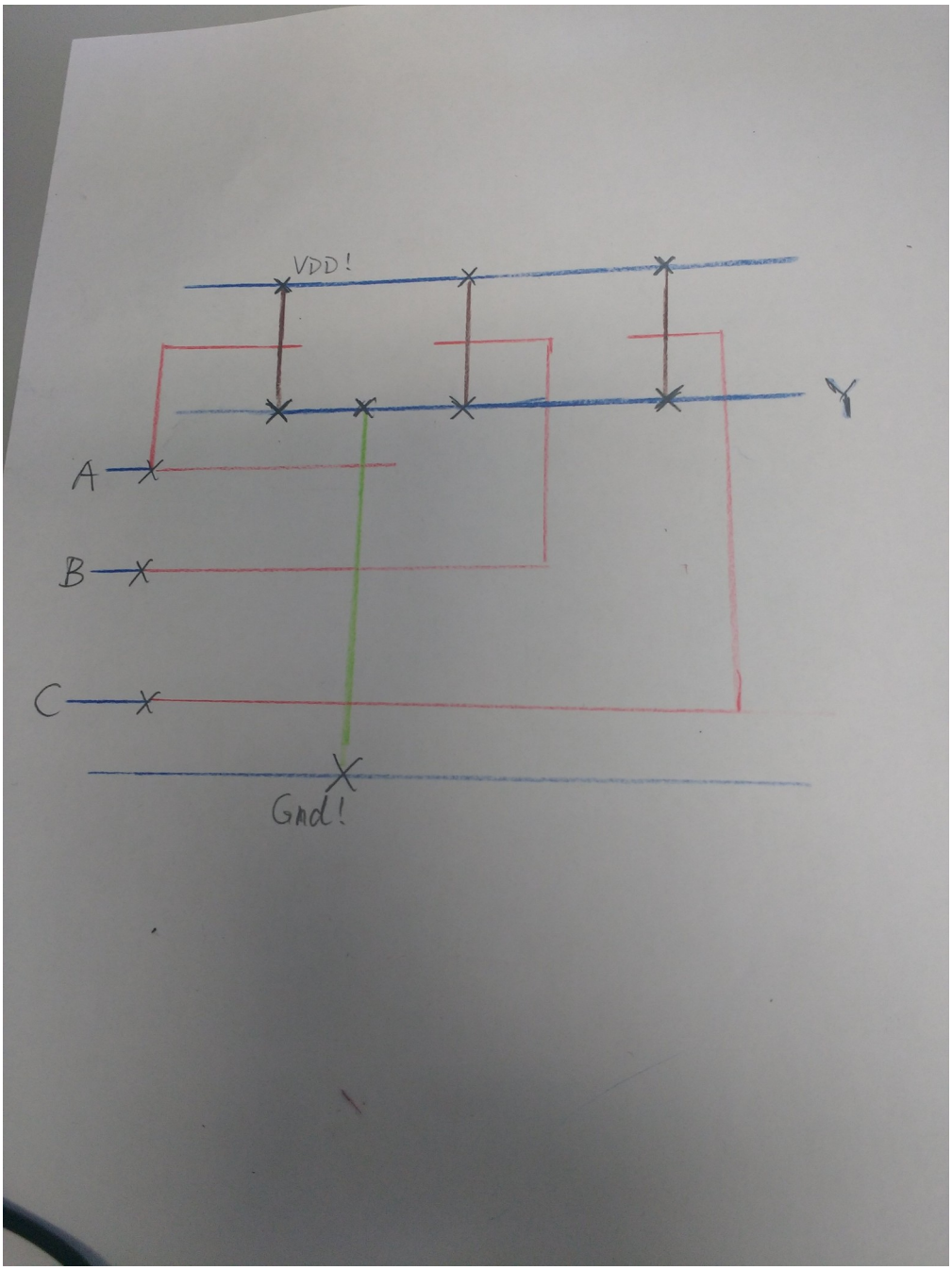
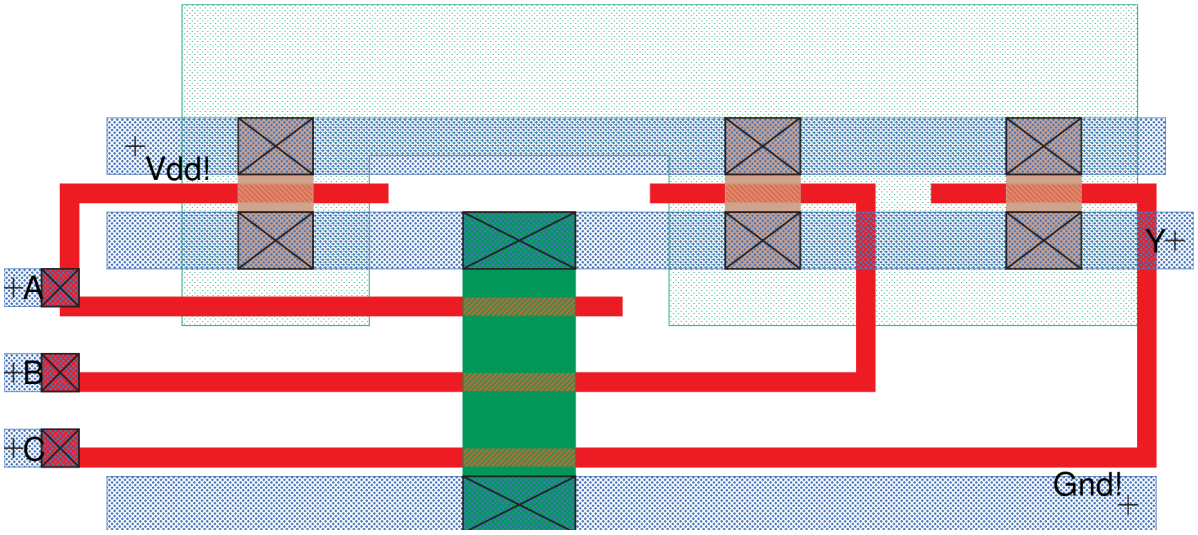
Time: Jan,31,2017

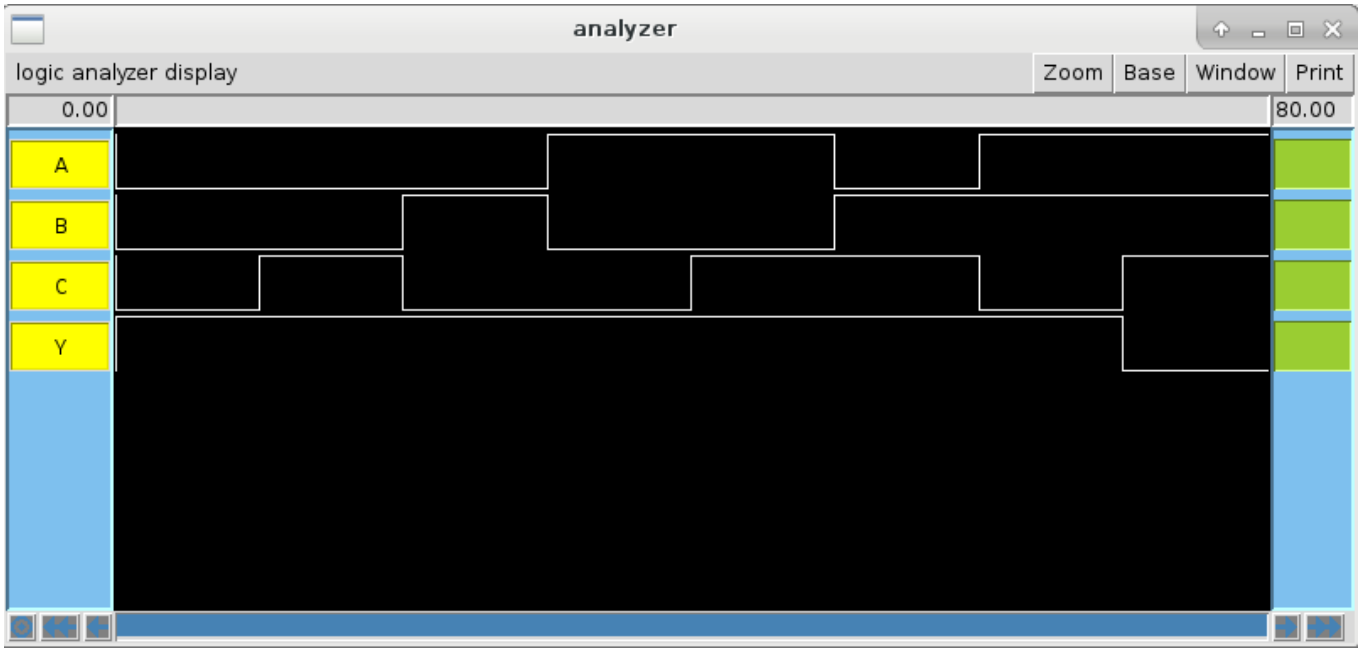
3-inputs NAND gate sticky diagram



3-inputs NAND gate diagram



3-inputs NAND gate results

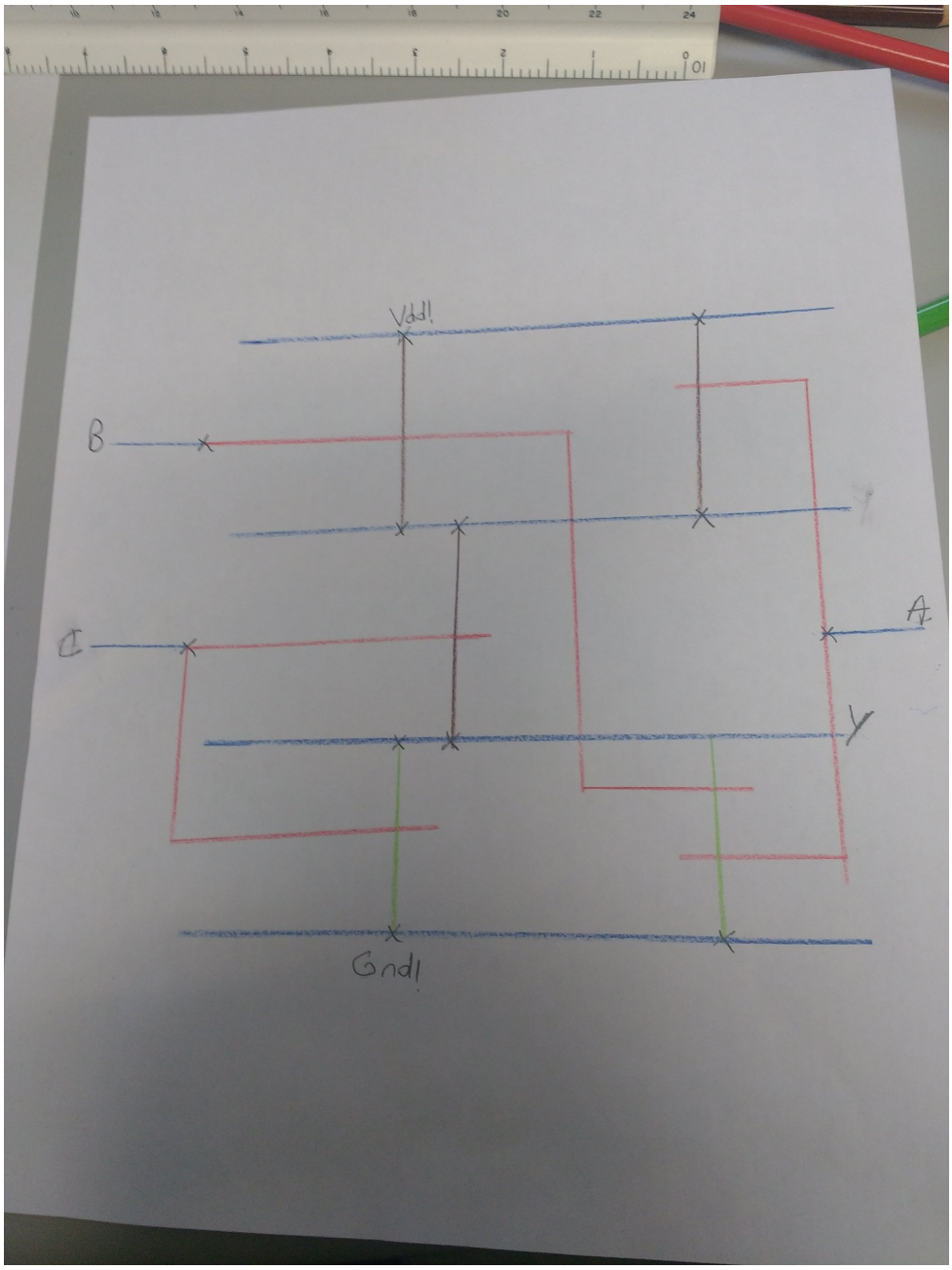


The cell sizes and are of 3-inputs NAND gate:

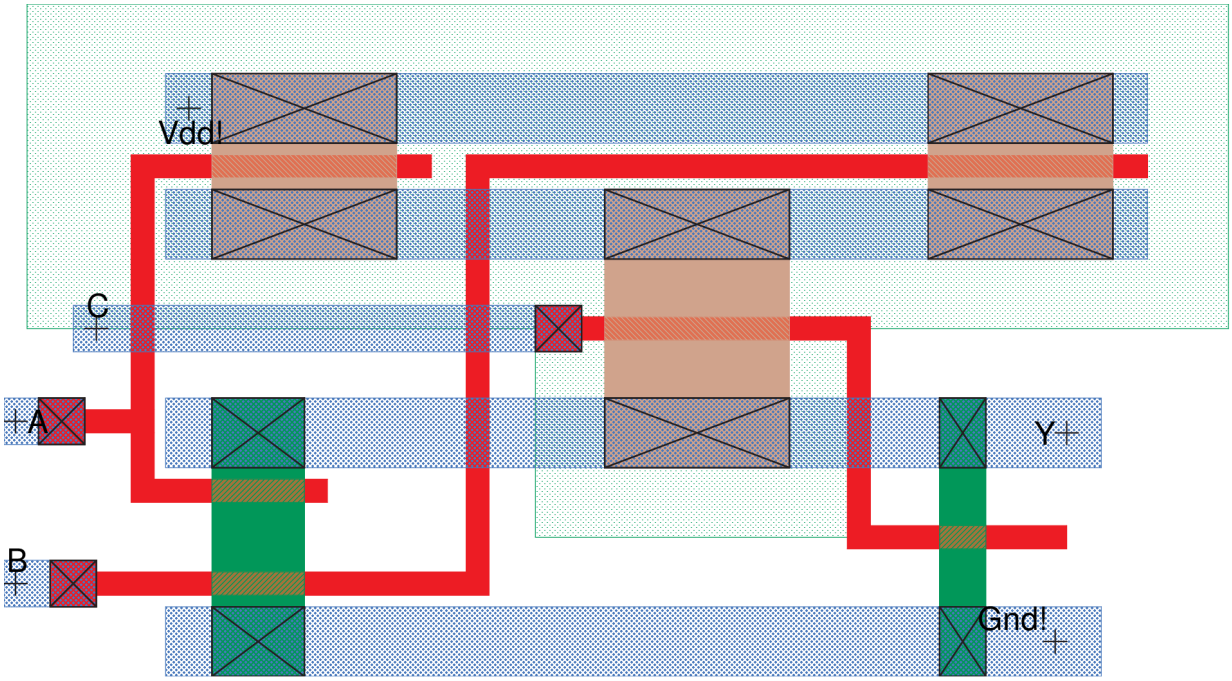
Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)

microns: 38.10 x 16.80 (-24.30, -6.60), (13.80, 10.20) 640.08
lambda: 127 x 56 (-81, -22), (46, 34) 7112

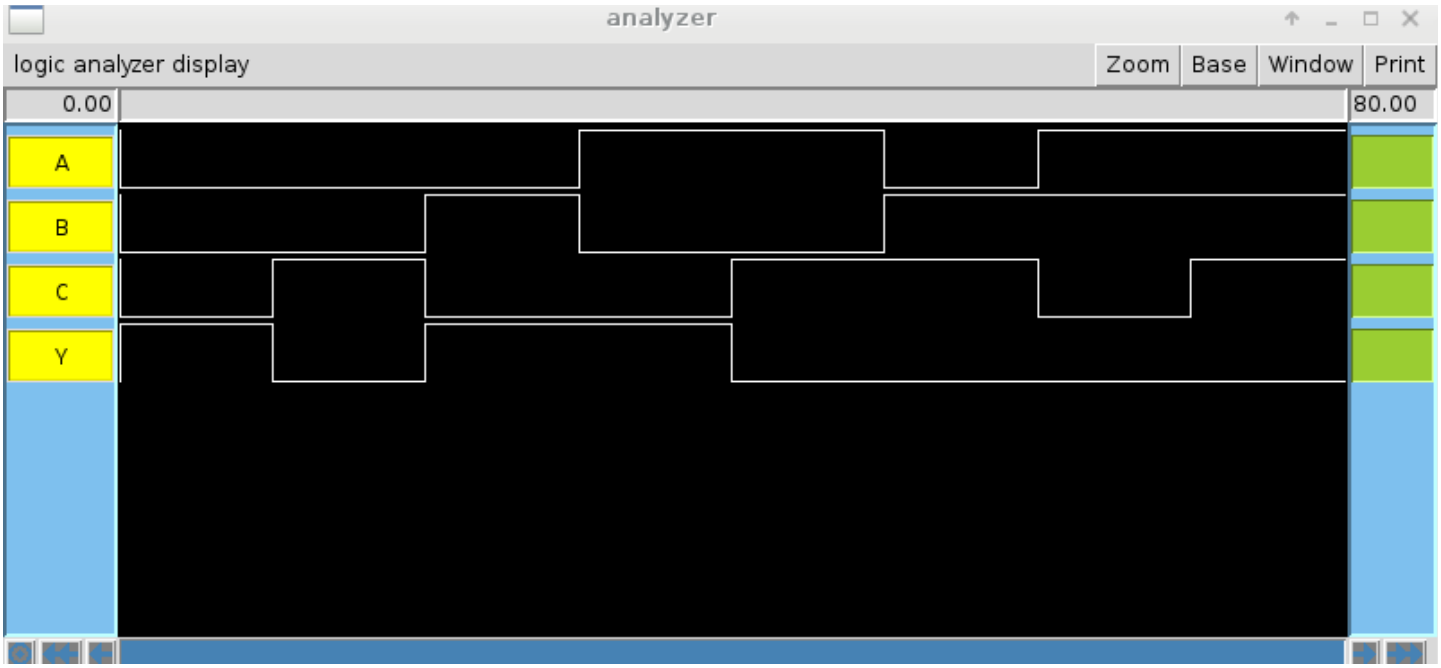
AiO21 gate sticky diagram



AiO21 gate diagram



AOI21 gate results



The cell sizes and are of AOI21 gate:

Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)

microns: 31.80 x 17.40 (-19.50, -6.60), (12.30, 10.80) 553.32
lambda: 106 x 58 (-65, -22), (41, 36) 6148

Time uses for the: 3.5 hours