ECE 425 VLSI Circuit Design Lab 4 prelab

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Time: Feb, 21, 2

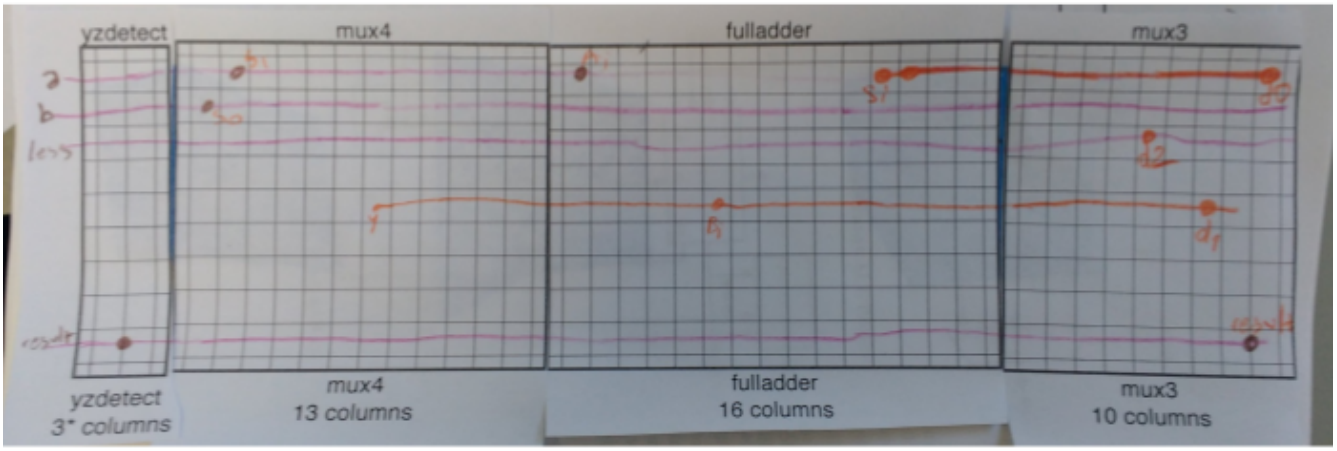
Truth table

Operation	op6	op5	op4	op3	op2	op1	op0
AND	0	0	0	1	–	0	0
OR	0	1	1	1	–	0	1
NOR	1	0	0	0	–	0	1
XOR	0	1	1	0	–	0	1
ADD	0	1	0	1	0	0	0
SUB	1	0	1	0	1	0	0
SLT	0	1	0	0	–	0	1

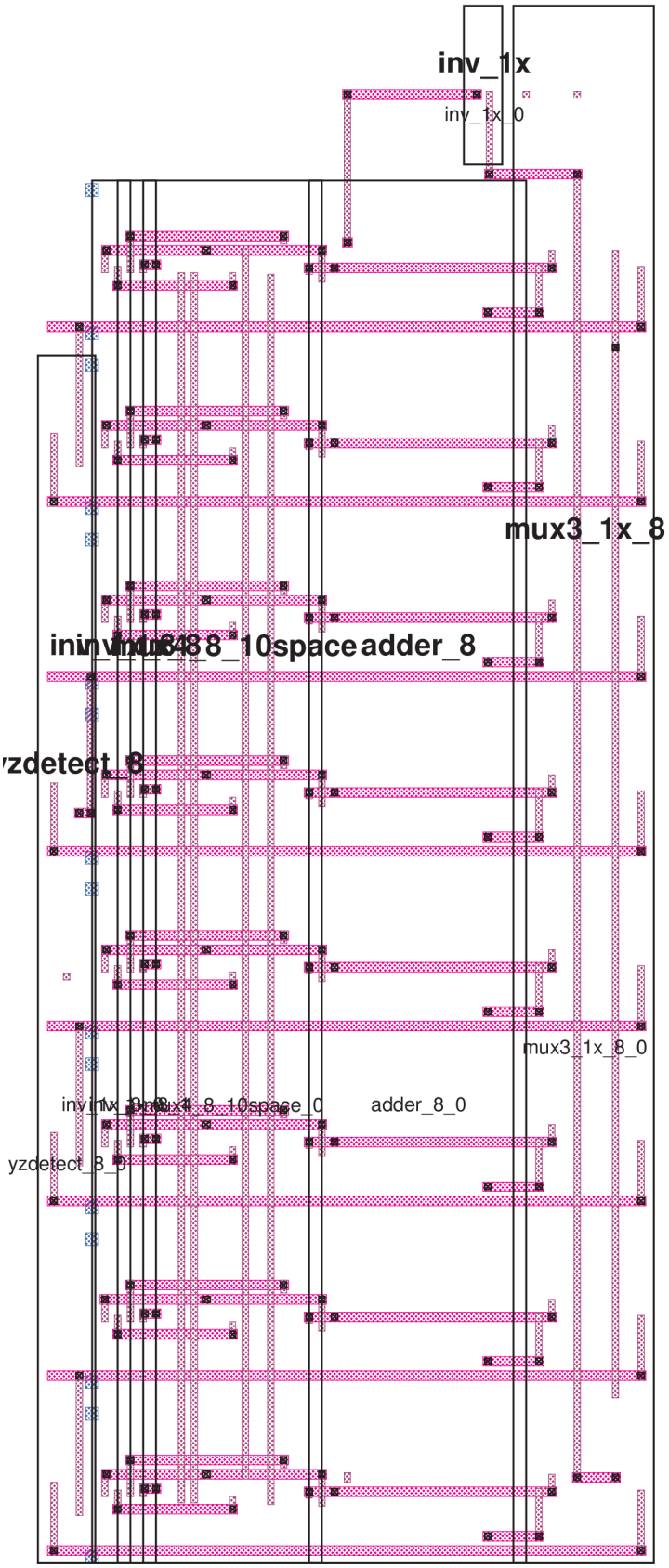
Table 1 – Partial Function Table for Alternative ALU

The SLT value should be 1010111

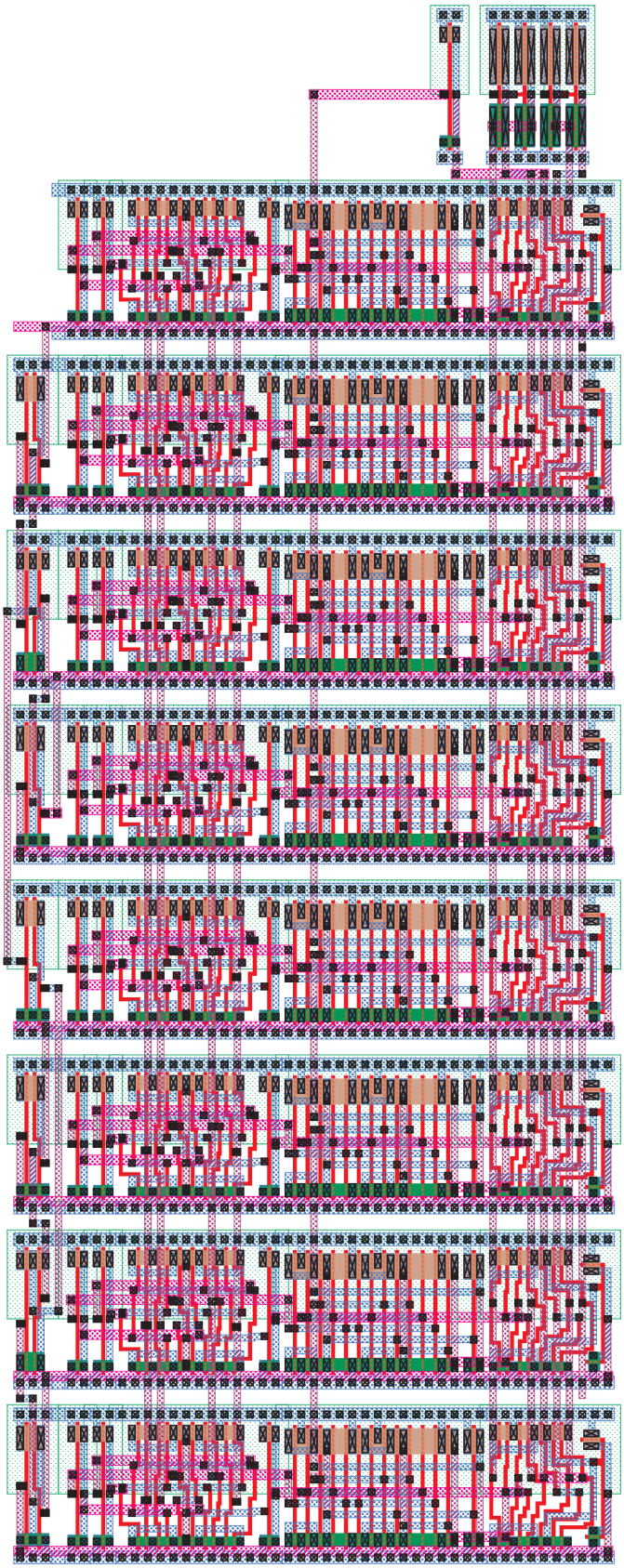
Slicing plan



ALU_unexpanded picture



ALU expanded picture



The size of our alt_alu

NEW ALU

Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)

microns: 115.80 x 294.00 (-2.40, 0.00), (113.40, 294.00) 34045.20
lambda: 386 x 980 (-8, 0), (378, 980) 378280

OLD ALU

Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)

microns: 123.30 x 294.00 (-5.10, -1.20), (118.20, 292.80) 36250.20
lambda: 411 x 980 (-17, -4), (394, 976) 402780

The new ALU decreases the total size significantly. In total, we have made the ALU width 25 lambdas shorter. Therefore, total size decrease is 25*980 lamdas

Simulation and Testing

We simulate each function in 3 or more times, we try to test some limit conditions, especially in SLT function. We tried to write tests that isolated op inputs to be able to see if each one of them worked individually. We also chose some points of interest in the ALU for testing to see if the values were passed correctly.

Total Time for completion: This lab took us approximately 6 hours.