Lab09
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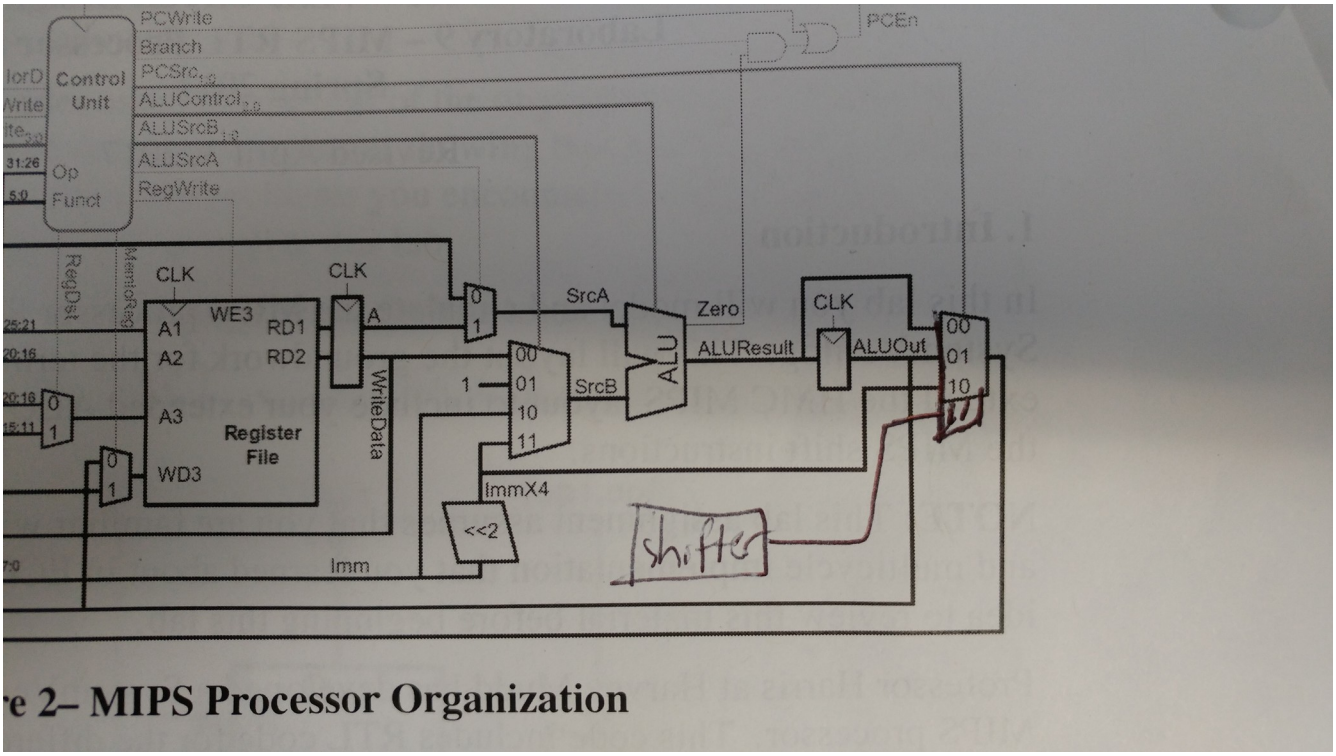
We added the shifter into datapath and put an extra input to ALU.

ALU result is decided with a mux4 like the picture below.

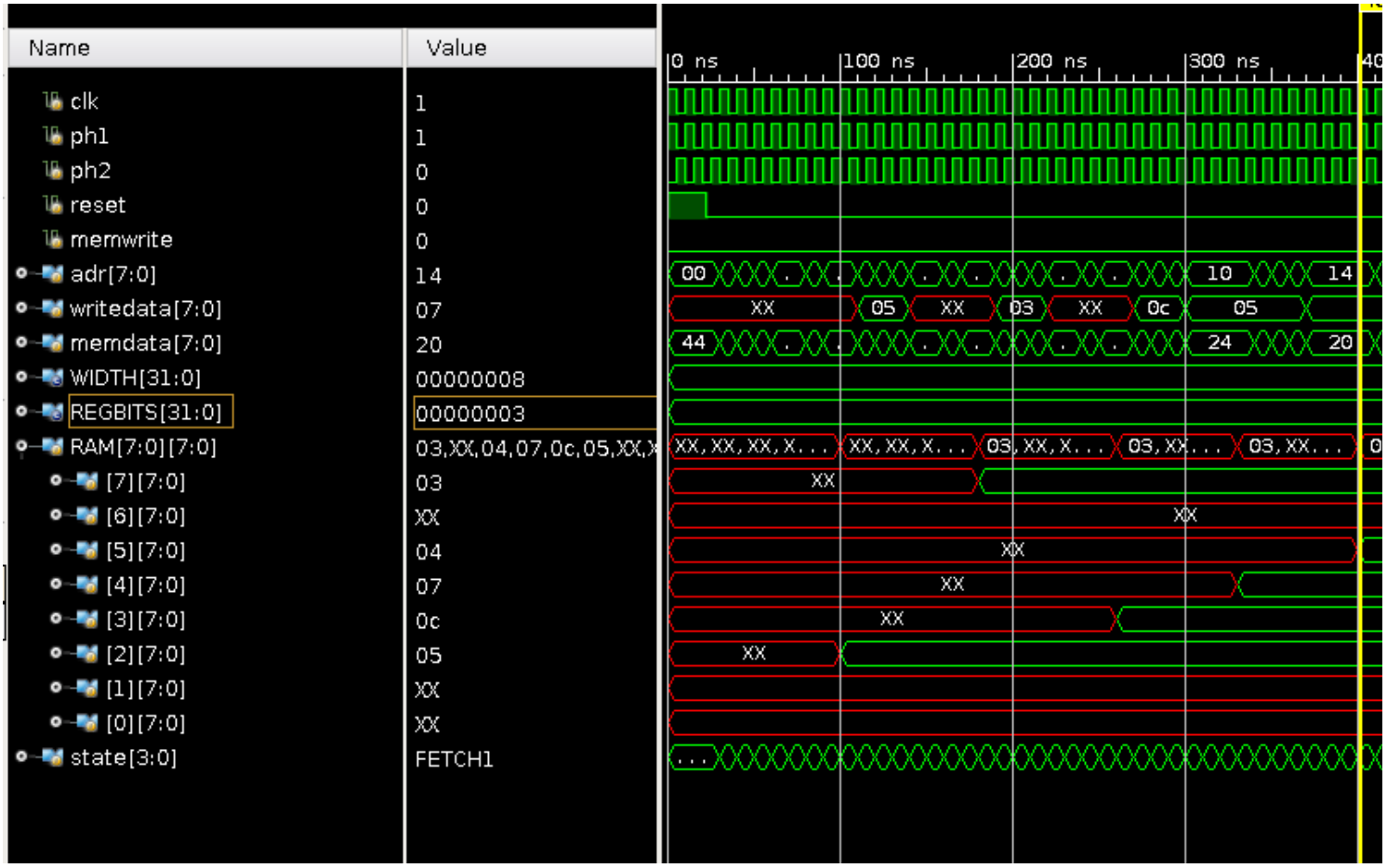


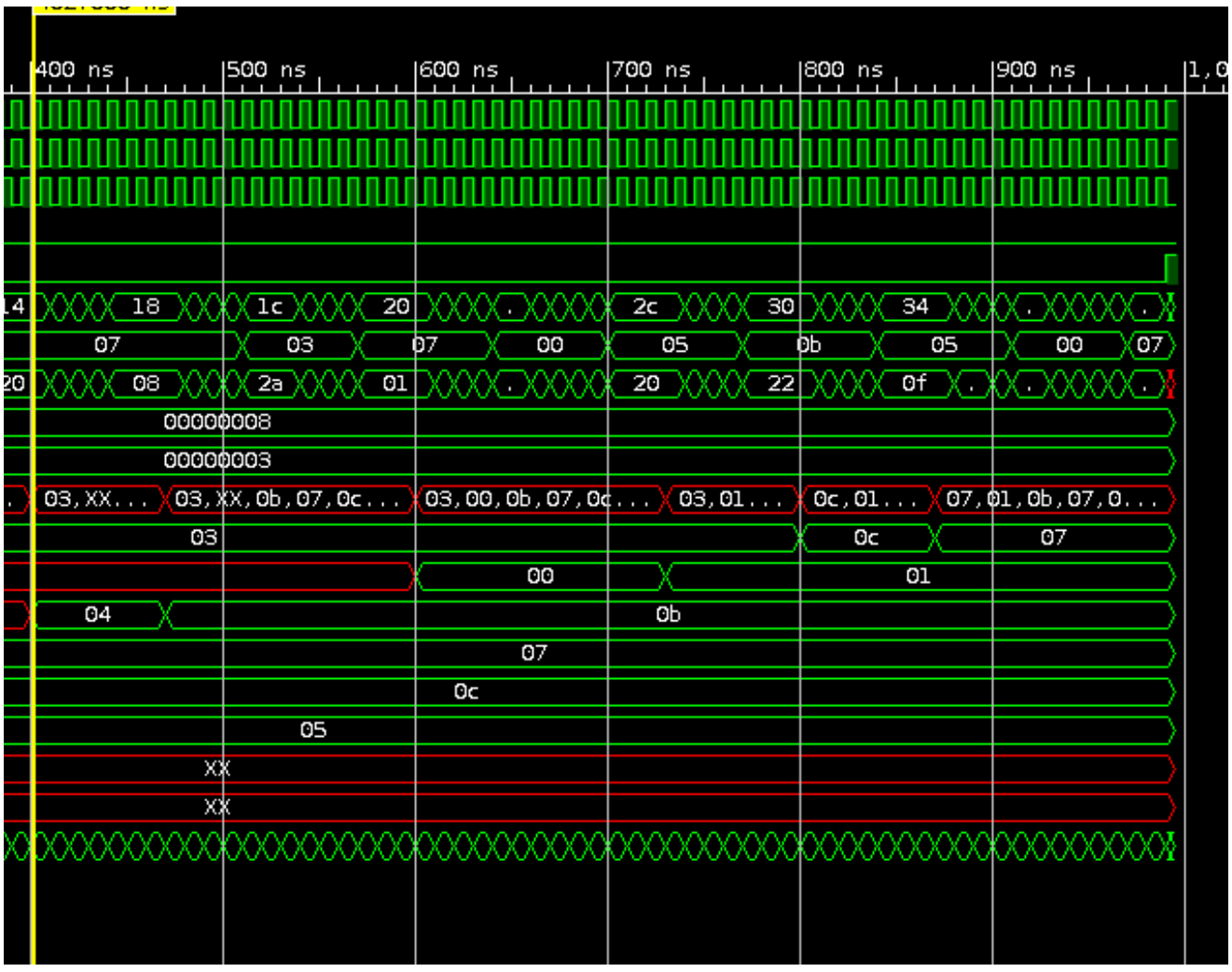
The input of the shifter is the instr[11:15] because that is the part which is being shifted.

Shamt comes from instr[16:21]. Right and Aith are decided according to the funct in datapath module as you can also see in our system verilog tar folder.

Below is the simulation successfully completed.

Requirements for the successful simulation are the same because we have tested xor, nor, sll, srl, and sra with commands that would not change the output.


Name
Value
clk
1
ph1
1
ph2
0
reset
0
memwrite
0
adr[7:0]
14
writedata[7:0]
07
memdata[7:0]
20
WIDTH[31:0]
00000008
REGBITS[31:0]
00000003
RAM[7:0][7:0]
03,XX,04,07,0c,05,XX,X
[7][7:0]
03
[6][7:0]
XX
[5][7:0]
04
[4][7:0]
07
[3][7:0]
0c
[2][7:0]
05
[1][7:0]
XX
[0][7:0]
XX
state[3:0]
FETCH1
0 ns
100 ns
200 ns
300 ns


400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
00000008
00000003
04