ECE 425 VLSI Circuit Design Lab 1

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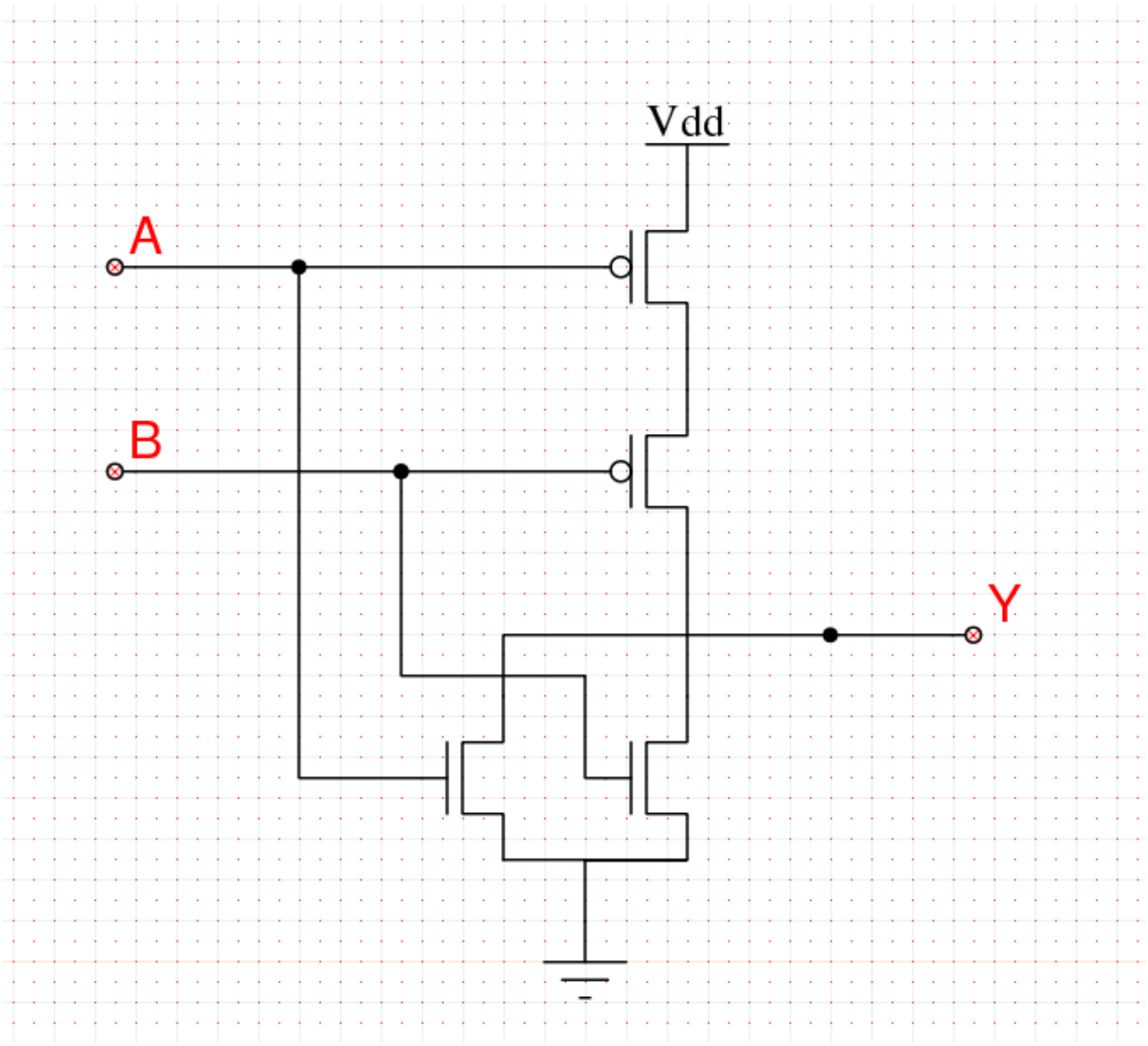
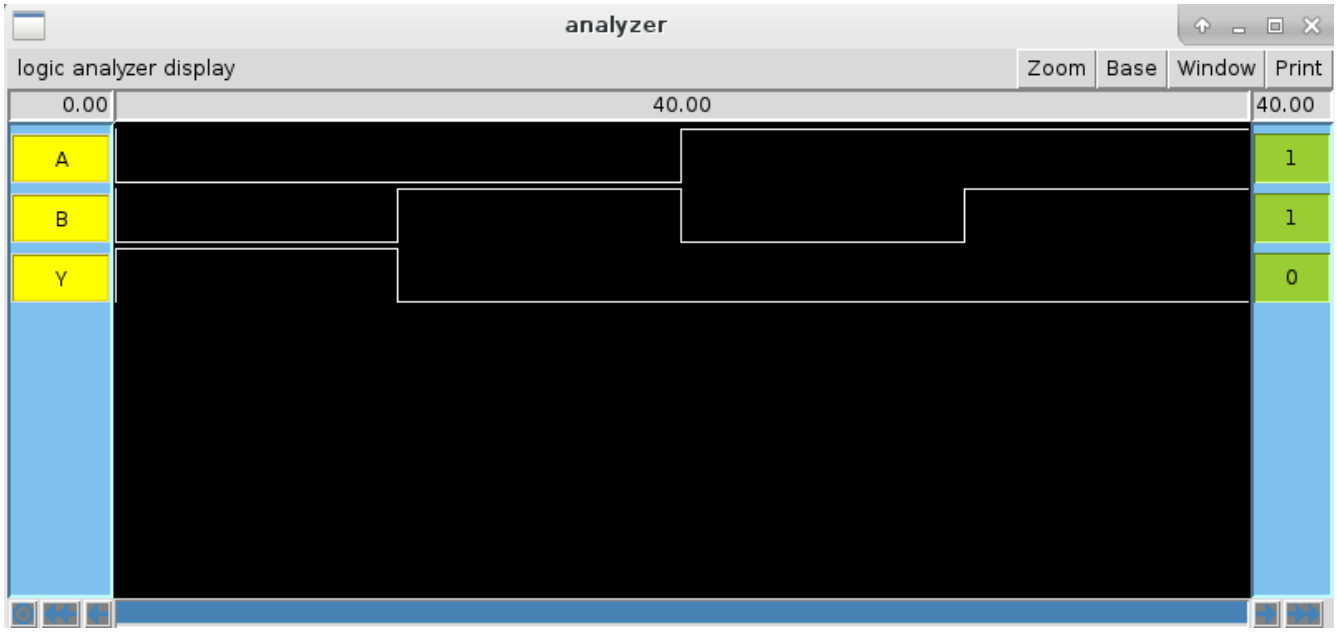
Time: Jan,24,2017

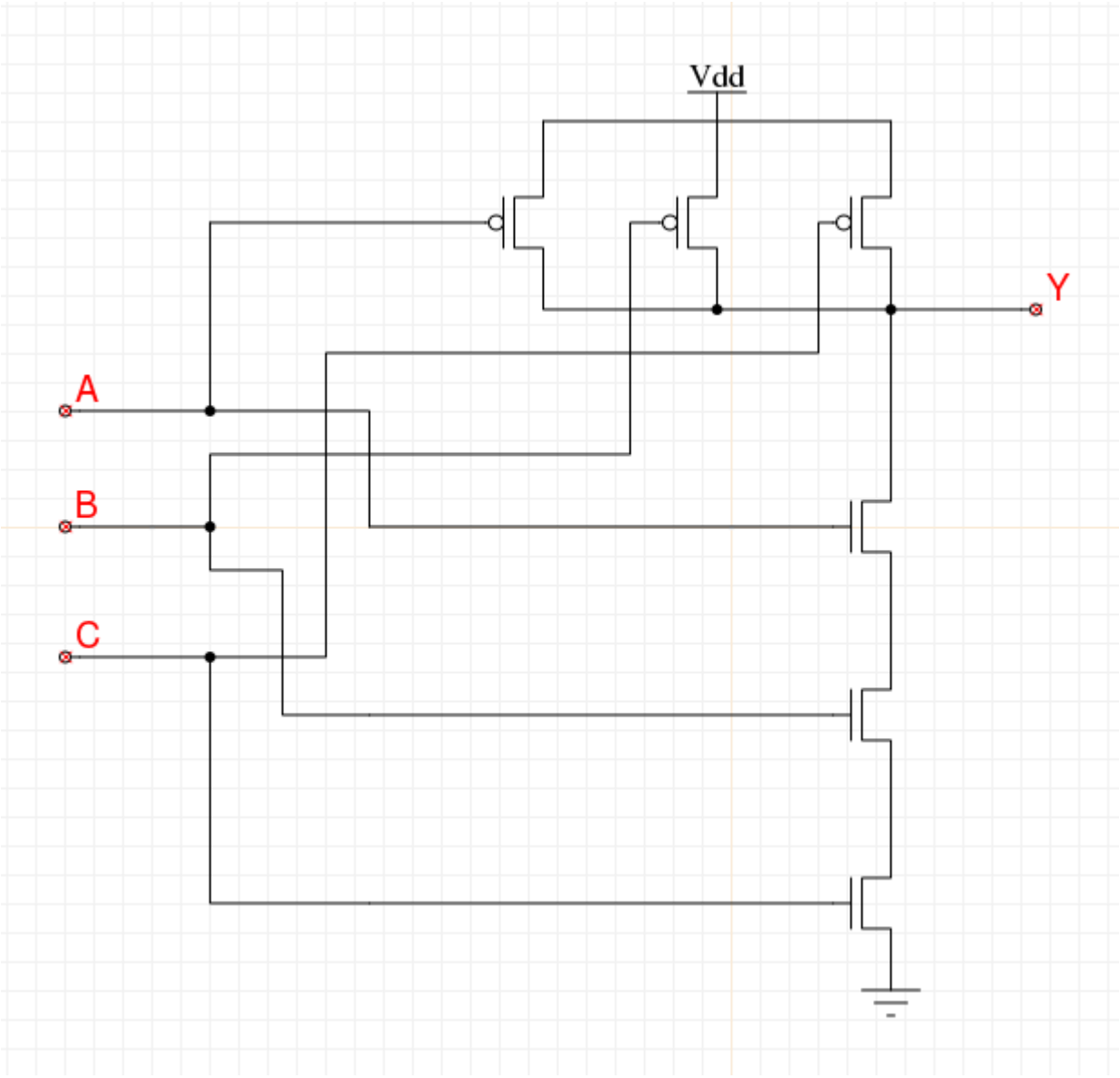
2-inputs nor gate diagram



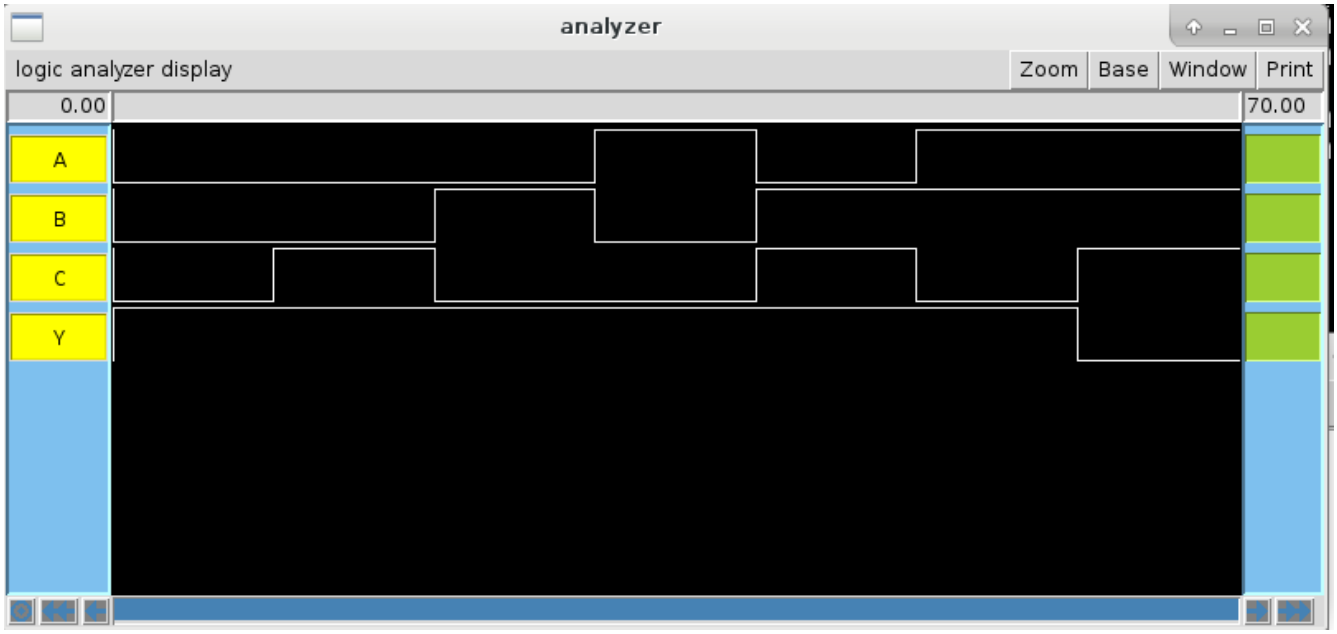
2-inputs nor gate irsim result



3-inputs NAND gate diagram



3-inputs NAND gate irsim result



3-inputs NAND gate command file

```
vector in A B C
setvector in 000
s
setvector in 001
s
setvector in 010
s
setvector in 100
s
setvector in 011
s
setvector in 110
s
setvector in 111
s
```