**ECE 425 – VLSI Circuit Design**

**Laboratory 7 – Transistor Sizing Using Logical Effort**

**Spring 2017**

Revised March 18, 2017

## 1. Introduction

In Lab 6 we used HSpice to extract and simulate the Zero Detect circuit from the HMC MIPS design. In this lab we will use the method of Logical Effort to improve the delay of the Zero Detect circuit.

In Logical Effort calculations, we have assumed that transistors in gate circuits are sized so that the pullup and pulldown networks have equal drive. However, as noted in Section 9.2.1.6 of the book, this leads to very large P-transistors in NOR gates which are difficult to lay out and have high input capacitances. For this reason, the Zero Detect circuit is constructed using LO-skew NOR gates where the width of the p-transistors is only twice the width of the n-transistors, as shown in Figure 1 (a). As discussed in class, skewed gates have different logical effort values for rising and falling transitions. Note that while the falling logical effort of the NOR gate is significantly improved over the equal-drive approach, the rising logical effort is significantly increased.

Because a equal-drive 2-input NAND gate has equally sized n-transistors and p-transistors, the circuit uses the conventional versions, as shown in Figure 1 (b). In this case the logical effort is the same for both rising and falling transitions.

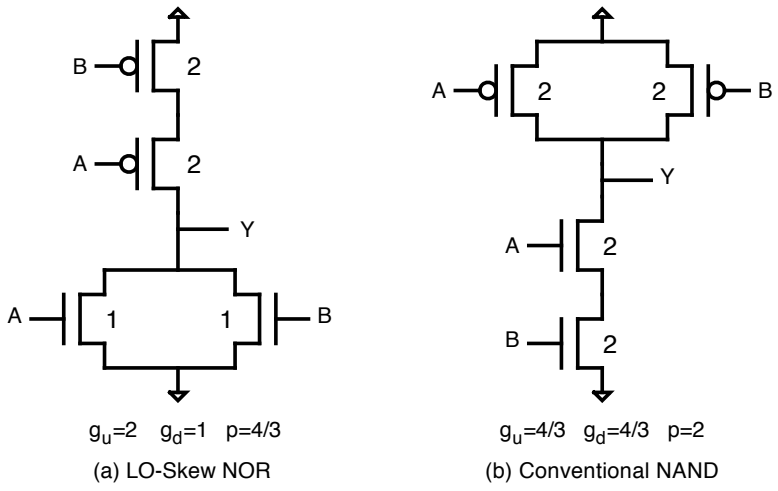


**Figure 1 – Gate Designs used in Zero Detect Circuit**

Figure 2 shows a schematic diagram of the zero detect circuit that we simulated in Lab 6, including an assumed load of 36 unit transistor capacitances. Each logic gate is annotated with its input capacitance of 6 unit transistor capacitances. If we examine the `yzdetect_8` layout, we find that the transistors are sized as follows: In the conventional NAND gate, the p-transistors and p-transistors have equal size and therefore

have a gate capacitance of 3C each; therefore all transistors are sized at three times the width of a 2λ × 4λ unit transistor, or 2λ × 12λ. In the LO-Skew NOR gate, the P-transistors have twice the input capacitance of the N-transistors and therefore have gate capacitances of 4C, and 2C, respectively. Thus the P-transistors are sized at 2λ × 16λ and the N-transistors are sized at 2λ × 8λ.

In this lab we will use the method of Logical Effort to estimate the delay of this circuit as it is currently laid out. We will then explore the best way to re-size gate transistors to improve the delay Zero Detect circuit under the constraint that the overall area and aspect ratio of the circuit must fit into the existing ALU design. We will then use Magic to modify the layout, extract the layout, and simulate with HSpice to verify that the delay was improved.

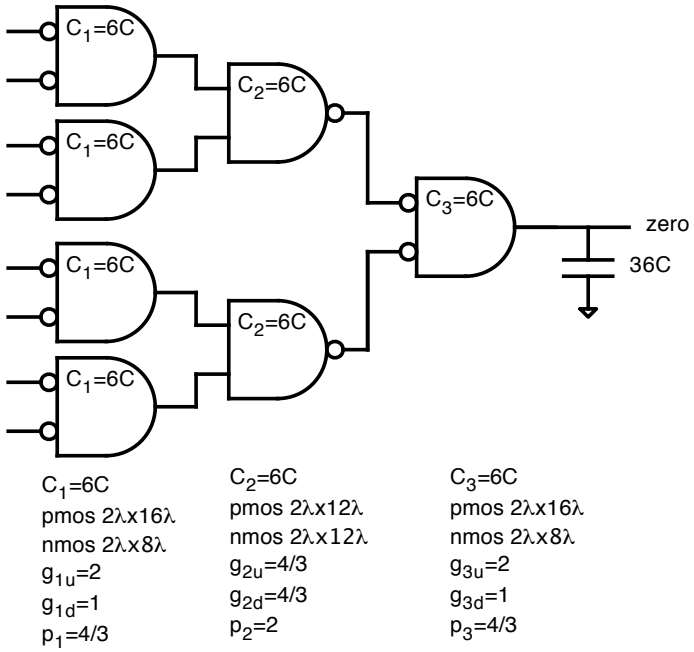


**Figure 2 – Zero-Detect Circuit**

## 2. Initial Calculations (Prelab)

When using Logical Effort to calculate timing estimates with skewed gates, we must consider the worst case in terms of rising and falling transitions in different gates. Since each stage of the Zero-Detect circuit is inverting, there are two scenarios:

- Rising in first stage, falling in second stage, and rising in third stage.
- Falling in first stage, rising in second stage, and falling in third stage.

Since the logical effort of the LO-Skew NOR gate is much higher for rising transitions, it is safe to assume that the Rising/Falling/Rising timing estimate is the worst case.

1. Complete **Worksheet 1: Initial Zero-Detect Circuit**. This provides an estimate of the delay of the Zero-Detect circuit in its current form. To complete the worksheet, we suggest that you create a spreadsheet that calculates the electrical effort *h* and delay *d* of each stage as a function of the input capacitances $C_1$, $C_2$, and $C_3$. Show

your completed worksheet to the Lab Instructor and pick up a copy of the solution to compare with your results.

2. Complete **Worksheet 2: Optimized Zero-Detect Circuit**. This uses the method of Logical Effort to calculate gate sizes that will minimize the delay of the circuit. Once it is complete, show it to your Lab Instructor and pick up a copy of the solution to compare with your results.
3. We would like to get the best delay possible, but we are also constrained to have our modified design fit into the existing ALU design. Examine the magic layouts of the cells you need to resize and note the maximum width p-transistor that can be realized in their current form factor. Note that when very wide transistors are needed, a common trick is to "fold" the transistor (essential putting multiple transistors in parallel, as described in Section 4.3.6 – see Figure 4.18 on p. 154). However, folding transistors in these cells will increase the width of the cells, which would increrease the overall size of the ALU! If this is a limiting factor, use the spreadsheet you constructed in step 1 to find a gate sizing that gives a delay that is within 10% of the minimum delay but still fits into the desired form factor.

**2. In the Lab**

1. Create new cells based on the original cells that implement the new sizes called for in the previous step. Be sure to rename these cells so that the original versions are left intact.
2. Create a new version of the Zero Detect circuit named `yzdetect_fast` that uses instances of the resized cells (along with any of the original cells that you continue to use.
3. Extract and simulate this circuit with IRSIM to quickly verify that it functions correctly.
4. Extract and simulate this circuit in HSPICE and capture its delay values $t_{pdr}$, $t_{pdf}$, $t_r$, and $t_f$ using the same testbench that you created for last week's lab. Compare these values to the original version. How much improvement did you get?
5. Modify both your testbench to measure the average power consumed by the circuit during the simulation run. Note that in order to do this the vdd connection of the "Device Under Test" must be connected to a separate voltage source from the driving circuit. Record the average power consumption for both your original and modified circuits.

**4. Report**

For your lab report, upload the following items to Moodle:

1. A PDF file per lab team, that reports the delay times and power values you recorded in your modified circuit simulation and compares them to the those of the original circuit. Include a summary that describes any problems you encountered and provides an estimate of how long it took you to complete this lab (this estimate will not be part of your grade, but will be used to calibrate the workload of these labs in the future).
2. A tarball containing all of the Magic files and spice deck files that you created in this lab, including the spice files extracted from Magic.

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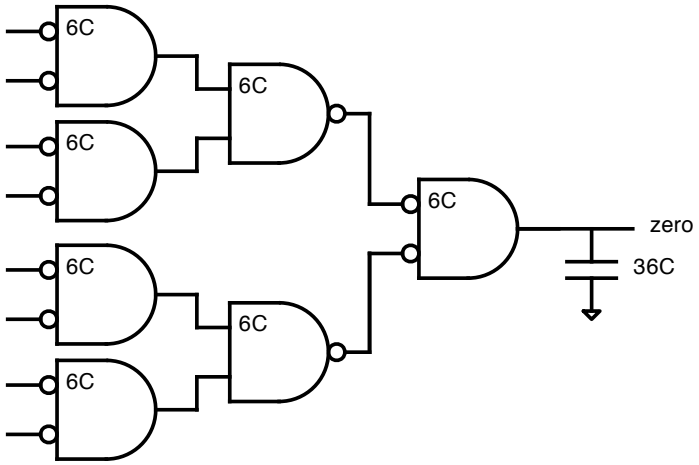
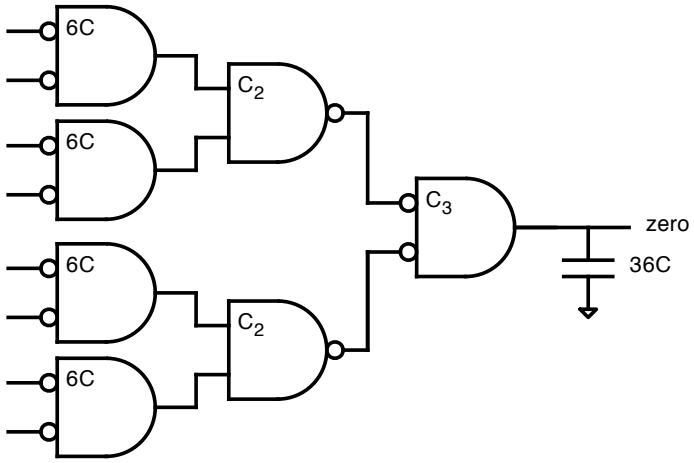
**Worksheet 1: Initial Zero Detect Circuit** **Name(s)** _____




| **Stage 1** | **Stage 2** | **Stage 3** |
|---|---|---|
| $C_1 = 6C$ | $C_2 = 6C$ | $C_3=6C$ |
| pmos size: 2λ×16λ | pmos size: 2λ×12λ | pmos size: 2λ×16λ |
| nmos size: 2λ×8λ | nmos size: 2λ×12λ | nmos size: 2λ×8λ |
| $g_{1u} = 2$ | $g_{2u} = 4/3$ | $g_{3u} = 2$ |
| $g_{1d} = 1$ | $g_{2d} = 4/3$ | $g_{3d} = 1$ |
| $p_1 = 4/3$ | $p_2 = 2$ | $p_3 = 4/3$ |
| $h_1 =$ _____ | $h_2 =$ _____ | $h_3 =$ _____ |
| $f_{1u} =$ _____ | $f_{2d} =$ _____ | $f_{3u} =$ _____ |
| $d_{1u} =$ _____ | $d_{2d} =$ _____ | $d_{3u} =$ _____ |

Total Delay (rising/falling/rising) $\mathbf{D_{udu} =}$ _____

**Worksheet 2: Optimized Zero Detect Circuit** **Name(s)** _____




| **Stage 1** | **Stage 2** | **Stage 3** |
|---|---|---|
| $g_{1u} = 2$ | $g_{2u} = 4/3$ | $g_{3u} = 2$ |
| $g_{1d} = 1$ | $g_{2d} = 4/3$ | $g_{3d} = 1$ |
| $p_1 = 4/3$ | $p_2 = 2$ | $p_3 = 4/3$ |

G = _____ B = _____ H = _____

P = _____

F = GBH = _____

$\hat{f} = F^{1/N} =$ _____

$D = N \cdot \hat{f} + P =$ _____

$C_3 = \frac{C_{out} \cdot g_3}{\hat{f}} =$ _____ pmos size: 2λ ×____λ nmos size: 2λ ×___λ

$C_2 = \frac{C_{out} \cdot g_2}{\hat{f}} =$ _____ pmos size: 2λ ×____λ nmos size: 2λ ×___λ

$C_1 = \frac{C_{out} \cdot g_1}{\hat{f}} =$ 6C pmos size: 2λ ×16 λ nmos size: 2λ ×_8_ λ