ECE 425 VLSI Circuit Design Lab 8 prelab

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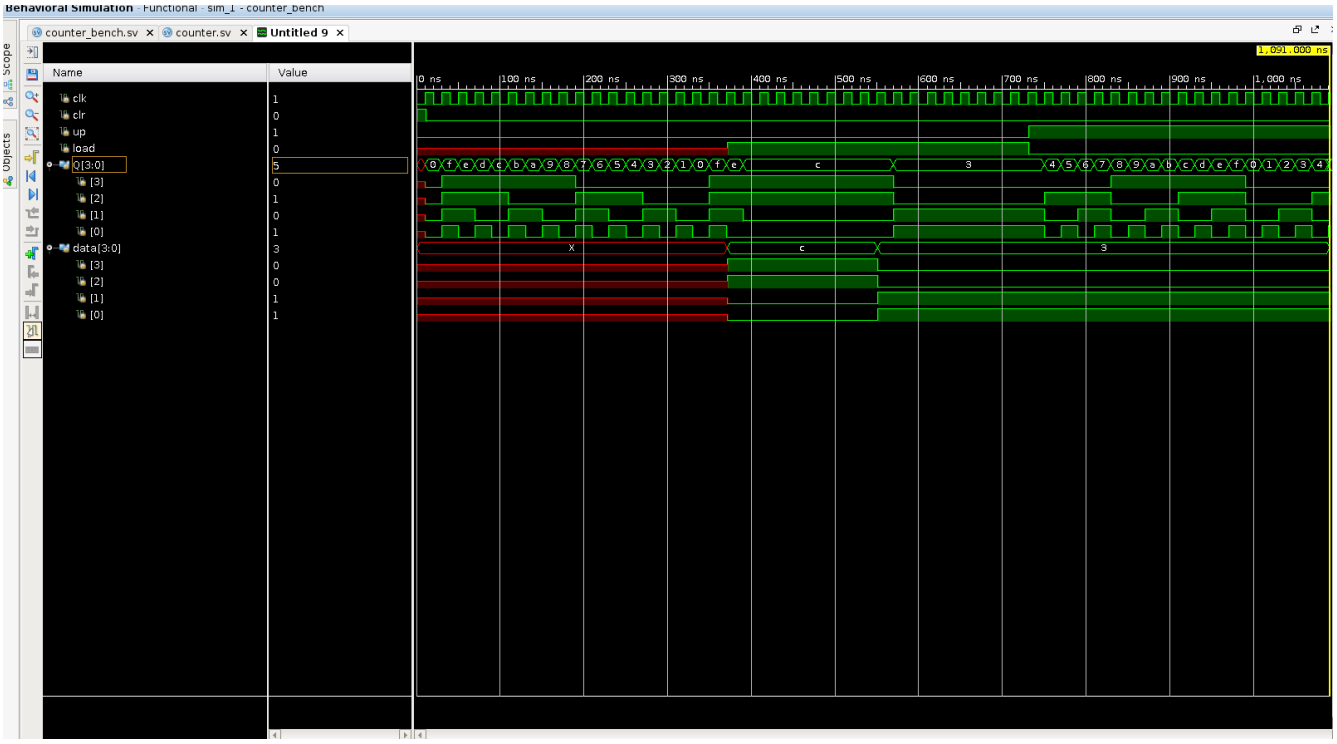
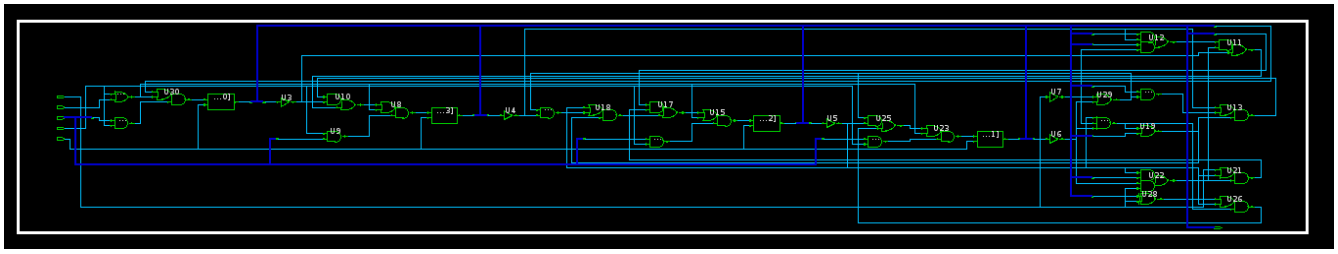
Time: Mar, 28, 2017

Simulation of counter testbench

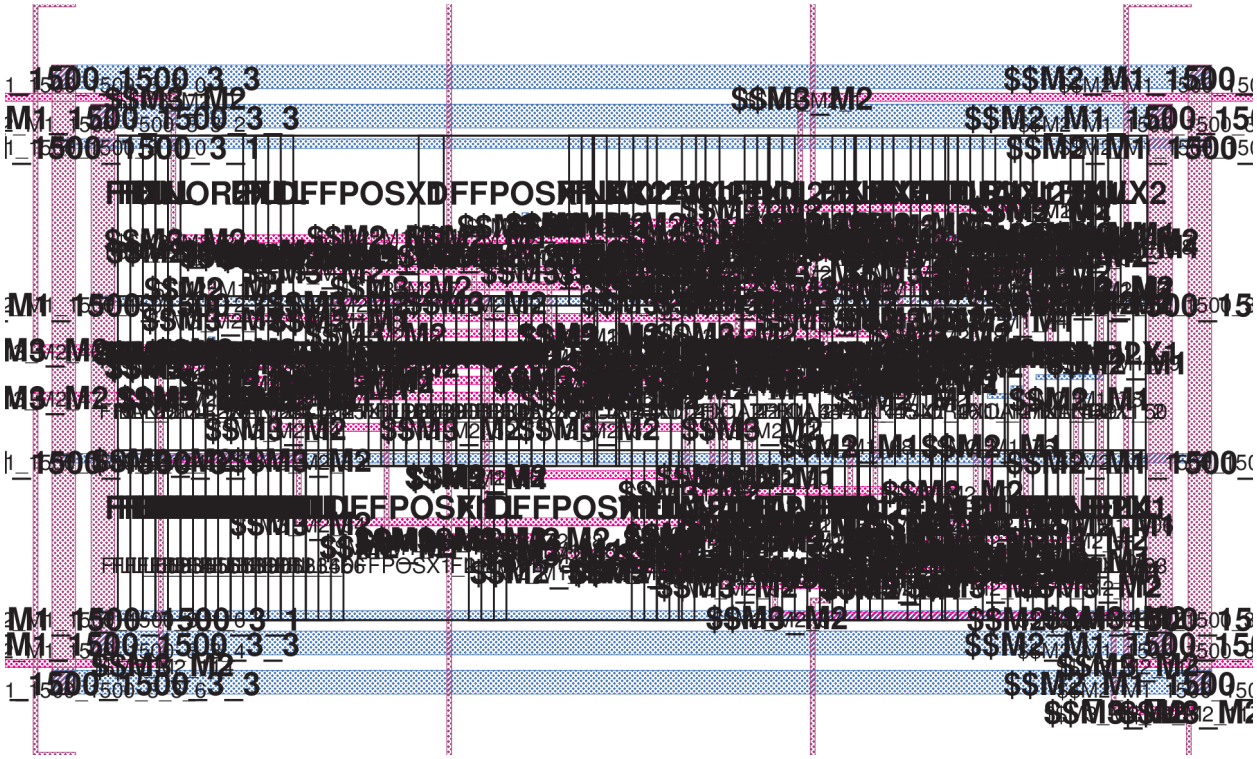


Schematic of counter

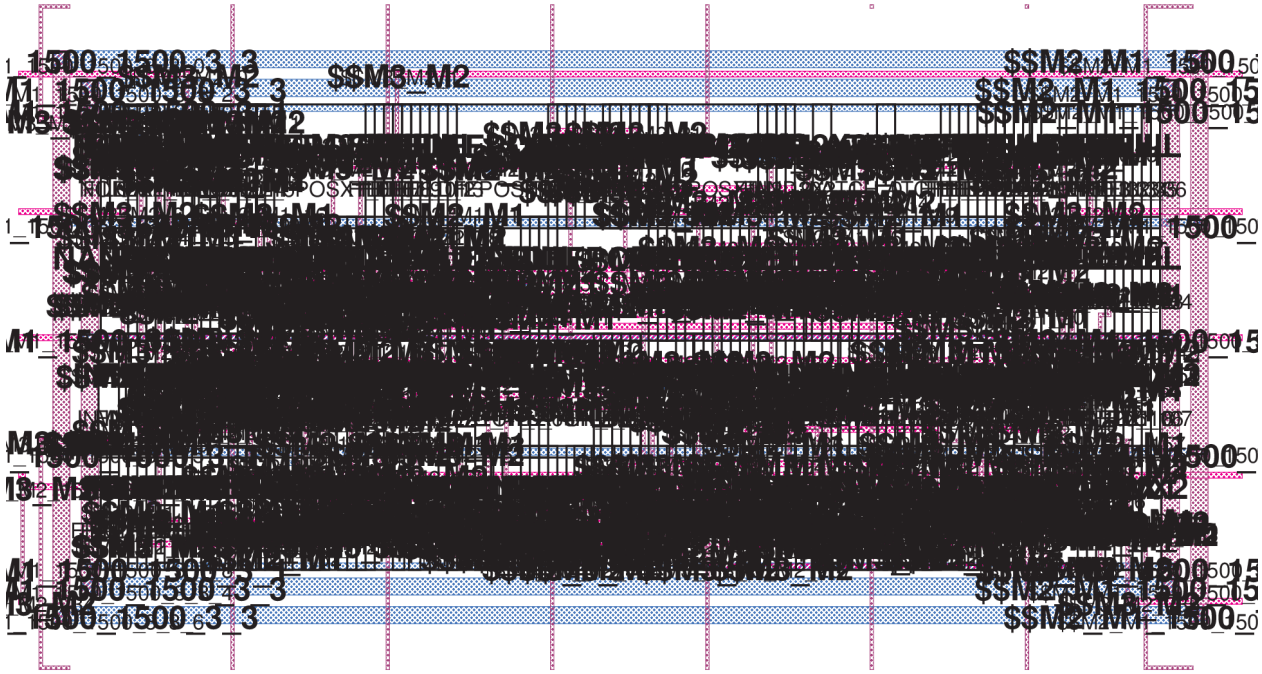


Counter simulatuon waveform

Counter layout



MIPS_FSM layout



MIPS_FSM size

Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)

microns: 321.60 x 174.00 (0.00, 0.00), (321.60, 174.00) 55958.40
lambda: 1072 x 580 (0, 0), (1072, 580) 621760