ECE 425 VLSI Circuit Design Lab 3

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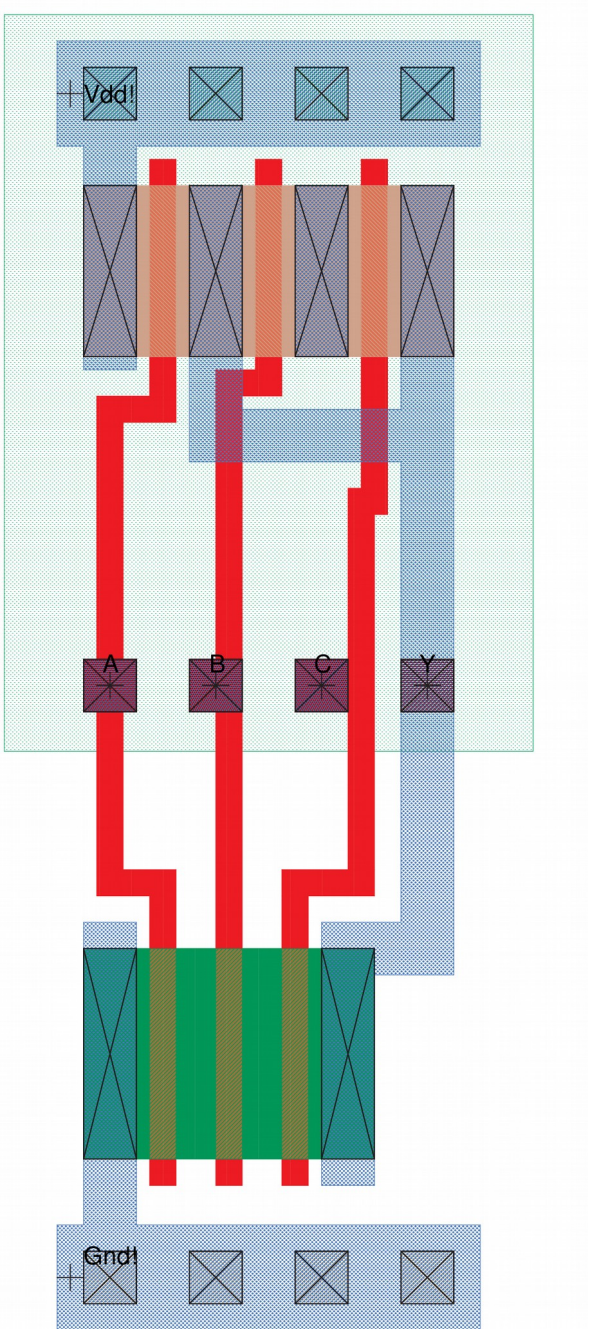
Time: Feb, 7 ,2017

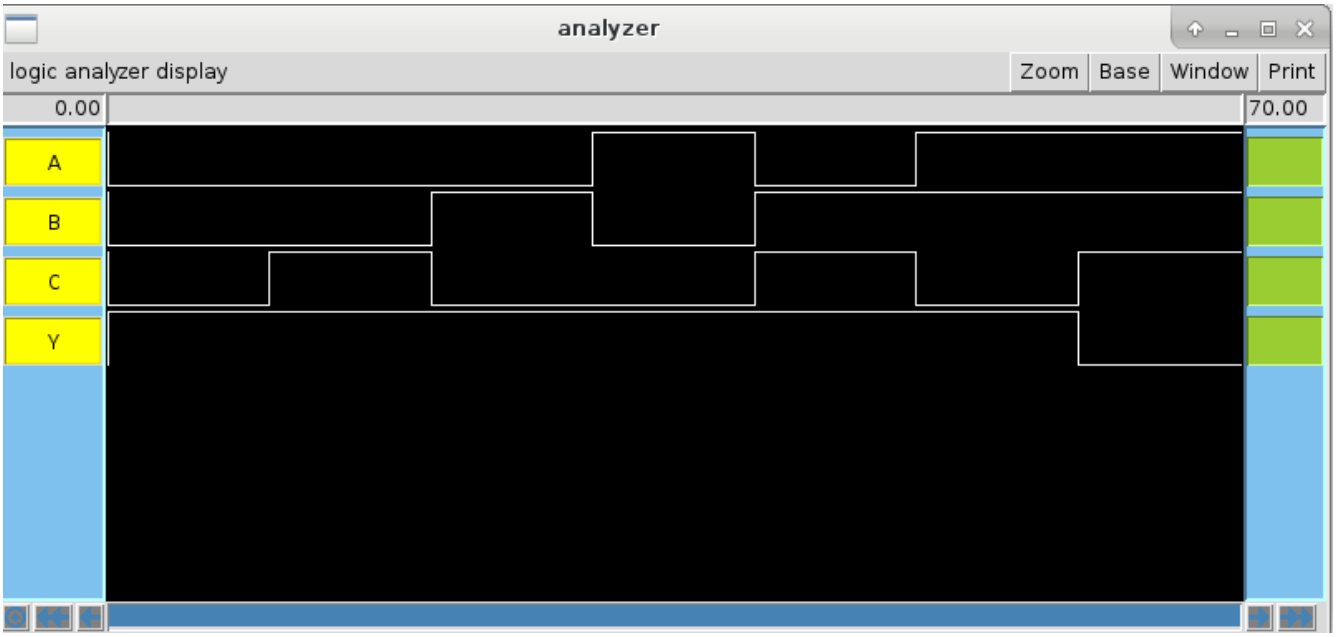
The size of the NAND3 gate
Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)

microns: 12.00 x 30.00 (-1.80, -1.20), (10.20, 28.80) 360.00
lambda: 40 x 100 (-6, -4), (34, 96) 4000

The diagram of the NAND3 gate



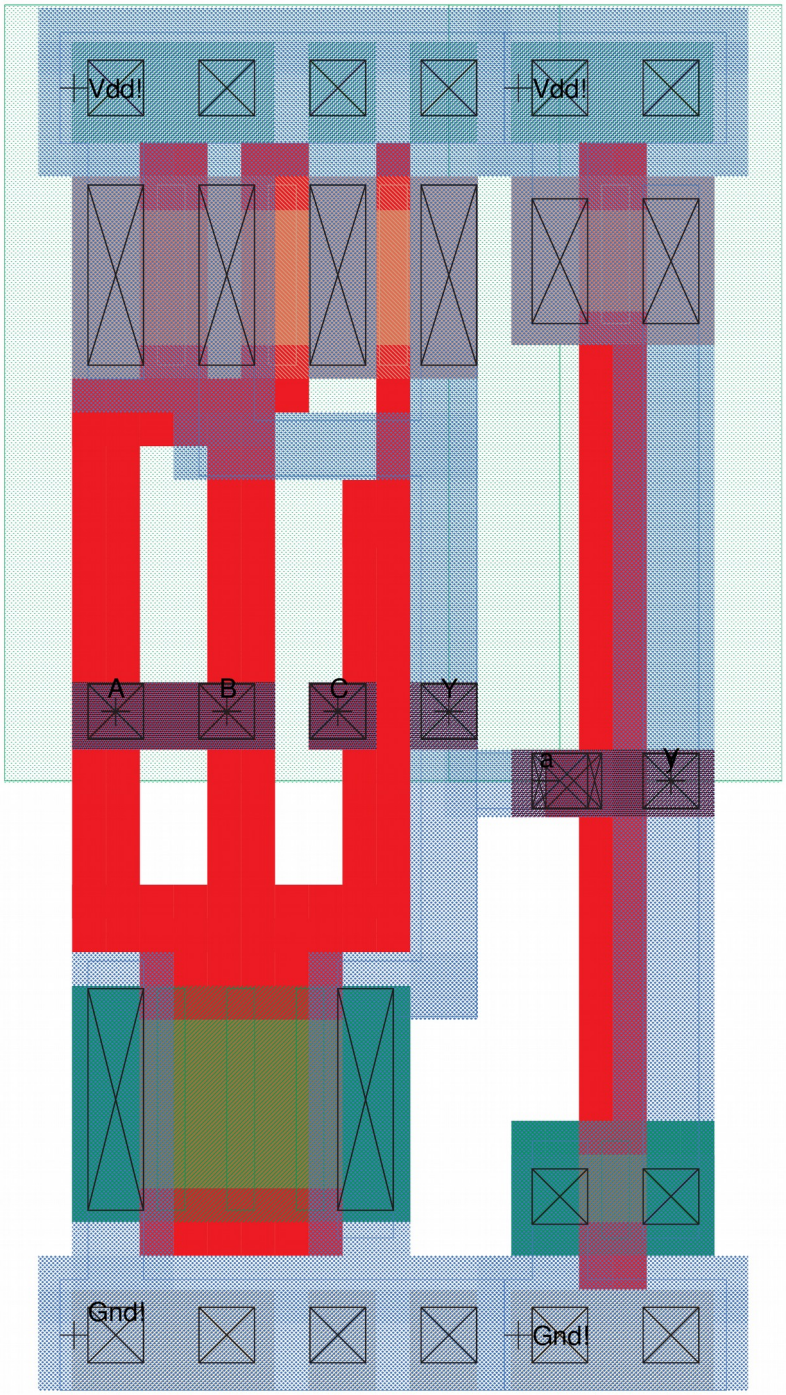
The result analyzer of the NAND3



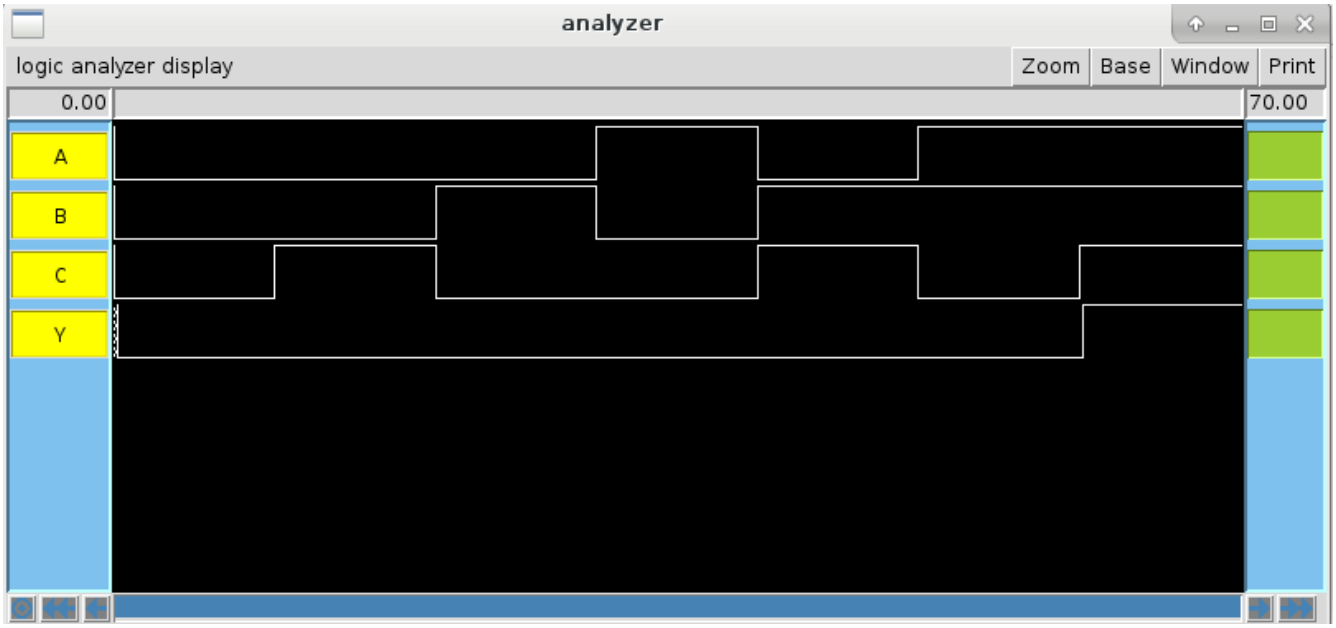
The size of the AND3 gate
Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)

microns: 16.80 x 30.00 (0.00, 0.00), (16.80, 30.00) 504.00
lambda: 56 x 100 (0, 0), (56, 100) 5600

The diagram of the AND3 gate



The result analyzer of the AND3 gate



spacing between or2gates
Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)

microns: 12.00 x 3.00 (-1.80, 94.80), (10.20, 97.80) 36.00
lambda: 40 x 10 (-6, 316), (34, 326) 400

The signals going through the bitslice

As discussed in class, the HMC MIPS processor implements an 8-bit version of the ALU design as part of a larger datapath module. Each bitslice is implemented using pitch-matched cells that connect from left to right as shown by the *slicing plan* in Figure 7. The slicing plan shows the arrangement of each cell along with the horizontal tracks that are used to connect their inputs and outputs together and realize the circuit in Figure 5. For clarity, vertical connections are not shown here, but can be determined by examining the layout in Magic.

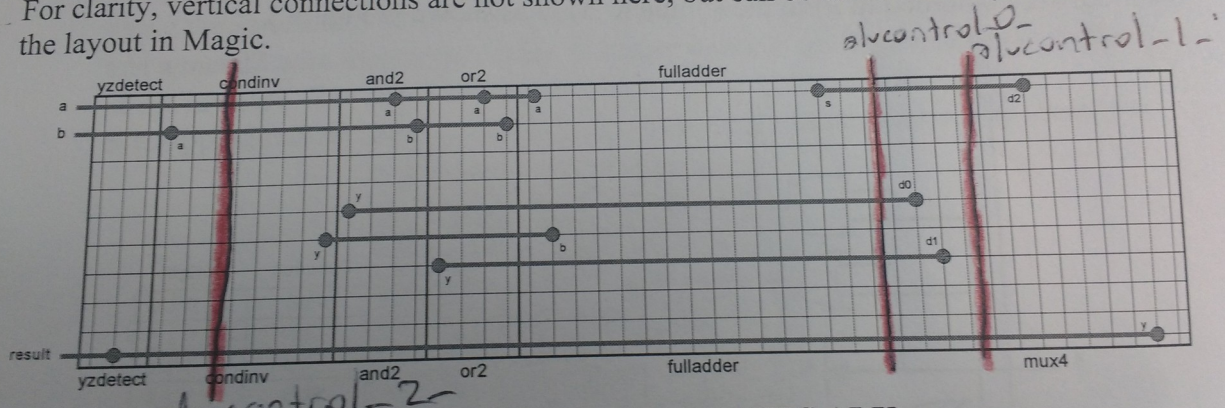
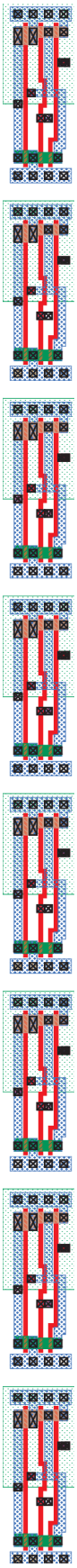


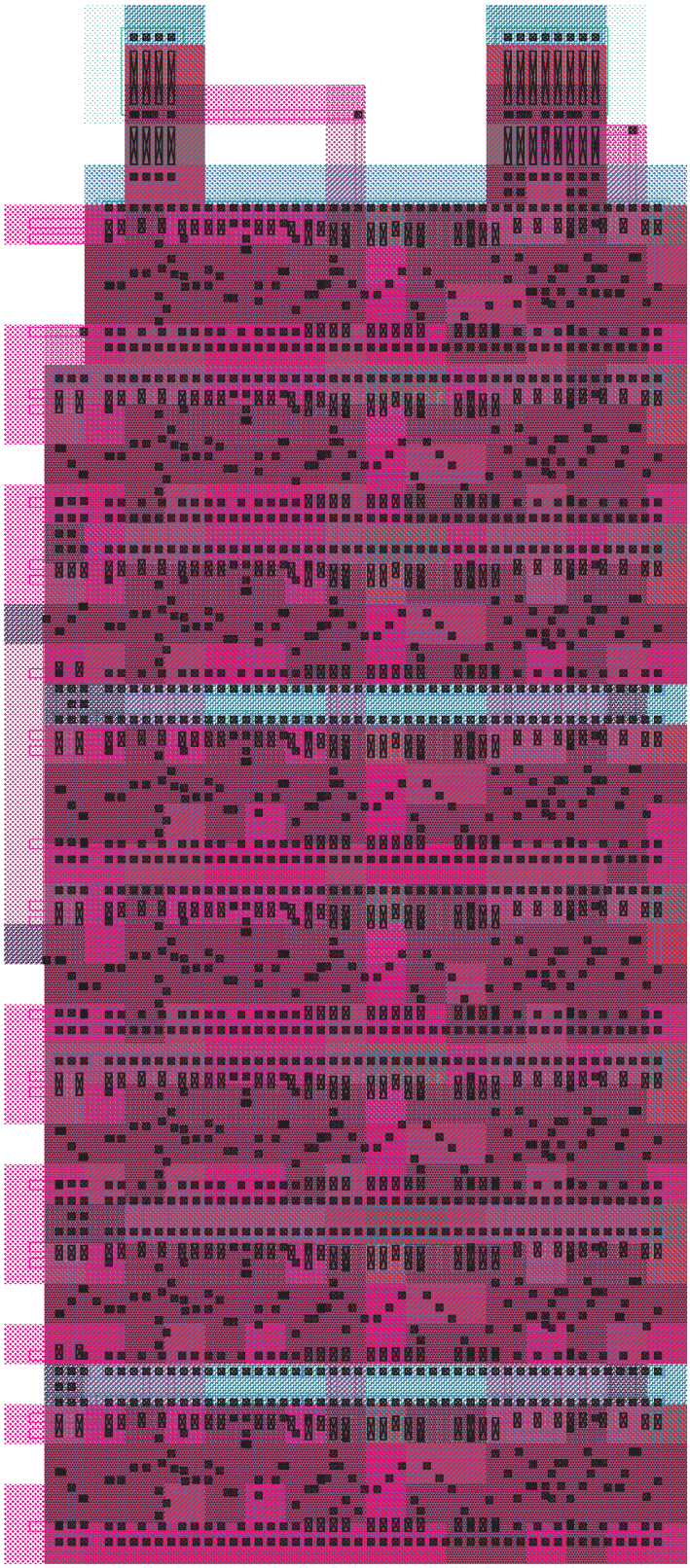
Figure 7 – Slicing Plan for the MIPS ALU

As described in the book, although the MIPS datapath is wired using a bitslice approach, the actual cell hierarchy is created using a *wordslices* – vertical connections that group each logic gate and functional unit into an 8-bit group. Metal3 and Metal2 wires are then

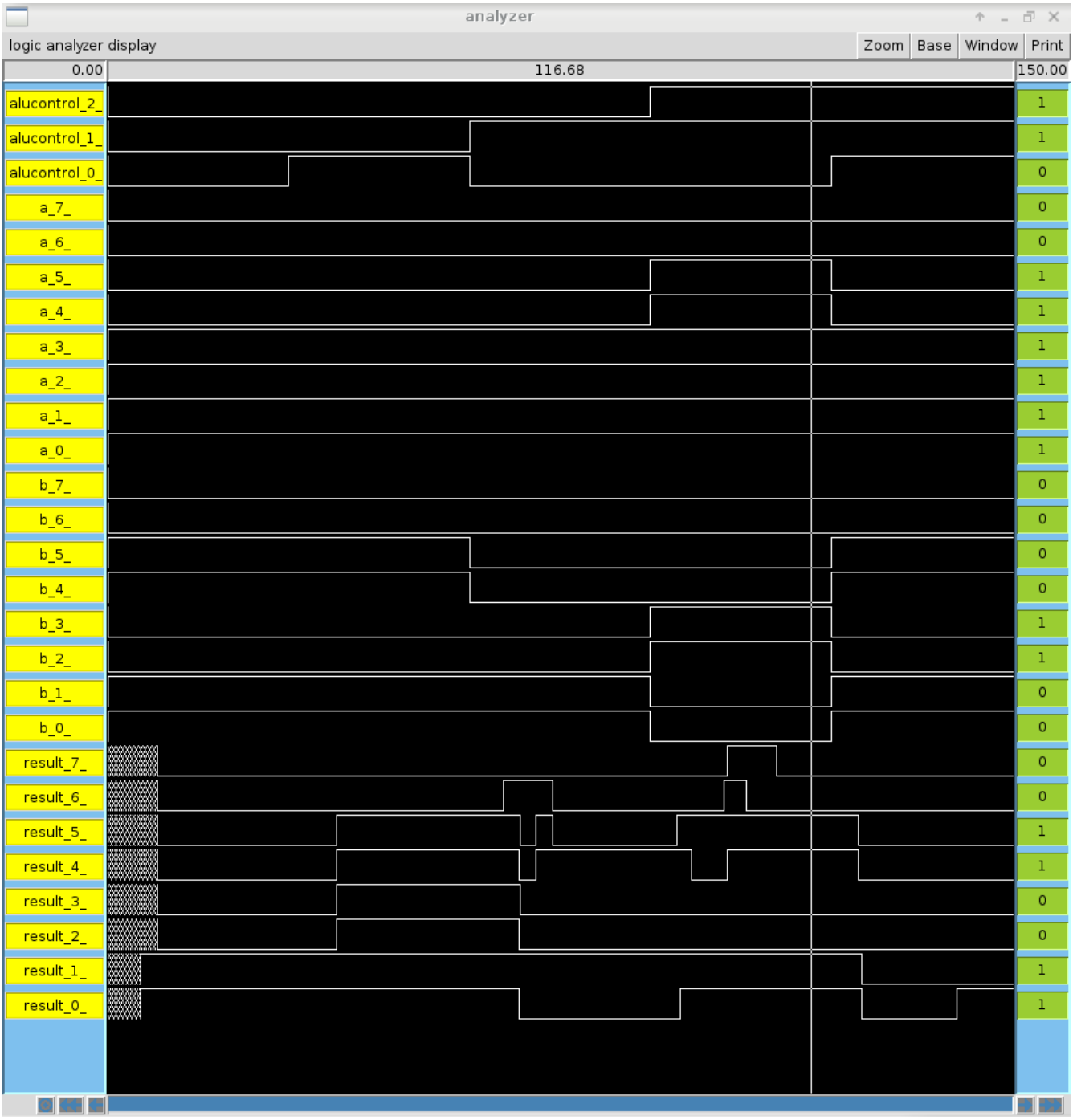
The diagram of the and2_1x_8



The diagram of the ALU



The result analyzer of the ALU



The size of the ALU

Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)

microns: 123.30 x 294.00 (-5.10, -1.20), (118.20, 292.80) 36250.20
lambda: 411 x 980 (-17, -4), (394, 976) 402780

The problems :

The problems we have is how to plot large amount of inputs and outputs in clear way

Time use:

3:30 hours