TECHNICAL MEMORANDUM
Lafayette College
Department of Electrical and Computer Engineering

Title: RF Link Test
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Date: November 12, 2016

Abstract

This lab is a RF Link testing communication to and from our station to the instructor and other student stations in class. This is through transmitting and receiving from our inherited lab 5 structure, i.e. Mx_test to Manchester transmitter to Manchester receiver to Fifo buffer to asynchronous transmitter outputted to Realterm computer simulation. The Murata TRC8000 916.5 MHz transceiver is the link that connects to out Nexys 4DDR board to facilitate this communication.

1. Introduction

The design for this lab is simply addition of transmitter test and receiver test logic to lab 5 provided in the Wimp Fi Radio Data Sheet provided by the instructor. The transmit and ASK receive modes of the transceiver are the ones used, such that as long as we are not transmitting, we should receive data from other stations.

2. The Design

The design of this lab is the same as that of lab 5, with the added logic to facilitate integration of the transceiver for the transmitter and receiver test.

3. Design Verification

This design follows this checklist from lab 5, along with some additional observations.

Description	Test Method	Detailed Results
1. Module Interface	Code Inspection	We added few extra inputs and outputs compared to the Lab design, i.e. 1. Check for error in PREAMBLE-SFD, bit and EOF via correlator use 2. Added Transmitter from Lab3 for switching in between RealTerm data input and user given switches data input
2 . Module function: accepts rxd input and receives data bits one by one, err output for when there is a frame error and indicates readiness for the next receiving with cardet output	Demonstration in oscilloscope and test bench simulation and Nexys4DDR board: **TEST BENCH** 1. Display of data received 2. Display of PREAMBLE-SFD transition 3. Display of RECEIVE-EOF transition 4. Proper display of reset 5. Proper display of the BaudRate	**OSCILLOSCOPE & FPGA HARDWARE** 1. Proper display of cardet output on oscilloscope 2. Proper display of reset on seven segment display on Nexys board 3. Proper display of manchester receiver data on seven segment display 4. Proper display of full, empty and ready on LEDs on Nexys board

	6. Proper display of correlator csum output relation to state transitions and proper detection of 1 and 0 Manchester bits.	5. Proper display of received data on the oscilloscope 6. Proper display of data transmission to other stations on realterm 7. Proper receival of data from other stations on our realterm*
3. Uses Nexys4 board 100Mhz clock; all flip-flop clock inputs tied directly to this signal	Code inspection *(all the instances of the clk use in the modules are provided)*	Provided the clock report from vivado
4. Contains no latches	Inspection of Synthesis Report	Provided the section in vivado synthesis report
5. Test circuit – show test that test circuit functions properly to exercises circuit.	Demonstration in hardware 1. Proper display of cardet output on oscilloscope 2. Proper display of reset on seven segment display on Nexys board 3. Proper display of manchester receiver data on seven segment display 4. Proper display of full, empty and ready on LEDs on Nexys board 5. Proper display of received data on the oscilloscope 6. Demostrated the transition from asynchronous transmitter to RealTerm input 6. Proper display of data transmission to other stations on realterm 7. Proper receival of data from other stations on our realterm*	Demonstration to Professor Nadovich
In submitting this checklist as part of our report, I/We certify that the tests described above were conducted and that the results of these tests are accurately described and represented. I/We understand that any misrepresentation of the tests or the results constitutes a violation of the College policy on academic dishonesty.		
Name(s):Kemal Dilsiz & Zainab Hussein Date: 11/10/2016		

*Demonstration was not satisfactory

Verification for this lab is not yet sufficient as have only been able to demonstrate transmission to the instructor and one other group (Rachel and Craig). The receival was not yet demonstrated as there is currently still unsatisfactory amount of noise present as we receive during the becon mode or when another student transmits to our station. We are working on making out noise tolerance efficient in the PREAMBLE state, where it seemed to show "synchronize" even without meeting the set threshold in the design.

4. Conclusion

We were able to transmit data to other stations, but the setbacks in our receival suggests rethinking our receiver synchronization procedure before having a realistic chance at proper functionality for the project.

Lessons learnt:

- Confidence in use of Realterm computer simulation in various data types

- Debugging and more debugging
- Proper time management

References

- WimpFi Wireless Basics Presentation Slides
- Wimp Fi Radio Data Sheet and Schematic