TECHNICAL MEMORANDUM

Lafayette College

Title: ECE 491 Lab 1

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Abstract

This lab is to explain the logic behind the code & testing.

1. Introduction

This design makes it possible to have Seven Segment display sections to be used individually by implementing a separate active-low "anode enable" signal. Every segment can count from 0 to 16 with hex system. Also can individually add a decimal point or not.

This makes it possible to control a lot of information with only 15 switches! Each number can be individually assigned and can be modified with a decimal point.

2. The Design

The design was provided in the lab report. I have simply connected the modules.

First I'm going to provide the figures again and then explain the connections.

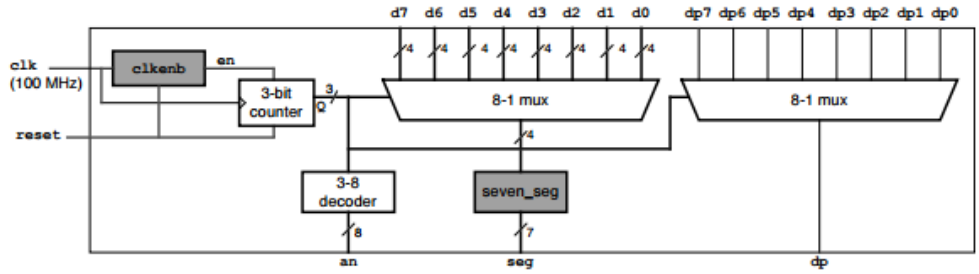
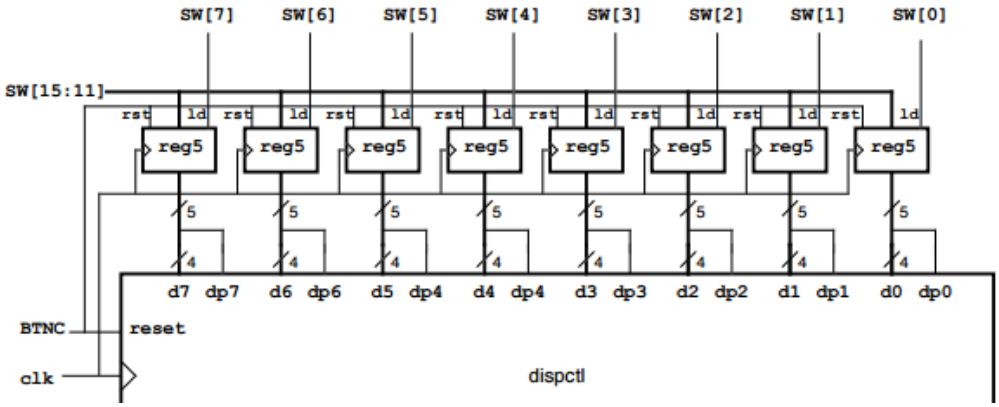


Figure 5 – Suggested Approach for `dispctl` Circuit



General design is exactly the same as the diagrams, where 8 **reg5** modules and a **dispctl** module is used and the **dispctl** module includes the modules included in figure 5.

Switches are passed through **reg_parm** module to get **d** and **dp** outputs which are passed through **muxes** inside the **dispctl** module.

Clock is provided to **3-bit counter** for the **3-8 decoder** which determines the specific anode to be enabled and also the same counter provides states into the **muxes** which will pull in the specific **d** and **dp** values for the seven segment. Therefore we can use this clock counter to determine how long each segment is going to stay lit up.

3. Design Verification

I only used Nexys 4 to physically test the code, I did not have a simulation module.

Description	**Test Method**	**Detailed Results**
1. Module Interface	Code Inspection	Code works, some of the input parameters had to be changed.
2. Module function: accepts four 4-bit inputs and four 1-bit "decimal point" inputs and displays 4 7-segment outputs without noticeable flicker.	Demonstration in hardware using Nexys 4 DDR board: Proper display of all 8 digits and 16 digit symbols. Proper display of 4 decimal points Free of noticeable flicker	Was demonstrated to Professor Nadovich with the following methods: >Ascending & Descending number combinations >Decimal points at random locations >Reset button functionality >Displaying both hex and decimal digits

3. Uses Nexys4 board 100Mhz clock; all flip-flop clock inputs tied directly to this signal	Code inspection
	(Providing both the clkenb module code and the instance of the module)
		//**module code**
		module clkenb(input logic clk, reset, output logic enb);
		parameter DIVFREQ = 100; // desired frequency in Hz (change as needed)
		parameter CLKFREQ = 100_000_000;
		//**instance of the module**
		clkenb #(.DIVFREQ(1000)) CLKENB(clk,reset, enb);

4. Contains no latches	Inspection of Synthesis Report	No muxes without default, or flip flops functionality with missing input
5. Test circuit – show test that test circuit functions properly to exercises circuit.	Demonstration in hardware	The demonstration was accepted by Prof Nadovich
In submitting this checklist as part of our report, I/We certify that the tests described above were conducted and that the results of these tests are accurately described and represented. I/We understand that any misrepresentation of the tests or the results constitutes a violation of the College policy on academic dishonesty.		
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4. Conclusion

We accomplished increasing the amount of data presented in seven segments with only 15 input switches. Our design works well and can be easily connected to other projects/modules for a seven segment that could have higher level use.

References

[1] ECE Department. *Lab 1 – 7-Segment LED Controller.* ECE Department, Lafayette College. Revised August 25, 2016