TECHNICAL MEMORANDUM
Lafayette College

Title: ECE 491 Lab 1
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Date: September 13, 2016

Abstract

In this project, we have built an asynchronous serial transmitter and tested it with boundary conditions with three different methods. We made use of Verilog Test benches, oscilloscope and RealTerm program simulation testing methods.

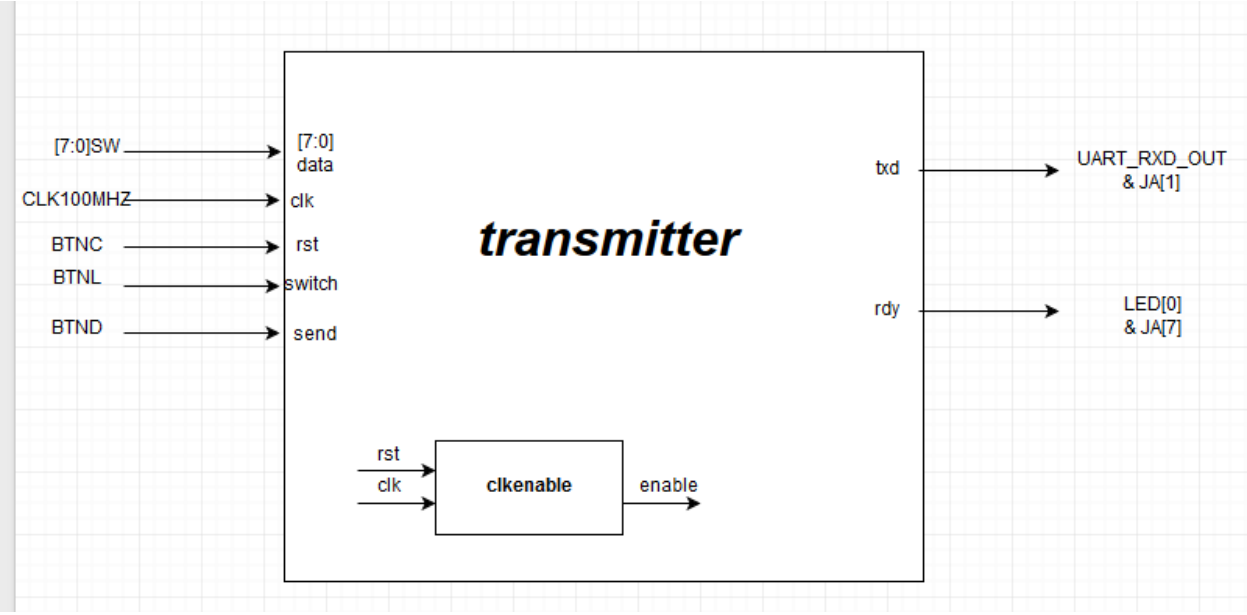
1. Introduction

This design is an old way of transmitting information with a single bit output. Whereas the information is 8 bits, the transferred data is required to be 10 bits for the receiver to recognize the pattern. Start bit of 0, transferred 8 bits and stop bit of 1 totals up to 10 bits.

BaudRate is modifiable in the design which makes it possible to send data with different frequencies.

2. The Design

The top module diagram is below.



In this diagram, the transfer of data depends on the inputs switch and send. We have built a state transition system with 12 states:

IDLE, START, TR0, TR1, …, TR7, STOP, WAIT

WAIT state is for single data transmission but first we will explain the rest.

When send is not registered as 1, IDLE state is present. If send is asserted, the data transmission starts with the state START. TR is an abbreviation for Transfer and each state transfers the corresponding data bit.

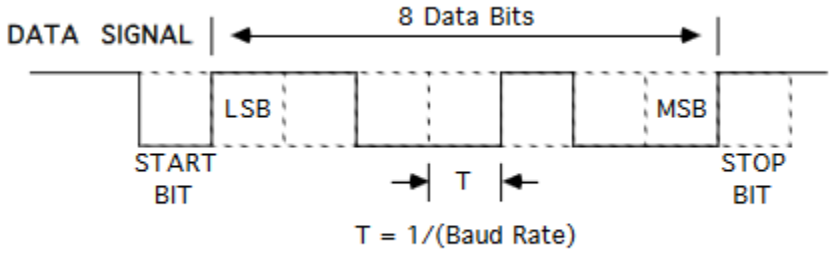


Figure 2 – Serial Data Transmission

Here in the diagram:

Start bit → START

Data[0] → TR0

Data[1] → TR1

…

Data[7] → TR7

Stop bit → STOP

Are the corresponding states and the transition happens when BAUDRATE is synced with the CLK100MHZ.

Therefore, simply, when the **send** is asserted, **rdy** goes to 0 and the data transmission happens without an interruption. In STOP state, **rdy** is asserted back to 1 to indicate being ready to accept new transmission.

WAIT state happens when switch is asserted as 1 and **send** is asserted as 0. This stops the next **state** from going back to IDLE or START to avoid a new transmission because of a long send signal.

clkenable module converts the CLK100MHZ to the desired BAUDRATE which was 9600 in this experiment except for the test bench where it was 25MHZ for easier calculation.

In our first design, we were considering few alternatives. We first decided to use a counter to change the transferred data and have only 4 states, IDLE, TRANSFER, STOP, WAIT where START was not necessary because the first loop of Transfer would give **txd** a value of 0. However, we decided to change the design for easier observation in test bench where we could clearly compare the **txd** values with TR states and the data input.

3. Design Verification

We have used three methods for testing our transmitter (~~which was a pain in the a**~~).

Description	Test Method	Detailed Results	
1. Module Interface	Code Inspection	We added few extra inputs and outputs compared to the Lab design and everything is connected and Vivado does not give any errors.	
2. Module function: accepts data of 8 bits and send input and transmits data bits one by one with a txd output and indicates readiness for the next transmission with rdy output	Demonstration in oscilloscope, test bench and RealTerm simulation and Nexys4DDR board: • Proper display of rdy output with a LED of the board • Proper display of 01010101, 00110011, 00001111, 00000000, 11111111 data inputs with oscilloscope • Proper display of BaudRate with oscilloscope • Proper display of ASCII values with RealTerm simulation • Proper display of single and multiple data transmissions with RealTerm transmission • Proper display of rdy output on oscilloscope • Proper display of different&random data transmissions in the oscilloscope • Display of data transmission in test bench • Display of STOP-START transition in the test bench • Display of 2 different data inputs in the test bench		Please check the diagrams below with the explanations under.

3. Uses Nexys4 board 100Mhz clock; all flip-flop clock inputs tied directly to this signal	Code inspection *(all the instances of the clk use in the modules are provided)*	//module nexys4DDR top module
		transmitter #(.BAUD(BAUD)) TRANS(.data(SW), .send(BTND), .clk(CLK100MHZ), .rst(BTNC), .switch(BTNL), .txd(UART_RXD_OUT), .rdy(LED));
		
		//module transmitter
		clkenb #(.DIVFREQ(BAUD)) CLKENB(.clk(clk), .reset(rst), .enb(BaudRate));
		
		always_ff@(posedge clk)
		begin
		if(rst)
		…
		else if(BaudRate)
		…	

4. Contains no latches	Inspection of Synthesis Report	No flip flops functionality with missing input State transition also has a default state to avoid latches.	
5. Test circuit – show test that test circuit functions properly to exercises circuit.	Demonstration in hardware	The demonstration was accepted by Prof Nadovich	

In submitting this checklist as part of our report, I/We certify that the tests described above were conducted and that the results of these tests are accurately described and represented. I/We understand that any misrepresentation of the tests or the results constitutes a violation of the College policy on academic dishonesty.

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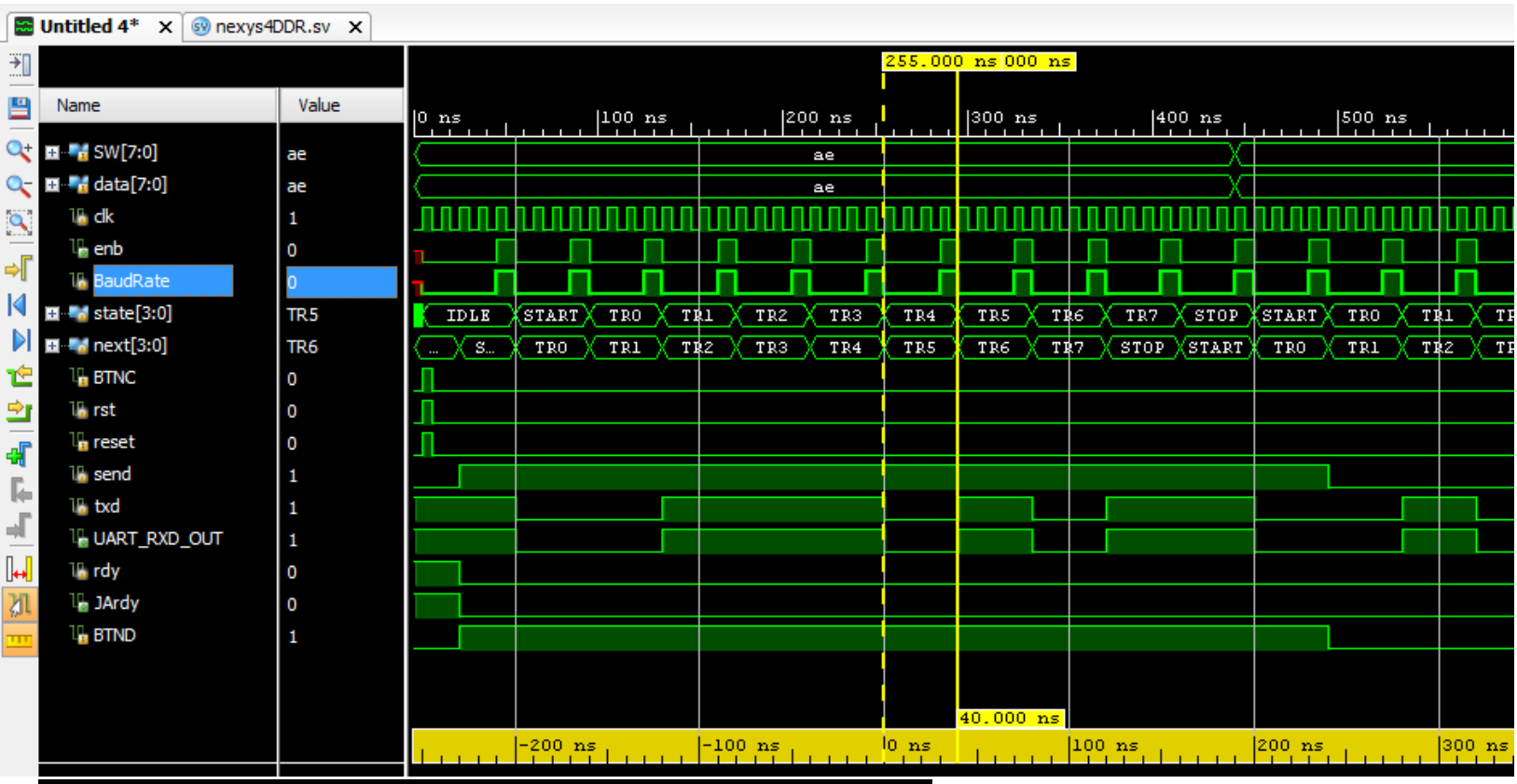
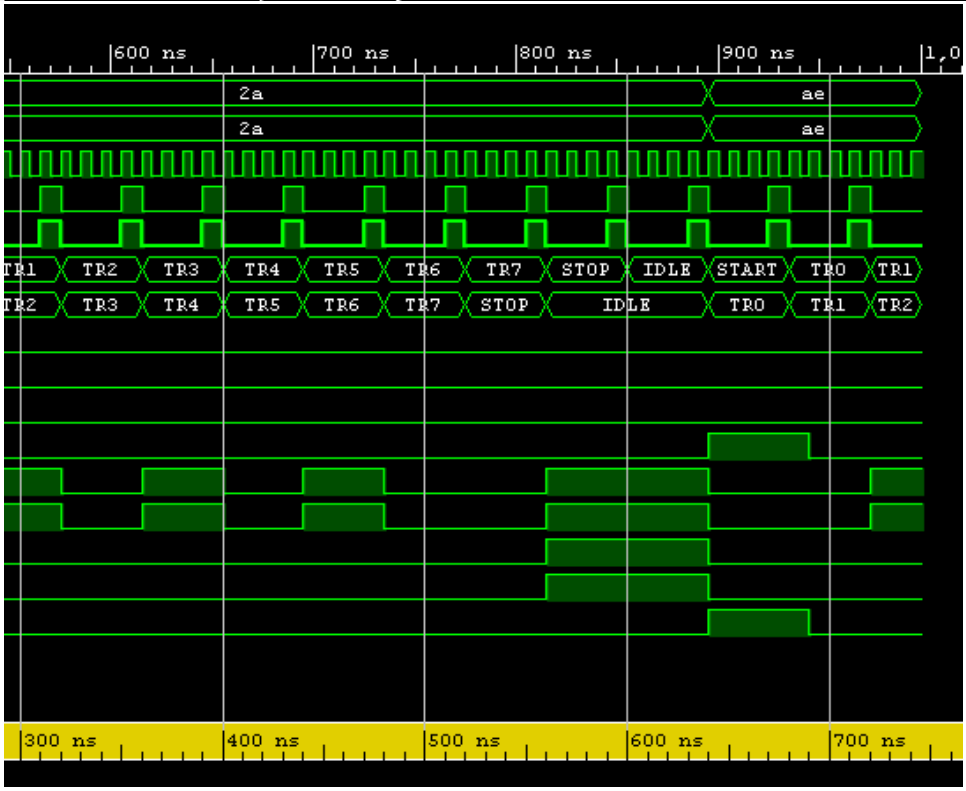
Test bench until 300ns, BaudRate is displayed → enable is every 40ns → 25MHZ BaudRate

At 450th ns, you can see the transition from STOP state to START state without IDLE



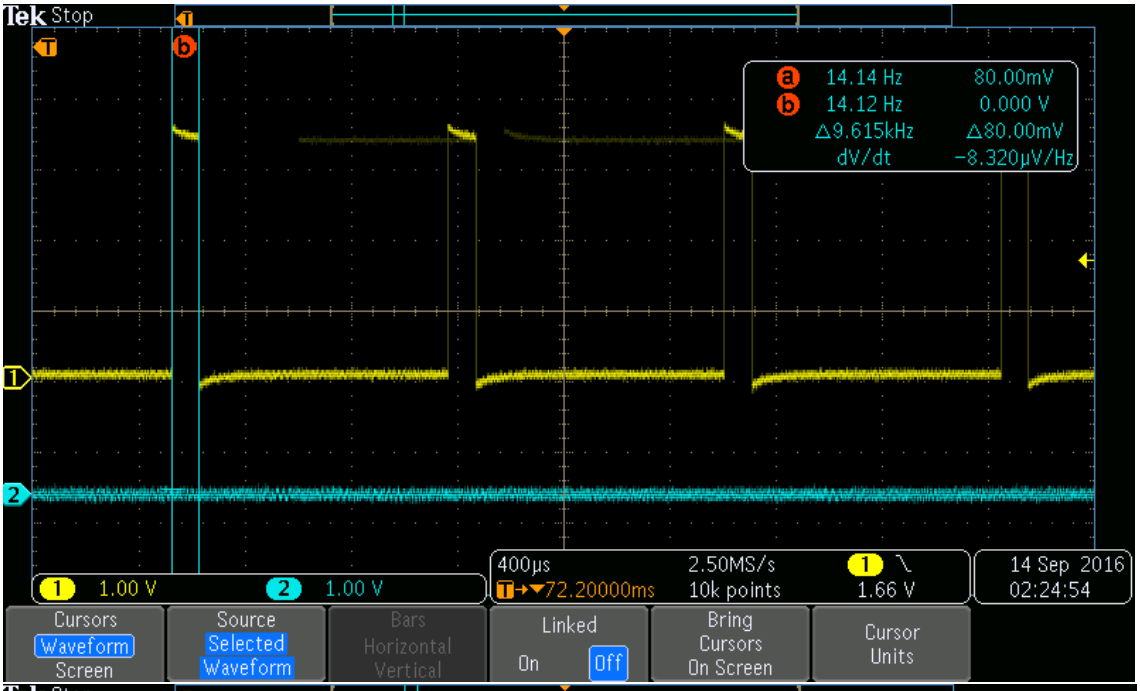


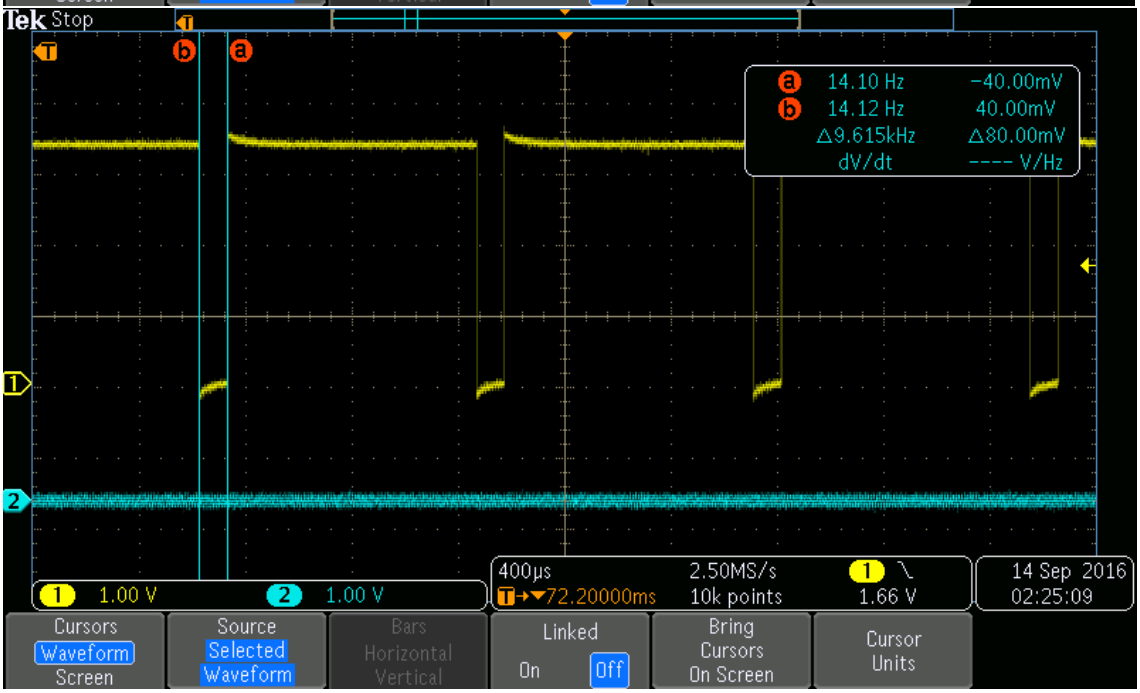
At 800th ns, you can see the STOP-IDLE-START transition compared to the 450th ns in the previous diagram.

Rest of the test bench results are self-explanatory.

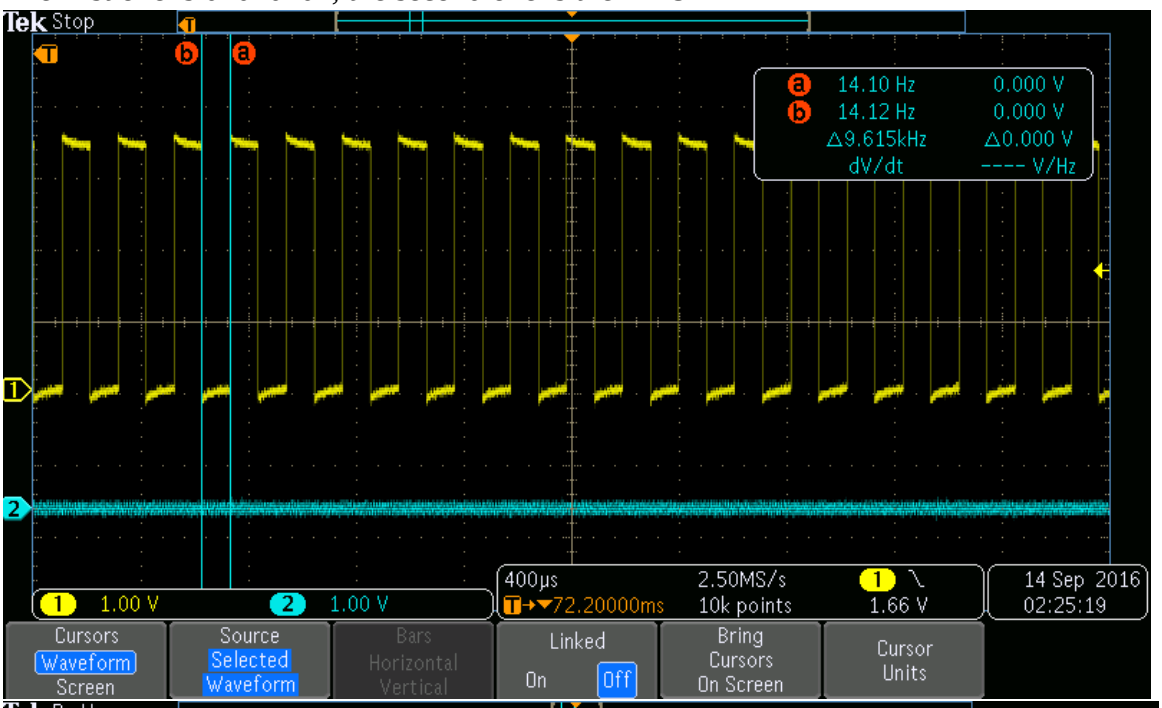
Oscilloscope Diagrams

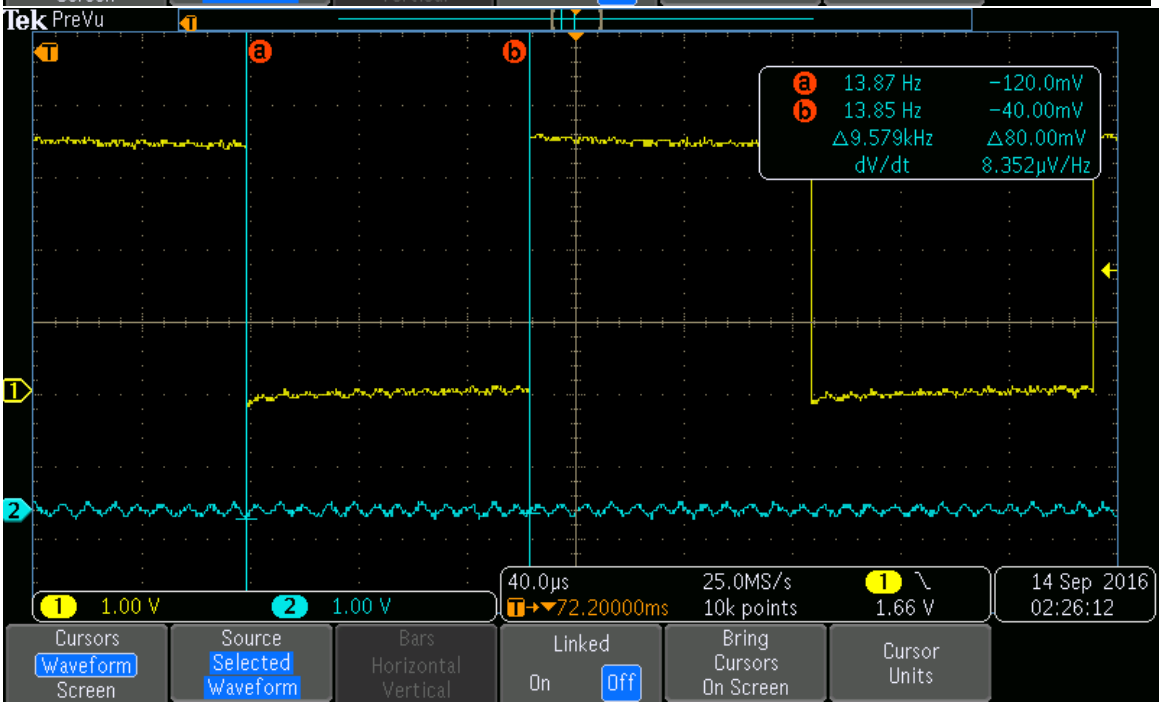
First one is 00000000, second one is 11111111



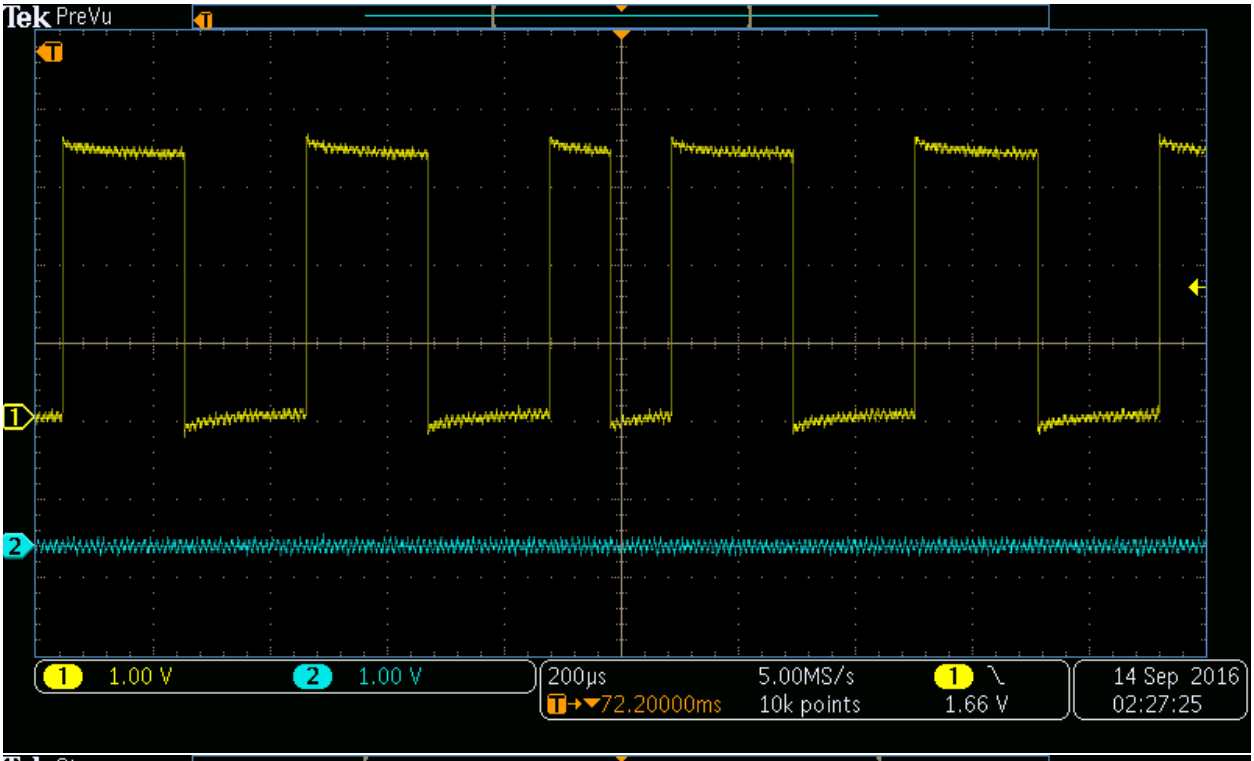


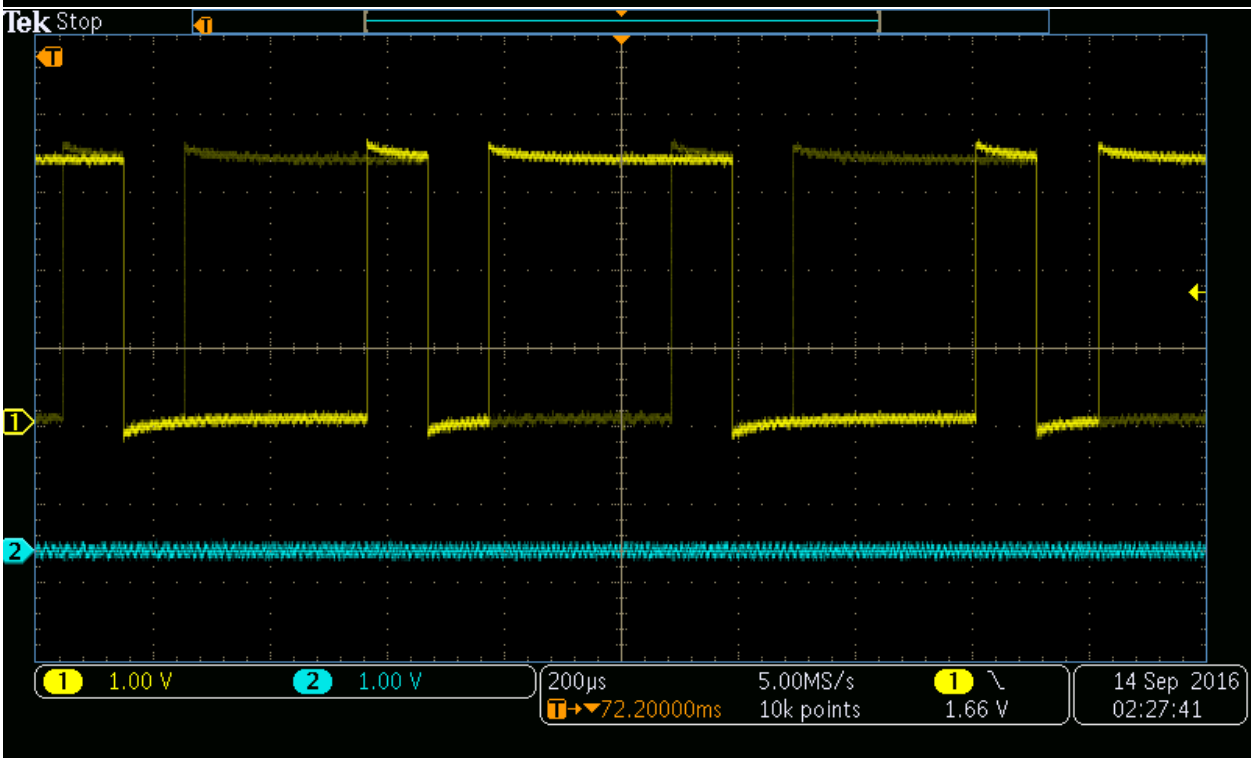
The first one is 01010101, the second one is the BAUDRATE



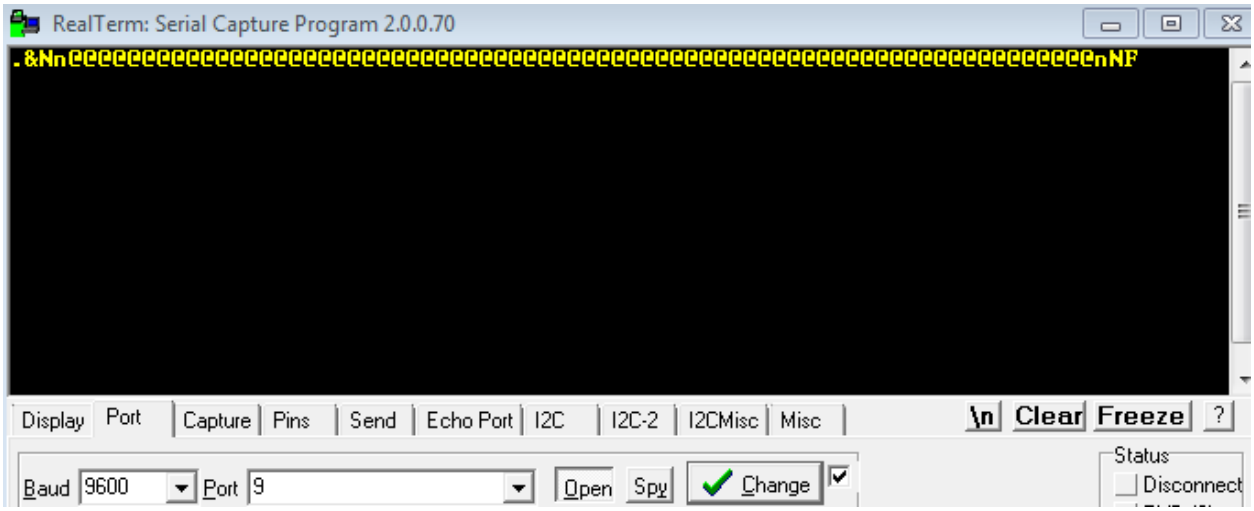


The first one is 11001100, the second one is 11110000





RealTerm simulation diagrams



4. Conclusion

We accomplished building an asynchronous serial transmitter where we could send both a single data transmission and a continuous data transmission.

Lessons learned:

- Creating a top module for the entire design is helpful (nexys4DDR module vs transmitter module)
- Test benches are the first step in debugging the code before other physical & visual tests
- Using oscilloscope to test the functionality of the transmitter module through Nexys4DDR board terminal connections
- Time management

References

[1] ECE Department. *Lab 2 – Sequential FPGA Design with Verilog.* ECE Department, Lafayette College. Revised September 4, 2016