

# MIPS Superscaler Cycle Processor Emulator Project

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## Description

In this project, you will create a simulator for a pipelined, super-scalar processor with cache. Your simulator will support the instruction set described in Project 1, and must be able to load a binary MIPS file and execute it. Furthermore, your simulator will produce the disassembled program code (exactly as you did in Project 1), and will produce a cycle-by-cycle simulation showing the processor state at each cycle. The processor state includes the contents of registers, buffers, cache, and data memory at each cycle. You do not need to implement exception/interrupt handling

## Implementation

You may use any programming language that you like. You **MUST** include instructions in a README file that indicate how to compile (if necessary) and run your program. You **MUST** include a **Makefile** that will compile your code (if necessary).

It is highly recommended that in each cycle, your program executes each pipeline stage in REVERSE order. That is, first handle the WB stage, then the MEM/ALU stages, then the ISSUE stage, then the IF stage. By executing the pipelines in this order, you will ensure that the cache is updated in the proper order, and you will not have collisions in the buffers between pipeline stages.

## Execution

Your program must accept command line arguments for execution. The following arguments must be supported (Executable named “mipssim”):

```
mipssim -i INPUTFILENAME -o OUTPUTFILENAME
```

Your program will produce 2 output files. One named **OUTPUTFILENAME\_pipeline.txt**, which contains the simulation output, and one named **OUTPUTFILENAME\_dis.txt**, which contains the disassembled program code for the input MIPS program.

Your program will be graded with the sample input and output provided to you

## Expected Output

Sample inputs and expected outputs are provided for testing. The most simple program is t1.bin and they are progressively more complex in the following order: t1.bin, t2.bin, t3.bin, t4.bin, sample.bin

One note: depending on when in the clock cycle you update cache, your program may end up with 2 cache lines switched from the provided output for t3.bin and t4.bin. This is OK.

## Details

Instruction format: The instruction format is exactly the same as in Project 1

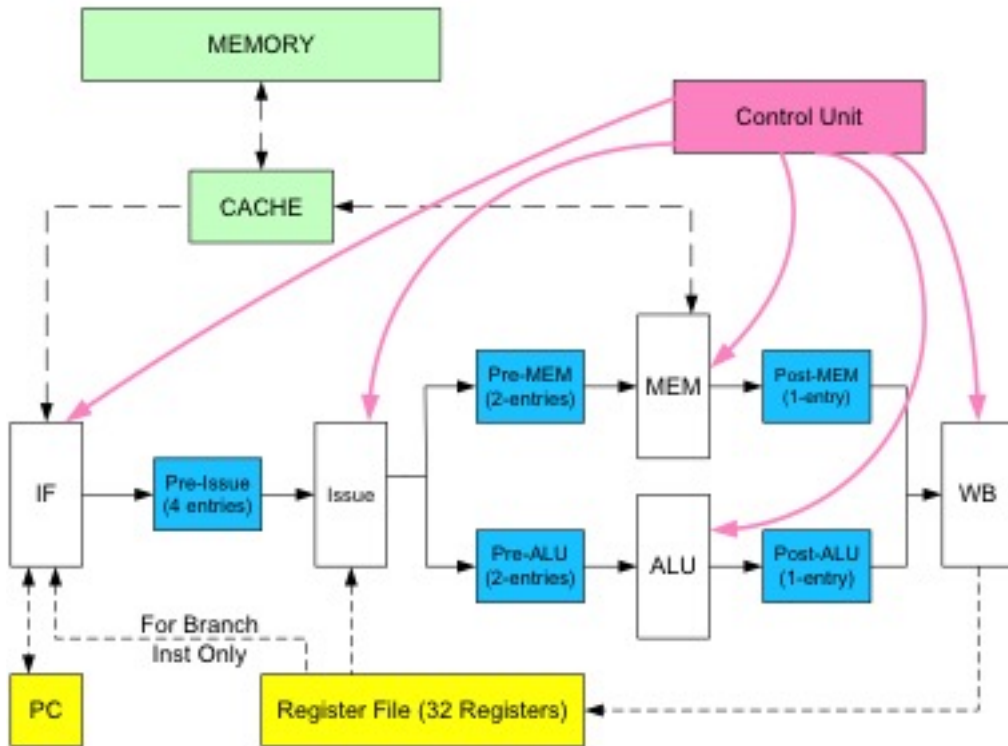


Figure 1: The processor datapath for this project.

White boxes represent functional units, blue boxes represent buffers (structured as queues) between the functional units, yellow boxes represent registers, and green boxes represent memory units. The various components are discussed in detail below:

## Instruction Fetch (IF)

Instruction fetch can fetch and decode up to two instructions at each clock cycle. Instructions are always fetched and decoded in program order. The following conditions must be met before instructions can be fetched:

1. If the fetch unit is stalled, no instruction can be fetched at the current cycle (no pre-fetching). The fetch unit can be stalled due to a branch instruction or a cache miss (cache is described below)
2. If there is no room in the pre-issue buffer, no instructions can be fetched at the current cycle
3. If there is only one empty slot in the pre-issue buffer, only one instruction will be fetched

The IF unit can only fetch and decode an instruction if it is in the cache. If the instruction to be fetched is in the cache, the entire fetch and decode process takes only 1 clock cycle. If the instruction to be fetched is not in the cache, the cache unit will fetch the instruction from memory and it will be in the cache at the next clock cycle. If the first instruction to be fetched is not in the cache, the second instruction cannot be fetched even if it is in the cache.

If a branch instruction (J, JR, BEQ, BLTZ) is fetched along with its next (in order) instruction, the next instruction will be discarded (it needs to be re-fetched based on the branch outcome).

If a branch instruction is fetched, the fetch unit will try to read all the argument registers in order to calculate the target address. If all registers are ready, or the target is immediate, the PC will be updated at the end of the cycle. Otherwise, the IF unit stalls until all argument registers are available. Therefore, if all registers are ready for a branch instruction, then no stalls are introduced.

A register can be written and read in the same clock cycle. Assume writes take place in the first half of the cycle, and reads take place in the second half of the cycle.

When a BREAK instruction is fetched, no more instructions will be fetched.

Branch, BREAK, NOP, and invalid instructions will all be fetched, but will not be written into the Pre-Issue Buffer (They are completely handled by IF). However, entries must be available in the Pre-Issue Buffer for any instruction to be fetched.

## Pre-Issue Buffer:

The pre-issue buffer has 4 entries, each entry can store a single instruction. The instructions are sorted in their program order (entry 0 always contains the oldest instruction and entry 3 contains the newest).

## Issue Unit:

The issue unit follows the basic scoreboard algorithm to issue instructions. It can issue up to two instructions, out of order, per clock cycle. When an instruction is issued, it moves out of the pre-issue buffer and into either the pre-mem buffer or the pre-ALU buffer. The issue unit searches from entry 0 to entry 3 (IN THAT ORDER) of the pre-issue buffer and issues instructions if:

1. No structural hazards exist (there is room in the pre-mem/pre-ALU destination buffer)

2. No WAW hazards exist active instructions (issued but not finished, or earlier no-issued instructions)
3. No WAR hazards exist with earlier not-issued instructions
4. No RAW hazards exist with active instructions (all operands are ready)
5. A load instruction must wait for all previous stores to be issued
6. Store instructions must be issued in order

Remember, registers can be written and read in the same cycle.

**Note**

ADD R3, R2, R1

ADD R3, R4, R5

Note that in the above instructions, the second instruction will not be issued until the first instruction has written back R3 in the write-back stage. The issue unit does not attempt to determine special cases in which WAW, RAW, or WAR hazards will be avoided.

## Pre-ALU Queue:

The pre-ALU buffer has two entries. Each entry can store an instruction with its operands. The buffer is managed as a FIFO queue

## ALU:

The ALU handles all non-memory instructions (everything except LW and SW and branch instructions that are handled in the IF stage). All ALU operations take one clock cycle. When the ALU finishes, the instruction is moved from the pre-ALU buffer to the post-ALU buffer. The ALU can only fetch one instruction from the pre-ALU buffer per clock cycle.

## Post-ALU buffer:

The post-ALU buffer has one entry that can store the instruction with the destination register ID and the result of the ALU operation

## Pre-Mem Queue:

The pre-mem buffer has two entries. Each entry can store an instruction with its address and data (for SW). It is managed as a FIFO queue.

## MEM Unit:

The MEM unit handles LW and SW operations.

For LW, it takes one cycle to finish if it hits in the cache. If it misses in the cache, then the operation cannot be performed and must be retried in the next cycle. In this case, the operation remains in the pre-mem buffer. When a cache hit occurs, the operation finishes and the instruction, destination register, and data will be written to the post-MEM buffer.

A SW takes one cycle to finish if it hits in the cache. If it misses in the cache, then the operation cannot be performed and must be retried in the next cycle. In this case, the operation remains in the pre-mem buffer. When a cache hit occurs, the SW instruction finishes. The SW instruction never goes into the post-MEM buffer.

## Write Back Unit:

The WB unit can execute two write-backs in one cycle. It fetches the contents of the post-ALU and post-MEM buffers and updates the register file.

## PC:

The PC holds the address of the next instruction. It should be initialized to 96.

## Register File:

There are 32 registers. Assume sufficient read/write ports to perform all necessary operations during a single clock cycle.

## Notes on Pipeline:

1. The execution finishes when a BREAK instruction is fetched and the pipeline is empty (all other instructions have finished)
2. No data forwarding
3. No delay slot will be used for branching
4. Different instructions finish in different stages:
  - NOP, Branch, BREAK only use IF stage
  - SW only uses IF, issue, MEM stages
  - LW uses IF, issue, MEM, WB stages
  - ALU ops use IF, issue, ALU, WB stages

## Cache Description:

The cache is uniform (holds both data and instructions) and is a 2-way associative cache with 4 sets. Each cache line/block contains 2 data words (1 word = 32 bits = 4 bytes). Because each cache line/block is 64 bits wide, all memory fetch operations will return two words (64 bits). The cache is organized as follows:

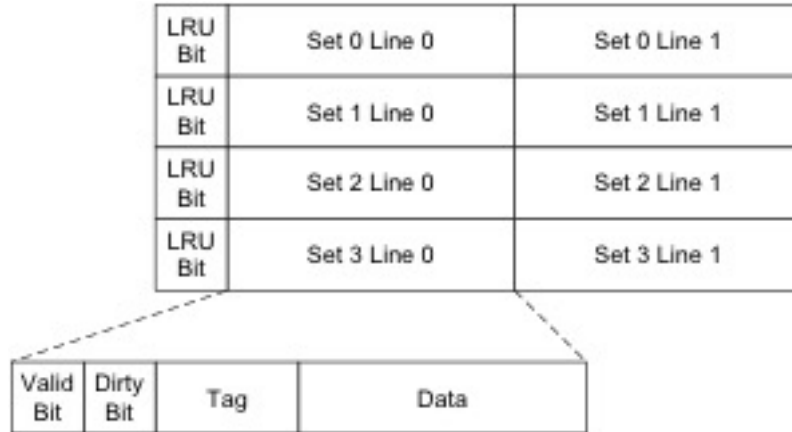


Figure 2: Cache diagram for the project.

Note that since all address are word aligned , the lower two bits will be discarded when calculating which set data will be written to in cache. Furthermore, since each cache line is 2 words wide, memory is effectively two word aligned, so the lower three bits of a memory address are discarded when calculating which cache set data should be written to.

There are sufficient ports of cache so that the IF and MEM unit can access the cache at the same cycle without any port conflict. If the two units are accessing the same set at the same time, assume MEM will be executed at the first half of the cycle and IF will be executed at the second half of the cycle.

Note that the IF unit can only execute 1 memory read per cycle. Therefore, if the IF unit is attempting to fetch the instructions as 100 and 104, and neither are in cache, then a memory read for the words at address 96 and 100 can be initiated. The memory read for the words at addresses 104 and 108 must be initiated during the next clock cycle.

All the bits will be initialized as 0. (The LRU bit is initialized to 0 also.)

When a valid line exists, the valid bit will be turned on (set to be 1).

The dirty bit will be turn on when the pipeline writes to any part of the line.

It takes 1 cycle to get data from main memory to cache. Assume bypassing is used here so that both the cache and the request unit (IF or MEM) can get the data at the same cycle. For example, if IF requests a data in cycle 5 and it is a miss the IF and cache will get the data in cycle 6.

The write-back from cache to main memory takes no time (for simplification).

All dirty blocks will be written back at the cycle the simulation is finished.

## Output Format

At the end of a clock cycle, the processor, cache, and memory state will be output.

If any entry in a buffer/queue is empty, no content should be printed. Only instructions are printed, not addresses or values computed. The instruction should be printed as it was for Project 1.

Every cache line must be printed, even if it is empty. Furthermore, the cache values should be printed as a bit string.

The output format is as follows:

```
20 hyphens and a new line
Cycle[value]:
<blank_line>
Pre-Issue Buffer:
<tab>Entry 0:<tab>[instruction]
<tab>Entry 1:<tab>[instruction]
<tab>Entry 2:<tab>[instruction]
<tab>Entry 3:<tab>[instruction]
Pre_ALU Queue:
<tab>Entry 0:<tab>[instruction]
<tab>Entry 1:<tab>[instruction]
Post_ALU Queue:
<tab>Entry 0 :<tab>[instruction]
Pre_MEM Queue:
<tab>Entry 0:<tab>[instruction]
<tab>Entry 1:<tab>[instruction]
Post_MEM Queue:
<tab> Entry 0:<tab>[instruction]
< blank_line >
Registers
R00:< tab >< int(R0) >< tab >< int(R1) >..
```

## Grading

A valid attempt that compiles successfully and produces simulation files for at least 10 clock cycles (even if the files do NOT match the expected output for those 10 cycles) will receive 72 points. Note that it is not sufficient for those 10 cycles to attempt to re-execute the same instruction. At the very least, it should fetch successive instructions. Your basic program should also disassemble the programs correctly (you should already have a working disassembler).

Each **simulation file** that matches the expected output provided in the following files will receive 7 points. Therefore, to get 100 percent you must match the output for each of the 4 binary files provided.

We expect your simulation file to EXACTLY match ours. We will use the diff program to verify exactness. We will use diff -w to suppress white space differences.

It may happen that in the t3.bin and t4.bin files you end up with 2 cache lines that are swapped. This occurs based on the timing of your IF and Memory unit access in a clock cycle. This is OK, and you will NOT be counted off for it. You only have to match t3.bin and t4.bin output up to 20 clock cycles for full credit.



**EX\_readBinaryFile.cpp**

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```
#include <iostream>
#include <unistd.h>
#include <fcntl.h>
#include <iomanip>
using namespace std;

int main()
{
    char buffer[4];
    int i;
    char * iPtr;
    iPtr = (char*)(void*) &i;

    int FD = open("test2.bin", O_RDONLY);

    int amt = 4;
    while( amt != 0 )
    {
        amt = read(FD, buffer, 4);
        if( amt == 4)
        {
            iPtr[0] = buffer[3];
            iPtr[1] = buffer[2];
            iPtr[2] = buffer[1];
            iPtr[3] = buffer[0];
            cout << "i = " << hex << i << endl;
        }
    }
}
```

```
import java.io.BufferedInputStream;
import java.io.DataInputStream;
import java.io.File;
import java.io.FileInputStream;
import java.io.FileNotFoundException;
import java.io.IOException;

class EX_readBinaryFile
{
    public static void main(String[] args) throws IOException, FileNotFoundException
    {
        File file = new File("test1.bin");
        byte[] fileData = new byte[(int) file.length()];
        DataInputStream dis = new DataInputStream(new FileInputStream(file));
        dis.readFully(fileData);
        dis.close();

        for( int i = 0; i < fileData.length; i+=4 )
        {
            int x = 0;
            x = x | ((fileData[i] & 0x000000FF)<<24);
            x = x | ((fileData[i+1] & 0x000000FF) << 16);
            x = x | ((fileData[i+2] & 0x000000FF) << 8);
            x = x | (fileData[i+3] & 0x000000FF);
            System.out.println(x);
            System.out.println((x>>26) & 0x0000003F);
            System.out.println(((x<<6)>>27) & 0x0000001F);
            System.out.println( Integer.toHexString(x) );

        }

    }

}
```

```
import sys
import os
import struct

# convert ints to signed
def imm16BitUnsignedTo32BitSignedConverter( num ):
    negBitMask = 0x00008000
    # if the 16th bit is 1, the 16 bit value is negative
    if( negBitMask & num ) > 0 :
        # put 1s in the upper 16 bits
        num = num | 0xFFFF0000
        # now perform a 2's complement conversion
        # flip the bits using XOR
        num = num ^ 0xFFFFFFFF
        # add 1
        num = num + 1
        # num is now the positive version of the number
        # multiply by -1 to get a signed integer with the negative number
        num = num * -1
    return num

# how to read binary file and get ints
inFile = open( sys.argv[1], 'rb' )

# get the file length
inFileLen = os.stat( sys.argv[1] )[6]
inFileWords = inFileLen / 4

instructions = []
address = []
# read the words from the file
for i in range( inFileWords ) :
    instructions.append( struct.unpack('>I', inFile.read(4))[0] )
    address.append( 96 + (i*4) )

    # use I to hold the current instruction
    I = instructions[ len(instructions)-1 ]
    # get IMMEDIATE bits
    IMM = ((I << 16) & 0xFFFFFFFF) >> 16
    IMM = imm16BitUnsignedTo32BitSignedConverter( IMM )
    print bin(I)
    print IMM
    # get the opcode bits
    OP = I>>26
    print OP
    # get the RS bits
    RS = ((I<<6) & 0xFFFFFFFF) >> 27
    print RS
    print '----'

inFile.close()
```

```

/*****
This program converts a binary file to a file
containing string representations of the 1's and 0's
in the binary file.
*****/

// gcc -o b2t b2t.c
// Usage ./a.out < inputfile > outputfile

#include<stdio.h>

main( int argc, char** argv)
{
    if ( argc >1 )
        fprintf(stderr,"Usage: ./a.out < input_txt > output_bin\n");
    char word[32];
    unsigned char vals[4];
    unsigned char w, div, b;
    unsigned char tot ;

    w = 0;
    while( scanf( "%c", &tot) != EOF )
    {
        div = 128;
        for( b=0; b<8; b++ )
        {
            if( tot >= div)
            {
                printf( "1" );
                tot -= div;
            }
            else
                printf( "0");
            div = div/2;
        }
        w ++;
        if ( w == 4 )
        {
            printf("\n");
            w = 0;
        }
    }
}

```

```
/******
This program converts a text file containing text
strings of 1's and 0's to a binary file.

for example, the text string:
00000001000000001111111110101010
would result in the following binary sequence
(written as hex here) in the output file:
0100FFAA
*****/

// gcc -o t2b t2b.c
// Usage ./a.out < inputfile > outputfile

#include<stdio.h>

main( int argc , char **argv )
{
    if( argc > 1 )
        fprintf(stderr,"Usage: ./a.out < input_txt > output_bin\n");
    char word[32];
    unsigned char vals[4];
    int w, mul, b;
    unsigned char tot ;

    while( scanf(" %s", word ) > 0 )
    {
        for( w=0; w<4; w++ )
        {
            mul = 128;
            tot = 0;
            for( b=0; b<8; b++ )
            {
                tot += (word[w*8+b]=='1')*mul;
                mul = mul/2;
            }
            fputc( tot, stdout);
        }
    }
}
```

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-----  
Cycle:1

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 3: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

128: 4 16

-----  
Cycle:2

Pre-Issue Buffer:

Entry 0: [LW R1, 128(R0)]  
Entry 1: [ADDI R1, R1, #-8]  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

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Post\_MEM Queue:  
Entry 0:

## Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010000000,1010000000100001111111111111000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

128: 4 16

-----  
Cycle:3

## Pre-Issue Buffer:

Entry 0: [ADDI R1, R1, #-8]

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R1, 128(R0)]

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010000000,1010000000100001111111111111000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0



```

      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Data

128: 4 16

-----  
Cycle:4

Pre-Issue Buffer:

```

      Entry 0:      [ADDI    R1, R1, #-8]
      Entry 1:      [SW      R1, 128(R0)]
      Entry 2:
      Entry 3:

```

Pre\_ALU Queue:

```

      Entry 0:
      Entry 1:

```

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R1, 128(R0)]

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

```

R00: 0 0 0 0 0 0 0 0
R08: 0 0 0 0 0 0 0 0
R16: 0 0 0 0 0 0 0 0
R24: 0 0 0 0 0 0 0 0

```

Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010000000,1010000000100001111111111111000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10101100000000010000000010000000,100001000010000000000000000000010&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Data

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128: 4 16

Cycle:5

Pre-Issue Buffer:

Entry 0: [ADDI R1, R1, #-8]  
Entry 1: [SW R1, 128(R0)]  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0: [LW R1, 128(R0)]

Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,3)<10001100000000010000000010000000,101000000010000111111111111000>]

Entry

1: [(1,0,4)<00000000000000000000000000000100,000000000000000000000000010000>]

Set 1: LRU=1

Entry

0: [(1,0,3)<10101100000000010000000010000000,10000100001000000000000000000010>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 3: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

128: 4 16

Cycle:6

Pre-Issue Buffer:

Entry 0: [SW R1, 128(R0)]  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0: [ADDI R1, R1, #-8]  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:  
Post\_MEM Queue:  
Entry 0:

## Registers

R00:	0	4	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000010000000,1010000000100001111111111111000&gt;]

Entry

1: [(1,0,4)&lt;00000000000000000000000000000100,000000000000000000000000010000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10101100000000010000000010000000,10000100001000000000000000000010&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

128: 4 16

Cycle:7

## Pre-Issue Buffer:

Entry 0: [SW R1, 128(R0)]

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0: [ADDI R1, R1, #-8]

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	4	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000010000000,1010000000100001111111111111000&gt;]

Entry

1: [(1,0,4)&lt;00000000000000000000000000000100,000000000000000000000000010000&gt;]

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```
Set 1: LRU=1
      Entry
0: [(1,0,3)<10101100000000010000000010000000,1000010000100000000000000000000010>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
```

```
Data
128:    4      16
-----
Cycle:8
```

```
Pre-Issue Buffer:
      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:
Pre_ALU Queue:
      Entry 0:
      Entry 1:
Post_ALU Queue:
      Entry 0:
Pre_MEM Queue:
      Entry 0:      [SW      R1, 128(R0)]
      Entry 1:
Post_MEM Queue:
      Entry 0:
```

```
Registers
R00:    0      -4      0      0      0      0      0      0
R08:    0      0      0      0      0      0      0      0
R16:    0      0      0      0      0      0      0      0
R24:    0      0      0      0      0      0      0      0
```

```
Cache
Set 0: LRU=0
      Entry
0: [(1,0,3)<10001100000000010000000010000000,101000000010000111111111111000>]
      Entry
1: [(1,0,4)<00000000000000000000000000000100,000000000000000000000000010000>]
Set 1: LRU=1
      Entry
0: [(1,0,3)<10101100000000010000000010000000,10000100001000000000000000000010>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
```

# t1\_pipeline.txt

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Data

```
128:      4      16
-----
Cycle:9
```

Pre-Issue Buffer:

```
Entry 0:
Entry 1:
Entry 2:
Entry 3:
```

Pre\_ALU Queue:

```
Entry 0:
Entry 1:
```

Post\_ALU Queue:

```
Entry 0:
```

Pre\_MEM Queue:

```
Entry 0:
Entry 1:
```

Post\_MEM Queue:

```
Entry 0:
```

Registers

```
R00:      0      -4      0      0      0      0      0      0
R08:      0      0      0      0      0      0      0      0
R16:      0      0      0      0      0      0      0      0
R24:      0      0      0      0      0      0      0      0
```

Cache

Set 0: LRU=0

Entry

```
0: [(1,0,3)<10001100000000010000000010000000,1010000000100001111111111111000>]
```

Entry

```
1: [(1,1,4)<11111111111111111111111111111100,000000000000000000000000010000>]
```

Set 1: LRU=1

Entry

```
0: [(1,0,3)<10101100000000010000000010000000,10000100001000000000000000000010>]
```

Entry

```
1: [(0,0,0)<00000000000000000000000000000000,0000000000000000000000000000000>]
```

Set 2: LRU=0

Entry

```
0: [(0,0,0)<00000000000000000000000000000000,0000000000000000000000000000000>]
```

Entry

```
1: [(0,0,0)<00000000000000000000000000000000,0000000000000000000000000000000>]
```

Set 3: LRU=0

Entry

```
0: [(0,0,0)<00000000000000000000000000000000,0000000000000000000000000000000>]
```

Entry

```
1: [(0,0,0)<00000000000000000000000000000000,0000000000000000000000000000000>]
```

Data

```
128:      4      16
-----
Cycle:10
```

Pre-Issue Buffer:

```
Entry 0:
Entry 1:
Entry 2:
Entry 3:
```

Pre\_ALU Queue:

```
Entry 0:
Entry 1:
```

Post\_ALU Queue:

```
Entry 0:
```

Pre\_MEM Queue:

Entry 0:  
 Entry 1:  
 Post\_MEM Queue:  
 Entry 0:

## Registers

R00:	0	-4	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000010000000,1010000000100001111111111111000&gt;]

Entry

1: [(1,0,4)&lt;11111111111111111111111111111100,000000000000000000000000010000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10101100000000010000000010000000,10000100001000000000000000000010&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;00000000000000000000000000000000,100000000000000000000000000001101&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

128: -4 16

t2\_dis.txt

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```
1 00011 00000 00001 00000 00010 000000 96 LW R1, 128(R0)
1 00011 00000 00010 00000 00010 100000 100 LW R2, 160(R0)
1 01011 00000 00001 00000 00010 000100 104 SW R1, 132(R0)
1 00011 00000 00011 00000 00011 000000 108 LW R3, 192(R0)
1 01011 00000 00001 00000 00010 100100 112 SW R1, 164(R0)
1 00011 00000 00100 00000 00011 000100 116 LW R4, 196(R0)
1 00001 00100 00000 11111 11111 111101 120 BLTZ R4, #-12
1 00000 00000 00000 00000 00000 001101 124 BREAK
0000000000000000000000000000000011 128 3
1111111111111111111111111111111011 132 -5
0000000000000000000000000000000000 136 0
0000000000000000000000000000000000 140 0
0000000000000000000000000000000000 144 0
0000000000000000000000000000000000 148 0
0000000000000000000000000000000000 152 0
0000000000000000000000000000000000 156 0
0000000000000000000000000000000100 160 4
1111111111111111111111111111111010 164 -6
0000000000000000000000000000000000 168 0
0000000000000000000000000000000000 172 0
0000000000000000000000000000000000 176 0
0000000000000000000000000000000000 180 0
0000000000000000000000000000000000 184 0
0000000000000000000000000000000000 188 0
1111111111111111111111111111111110 192 -2
0000000000000000000000000000000000 196 0
```

-----  
Cycle:1

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 3: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

128:	3	-5	0	0	0	0	0	0
160:	4	-6	0	0	0	0	0	0
192:	-2	0						

-----  
Cycle:2

Pre-Issue Buffer:

Entry 0: [LW R1, 128(R0)]  
Entry 1: [LW R2, 160(R0)]  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:



Entry 0:  
Entry 1:  
Post\_MEM Queue:  
Entry 0:

## Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010000000,10001100000000100000000010100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

128:	3	-5	0	0	0	0	0	0
160:	4	-6	0	0	0	0	0	0
192:	-2	0						

-----  
Cycle:3

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R1, 128(R0)]

Entry 1: [LW R2, 160(R0)]

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

```

0: [(1,0,3)<100011000000000100000000,10001100000000100000000010100000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=0
    Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
    Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

## Data

```

128:  3    -5    0    0    0    0    0    0
160:  4    -6    0    0    0    0    0    0
192: -2     0
-----

```

Cycle:4

## Pre-Issue Buffer:

```

    Entry 0:      [SW    R1, 132(R0)]
    Entry 1:      [LW    R3, 192(R0)]
    Entry 2:
    Entry 3:

```

## Pre\_ALU Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_ALU Queue:

```

    Entry 0:

```

## Pre\_MEM Queue:

```

    Entry 0:      [LW    R1, 128(R0)]
    Entry 1:      [LW    R2, 160(R0)]

```

## Post\_MEM Queue:

```

    Entry 0:

```

## Registers

```

R00:  0    0    0    0    0    0    0    0
R08:  0    0    0    0    0    0    0    0
R16:  0    0    0    0    0    0    0    0
R24:  0    0    0    0    0    0    0    0

```

## Cache

Set 0: LRU=1

Entry

```

0: [(1,0,3)<100011000000000100000000,10001100000000100000000010100000>]

```

Entry

```

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 1: LRU=1

Entry

```

0: [(1,0,3)<10101100000000010000000010000100,10001100000000110000000011000000>]

```

Entry

```

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 2: LRU=0

Entry

```

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Entry

```

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 3: LRU=0

```

Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
128:  3      -5      0      0      0      0      0      0
160:  4      -6      0      0      0      0      0      0
192: -2       0
-----

```

Cycle:5

```

Pre-Issue Buffer:
Entry 0:      [SW      R1, 132(R0)]
Entry 1:      [LW      R3, 192(R0)]
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R2, 160(R0)]
Entry 1:
Post_MEM Queue:
Entry 0:      [LW      R1, 128(R0)]

```

```

Registers
R00:  0      0      0      0      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

Cache

Set 0: LRU=0

```

Entry
0: [(1,0,3)<10001100000000010000000010000000,10001100000000100000000010100000>]
Entry
1: [(1,0,4)<00000000000000000000000000000011,1111111111111111111111111111011>]

```

Set 1: LRU=1

```

Entry
0: [(1,0,3)<10101100000000010000000010000100,10001100000000110000000011000000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 2: LRU=0

```

Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 3: LRU=0

```

Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
128:  3      -5      0      0      0      0      0      0
160:  4      -6      0      0      0      0      0      0
192: -2       0
-----

```

Cycle:6

```

Pre-Issue Buffer:
Entry 0:      [LW      R3, 192(R0)]

```

# t2\_pipeline.txt

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```

Entry 1:      [SW      R1, 164(R0)]
Entry 2:      [LW      R4, 196(R0)]
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R2, 160(R0)]
Entry 1:      [SW      R1, 132(R0)]
Post_MEM Queue:
Entry 0:

```

## Registers

```

R00:  0      3      0      0      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

```

Entry
0: [(1,0,3)<10001100000000001000000001000000,10001100000000100000000010100000>]
Entry

```

```

1: [(1,0,4)<00000000000000000000000000000011,111111111111111111111111111111011>]
Set 1: LRU=1
Entry

```

```

0: [(1,0,3)<101011000000000010000000010000100,10001100000000110000000011000000>]
Entry

```

```

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=1
Entry

```

```

0: [(1,0,3)<101011000000000010000000010100100,100011000000001000000000011000100>]
Entry

```

```

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
Entry

```

```

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Entry

```

```

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
128:  3      -5      0      0      0      0      0      0
160:  4      -6      0      0      0      0      0      0
192: -2       0
-----

```

```

Cycle:7

```

```

Pre-Issue Buffer:
Entry 0:      [SW      R1, 164(R0)]
Entry 1:      [LW      R4, 196(R0)]
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [SW      R1, 132(R0)]
Entry 1:      [LW      R3, 192(R0)]
Post_MEM Queue:
Entry 0:      [LW      R2, 160(R0)]

```

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R00:	0	3	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

[illegible]

128:	3	-5	0	0	0	0	0	0
160:	4	-6	0	0	0	0	0	0
192:	-2	0						

```

M Queue:
  Entry 0:

```

R00:	0	3	4	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Entry

```

0: [(1,0,3)<10101100000000010000000010000100,10001100000000110000000011000000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<10101100000000010000000010100100,10001100000001000000000011000100>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<1000010010000000111111111111101,100000000000000000000000000001101>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
128:  3      -5      0      0      0      0      0      0
160:  4      -6      0      0      0      0      0      0
192: -2       0
-----

```

Cycle:9

```

Pre-Issue Buffer:
    Entry 0:      [LW      R4, 196(R0)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:      [LW      R3, 192(R0)]
    Entry 1:      [SW      R1, 164(R0)]
Post_MEM Queue:
    Entry 0:

```

```

Registers
R00:  0      3      4      0      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

```

Cache
Set 0: LRU=0
    Entry
0: [(1,0,5)<00000000000000000000000000000100,11111111111111111111111111111010>]
    Entry
1: [(1,1,4)<00000000000000000000000000000011,00000000000000000000000000000011>]
Set 1: LRU=1
    Entry
0: [(1,0,3)<10101100000000010000000010000100,10001100000000110000000011000000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<10101100000000010000000010100100,10001100000001000000000011000100>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<1000010010000000111111111111101,100000000000000000000000000001101>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```
Data
128:  3      -5      0      0      0      0      0      0
160:  4      -6      0      0      0      0      0      0
192: -2       0
```

-----  
Cycle:10

Pre-Issue Buffer:

```
Entry 0:
Entry 1:
Entry 2:
Entry 3:
```

Pre\_ALU Queue:

```
Entry 0:
Entry 1:
```

Post\_ALU Queue:

```
Entry 0:
```

Pre\_MEM Queue:

```
Entry 0:      [SW      R1, 164(R0)]
Entry 1:      [LW      R4, 196(R0)]
```

Post\_MEM Queue:

```
Entry 0:      [LW      R3, 192(R0)]
```

Registers

```
R00:  0      3      4      0      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0
```

Cache

Set 0: LRU=1

Entry

0: [(1,0,6)<111111111111111111111111111111110,000000000000000000000000000000>]

Entry

1: [(1,1,4)<0000000000000000000000000000000011,000000000000000000000000000011>]

Set 1: LRU=1

Entry

0: [(1,0,3)<10101100000000010000000010000100,10001100000000110000000011000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,000000000000000000000000000000>]

Set 2: LRU=1

Entry

0: [(1,0,3)<10101100000000010000000010100100,10001100000001000000000011000100>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,000000000000000000000000000000>]

Set 3: LRU=1

Entry

0: [(1,0,3)<10000100100000001111111111111101,10000000000000000000000000001101>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,000000000000000000000000000000>]

Data

```
128:  3      -5      0      0      0      0      0      0
160:  4      -6      0      0      0      0      0      0
192: -2       0
```

-----  
Cycle:11

Pre-Issue Buffer:

```
Entry 0:
Entry 1:
Entry 2:
Entry 3:
```

Pre\_ALU Queue:

```
Entry 0:
```

```

Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [SW      R1, 164(R0)]
Entry 1:      [LW      R4, 196(R0)]
Post_MEM Queue:
Entry 0:

```

```

Registers
R00:  0      3      4      -2      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

```

Cache
Set 0: LRU=1
Entry
0: [(1,0,6)<111111111111111111111111111111110,00000000000000000000000000000000>]
Entry
1: [(1,1,4)<0000000000000000000000000000000011,000000000000000000000000000011>]
Set 1: LRU=1
Entry
0: [(1,0,3)<1010110000000001000000001000100,10001100000000110000000011000000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10101100000000010000000010100100,10001100000001000000000011000100>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=1
Entry
0: [(1,0,3)<10000100100000001111111111111101,100000000000000000000000000001101>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
128:  3      -5      0      0      0      0      0      0
160:  4      -6      0      0      0      0      0      0
192: -2       0
-----

```

Cycle:12

```

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R4, 196(R0)]
Entry 1:
Post_MEM Queue:
Entry 0:

```

```

Registers
R00:  0      3      4      -2      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```



```

Cache
Set 0: LRU=0
      Entry
0: [(1,0,6)<111111111111111111111111111111110,00000000000000000000000000000000>]
      Entry
1: [(1,1,5)<00000000000000000000000000000000100,000000000000000000000000000011>]
Set 1: LRU=1
      Entry
0: [(1,0,3)<101011000000000010000000010000100,10001100000000110000000011000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=1
      Entry
0: [(1,0,3)<101011000000000010000000010100100,10001100000000100000000011000100>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<100001001000000001111111111111101,100000000000000000000000000001101>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data
128:   3     3     0     0     0     0     0     0
160:   4    -6     0     0     0     0     0     0
192:  -2     0
-----
Cycle:13

Pre-Issue Buffer:
      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:
Pre_ALU Queue:
      Entry 0:
      Entry 1:
Post_ALU Queue:
      Entry 0:
Pre_MEM Queue:
      Entry 0:
      Entry 1:
Post_MEM Queue:
      Entry 0:          [LW      R4, 196(R0)]

Registers
R00:   0     3     4     -2     0     0     0     0
R08:   0     0     0     0     0     0     0     0
R16:   0     0     0     0     0     0     0     0
R24:   0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=1
      Entry
0: [(1,0,6)<111111111111111111111111111111110,00000000000000000000000000000000>]
      Entry
1: [(1,1,5)<00000000000000000000000000000000100,000000000000000000000000000011>]
Set 1: LRU=1
      Entry
0: [(1,0,3)<101011000000000010000000010000100,10001100000000110000000011000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=1
      Entry

```

```

0: [(1,0,3)<10101100000000010000000010100100,10001100000001000000000011000100>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<1000010010000000111111111111101,100000000000000000000000000001101>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
128:  3      3      0      0      0      0      0      0
160:  4     -6      0      0      0      0      0      0
192: -2      0
-----

```

Cycle:14

Pre-Issue Buffer:

```

    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:

```

Pre\_ALU Queue:

```

    Entry 0:
    Entry 1:

```

Post\_ALU Queue:

```

    Entry 0:

```

Pre\_MEM Queue:

```

    Entry 0:
    Entry 1:

```

Post\_MEM Queue:

```

    Entry 0:

```

Registers

```

R00:  0      3      4     -2      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

Cache

Set 0: LRU=1

Entry

```

0: [(1,0,6)<11111111111111111111111111111110,00000000000000000000000000000000>]
    Entry

```

```

1: [(1,1,5)<0000000000000000000000000000000100,0000000000000000000000000000011>]

```

Set 1: LRU=1

Entry

```

0: [(1,0,3)<10101100000000010000000010000100,10001100000000110000000011000000>]
    Entry

```

```

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 2: LRU=1

Entry

```

0: [(1,0,3)<10101100000000010000000010100100,10001100000001000000000011000100>]
    Entry

```

```

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 3: LRU=1

Entry

```

0: [(1,0,3)<1000010010000000111111111111101,100000000000000000000000000001101>]
    Entry

```

```

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
128:  3      3      0      0      0      0      0      0
160:  4     -6      0      0      0      0      0      0
192: -2      0
-----

```

Cycle:15

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	3	4	-2	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,6)&lt;111111111111111111111111111111110,000000000000000000000000000000&gt;]

Entry

1: [(1,0,5)&lt;00000000000000000000000000000000100,000000000000000000000000000011&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10101100000000010000000010000100,10001100000000110000000011000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,000000000000000000000000000000&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10101100000000010000000010100100,10001100000001000000000011000100&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,000000000000000000000000000000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10000100100000001111111111111101,100000000000000000000000000001101&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,000000000000000000000000000000&gt;]

Data

128:	3	3	0	0	0	0	0	0
160:	4	3	0	0	0	0	0	0
192:	-2	0						

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-----  
Cycle:1

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 3: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

136:	12	0	0	20	0	-5
------	----	---	---	----	---	----

-----  
Cycle:2

Pre-Issue Buffer:

Entry 0: [LW R1, 136(R0)]  
Entry 1: [LW R2, 136(R1)]  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

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Post\_MEM Queue:  
Entry 0:

## Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010001000,10001100001000100000000010001000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

136: 12 0 0 20 0 -5

-----  
Cycle:3

## Pre-Issue Buffer:

Entry 0: [LW R2, 136(R1)]

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R1, 136(R0)]

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010001000,10001100001000100000000010001000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

```

      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Data

```
136:    12      0      0      20      0      -5
```

-----  
Cycle:4

Pre-Issue Buffer:

```

      Entry 0:      [LW      R2, 136(R1)]
      Entry 1:      [LW      R3, 136(R2)]
      Entry 2:      [ADD      R4, R1, R3]
      Entry 3:

```

Pre\_ALU Queue:

```

      Entry 0:
      Entry 1:

```

Post\_ALU Queue:

```

      Entry 0:

```

Pre\_MEM Queue:

```

      Entry 0:      [LW      R1, 136(R0)]
      Entry 1:

```

Post\_MEM Queue:

```

      Entry 0:

```

Registers

```

R00:    0      0      0      0      0      0      0      0
R08:    0      0      0      0      0      0      0      0
R16:    0      0      0      0      0      0      0      0
R24:    0      0      0      0      0      0      0      0

```

Cache

Set 0: LRU=1

```

      Entry

```

```
0: [(1,0,3)<100011000000000010000000010001000,10001100001000100000000010001000>]

```

```

      Entry

```

```
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 1: LRU=1

```

      Entry

```

```
0: [(1,0,3)<100011000100001100000000010001000,100000000001000110010000000100000>]

```

```

      Entry

```

```
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 2: LRU=0

```

      Entry

```

```
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

      Entry

```

```
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 3: LRU=0

```

      Entry

```

```
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

      Entry

```

```
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Data

```
136:    12      0      0      20      0      -5
```

```
-----
Cycle:5
```

```
Pre-Issue Buffer:
```

```
Entry 0:    [LW      R2, 136(R1)]
Entry 1:    [LW      R3, 136(R2)]
Entry 2:    [ADD     R4, R1, R3]
Entry 3:
```

```
Pre_ALU Queue:
```

```
Entry 0:
Entry 1:
```

```
Post_ALU Queue:
```

```
Entry 0:
```

```
Pre_MEM Queue:
```

```
Entry 0:
Entry 1:
```

```
Post_MEM Queue:
```

```
Entry 0:    [LW      R1, 136(R0)]
```

```
Registers
```

```
R00:    0      0      0      0      0      0      0      0
R08:    0      0      0      0      0      0      0      0
R16:    0      0      0      0      0      0      0      0
R24:    0      0      0      0      0      0      0      0
```

```
Cache
```

```
Set 0: LRU=1
```

```
Entry
```

```
0: [(1,0,3)<10001100000000010000000010001000,10001100001000100000000010001000>]
```

```
Entry
```

```
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
```

```
Set 1: LRU=0
```

```
Entry
```

```
0: [(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]
```

```
Entry
```

```
1: [(1,0,4)<000000000000000000000000000000001100,00000000000000000000000000000000>]
```

```
Set 2: LRU=0
```

```
Entry
```

```
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
```

```
Entry
```

```
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
```

```
Set 3: LRU=0
```

```
Entry
```

```
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
```

```
Entry
```

```
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
```

```
Data
```

```
136:    12      0      0      20      0      -5
```

```
-----
Cycle:6
```

```
Pre-Issue Buffer:
```

```
Entry 0:    [LW      R3, 136(R2)]
Entry 1:    [ADD     R4, R1, R3]
Entry 2:    [ADD     R3, R4, R2]
Entry 3:    [ADDI    R1, R2, #-5]
```

```
Pre_ALU Queue:
```

```
Entry 0:
Entry 1:
```

```
Post_ALU Queue:
```

```
Entry 0:
```

```
Pre_MEM Queue:
```

```
Entry 0:    [LW      R2, 136(R1)]
```



Entry 1:  
Post\_MEM Queue:  
Entry 0:

## Registers

R00:	0	12	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010001000,10001100001000100000000010001000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,3)&lt;10001100010000110000000010001000,10000000001000110010000000100000&gt;]

Entry

1: [(1,0,4)&lt;000000000000000000000000000001100,00000000000000000000000000000000&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;100000000100000100001100000100000,1010000001000001111111111111011&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

136: 12 0 0 20 0 -5

-----  
Cycle:7

## Pre-Issue Buffer:

Entry 0: [LW R3, 136(R2)]

Entry 1: [ADD R4, R1, R3]

Entry 2: [ADD R3, R4, R2]

Entry 3: [ADDI R1, R2, #-5]

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R2, 136(R1)]

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	12	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010001000,10001100001000100000000010001000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

```

Set 1: LRU=0
      Entry
0: [(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]
      Entry
1: [(1,0,4)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=1
      Entry
0: [(1,0,3)<10000000100000100001100000100000,1010000001000001111111111111011>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
136:  12    0    0    20    0   -5
-----

```

Cycle:8

```

Pre-Issue Buffer:
      Entry 0:      [LW      R3, 136(R2)]
      Entry 1:      [ADD      R4, R1, R3]
      Entry 2:      [ADD      R3, R4, R2]
      Entry 3:      [ADDI     R1, R2, #-5]

```

```

Pre_ALU Queue:
      Entry 0:
      Entry 1:

```

```

Post_ALU Queue:
      Entry 0:

```

```

Pre_MEM Queue:
      Entry 0:
      Entry 1:

```

```

Post_MEM Queue:
      Entry 0:      [LW      R2, 136(R1)]

```

```

Registers
R00:  0    12    0    0    0    0    0    0
R08:  0    0    0    0    0    0    0    0
R16:  0    0    0    0    0    0    0    0
R24:  0    0    0    0    0    0    0    0

```

Cache

```

Set 0: LRU=1
      Entry
0: [(1,0,3)<10001100000000010000000010001000,10001100001000100000000010001000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=0
      Entry
0: [(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]
      Entry
1: [(1,0,4)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(1,0,3)<10000000100000100001100000100000,1010000001000001111111111111011>]
      Entry
1: [(1,0,4)<00000000000000000000000000000000,000000000000000000000000010100>]
Set 3: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Data  
136: 12 0 0 20 0 -5  
-----

Cycle:9

Pre-Issue Buffer:  
Entry 0: [ADD R4, R1, R3]  
Entry 1: [ADD R3, R4, R2]  
Entry 2: [ADDI R1, R2, #-5]  
Entry 3:

Pre\_ALU Queue:  
Entry 0:  
Entry 1:

Post\_ALU Queue:  
Entry 0:

Pre\_MEM Queue:  
Entry 0: [LW R3, 136(R2)]  
Entry 1:  
Post\_MEM Queue:  
Entry 0:

Registers  
R00: 0 12 20 0 0 0 0 0  
R08: 0 0 0 0 0 0 0 0  
R16: 0 0 0 0 0 0 0 0  
R24: 0 0 0 0 0 0 0 0

Cache

Set 0: LRU=1

Entry  
0: [(1,0,3)<10001100000000010000000010001000,10001100001000100000000010001000>]

Entry  
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=0

Entry  
0: [(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]

Entry  
1: [(1,0,4)<000000000000000000000000000001100,00000000000000000000000000000000>]

Set 2: LRU=0

Entry  
0: [(1,0,3)<1000000001000001000001100000100000,1010000001000001111111111111011>]

Entry  
1: [(1,0,4)<00000000000000000000000000000000,000000000000000000000000010100>]

Set 3: LRU=0

Entry  
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry  
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data  
136: 12 0 0 20 0 -5  
-----

Cycle:10

Pre-Issue Buffer:  
Entry 0: [ADD R4, R1, R3]  
Entry 1: [ADD R3, R4, R2]  
Entry 2: [ADDI R1, R2, #-5]  
Entry 3: [ADDI R3, R2, #-5]

Pre\_ALU Queue:  
Entry 0:  
Entry 1:

Post\_ALU Queue:  
Entry 0:

Pre\_MEM Queue:

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```

Entry 0:      [LW      R3, 136(R2)]
Entry 1:
Post_MEM Queue:
Entry 0:

```

```

Registers
R00:  0      12      20      0      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

```

Cache
Set 0: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000010001000,10001100001000100000000010001000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=0
Entry
0: [(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]
Entry
1: [(1,0,4)<00000000000000000000000000001100,00000000000000000000000000000000>]
Set 2: LRU=0
Entry
0: [(1,0,3)<10000000100000100001100000100000,1010000001000001111111111111011>]
Entry
1: [(1,0,4)<00000000000000000000000000000000,000000000000000000000000000010100>]
Set 3: LRU=1
Entry
0: [(1,0,3)<1010000001000011111111111111011,10101100000000010000000010001000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
136:  12      0      0      20      0      -5
-----

```

Cycle:11

```

Pre-Issue Buffer:
Entry 0:      [ADD      R4, R1, R3]
Entry 1:      [ADD      R3, R4, R2]
Entry 2:      [ADDI     R1, R2, #-5]
Entry 3:      [ADDI     R3, R2, #-5]

```

```

Pre_ALU Queue:
Entry 0:
Entry 1:

```

```

Post_ALU Queue:
Entry 0:

```

```

Pre_MEM Queue:
Entry 0:
Entry 1:

```

```

Post_MEM Queue:
Entry 0:      [LW      R3, 136(R2)]

```

```

Registers
R00:  0      12      20      0      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

```

Cache
Set 0: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000010001000,10001100001000100000000010001000>]
Entry

```

```

1:[(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=0
    Entry
0:[(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]
    Entry
1:[(1,0,4)<000000000000000000000000000001100,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry
0:[(1,0,3)<10000000100000100001100000100000,1010000001000001111111111111011>]
    Entry
1:[(1,0,4)<00000000000000000000000000000000,000000000000000000000000000010100>]
Set 3: LRU=0
    Entry
0:[(1,0,3)<101000000100001111111111111011,10101100000000010000000010001000>]
    Entry
1:[(1,0,4)<00000000000000000000000000000000,11111111111111111111111111111011>]

```

```

Data
136:    12      0      0      20      0      -5
-----

```

Cycle:12

Pre-Issue Buffer:

```

    Entry 0:      [ADD    R3, R4, R2]
    Entry 1:      [ADDI   R3, R2, #-5]
    Entry 2:      [SW     R1, 136(R0)]
    Entry 3:

```

Pre\_ALU Queue:

```

    Entry 0:      [ADD    R4, R1, R3]
    Entry 1:      [ADDI   R1, R2, #-5]

```

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

```

R00:    0      12      20      -5      0      0      0      0
R08:    0      0      0      0      0      0      0      0
R16:    0      0      0      0      0      0      0      0
R24:    0      0      0      0      0      0      0      0

```

Cache

Set 0: LRU=1

Entry

```

0:[(1,0,3)<10001100000000010000000010001000,10001100001000100000000010001000>]
    Entry

```

```

1:[(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=0
    Entry

```

```

0:[(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]
    Entry

```

```

1:[(1,0,4)<000000000000000000000000000001100,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry

```

```

0:[(1,0,3)<10000000100000100001100000100000,1010000001000001111111111111011>]
    Entry

```

```

1:[(1,0,4)<00000000000000000000000000000000,000000000000000000000000000010100>]
Set 3: LRU=1
    Entry

```

```

0:[(1,0,3)<101000000100001111111111111011,10101100000000010000000010001000>]
    Entry

```

```

1:[(1,0,4)<00000000000000000000000000000000,11111111111111111111111111111011>]

```

Data  
136: 12 0 0 20 0 -5  
-----

Cycle:13

Pre-Issue Buffer:

Entry 0: [ADD R3, R4, R2]  
Entry 1: [ADDI R3, R2, #-5]  
Entry 2: [SW R1, 136(R0)]  
Entry 3:

Pre\_ALU Queue:

Entry 0: [ADDI R1, R2, #-5]  
Entry 1:

Post\_ALU Queue:

Entry 0: [ADD R4, R1, R3]

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	12	20	-5	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,3)<10001100000000010000000010001000,10001100001000100000000010001000>]

Entry

1: [(1,0,4)<1000010001100000111111111110111,100000000000000000000000000001101>]

Set 1: LRU=0

Entry

0: [(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]

Entry

1: [(1,0,4)<00000000000000000000000000001100,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(1,0,3)<100000001000001000001100000100000,101000000100000111111111111011>]

Entry

1: [(1,0,4)<00000000000000000000000000000000,0000000000000000000000000000010100>]

Set 3: LRU=1

Entry

0: [(1,0,3)<101000000100001111111111111011,10101100000000010000000010001000>]

Entry

1: [(1,0,4)<00000000000000000000000000000000,11111111111111111111111111111011>]

Data

136: 12 0 0 20 0 -5  
-----

Cycle:14

Pre-Issue Buffer:

Entry 0: [ADDI R3, R2, #-5]  
Entry 1: [SW R1, 136(R0)]  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0: [ADD R3, R4, R2]  
Entry 1:

Post\_ALU Queue:

Entry 0: [ADDI R1, R2, #-5]

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Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	12	20	-5	7	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,3)<10001100000000010000000010001000,10001100001000100000000010001000>]

Entry

1: [(1,0,4)<1000010001100000111111111110111,100000000000000000000000000000001101>]

Set 1: LRU=0

Entry

0: [(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]

Entry

1: [(1,0,4)<000000000000000000000000000000001100,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(1,0,3)<100000001000001000001100000100000,1010000001000001111111111111011>]

Entry

1: [(1,0,4)<00000000000000000000000000000000,0000000000000000000000000000000010100>]

Set 3: LRU=1

Entry

0: [(1,0,3)<101000000100001111111111111011,10101100000000010000000010001000>]

Entry

1: [(1,0,4)<00000000000000000000000000000000,11111111111111111111111111111011>]

Data

136:	12	0	0	20	0	-5
------	----	---	---	----	---	----

-----

Cycle:15

Pre-Issue Buffer:

Entry 0: [ADDI R3, R2, #-5]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0: [ADD R3, R4, R2]

Pre\_MEM Queue:

Entry 0: [SW R1, 136(R0)]

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	15	20	-5	7	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,3)<10001100000000010000000010001000,10001100001000100000000010001000>]

```

Entry
1: [(1,0,4)<1000010001100000111111111110111,100000000000000000000000000001101>]
Set 1: LRU=0
Entry
0: [(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]
Entry
1: [(1,0,4)<000000000000000000000000000001100,00000000000000000000000000000000>]
Set 2: LRU=0
Entry
0: [(1,0,3)<10000000100000100001100000100000,10100000010000011111111111111011>]
Entry
1: [(1,0,4)<00000000000000000000000000000000,0000000000000000000000000000010100>]
Set 3: LRU=1
Entry
0: [(1,0,3)<10100000010000111111111111111011,10101100000000010000000010001000>]
Entry
1: [(1,0,4)<00000000000000000000000000000000,111111111111111111111111111111011>]

```

## Data

```
136: 12 0 0 20 0 -5
```

```
-----
Cycle:16
```

## Pre-Issue Buffer:

```

Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0: [ADDI R3, R2, #-5]
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

```

## Registers

```

R00: 0 15 20 27 7 0 0 0
R08: 0 0 0 0 0 0 0 0
R16: 0 0 0 0 0 0 0 0
R24: 0 0 0 0 0 0 0 0

```

## Cache

```

Set 0: LRU=0
Entry
0: [(1,0,3)<10001100000000010000000010001000,10001100001000100000000010001000>]
Entry
1: [(1,0,4)<1000010001100000111111111110111,100000000000000000000000000001101>]
Set 1: LRU=0
Entry
0: [(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]
Entry
1: [(1,1,4)<000000000000000000000000000001111,00000000000000000000000000000000>]
Set 2: LRU=0
Entry
0: [(1,0,3)<10000000100000100001100000100000,10100000010000011111111111111011>]
Entry
1: [(1,0,4)<00000000000000000000000000000000,0000000000000000000000000000010100>]
Set 3: LRU=1
Entry
0: [(1,0,3)<10100000010000111111111111111011,10101100000000010000000010001000>]
Entry

```



1: [(1,0,4)<00000000000000000000000000000000,11111111111111111111111111111011>]

Data  
136: 12 0 0 20 0 -5

-----  
Cycle:17

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0: [ADDI R3, R2, #-5]

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	15	20	27	7	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,3)<10001100000000010000000010001000,10001100001000100000000010001000>]

Entry

1: [(1,0,4)<1000010001100000111111111110111,100000000000000000000000000001101>]

Set 1: LRU=0

Entry

0: [(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]

Entry

1: [(1,1,4)<000000000000000000000000000001111,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(1,0,3)<10000000100000100001100000100000,101000000100000111111111111011>]

Entry

1: [(1,0,4)<00000000000000000000000000000000,000000000000000000000000000010100>]

Set 3: LRU=1

Entry

0: [(1,0,3)<101000000100001111111111111011,1010110000000010000000010001000>]

Entry

1: [(1,0,4)<00000000000000000000000000000000,11111111111111111111111111111011>]

Data  
136: 12 0 0 20 0 -5

-----  
Cycle:18

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:  
 Pre\_MEM Queue:  
 Entry 0:  
 Entry 1:  
 Post\_MEM Queue:  
 Entry 0:

## Registers

R00:	0	15	20	15	7	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000010001000,10001100001000100000000010001000&gt;]

Entry

1: [(1,0,4)&lt;1000010001100000111111111110111,100000000000000000000000000001101&gt;]

Set 1: LRU=0

Entry

0: [(1,0,3)&lt;10001100010000110000000010001000,10000000001000110010000000100000&gt;]

Entry

1: [(1,1,4)&lt;000000000000000000000000000001111,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,3)&lt;1000000001000001000001100000100000,10100000010000011111111111111011&gt;]

Entry

1: [(1,0,4)&lt;00000000000000000000000000000000,000000000000000000000000000010100&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;101000000100001111111111111011,10101100000000010000000010001000&gt;]

Entry

1: [(1,0,4)&lt;00000000000000000000000000000000,11111111111111111111111111111011&gt;]

## Data

136:	12	0	0	20	0	-5
------	----	---	---	----	---	----

-----  
Cycle:19

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	15	20	15	7	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

```
0: [(1,0,3)<10001100000000010000000010001000,10001100001000100000000010001000>]
    Entry
1: [(1,0,4)<10000100011000001111111111110111,100000000000000000000000000001101>]
Set 1: LRU=0
    Entry
0: [(1,0,3)<10001100010000110000000010001000,10000000001000110010000000100000>]
    Entry
1: [(1,0,4)<000000000000000000000000000001111,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry
0: [(1,0,3)<100000001000001000001100000100000,1010000001000001111111111111011>]
    Entry
1: [(1,0,4)<00000000000000000000000000000000,000000000000000000000000000010100>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<1010000001000011111111111111011,10101100000000010000000010001000>]
    Entry
1: [(1,0,4)<00000000000000000000000000000000,111111111111111111111111111111011>]
```

Data

136:	15	0	0	20	0	-5
------	----	---	---	----	---	----

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-----  
Cycle:1

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 3: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

144: 1 1

-----  
Cycle:2

Pre-Issue Buffer:

Entry 0: [LW R1, 144(R0)]  
Entry 1: [LW R2, 148(R0)]  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:  
Entry 0:

## Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

144: 1 1

-----  
Cycle:3

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R1, 144(R0)]

Entry 1: [LW R2, 148(R0)]

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

```

      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Data

144: 1 1

-----  
Cycle:4

Pre-Issue Buffer:

Entry 0: [ADD R3, R3, R1]

Entry 1: [ADD R3, R3, R2]

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R1, 144(R0)]

Entry 1: [LW R2, 148(R0)]

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Data

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144: 1 1

Cycle:5

Pre-Issue Buffer:

Entry 0: [ADD R3, R3, R1]  
Entry 1: [ADD R3, R3, R2]  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R2, 148(R0)]  
Entry 1:

Post\_MEM Queue:

Entry 0: [LW R1, 144(R0)]

Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=1

Entry

0: [(1,0,3)<100000000110001000110000100000,100000000110001000110000100000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 2: LRU=1

Entry

0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 3: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

144: 1 1

Cycle:6

Pre-Issue Buffer:

Entry 0: [ADD R3, R3, R2]  
Entry 1: [ADDI R2, R2, #-1]  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0: [ADD R3, R3, R1]  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:



```

Entry 1:
Post_MEM Queue:
Entry 0:          [LW      R2, 148(R0)]

Registers
R00:  0      1      0      0      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=1
Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=0
Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data
144:  1      1
-----
Cycle:7

Pre-Issue Buffer:
Entry 0:          [ADD      R3, R3, R2]
Entry 1:          [ADDI     R2, R2, #-1]
Entry 2:
Entry 3:

Pre_ALU Queue:
Entry 0:
Entry 1:

Post_ALU Queue:
Entry 0:          [ADD      R3, R3, R1]

Pre_MEM Queue:
Entry 0:
Entry 1:

Post_MEM Queue:
Entry 0:

Registers
R00:  0      1      1      0      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Set 1: LRU=1
      Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
      Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=0
      Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Data

144: 1 1

-----  
Cycle:8

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0: [ADD R3, R3, R2]

Entry 1: [ADDI R2, R2, #-1]

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	1	1	1	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Entry

1: [(1,0,3)&lt;10100000010000101111111111111111,10000100010000000000000000000001&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

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Data

144: 1 1

Cycle:9

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0: [ADDI R2, R2, #-1]

Entry 1:

Post\_ALU Queue:

Entry 0: [ADD R3, R3, R2]

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00: 0 1 1 1 0 0 0 0

R08: 0 0 0 0 0 0 0 0

R16: 0 0 0 0 0 0 0 0

R24: 0 0 0 0 0 0 0 0

Cache

Set 0: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=1

Entry

0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]

Entry

1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]

Set 3: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

144: 1 1

Cycle:10

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0: [ADDI R2, R2, #-1]

Pre\_MEM Queue:

Entry 0:  
Entry 1:  
Post\_MEM Queue:  
Entry 0:

## Registers

R00:	0	1	1	2	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Entry

1: [(1,0,3)&lt;10100000010000101111111111111111,10000100010000000000000000000001&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

144: 1 1

-----  
Cycle:11

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	1	0	2	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

```

1:[(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=1
    Entry
0:[(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
    Entry
1:[(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry
0:[(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
    Entry
1:[(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=0
    Entry
0:[(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
    Entry
1:[(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Data

144: 1 1

-----  
Cycle:12

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	1	0	2	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0:[(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1:[(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=1

Entry

0:[(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1:[(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0:[(1,0,4)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Entry

1:[(1,0,3)&lt;10100000010000101111111111111111,10000100010000000000000000000001&gt;]

Set 3: LRU=0

Entry

0:[(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1:[(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Data

144: 1 1

-----  
Cycle:13

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00: 0 1 0 2 0 0 0 0

R08: 0 0 0 0 0 0 0 0

R16: 0 0 0 0 0 0 0 0

R24: 0 0 0 0 0 0 0 0

Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Entry

1: [(1,0,3)&lt;10100000010000101111111111111111,10000100010000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10001000000000000000000000011010,101000000010000111111111111111&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Data

144: 1 1

-----  
Cycle:14

Pre-Issue Buffer:

Entry 0: [ADD R3, R3, R1]

Entry 1: [ADD R3, R3, R2]

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

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Pre\_MEM Queue:  
     Entry 0:  
     Entry 1:  
 Post\_MEM Queue:  
     Entry 0:

Registers  
 R00: 0 1 0 2 0 0 0 0  
 R08: 0 0 0 0 0 0 0 0  
 R16: 0 0 0 0 0 0 0 0  
 R24: 0 0 0 0 0 0 0 0

Cache  
 Set 0: LRU=1  
     Entry  
 0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]  
     Entry  
 1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]  
 Set 1: LRU=1  
     Entry  
 0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]  
     Entry  
 1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]  
 Set 2: LRU=0  
     Entry  
 0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]  
     Entry  
 1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]  
 Set 3: LRU=1  
     Entry  
 0: [(1,0,3)<100010000000000000000000000011010,101000000010000111111111111111>]  
     Entry  
 1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data  
 144: 1 1  
 -----

Cycle:15

Pre-Issue Buffer:  
     Entry 0: [ADD R3, R3, R2]  
     Entry 1: [ADDI R2, R2, #-1]  
     Entry 2:  
     Entry 3:  
 Pre\_ALU Queue:  
     Entry 0: [ADD R3, R3, R1]  
     Entry 1:  
 Post\_ALU Queue:  
     Entry 0:  
 Pre\_MEM Queue:  
     Entry 0:  
     Entry 1:  
 Post\_MEM Queue:  
     Entry 0:

Registers  
 R00: 0 1 0 2 0 0 0 0  
 R08: 0 0 0 0 0 0 0 0  
 R16: 0 0 0 0 0 0 0 0  
 R24: 0 0 0 0 0 0 0 0

Cache  
 Set 0: LRU=1  
     Entry  
 0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]

```

      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=1
      Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
      Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<100010000000000000000000000011010,1010000000100001111111111111111>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Data

144: 1 1

-----  
Cycle:16

Pre-Issue Buffer:

```

      Entry 0: [ADD R3, R3, R2]
      Entry 1: [ADDI R2, R2, #-1]
      Entry 2:
      Entry 3:

```

Pre\_ALU Queue:

```

      Entry 0:
      Entry 1:

```

Post\_ALU Queue:

```

      Entry 0: [ADD R3, R3, R1]

```

Pre\_MEM Queue:

```

      Entry 0:
      Entry 1:

```

Post\_MEM Queue:

```

      Entry 0:

```

Registers

```

R00: 0 1 0 2 0 0 0 0
R08: 0 0 0 0 0 0 0 0
R16: 0 0 0 0 0 0 0 0
R24: 0 0 0 0 0 0 0 0

```

Cache

Set 0: LRU=1

```

      Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=1
      Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
      Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<100010000000000000000000000011010,1010000000100001111111111111111>]
      Entry

```



1:[(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

144: 1 1

-----  
Cycle:17

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0: [ADD R3, R3, R2]

Entry 1: [ADDI R2, R2, #-1]

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00: 0 1 0 3 0 0 0 0

R08: 0 0 0 0 0 0 0 0

R16: 0 0 0 0 0 0 0 0

R24: 0 0 0 0 0 0 0 0

Cache

Set 0: LRU=1

Entry

0:[(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]

Entry

1:[(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=1

Entry

0:[(1,0,3)<100000000011000010001100000100000,100000000011000100001100000100000>]

Entry

1:[(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0:[(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]

Entry

1:[(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]

Set 3: LRU=1

Entry

0:[(1,0,3)<100010000000000000000000000011010,1010000000100001111111111111111>]

Entry

1:[(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

144: 1 1

-----  
Cycle:18

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0: [ADDI R2, R2, #-1]

Entry 1:

Post\_ALU Queue:

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```
Entry 0:          [ADD    R3, R3, R2]
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      1      0      3      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=1
Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
Entry
0: [(1,0,3)<100010000000000000000000000011010,101000000010000111111111111111>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data
144:  1      1
-----
Cycle:19

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:          [ADDI   R2, R2, #-1]
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      1      0      3      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
```

```

0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=1
    Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
    Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<100010000000000000000000000001010,101000000010000111111111111111>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Data

144: 1 1

-----  
Cycle:20

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	1	-1	3	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Entry

1: [(1,0,3)&lt;10100000010000101111111111111111,10000100010000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100010000000000000000000000001010,101000000010000111111111111111&gt;]

Entry  
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

144: 1 1

-----  
Cycle:21

Pre-Issue Buffer:

Entry 0: [ADDI R1, R1, #-1]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00: 0 1 -1 3 0 0 0 0

R08: 0 0 0 0 0 0 0 0

R16: 0 0 0 0 0 0 0 0

R24: 0 0 0 0 0 0 0 0

Cache

Set 0: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=1

Entry

0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]

Entry

1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]

Set 3: LRU=1

Entry

0: [(1,0,3)<100010000000000000000000000011010,101000000010000111111111111111>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

144: 1 1

-----  
Cycle:22

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0: [ADDI R1, R1, #-1]

Entry 1:

```

Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

```

## Registers

```

R00:  0      1      -1      3      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

```

    Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
    Entry
1: [(1,0,4)<1000010000100000000000000000000001,100010000000000000000000000000011001>]

```

Set 1: LRU=1

```

    Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 2: LRU=0

```

    Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
    Entry
1: [(1,0,3)<10100000010000101111111111111111,1000010001000000000000000000000001>]

```

Set 3: LRU=1

```

    Entry
0: [(1,0,3)<1000100000000000000000000000011010,1010000000100001111111111111111>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

## Data

144: 1 1

Cycle:23

## Pre-Issue Buffer:

```

    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:

```

## Pre\_ALU Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_ALU Queue:

Entry 0: [ADDI R1, R1, #-1]

## Pre\_MEM Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_MEM Queue:

Entry 0:

## Registers

```

R00:  0      1      -1      3      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

```

      Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
      Entry
1: [(1,0,4)<100001000010000000000000000000001,10001000000000000000000000000011001>]
Set 1: LRU=1
      Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
      Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<100010000000000000000000000011010,1010000000100001111111111111111>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Data

144: 1 1

-----  
Cycle:24

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	-1	3	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(1,0,4)&lt;10000100001000000000000000000001,10001000000000000000000000000011001&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Entry

1: [(1,0,3)&lt;10100000010000101111111111111111,10000100010000000000000000000001&gt;]

Set 3: LRU=1

Entry

```
Data
144:      1      1
-----
Cycle:25
```

Registers							
R00:	0	0	-1	3	0	0	0
R08:	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0

```
Data
144:      1      1
-----
Cycle:26
```

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Entry 1:  
 Post\_ALU Queue:  
 Entry 0:  
 Pre\_MEM Queue:  
 Entry 0:  
 Entry 1:  
 Post\_MEM Queue:  
 Entry 0:

## Registers

R00:	0	0	-1	3	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(1,0,4)&lt;1000010000100000000000000000000001,1000100000000000000000000000011001&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;100000000011000010001100000100000,100000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Entry

1: [(1,0,3)&lt;10100000010000101111111111111111,10000100010000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100010000000000000000000000011010,1010000000100001111111111111111&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

144: 1 1

-----  
Cycle:27

## Pre-Issue Buffer:

Entry 0:

[ADD R3, R3, R2]

Entry 1:

[ADDI R2, R2, #-1]

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

[ADD R3, R3, R1]

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

[LW R2, 148(R0)]

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	0	-1	3	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache



```

Set 0: LRU=1
      Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
      Entry
1: [(1,0,4)<100001000010000000000000000000000001,1000100000000000000000000000011001>]
Set 1: LRU=1
      Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(1,0,4)<000000000000000000000000000000000001,00000000000000000000000000000001>]
      Entry
1: [(1,0,3)<10100000010000101111111111111111,1000010001000000000000000000000001>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<100010000000000000000000000001010,1010000000100001111111111111111>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Data

144: 1 1

-----  
Cycle:28

Pre-Issue Buffer:

```

      Entry 0: [ADD R3, R3, R2]
      Entry 1: [ADDI R2, R2, #-1]
      Entry 2:
      Entry 3:

```

Pre\_ALU Queue:

```

      Entry 0:
      Entry 1:

```

Post\_ALU Queue:

```

      Entry 0: [ADD R3, R3, R1]

```

Pre\_MEM Queue:

```

      Entry 0:
      Entry 1:

```

Post\_MEM Queue:

```

      Entry 0: [LW R2, 148(R0)]

```

Registers

```

R00: 0 0 -1 3 0 0 0 0
R08: 0 0 0 0 0 0 0 0
R16: 0 0 0 0 0 0 0 0
R24: 0 0 0 0 0 0 0 0

```

Cache

Set 0: LRU=1

```

      Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
      Entry
1: [(1,0,4)<100001000010000000000000000000000001,1000100000000000000000000000011001>]
Set 1: LRU=1
      Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(1,0,4)<000000000000000000000000000000000001,00000000000000000000000000000001>]
      Entry
1: [(1,0,3)<10100000010000101111111111111111,1000010001000000000000000000000001>]
Set 3: LRU=1

```

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```

Data
144:      1      1
-----
Cycle:29

```

Registers							
R00:	0	0	1	3	0	0	0
R08:	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0

```

Data
144:      1      1
-----
Cycle:30

```

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```

    Entry 0:      [ADDI    R2, R2, #-1]
    Entry 1:
Post_ALU Queue:
    Entry 0:      [ADD     R3, R3, R2]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

Registers
R00:  0      0      1      3      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
    Entry
1: [(1,0,4)<1000010000100000000000000000000001,1000100000000000000000000000011001>]
Set 1: LRU=1
    Entry
0: [(1,0,3)<100000000011000010001100000100000,10000000011000100001100000100000>]
    Entry
1: [(0,0,0)<000000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry
0: [(1,0,4)<0000000000000000000000000000000001,00000000000000000000000000000001>]
    Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<1000100000000000000000000000011010,1010000000100001111111111111111>]
    Entry
1: [(0,0,0)<000000000000000000000000000000000,00000000000000000000000000000000>]

Data
144:  1      1
-----
Cycle:31

Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:      [ADDI    R2, R2, #-1]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

Registers
R00:  0      0      1      4      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

```

Cache
Set 0: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
    Entry
1: [(1,0,4)<100001000010000000000000000000001,100010000000000000000000000011001>]
Set 1: LRU=1
    Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
    Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<100010000000000000000000000011010,1010000000100001111111111111111>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data
144:    1        1
-----
Cycle:32

Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

Registers
R00:    0        0        0        4        0        0        0        0
R08:    0        0        0        0        0        0        0        0
R16:    0        0        0        0        0        0        0        0
R24:    0        0        0        0        0        0        0        0

```

```

Cache
Set 0: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
    Entry
1: [(1,0,4)<100001000010000000000000000000001,100010000000000000000000000011001>]
Set 1: LRU=1
    Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
    Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]

```

```
Set 3: LRU=1
      Entry
0: [(1,0,3)<100010000000000000000000000011010,1010000000100001111111111111111>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
```

```
Data
144: 1      1
-----
Cycle:33
```

```
Pre-Issue Buffer:
      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:
Pre_ALU Queue:
      Entry 0:
      Entry 1:
Post_ALU Queue:
      Entry 0:
Pre_MEM Queue:
      Entry 0:
      Entry 1:
Post_MEM Queue:
      Entry 0:
```

```
Registers
R00:  0      0      0      4      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0
```

```
Cache
Set 0: LRU=1
      Entry
0: [(1,0,3)<100011000000000010000000010010000,10001100000000100000000010010100>]
      Entry
1: [(1,0,4)<100001000010000000000000000000001,100010000000000000000000000011001>]
Set 1: LRU=1
      Entry
0: [(1,0,3)<100000000011000010001100000100000,100000000011000100001100000100000>]
      Entry
1: [(0,0,0)<000000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
      Entry
0: [(1,0,4)<000000000000000000000000000000001,00000000000000000000000000000001>]
      Entry
1: [(1,0,3)<10100000010000101111111111111111,100001000100000000000000000000001>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<1000100000000000000000000000011010,1010000000100001111111111111111>]
      Entry
1: [(0,0,0)<000000000000000000000000000000000,00000000000000000000000000000000>]
```

```
Data
144: 1      1
-----
Cycle:34
```

```
Pre-Issue Buffer:
      Entry 0:      [ADD    R3, R3, R1]
      Entry 1:      [ADD    R3, R3, R2]
      Entry 2:
      Entry 3:
```

```

Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

```

## Registers

```

R00:  0      0      0      4      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(1,0,4)&lt;100001000010000000000000000000000001,1000100000000000000000000000000000011001&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;000000000000000000000000000000000001,000000000000000000000000000000000001&gt;]

Entry

1: [(1,0,3)&lt;10100000010000101111111111111111,100001000100000000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100010000000000000000000000011010,1010000000100001111111111111111&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

144: 1 1

-----

Cycle:35

## Pre-Issue Buffer:

Entry 0: [ADD R3, R3, R2]

Entry 1: [ADDI R2, R2, #-1]

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0: [ADD R3, R3, R1]

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

```

R00:  0      0      0      4      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

```

Cache
Set 0: LRU=1
    Entry
0: [(1,0,3)<100011000000000010000000010010000,100011000000000100000000010010100>]
    Entry
1: [(1,0,4)<1000010000100000000000000000000001,1000100000000000000000000000011001>]
Set 1: LRU=1
    Entry
0: [(1,0,3)<100000000011000010001100000100000,100000000011000100001100000100000>]
    Entry
1: [(0,0,0)<000000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry
0: [(1,0,4)<000000000000000000000000000000001,00000000000000000000000000000001>]
    Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<1000100000000000000000000000011010,1010000000100001111111111111111>]
    Entry
1: [(0,0,0)<000000000000000000000000000000000,00000000000000000000000000000000>]

Data
144:      1      1
-----
Cycle:36

Pre-Issue Buffer:
    Entry 0:      [ADD      R3, R3, R2]
    Entry 1:      [ADDI     R2, R2, #-1]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:      [ADD      R3, R3, R1]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

Registers
R00:  0      0      0      4      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

```

Cache
Set 0: LRU=1
    Entry
0: [(1,0,3)<100011000000000010000000010010000,100011000000000100000000010010100>]
    Entry
1: [(1,0,4)<1000010000100000000000000000000001,1000100000000000000000000000011001>]
Set 1: LRU=1
    Entry
0: [(1,0,3)<100000000011000010001100000100000,100000000011000100001100000100000>]
    Entry
1: [(0,0,0)<000000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry
0: [(1,0,4)<000000000000000000000000000000001,00000000000000000000000000000001>]
    Entry

```

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```
1: [(1,0,3)<1010000001000010111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
Entry
0: [(1,0,3)<100010000000000000000000000000011010,1010000000100001111111111111111>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
```

Data

144: 1 1

-----  
Cycle:37

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0: [ADD R3, R3, R2]

Entry 1: [ADDI R2, R2, #-1]

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	0	4	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(1,0,4)&lt;10000100001000000000000000000001,100010000000000000000000000011001&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Entry

1: [(1,0,3)&lt;1010000001000010111111111111111,10000100010000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100010000000000000000000000000011010,1010000000100001111111111111111&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Data

144: 1 1

-----  
Cycle:38

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:



```

Entry 3:
Pre_ALU Queue:
Entry 0:      [ADDI    R2, R2, #-1]
Entry 1:
Post_ALU Queue:
Entry 0:      [ADD     R3, R3, R2]
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      0      0      4      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
Entry
1: [(1,0,4)<1000010000100000000000000000000001,100010000000000000000000000011001>]
Set 1: LRU=1
Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
Entry
0: [(1,0,3)<1000100000000000000000000000011010,101000000010000111111111111111>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data
144:  1      1
-----
Cycle:39

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:      [ADDI    R2, R2, #-1]
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      0      0      4      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0

```

R24: 0 0 0 0 0 0 0 0

Cache

Set 0: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]

Entry

1: [(1,0,4)<100001000010000000000000000000001,100010000000000000000000000011001>]

Set 1: LRU=1

Entry

0: [(1,0,3)<100000000011000010001100000100000,10000000011000100001100000100000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]

Entry

1: [(1,0,3)<1010000001000010111111111111111,10000100010000000000000000000001>]

Set 3: LRU=1

Entry

0: [(1,0,3)<100010000000000000000000000011010,101000000010000111111111111111>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

144: 1 1

-----  
Cycle:40

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00: 0 0 -1 4 0 0 0 0

R08: 0 0 0 0 0 0 0 0

R16: 0 0 0 0 0 0 0 0

R24: 0 0 0 0 0 0 0 0

Cache

Set 0: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]

Entry

1: [(1,0,4)<10000100001000000000000000000001,100010000000000000000000000011001>]

Set 1: LRU=1

Entry

0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]

```

      Entry
1: [(1,0,3)<101000000100001011111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<100010000000000000000000000011010,101000000010000111111111111111>]
      Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Data

144: 1 1

-----  
Cycle:41

Pre-Issue Buffer:

Entry 0: [ADDI R1, R1, #-1]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	-1	4	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(1,0,4)&lt;10000100001000000000000000000001,100010000000000000000000000011001&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;100000000011000010001100000100000,100000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Entry

1: [(1,0,3)&lt;101000000100001011111111111111,10000100010000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100010000000000000000000000011010,101000000010000111111111111111&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Data

144: 1 1

-----  
Cycle:42

Pre-Issue Buffer:

Entry 0:

Entry 1:

```

    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:      [ADDI    R1, R1, #-1]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

Registers
R00:  0      0      -1      4      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=0
    Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
    Entry
1: [(1,0,4)<100001000010000000000000000000001,100010000000000000000000000011001>]
Set 1: LRU=1
    Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
    Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<100010000000000000000000000011010,1010000000100001111111111111111>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data
144:  1      1
-----
Cycle:43

Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:      [ADDI    R1, R1, #-1]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

Registers
R00:  0      0      -1      4      0      0      0      0
R08:  0      0      0      0      0      0      0      0

```

```

R16:    0      0      0      0      0      0      0      0
R24:    0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(1,0,4)&lt;100001000010000000000000000000001,100010000000000000000000000011001&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Entry

1: [(1,0,3)&lt;10100000010000101111111111111111,10000100010000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100010000000000000000000000001010,1010000000100001111111111111111&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

144: 1 1

-----  
Cycle:44

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

```

R00:    0      -1      -1      4      0      0      0      0
R08:    0      0      0      0      0      0      0      0
R16:    0      0      0      0      0      0      0      0
R24:    0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(1,0,4)&lt;100001000010000000000000000000001,100010000000000000000000000011001&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

```

0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
    Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<1000100000000000000000000000011010,101000000010000111111111111111>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,0000000000000000000000000000000>]

```

Data

144: 1 1

-----  
Cycle:45

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

```

R00: 0 -1 -1 4 0 0 0 0
R08: 0 0 0 0 0 0 0 0
R16: 0 0 0 0 0 0 0 0
R24: 0 0 0 0 0 0 0 0

```

Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,100011000000000100000000010010100&gt;]

Entry

1: [(1,0,4)&lt;10000100001000000000000000000001,1000100000000000000000000000011001&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,0000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Entry

1: [(1,0,3)&lt;10100000010000101111111111111111,10000100010000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;1000100000000000000000000000011010,101000000010000111111111111111&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,0000000000000000000000000000000&gt;]

Data

144: 1 1

-----  
Cycle:46

Pre-Issue Buffer:

Entry 0: [SW R3, 144(R0)]

```

Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      -1      -1      4      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=0
Entry
0: [(1,0,3)<10001100000000010000000010010000,10001100000000100000000010010100>]
Entry
1: [(1,0,4)<1000010000100000000000000000000001,100010000000000000000000000011001>]
Set 1: LRU=0
Entry
0: [(1,0,3)<10000000011000010001100000100000,10000000011000100001100000100000>]
Entry
1: [(1,0,4)<10101100000000110000000010010000,100000000000000000000000000001101>]
Set 2: LRU=0
Entry
0: [(1,0,4)<00000000000000000000000000000001,00000000000000000000000000000001>]
Entry
1: [(1,0,3)<10100000010000101111111111111111,10000100010000000000000000000001>]
Set 3: LRU=1
Entry
0: [(1,0,3)<1000100000000000000000000000011010,1010000000100001111111111111111>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,0000000000000000000000000000000>]

Data
144:  1      1
-----
Cycle:47

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [SW      R3, 144(R0)]
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      -1      -1      4      0      0      0      0

```

```

R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(1,0,4)&lt;10000100001000000000000000000001,100010000000000000000000000011001&gt;]

Set 1: LRU=0

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(1,0,4)&lt;10101100000000110000000010010000,100000000000000000000000000001101&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Entry

1: [(1,0,3)&lt;10100000010000101111111111111111,10000100010000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10001000000000000000000000001010,1010000000100001111111111111111&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

144: 1 1

-----  
Cycle:48

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

```

R00:  0      -1      -1      4      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000010010000,10001100000000100000000010010100&gt;]

Entry

1: [(1,0,4)&lt;10000100001000000000000000000001,100010000000000000000000000011001&gt;]

Set 1: LRU=0

Entry

0: [(1,0,3)&lt;10000000011000010001100000100000,10000000011000100001100000100000&gt;]

Entry

1: [(1,0,4)&lt;10101100000000110000000010010000,100000000000000000000000000001101&gt;]

Set 2: LRU=1



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Data		
144:	4	1

sample\_bin.txt

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```
00100000000000010000000000001010
10100000000000010000000000001010
10101100000000010000000100001100
00001010000000000000000000000000
10001100000000010000000100001100
10000100001000000000000000001100
10000000000000010101000010000000
10001101010000110000000010110000
10001101010001000000000011011100
10001100000001010000000100001000
10000100011000000000000000000010
10000000100001010011000000100010
10001000000000000000000000100110
10000000100001010011000000100000
10101101010001100000000010110000
10100000001000011111111111111111
10101100000000010000000100001100
10001000000000000000000000001100
00000000000000000000000000000000
10000000000000000000000000001101
11111111111111111111111111111111
11111111111111111111111111111110
11111111111111111111111111111101
00000000000000000000000000000001
00000000000000000000000000000010
00000000000000000000000000000011
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000101
11111111111111111111111111111011
000000000000000000000000000000110
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000001
00000000000000000000000000000000
```

**sample\_c.txt**

**Page 1 of 1**

```
int A[11] = {-1, -2, -3, 1, 2, 3, 0, 0, 5, -5, 6};
int B[11] = { 0,  0,  0, 0, 0, 0, 0, 0, 0,  0, 0};
int C = 1;

main()
{
    int i;

    for (i=10; i>=0; i--) {
        if (A[i] >= 0)
            A[i] = B[i] - C;
        else
            A[i] = B[i] + C;
    }
}
```

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```
Invalid Instruction
ADDI    R1, R0, #10
SW      R1, 268(R0)
Invalid Instruction
LW      R1, 268(R0)
BLTZ    R1, #48
SLL     R10, R1, #2
LW      R3, 176(R10)
LW      R4, 220(R10)
LW      R5, 264(R0)
BLTZ    R3, #8
SUB     R6, R4, R5
J       #152
ADD     R6, R4, R5
SW      R6, 176(R10)
ADDI    R1, R1, #-1
SW      R1, 268(R0)
J       #112
Invalid Instruction
BREAK
-1
-2
3
1
2
3
0
0
5
-5
6
0
0
0
0
0
0
0
0
0
0
0
0
```

```
; Initially PC is set to 96
; Data section is right after the code section

.text 96
.global _main

_main:
    ADDI    R1, R0, #10    ; init i
    SW      R1, VAR_i(R0)  ; store i
FOR_0:
    LW      R1, VAR_i(R0)
    BLTZ    R1, END_FOR_0  ; i >= 0?
    SLL     R10, R1, #2    ; get correct word boundary
    LW      R3, A(R10)     ; read A[i]
    LW      R4, B(R10)     ; read B[i]
    LW      R5, C(R0)      ; read C
    BLTZ    R3, ELSE_0     ; A[i] >= 0 ?
    SUB     R6, R4, R5     ; B[i] - C
    J       TAIL_0

ELSE_0:
    ADD     R6, R4, R5     ; B[i] + C

TAIL_0:
    SW      R6, A(R10)     ; rewrite A[i]
    ADDI    R1, R1, #-1    ; i--
    SW      R1, VAR_i(R0)
    J       FOR_0

END_FOR_0:
    BREAK

A:
    .word   -1, -2, -3, 1, 2, 3, 0, 0, 5, -5, 6
B:
    .word   0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0
C:
; let C be 1
    .word   1
VAR_i:
; for var i
    .word   0
```

-----  
Cycle:1

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 2: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 3: LRU=0

Entry

0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:2

Pre-Issue Buffer:

Entry 0: [ADDI R1, R0, #10]  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:  
Post\_MEM Queue:  
Entry 0:

## Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;0010000000000001000000000001010,1010000000000001000000000001010&gt;]

Entry

1: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:3

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0: [ADDI R1, R0, #10]

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

```
0: [(1,0,3)<0010000000000001000000000001010,1010000000000001000000000001010>]
  Entry
1: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]
Set 1: LRU=0
  Entry
0: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]
  Entry
1: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]
Set 2: LRU=0
  Entry
0: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]
  Entry
1: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]
Set 3: LRU=0
  Entry
0: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]
  Entry
1: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]
```

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:4

## Pre-Issue Buffer:

```
Entry 0:      [SW      R1, 268(R0)]
Entry 1:
Entry 2:
Entry 3:
```

## Pre\_ALU Queue:

```
Entry 0:
Entry 1:
```

## Post\_ALU Queue:

```
Entry 0:      [ADDI    R1, R0, #10]
```

## Pre\_MEM Queue:

```
Entry 0:
Entry 1:
```

## Post\_MEM Queue:

```
Entry 0:
```

## Registers

R00:	0	0	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;0010000000000001000000000001010,1010000000000001000000000001010&gt;]

Entry

1: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,3)&lt;10101100000000010000000100001100,0000101000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Set 3: LRU=0



```

Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
176:  -1    -2    -3    1    2    3    0    0
208:   5    -5    6    0    0    0    0    0
240:   0     0    0    0    0    0    1    0
-----

```

Cycle:5

```

Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:      [SW      R1, 268(R0)]
  Entry 1:
Post_MEM Queue:
  Entry 0:

```

```

Registers
R00:  0    10    0    0    0    0    0    0
R08:  0     0    0    0    0    0    0    0
R16:  0     0    0    0    0    0    0    0
R24:  0     0    0    0    0    0    0    0

```

```

Cache
Set 0: LRU=1
  Entry
0: [(1,0,3)<0010000000000001000000000001010,1010000000000001000000000001010>]
  Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=1
  Entry
0: [(1,0,3)<10101100000000010000000100001100,00001010000000000000000000000000>]
  Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
  Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
  Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
  Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
  Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
176:  -1    -2    -3    1    2    3    0    0
208:   5    -5    6    0    0    0    0    0
240:   0     0    0    0    0    0    1    0
-----

```

Cycle:6

```

Pre-Issue Buffer:
  Entry 0:      [LW      R1, 268(R0)]

```

```

Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [SW      R1, 268(R0)]
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      10      0      0      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,3)<00100000000000001000000000001010,10100000000000001000000000001010>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=1
Entry
0: [(1,0,3)<101011000000000010000000100001100,00001010000000000000000000000000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=1
Entry
0: [(1,0,3)<100011000000000010000000100001100,10000100001000000000000000001100>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data
176:  -1      -2      -3      1      2      3      0      0
208:   5       -5       6      0      0      0      0      0
240:   0       0       0      0      0      0      1      0
-----
Cycle:7

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R1, 268(R0)]
Entry 1:
Post_MEM Queue:
Entry 0:

```

## Registers

R00:	0	10	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;0010000000000001000000000001010,1010000000000001000000000001010&gt;]

Entry

1: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,3)&lt;10101100000000010000000100001100,0000101000000000000000000000000&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000001010&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,10000100001000000000000000001100&gt;]

Entry

1: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:8

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0: [LW R1, 268(R0)]

## Registers

R00:	0	10	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;0010000000000001000000000001010,1010000000000001000000000001010&gt;]

Entry

1: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

```

0: [(1,0,3)<10101100000000010000000100001100,000010100000000000000000000000>]
    Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000001010>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
    Entry
0: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:9

## Pre-Issue Buffer:

```

    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:

```

## Pre\_ALU Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_ALU Queue:

```

    Entry 0:

```

## Pre\_MEM Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_MEM Queue:

```

    Entry 0:

```

## Registers

R00:	0	10	0	0	0	0	0	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,3)&lt;0010000000000001000000000001010,1010000000000001000000000001010&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,3)&lt;10101100000000010000000100001100,00001010000000000000000000000000&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000001010&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

0: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

```
Data
176:  -1    -2    -3    1    2    3    0    0
208:   5    -5    6    0    0    0    0    0
240:   0     0    0    0    0    0    1    0
```

-----  
Cycle:10

Pre-Issue Buffer:

```
Entry 0:
Entry 1:
Entry 2:
Entry 3:
```

Pre\_ALU Queue:

```
Entry 0:
Entry 1:
```

Post\_ALU Queue:

```
Entry 0:
```

Pre\_MEM Queue:

```
Entry 0:
Entry 1:
```

Post\_MEM Queue:

```
Entry 0:
```

Registers

```
R00:  0    10    0    0    0    0    0    0
R08:  0    0    0    0    0    0    0    0
R16:  0    0    0    0    0    0    0    0
R24:  0    0    0    0    0    0    0    0
```

Cache

Set 0: LRU=1

Entry

0: [(1,0,3)<0010000000000001000000000001010,1010000000000001000000000001010>]

Entry

1: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]

Set 1: LRU=0

Entry

0: [(1,0,3)<10101100000000010000000100001100,0000101000000000000000000000000>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,0000000000000000000000000001010>]

Set 2: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]

Entry

1: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]

Set 3: LRU=0

Entry

0: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]

Entry

1: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]

Data

```
176:  -1    -2    -3    1    2    3    0    0
208:   5    -5    6    0    0    0    0    0
240:   0     0    0    0    0    0    1    0
```

-----  
Cycle:11

Pre-Issue Buffer:

```
Entry 0:  [SLL    R10, R1, #2]
Entry 1:  [LW     R3, 176(R10)]
Entry 2:
Entry 3:
```

Pre\_ALU Queue:

```
Entry 0:
```

```

Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      10      0      0      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,3)<00100000000000010000000000001010,10100000000000010000000000001010>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=0
Entry
0: [(1,0,3)<10101100000000010000000100001100,00001010000000000000000000000000>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000001010>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=1
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data
176:  -1      -2      -3      1      2      3      0      0
208:   5      -5      6      0      0      0      0      0
240:   0      0      0      0      0      0      1      0
-----
Cycle:12

Pre-Issue Buffer:
Entry 0:      [LW      R3, 176(R10)]
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:      [SLL      R10, R1, #2]
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      10      0      0      0      0      0      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

```

Cache
Set 0: LRU=1
    Entry
0: [(1,0,3)<0010000000000001000000000001010,1010000000000001000000000001010>]
    Entry
1: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]
Set 1: LRU=0
    Entry
0: [(1,0,3)<10101100000000010000000100001100,0000101000000000000000000000000>]
    Entry
1: [(1,1,8)<00000000000000000000000000000001,0000000000000000000000000001010>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
    Entry
1: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(0,0,0)<0000000000000000000000000000000,0000000000000000000000000000000>]

Data
176:  -1    -2    -3     1     2     3     0     0
208:   5    -5     6     0     0     0     0     0
240:   0     0     0     0     0     0     1     0
-----
Cycle:13

Pre-Issue Buffer:
    Entry 0:      [LW      R3, 176(R10)]
    Entry 1:      [LW      R4, 220(R10)]
    Entry 2:      [LW      R5, 264(R0)]
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:      [SLL      R10, R1, #2]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

Registers
R00:  0     10     0     0     0     0     0     0
R08:  0     0     0     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=0
    Entry
0: [(1,0,3)<0010000000000001000000000001010,1010000000000001000000000001010>]
    Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
    Entry
0: [(1,0,3)<10101100000000010000000100001100,0000101000000000000000000000000>]
    Entry
1: [(1,1,8)<00000000000000000000000000000001,0000000000000000000000000001010>]
Set 2: LRU=1
    Entry

```

```

0: [(1,0,3)<100011000000000010000000100001100,10000100001000000000000000000001100>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:   5    -5     6     0     0     0     0     0
240:   0     0     0     0     0     0     1     0
-----

```

Cycle:14

```

Pre-Issue Buffer:
    Entry 0:      [LW      R5, 264(R0)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:      [LW      R3, 176(R10)]
    Entry 1:      [LW      R4, 220(R10)]
Post_MEM Queue:
    Entry 0:

```

```

Registers
R00:   0     10     0     0     0     0     0     0
R08:   0     0    40     0     0     0     0     0
R16:   0     0     0     0     0     0     0     0
R24:   0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=0
    Entry
0: [(1,0,3)<00100000000000001000000000001010,10100000000000001000000000001010>]
    Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
    Entry
0: [(1,0,3)<10101100000000010000000100001100,00001010000000000000000000000000>]
    Entry
1: [(1,1,8)<000000000000000000000000000000001,00000000000000000000000000001010>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:   5    -5     6     0     0     0     0     0
240:   0     0     0     0     0     0     1     0
-----

```



Cycle:15

Pre-Issue Buffer:

Entry 0: [LW R5, 264(R0)]  
 Entry 1:  
 Entry 2:  
 Entry 3:

Pre\_ALU Queue:

Entry 0:  
 Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R3, 176(R10)]  
 Entry 1: [LW R4, 220(R10)]

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	10	0	0	0	0	0	0
R08:	0	0	40	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;0010000000000001000000000001010,1010000000000001000000000001010&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;1000010001100000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,000000000000000000000000000001010&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

Cycle:16

Pre-Issue Buffer:

Entry 0:  
 Entry 1:  
 Entry 2:  
 Entry 3:

Pre\_ALU Queue:

Entry 0:  
 Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R4, 220(R10)]

```

Entry 1:      [LW      R5, 264(R0)]
Post_MEM Queue:
Entry 0:      [LW      R3, 176(R10)]

```

## Registers

```

R00:  0      10      0      0      0      0      0      0
R08:  0      0      40     0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;0010000000000001000000000001010,1010000000000001000000000001010&gt;]

Entry

1: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;1000010001100000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;0000000000000000000000000000001,0000000000000000000000000001010&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,10000100001000000000000000001100&gt;]

Entry

1: [(0,0,0)&lt;0000000000000000000000000000000,0000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,6)&lt;00000000000000000000000000000110,0000000000000000000000000000000&gt;]

## Data

```

176:  -1      -2      -3      1      2      3      0      0
208:   5      -5      6      0      0      0      0      0
240:   0      0      0      0      0      0      1      0
-----

```

Cycle:17

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue: Entry 0: [LW R4, 220(R10)]

Entry 1: [LW R5, 264(R0)]

## Post\_MEM Queue:

Entry 0:

## Registers

```

R00:  0      10      0      6      0      0      0      0
R08:  0      0      40     0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

Entry

0: [(1,0,3)&lt;0010000000000001000000000001010,1010000000000001000000000001010&gt;]

```

Entry
1: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000001010>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,1000010000100000000000000000001100>]
Entry
1: [(0,0,0)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,6)<00000000000000000000000000000110,00000000000000000000000000000000>]

```

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:18

## Pre-Issue Buffer:

```

Entry 0:      [SUB    R6, R4, R5]
Entry 1:
Entry 2:
Entry 3:

```

## Pre\_ALU Queue:

```

Entry 0:
Entry 1:

```

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R5, 264(R0)]

Entry 1:

## Post\_MEM Queue:

Entry 0: [LW R4, 220(R10)]

## Registers

R00:	0	10	0	6	0	0	0	0
R08:	0	0	40	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,8)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000001010&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,1000010000100000000000000000001100&gt;]

Entry

1: [(0,0,0)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=0

Entry

```

0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,0,6)<00000000000000000000000000000110,00000000000000000000000000000000>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:   5    -5     6     0     0     0     0     0
240:   0     0     0     0     0     0     1     0
-----

```

Cycle:19

```

Pre-Issue Buffer:
    Entry 0:      [SUB    R6, R4, R5]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:      [LW     R5, 264(R0)]

```

```

Registers
R00:  0     10     0     6     0     0     0     0
R08:  0     0     40     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

Cache

```

Set 0: LRU=1
    Entry
0: [(1,0,8)<00000000000000000000000000000000,00000000000000000000000000000000>]
    Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
    Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,1,8)<000000000000000000000000000000001,000000000000000000000000000001010>]
Set 2: LRU=0
    Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
    Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,0,6)<00000000000000000000000000000110,00000000000000000000000000000000>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:   5    -5     6     0     0     0     0     0
240:   0     0     0     0     0     0     1     0
-----

```

Cycle:20

```

Pre-Issue Buffer:
    Entry 0:
    Entry 1:

```

```

Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:      [SUB    R6, R4, R5]
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      10      0      6      0      1      0      0
R08:  0      0      40      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,8)<00000000000000000000000000000000,00000000000000000000000000000000>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<000000000000000000000000000000001,00000000000000000000000000001010>]
Set 2: LRU=0
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
Entry
0: [(1,0,3)<10000000000000001010100001000000,10001101010000110000000010110000>]
Entry
1: [(1,0,6)<00000000000000000000000000000110,0000000000000000000000000000000>]

Data
176:  -1      -2      -3      1      2      3      0      0
208:   5      -5      6      0      0      0      0      0
240:   0      0      0      0      0      0      1      0
-----
Cycle:21

Pre-Issue Buffer:
Entry 0:      [SW      R6, 176(R10)]
Entry 1:      [ADDI    R1, R1, #-1]
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:      [SUB      R6, R4, R5]
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers

```

```

R00:  0      10      0      6      0      1      0      0
R08:  0      0      40      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=1

Entry

0: [(1,0,8)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000001010&gt;]

Set 2: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,10000100001000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,4)&lt;101011010100011000000000010110000,1010000000100001111111111111111&gt;]

Entry

1: [(1,0,6)&lt;000000000000000000000000000000110,00000000000000000000000000000000&gt;]

## Data

```

176:  -1      -2      -3      1      2      3      0      0
208:   5       -5       6       0       0       0       0       0
240:   0        0        0       0       0       0       1       0
-----

```

Cycle:22

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0: [ADDI R1, R1, #-1]

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [SW R6, 176(R10)]

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

```

R00:  0      10      0      6      0      1      -1      0
R08:  0      0      40      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=1

Entry

0: [(1,0,8)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Data							
176:	-1	-2	-3	1	2	3	0
208:	5	-5	6	0	0	0	0
240:	0	0	0	0	0	0	1

```

Pre-Issue Buffer:
    Entry 0:      [SW      R1, 268(R0)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:      [ADDI    R1, R1, #-1]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

```

[illegible]

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:24

Pre-Issue Buffer:

Entry 0: [LW R1, 268(R0)]  
 Entry 1:  
 Entry 2:  
 Entry 3:

Pre\_ALU Queue:

Entry 0:  
 Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [SW R1, 268(R0)]  
 Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	9	0	6	0	1	-1	0
R08:	0	0	40	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,8)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,100010000000000000000000000011100&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,000000000000000000000000000001010&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=0

Entry

0: [(1,0,4)&lt;10101101010001100000000010110000,1010000000100001111111111111111&gt;]

Entry

1: [(1,1,6)&lt;11111111111111111111111111111111,00000000000000000000000000000000&gt;]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:25

Pre-Issue Buffer:

Entry 0:  
 Entry 1:  
 Entry 2:  
 Entry 3:

Pre\_ALU Queue:

Entry 0:  
 Entry 1:



Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R1, 268(R0)]

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	9	0	6	0	1	-1	0
R08:	0	0	40	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,8)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,100010000000000000000000000011100&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000001001&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,10000100001000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=0

Entry

0: [(1,0,4)&lt;10101101010001100000000010110000,1010000000100001111111111111111&gt;]

Entry

1: [(1,1,6)&lt;11111111111111111111111111111111,00000000000000000000000000000000&gt;]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

Cycle:26

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0: [LW R1, 268(R0)]

Registers

R00:	0	9	0	6	0	1	-1	0
R08:	0	0	40	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

```

Cache
Set 0: LRU=0
  Entry
0: [(1,0,8)<00000000000000000000000000000000,00000000000000000000000000000000>]
  Entry
1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]
Set 1: LRU=0
  Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
  Entry
1: [(1,1,8)<000000000000000000000000000000001,00000000000000000000000000001001>]
Set 2: LRU=1
  Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
  Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
  Entry
0: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]
  Entry
1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

Data
176:   -1    -2    -3     1     2     3     0     0
208:     5    -5     6     0     0     0     0     0
240:     0     0     0     0     0     0     1     0
-----
Cycle:27

Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:

Registers
R00:   0     9     0     6     0     1    -1     0
R08:   0     0    40     0     0     0     0     0
R16:   0     0     0     0     0     0     0     0
R24:   0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=0
  Entry
0: [(1,0,8)<00000000000000000000000000000000,00000000000000000000000000000000>]
  Entry
1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]
Set 1: LRU=0
  Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
  Entry
1: [(1,1,8)<000000000000000000000000000000001,00000000000000000000000000001001>]
Set 2: LRU=1
  Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

```

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Data									
176:	-1	-2	-3	1	2	3	0	0	
208:	5	-5	6	0	0	0	0	0	
240:	0	0	0	0	0	0	1	0	

Entry 0:

R00:	0	9	0	6	0	1	-1	0
R08:	0	0	40	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

[illegible]

Data								
176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

Cycle:29

Pre-Issue Buffer:

Entry 0: [SLL R10, R1, #2]  
 Entry 1: [LW R3, 176(R10)]  
 Entry 2:  
 Entry 3:

Pre\_ALU Queue:

Entry 0:  
 Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
 Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	9	0	6	0	1	-1	0
R08:	0	0	40	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,8)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,100010000000000000000000000011100&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000001001&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,10000100001000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,1,6)&lt;11111111111111111111111111111111,00000000000000000000000000000000&gt;]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:30

Pre-Issue Buffer:

Entry 0: [LW R3, 176(R10)]  
 Entry 1:  
 Entry 2:  
 Entry 3:

Pre\_ALU Queue:

Entry 0: [SLL R10, R1, #2]  
 Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
 Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	9	0	6	0	1	-1	0
R08:	0	0	40	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,8)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,100010000000000000000000000011100&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000001001&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,10000100001000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,1,6)&lt;11111111111111111111111111111111,00000000000000000000000000000000&gt;]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:31

Pre-Issue Buffer:

Entry 0: [LW R3, 176(R10)]

Entry 1: [LW R4, 220(R10)]

Entry 2: [LW R5, 264(R0)]

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0: [SLL R10, R1, #2]

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	9	0	6	0	1	-1	0
R08:	0	0	40	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

```

1:[(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Set 1: LRU=0
    Entry
0:[(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1:[(1,1,8)<00000000000000000000000000000001,000000000000000000000000000001001>]
Set 2: LRU=1
    Entry
0:[(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1:[(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
    Entry
0:[(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1:[(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

```

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:32

## Pre-Issue Buffer:

```

    Entry 0:      [LW      R5, 264(R0)]
    Entry 1:
    Entry 2:
    Entry 3:

```

## Pre\_ALU Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_ALU Queue:

```

    Entry 0:

```

## Pre\_MEM Queue:

```

    Entry 0:      [LW      R3, 176(R10)]
    Entry 1:      [LW      R4, 220(R10)]

```

## Post\_MEM Queue:

```

    Entry 0:

```

## Registers

R00:	0	9	0	6	0	1	-1	0
R08:	0	0	36	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

```

    Entry

```

```

0:[(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

```

```

    Entry

```

```

1:[(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

```

Set 1: LRU=1

```

    Entry

```

```

0:[(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

```

```

    Entry

```

```

1:[(1,1,8)<00000000000000000000000000000001,000000000000000000000000000001001>]

```

Set 2: LRU=1

```

    Entry

```

```

0:[(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

```

```

    Entry

```

```

1:[(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]

```

Set 3: LRU=1

```

    Entry

```

```

0:[(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]

```

Entry  
1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

Data  
176:    -1       -2       -3       1       2       3       0       0  
208:    5       -5       6       0       0       0       0       0  
240:    0       0       0       0       0       0       1       0

-----  
Cycle:33

Pre-Issue Buffer:  
  Entry 0:            [LW       R5, 264(R0)]  
  Entry 1:  
  Entry 2:  
  Entry 3:  
Pre\_ALU Queue:  
  Entry 0:  
  Entry 1:  
Post\_ALU Queue:  
  Entry 0:  
Pre\_MEM Queue:  
  Entry 0:            [LW       R3, 176(R10)]  
  Entry 1:            [LW       R4, 220(R10)]  
Post\_MEM Queue:  
  Entry 0:

Registers  
R00:    0       9       0       6       0       1       -1       0  
R08:    0       0       36      0       0       0       0       0  
R16:    0       0       0       0       0       0       0       0  
R24:    0       0       0       0       0       0       0       0

Cache  
Set 0: LRU=1  
  Entry  
0: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]  
  Entry  
1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]  
Set 1: LRU=1  
  Entry  
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]  
  Entry  
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000001001>]  
Set 2: LRU=1  
  Entry  
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]  
  Entry  
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]  
Set 3: LRU=1  
  Entry  
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]  
  Entry  
1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

Data  
176:    -1       -2       -3       1       2       3       0       0  
208:    5       -5       6       0       0       0       0       0  
240:    0       0       0       0       0       0       1       0

-----  
Cycle:34

Pre-Issue Buffer:  
  Entry 0:  
  Entry 1:  
  Entry 2:

```

Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R4, 220(R10)]
Entry 1:      [LW      R5, 264(R0)]
Post_MEM Queue:
Entry 0:      [LW      R3, 176(R10)]

Registers
R00:   0      9      0      6      0      1      -1      0
R08:   0      0     36      0      0      0      0      0
R16:   0      0      0      0      0      0      0      0
R24:   0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
Entry
1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]
Set 1: LRU=1
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000001001>]
Set 2: LRU=0
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,0,6)<00000000000000000000000000000101,11111111111111111111111111111011>]
Set 3: LRU=1
Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

Data
176:  -1      -2      -3      1      2      3      0      0
208:   5      -5      6      0      0      0      0      0
240:   0      0      0      0      0      0      1      0
-----
Cycle:35

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R4, 220(R10)]
Entry 1:      [LW      R5, 264(R0)]
Post_MEM Queue:
Entry 0:

Registers
R00:   0      9      0     -5      0      1     -1      0

```



```
R08:  0      0      36      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0
```

## Cache

Set 0: LRU=1

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,000000000000000000000000000001001&gt;]

Set 2: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,6)&lt;0000000000000000000000000000000101,111111111111111111111111111111011&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,1,6)&lt;11111111111111111111111111111111,00000000000000000000000000000000&gt;]

## Data

```
176:  -1      -2      -3      1      2      3      0      0
208:   5      -5      6      0      0      0      0      0
240:   0      0      0      0      0      0      1      0
```

-----  
Cycle:36

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R5, 264(R0)]

Entry 1:

## Post\_MEM Queue:

Entry 0: [LW R4, 220(R10)]

## Registers

```
R00:  0      9      0      -5      0      1      -1      0
R08:  0      0      36      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0
```

## Cache

Set 0: LRU=0

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,8)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

```

1: [(1,1,8)<00000000000000000000000000000001,000000000000000000000000000000001001>]
Set 2: LRU=0
    Entry
0: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000000001100>]
    Entry
1: [(1,0,6)<00000000000000000000000000000000101,1111111111111111111111111111111011>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

```

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	6	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:37

## Pre-Issue Buffer:

```

    Entry 0:      [ADD    R6, R4, R5]
    Entry 1:
    Entry 2:
    Entry 3:

```

## Pre\_ALU Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_ALU Queue:

```

    Entry 0:

```

## Pre\_MEM Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_MEM Queue:

```

    Entry 0:      [LW     R5, 264(R0)]

```

## Registers

R00:	0	9	0	-5	0	1	-1	0
R08:	0	0	36	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,8)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Set 2: LRU=1

Entry

0: [(1,0,4)&lt;100010000000000000000000000000100110,10000000100001010011000000100000&gt;]

Entry

1: [(1,0,6)&lt;000000000000000000000000000000101,111111111111111111111111111111011&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,1,6)&lt;11111111111111111111111111111111,00000000000000000000000000000000&gt;]

## Data

176:	-1	-2	-3	1	2	3	0	0
------	----	----	----	---	---	---	---	---

```

208:    5      -5      6      0      0      0      0      0
240:    0      0      0      0      0      0      0      1      0
-----

```

Cycle:38

Pre-Issue Buffer:

```

Entry 0:      [SW      R6, 176(R10)]
Entry 1:      [ADDI    R1, R1, #-1]
Entry 2:
Entry 3:

```

Pre\_ALU Queue:

```

Entry 0:      [ADD     R6, R4, R5]
Entry 1:

```

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

```

R00:    0      9      0      -5      0      1      -1      0
R08:    0      0      36     0      0      0      0      0
R16:    0      0      0      0      0      0      0      0
R24:    0      0      0      0      0      0      0      0

```

Cache

Set 0: LRU=0

Entry

0: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,8)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000001001&gt;]

Set 2: LRU=1

Entry

0: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Entry

1: [(1,0,6)&lt;00000000000000000000000000000101,11111111111111111111111111111011&gt;]

Set 3: LRU=0

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

Data

```

176:   -1      -2      -3      1      2      3      0      0
208:    5      -5      -1      0      0      0      0      0
240:    0      0      0      0      0      0      1      0
-----

```

Cycle:39

Pre-Issue Buffer:

```

Entry 0:      [SW      R6, 176(R10)]
Entry 1:
Entry 2:
Entry 3:

```

Pre\_ALU Queue:

```

Entry 0:      [ADDI    R1, R1, #-1]
Entry 1:

```

Post\_ALU Queue:

Entry 0: [ADD R6, R4, R5]

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	9	0	-5	0	1	-1	0
R08:	0	0	36	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]

Entry

1: [(1,0,8)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000001001>]

Set 2: LRU=1

Entry

0: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]

Entry

1: [(1,0,6)<0000000000000000000000000000101,111111111111111111111111111111011>]

Set 3: LRU=0

Entry

0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]

Entry

1: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:40

Pre-Issue Buffer:

Entry 0: [SW R1, 268(R0)]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0: [ADDI R1, R1, #-1]

Pre\_MEM Queue:

Entry 0: [SW R6, 176(R10)]

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	9	0	-5	0	1	1	0
R08:	0	0	36	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

```

Set 0: LRU=1
      Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
      Entry
1: [(1,0,8)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=0
      Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000001001>]
Set 2: LRU=1
      Entry
0: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]
      Entry
1: [(1,0,6)<00000000000000000000000000000101,11111111111111111111111111111011>]
Set 3: LRU=0
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1      -2      -3      1      2      3      0      0
208:   5      -5      -1      0      0      0      0      0
240:   0       0       0      0      0      0      1      0
-----

```

Cycle:41

Pre-Issue Buffer:

```

      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:

```

Pre\_ALU Queue:

```

      Entry 0:
      Entry 1:

```

Post\_ALU Queue:

```

      Entry 0:

```

Pre\_MEM Queue:

```

      Entry 0:      [SW      R1, 268(R0)]
      Entry 1:

```

Post\_MEM Queue:

```

      Entry 0:

```

Registers

```

R00:  0      8      0      -5      0      1      1      0
R08:  0      0     36      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

Cache

Set 0: LRU=1

Entry

```

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

```

Entry

```

1: [(1,0,8)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 1: LRU=0

Entry

```

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

```

Entry

```

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000001001>]

```

Set 2: LRU=0

Entry

```

0: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]

```

Entry

Data								
176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

```

Pre-Issue Buffer:
    Entry 0:          [LW      R1, 268(R0)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

```

```
Cache
Set 0: LRU=1
      Entry
0: [(1,0,5)<101011000000000010000000100001100,100010000000000000000000000000000011100>]
      Entry
1: [(1,0,8)<0000000000000000000000000000000000,0000000000000000000000000000000000>]
Set 1: LRU=0
      Entry
0: [(1,0,4)<100001000110000000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000000001,000000000000000000000000000001000>]
Set 2: LRU=1
      Entry
0: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000000001100>]
      Entry
1: [(1,1,6)<00000000000000000000000000000000101,0000000000000000000000000000000001>]
Set 3: LRU=0
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<101011010100011000000000010110000,1010000000100001111111111111111>]
```

Data								
176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R1, 268(R0)]  
Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	8	0	-5	0	1	1	0
R08:	0	0	36	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,8)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,000000000000000000000000000001000&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,1,6)&lt;00000000000000000000000000000101,00000000000000000000000000000001&gt;]

Set 3: LRU=0

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,1010000000100001111111111111111&gt;]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:44

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

```

Entry 0:          [LW      R1, 268(R0)]

Registers
R00:   0      8      0      -5      0      1      1      0
R08:   0      0     36      0      0      0      0      0
R16:   0      0      0      0      0      0      0      0
R24:   0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]
Entry
1: [(1,0,8)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000001000>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
Entry
1: [(1,1,6)<00000000000000000000000000000101,00000000000000000000000000000001>]
Set 3: LRU=0
Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Data
176:  -1      -2      -3      1      2      3      0      0
208:   5      -5      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      0
-----
Cycle:45

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:   0      8      0      -5      0      1      1      0
R08:   0      0     36      0      0      0      0      0
R16:   0      0      0      0      0      0      0      0
R24:   0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]
Entry
1: [(1,0,8)<00000000000000000000000000000000,00000000000000000000000000000000>]

```



```

Set 1: LRU=0
      Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000001000>]
Set 2: LRU=1
      Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
      Entry
1: [(1,1,6)<0000000000000000000000000000000101,00000000000000000000000000000001>]
Set 3: LRU=0
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:   5    -5    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     0
-----

```

Cycle:46

```

Pre-Issue Buffer:
      Entry 0:      [SLL    R10, R1, #2]
      Entry 1:      [LW     R3, 176(R10)]
      Entry 2:
      Entry 3:
Pre_ALU Queue:
      Entry 0:
      Entry 1:
Post_ALU Queue:
      Entry 0:
Pre_MEM Queue:
      Entry 0:
      Entry 1:
Post_MEM Queue:
      Entry 0:

```

```

Registers
R00:  0     8     0    -5     0     1     1     0
R08:  0     0    36     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=1
      Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
      Entry
1: [(1,0,8)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=0
      Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000001000>]
Set 2: LRU=1
      Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
      Entry
1: [(1,1,6)<0000000000000000000000000000000101,00000000000000000000000000000001>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry

```

1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Data								
176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:47

Pre-Issue Buffer:  
 Entry 0: [LW R3, 176(R10)]  
 Entry 1:  
 Entry 2:  
 Entry 3:

Pre\_ALU Queue:  
 Entry 0: [SLL R10, R1, #2]  
 Entry 1:

Post\_ALU Queue:  
 Entry 0:

Pre\_MEM Queue:  
 Entry 0:  
 Entry 1:

Post\_MEM Queue:  
 Entry 0:

Registers								
R00:	0	8	0	-5	0	1	1	0
R08:	0	0	36	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry  
 0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]  
 Entry  
 1: [(1,0,8)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=0

Entry  
 0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]  
 Entry  
 1: [(1,1,8)<00000000000000000000000000000001,000000000000000000000000000001000>]

Set 2: LRU=1

Entry  
 0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]  
 Entry  
 1: [(1,1,6)<0000000000000000000000000000000101,00000000000000000000000000000001>]

Set 3: LRU=1

Entry  
 0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]  
 Entry  
 1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Data								
176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:48

Pre-Issue Buffer:  
 Entry 0: [LW R3, 176(R10)]  
 Entry 1: [LW R4, 220(R10)]  
 Entry 2: [LW R5, 264(R0)]  
 Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0: [SLL R10, R1, #2]

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	8	0	-5	0	1	1	0
R08:	0	0	36	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;1010110000000001000000100001100,100010000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000001000&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,1,6)&lt;000000000000000000000000000000101,00000000000000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;101011010100011000000000010110000,1010000000100001111111111111111&gt;]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:49

Pre-Issue Buffer:

Entry 0: [LW R5, 264(R0)]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R3, 176(R10)]

Entry 1: [LW R4, 220(R10)]

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	8	0	-5	0	1	1	0
R08:	0	0	32	0	0	0	0	0

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Cache

Entry

Entry

LRU=1

$$, 4) < 10$$
$$, 8) < 00$$

Entry

Entry

LRU=1

$$, 3) < 10$$
$$.4) < 10$$

5

-----

9

Entry

Entry

## Entity Queue

Entry

Enter

Queue  
Front

## ENERGY

Entry

rs  
o0  
2

0

Entry

Entry

LRU=1

$$, 4) < 10$$
$$, 8) < 00$$

\_\_\_\_\_

```

Set 2: LRU=0
      Entry
0: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000000001100>]
      Entry
1: [(1,1,6)<0000000000000000000000000000000000101,000000000000000000000000000000001>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<101011010100011000000000010110000,10100000001000011111111111111111>]

```

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:51

## Pre-Issue Buffer:

```

      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:

```

## Pre\_ALU Queue:

```

      Entry 0:
      Entry 1:

```

## Post\_ALU Queue:

```

      Entry 0:

```

## Pre\_MEM Queue:

```

      Entry 0:      [LW      R4, 220(R10)]
      Entry 1:      [LW      R5, 264(R0)]

```

## Post\_MEM Queue:

```

      Entry 0:

```

## Registers

R00:	0	8	0	5	0	1	1	0
R08:	0	0	32	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

```

      Entry
0: [(1,0,5)<101011000000000010000000100001100,1000100000000000000000000000000011100>]
      Entry
1: [(1,0,4)<1000110101000100000000000011011100,100011000000001010000000100001000>]

```

Set 1: LRU=1

```

      Entry
0: [(1,0,4)<1000010001100000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000000001,000000000000000000000000000000001000>]

```

Set 2: LRU=0

```

      Entry
0: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000000001100>]
      Entry
1: [(1,1,6)<0000000000000000000000000000000000101,000000000000000000000000000000001>]

```

Set 3: LRU=1

```

      Entry
0: [(1,0,3)<10000000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<101011010100011000000000010110000,10100000001000011111111111111111>]

```

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0

240: 0 0 0 0 0 0 1 0

-----  
Cycle:52

Pre-Issue Buffer:

Entry 0: [SUB R6, R4, R5]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R5, 264(R0)]

Entry 1:

Post\_MEM Queue:

Entry 0: [LW R4, 220(R10)]

Registers

R00:	0	8	0	5	0	1	1	0
R08:	0	0	32	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

Entry

1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

Set 1: LRU=1

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,000000000000000000000000000001000>]

Set 2: LRU=0

Entry

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

Entry

1: [(1,1,6)<00000000000000000000000000000101,00000000000000000000000000000001>]

Set 3: LRU=0

Entry

0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]

Entry

1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:53

Pre-Issue Buffer:

Entry 0: [SUB R6, R4, R5]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0: [LW R5, 264(R0)]

Registers

R00:	0	8	0	5	0	1	1	0
R08:	0	0	32	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,000000000000000000000000000001000&gt;]

Set 2: LRU=1

Entry

0: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Entry

1: [(1,1,6)&lt;000000000000000000000000000000101,00000000000000000000000000000001&gt;]

Set 3: LRU=0

Entry

0: [(1,0,3)&lt;1000000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:54

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0: [SUB R6, R4, R5]

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	8	0	5	0	1	1	0
R08:	0	0	32	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

```

Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
Entry
0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<000000000000000000000000000000001,000000000000000000000000000001000>]
Set 2: LRU=1
Entry
0: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]
Entry
1: [(1,1,6)<00000000000000000000000000000000101,00000000000000000000000000000001>]
Set 3: LRU=0
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:55

## Pre-Issue Buffer:

```

Entry 0: [SW R6, 176(R10)]
Entry 1: [ADDI R1, R1, #-1]
Entry 2:
Entry 3:

```

## Pre\_ALU Queue:

```

Entry 0:
Entry 1:

```

## Post\_ALU Queue:

```

Entry 0: [SUB R6, R4, R5]

```

## Pre\_MEM Queue:

```

Entry 0:
Entry 1:

```

## Post\_MEM Queue:

```

Entry 0:

```

## Registers

R00:	0	8	0	5	0	1	1	0
R08:	0	0	32	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

```

Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
Entry
0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<000000000000000000000000000000001,000000000000000000000000000001000>]
Set 2: LRU=1
Entry
0: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]
Entry
1: [(1,1,6)<00000000000000000000000000000000101,00000000000000000000000000000001>]

```



```

Set 3: LRU=1
      Entry
0: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
      Entry
1: [(1,0,7)<00000000000000000000000000000000,000000000000000000000000000000>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:   5    -5    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     0
-----

```

Cycle:56

```

Pre-Issue Buffer:
      Entry 0:      [SW      R1, 268(R0)]
      Entry 1:
      Entry 2:
      Entry 3:
Pre_ALU Queue:
      Entry 0:      [ADDI    R1, R1, #-1]
      Entry 1:
Post_ALU Queue:
      Entry 0:
Pre_MEM Queue:
      Entry 0:      [SW      R6, 176(R10)]
      Entry 1:
Post_MEM Queue:
      Entry 0:

```

```

Registers
R00:  0     8     0     5     0     1    -1     0
R08:  0     0    32     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=1
      Entry
0: [(1,0,5)<101011000000000010000000100001100,100010000000000000000000000011100>]
      Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
      Entry
0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<000000000000000000000000000000001,00000000000000000000000000001000>]
Set 2: LRU=1
      Entry
0: [(1,0,4)<100010000000000000000000000000010,10000000100001010011000000100000>]
      Entry
1: [(1,1,6)<00000000000000000000000000000000101,00000000000000000000000000000001>]
Set 3: LRU=1
      Entry
0: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
      Entry
1: [(1,0,7)<00000000000000000000000000000000,000000000000000000000000000000>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:   5    -5    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     0
-----

```

Cycle:57

Pre-Issue Buffer:

```

Entry 0:      [SW      R1, 268(R0)]
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:      [ADDI    R1, R1, #-1]
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

```

## Registers

R00:	0	8	0	5	0	1	-1	0
R08:	0	0	32	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,000000000000000000000000000001000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;100010000000000000000000000100110,10000000100001010011000000100000&gt;]

Entry

1: [(1,1,6)&lt;11111111111111111111111111111111,00000000000000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,4)&lt;10101101010001100000000010110000,1010000000100001111111111111111&gt;]

Entry

1: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:58

## Pre-Issue Buffer:

Entry 0: [LW R1, 268(R0)]

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [SW R1, 268(R0)]

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	7	0	5	0	1	-1	0
R08:	0	0	32	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,000000000000000000000000000001000&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,1,6)&lt;11111111111111111111111111111111,00000000000000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,4)&lt;10101101010001100000000010110000,1010000000100001111111111111111&gt;]

Entry

1: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:59

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R1, 268(R0)]

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	7	0	5	0	1	-1	0
R08:	0	0	32	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

```

Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000111>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000001>]
Set 3: LRU=1
Entry
0: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]
Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:60

## Pre-Issue Buffer:

```

Entry 0:
Entry 1:
Entry 2:
Entry 3:

```

## Pre\_ALU Queue:

```

Entry 0:
Entry 1:

```

## Post\_ALU Queue:

```

Entry 0:

```

## Pre\_MEM Queue:

```

Entry 0:
Entry 1:

```

## Post\_MEM Queue:

```

Entry 0:          [LW      R1, 268(R0)]

```

## Registers

R00:	0	7	0	5	0	1	-1	0
R08:	0	0	32	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

```

Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000111>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000001>]
Set 3: LRU=1
Entry
0: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]
Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```
Data
176:  -1    -2    -3    1    2    3    0    0
208:   5    -5    -1    0    0    0    0    0
240:   0     0     0    0    0    0    1    0
```

-----  
Cycle:61

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

```
R00:  0     7     0     5     0     1    -1     0
R08:  0     0    32     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0
```

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]

Entry

1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000111>]

Set 2: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

Entry

1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000001>]

Set 3: LRU=1

Entry

0: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Entry

1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data

```
176:  -1    -2    -3    1    2    3    0    0
208:   5    -5    -1    0    0    0    0    0
240:   0     0     0    0    0    0    1    0
```

-----  
Cycle:62

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

```

Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      7      0      5      0      1      -1      0
R08:  0      0     32      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
Entry
0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<0000000000000000000000000000000001,00000000000000000000000000000111>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000001>]
Set 3: LRU=1
Entry
0: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

Data
176:  -1     -2     -3      1      2      3      0      0
208:   5      -5     -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      0
-----
Cycle:63

Pre-Issue Buffer:
Entry 0:      [SLL    R10, R1, #2]
Entry 1:      [LW     R3, 176(R10)]
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      7      0      5      0      1      -1      0
R08:  0      0     32      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0

```

R24: 0 0 0 0 0 0 0 0

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

Entry

1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000111>]

Set 2: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

Entry

1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000001>]

Set 3: LRU=0

Entry

0: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Entry

1: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:64

Pre-Issue Buffer:

Entry 0: [LW R3, 176(R10)]

Entry 1: [LW R4, 220(R10)]

Entry 2: [LW R5, 264(R0)]

Entry 3:

Pre\_ALU Queue:

Entry 0: [SLL R10, R1, #2]

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	7	0	5	0	1	-1	0
R08:	0	0	32	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

Entry

1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000111>]

Set 2: LRU=1

```

Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,1,6)<11111111111111111111111111111111,0000000000000000000000000000000001>]
Set 3: LRU=0
Entry
0: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
Entry
1: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:   5    -5    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     0
-----

```

Cycle:65

```

Pre-Issue Buffer:
Entry 0:      [LW      R3, 176(R10)]
Entry 1:      [LW      R4, 220(R10)]
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:      [SLL      R10, R1, #2]
Pre_MEM Queue:
Entry 0:      [LW      R5, 264(R0)]
Entry 1:
Post_MEM Queue:
Entry 0:

```

```

Registers
R00:  0     7     0     5     0     1    -1     0
R08:  0     0    32     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=0
Entry
0: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000001100>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000111>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000001>]
Set 3: LRU=0
Entry
0: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
Entry
1: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:   5    -5    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     0

```



-----  
Cycle:66

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R3, 176(R10)]  
Entry 1: [LW R4, 220(R10)]

Post\_MEM Queue:

Entry 0: [LW R5, 264(R0)]

Registers

R00:	0	7	0	5	0	1	-1	0
R08:	0	0	28	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]

Entry

1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

Set 1: LRU=1

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000111>]

Set 2: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000100001100,100010000100000000000000000001100>]

Entry

1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000001>]

Set 3: LRU=0

Entry

0: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Entry

1: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	0

-----  
Cycle:67

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

```

Entry 0:      [LW      R3, 176(R10)]
Entry 1:      [LW      R4, 220(R10)]
Post_MEM Queue:
Entry 0:

```

```

Registers
R00:  0      7      0      5      0      1      -1      0
R08:  0      0     28      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000111&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,1,6)&lt;11111111111111111111111111111111,00000000000000000000000000000001&gt;]

Set 3: LRU=0

Entry

0: [(1,0,4)&lt;101011010100011000000000010110000,10100000001000011111111111111111&gt;]

Entry

1: [(1,0,3)&lt;10000000000000010101000010000000,100011010100001100000000010110000&gt;]

## Data

```

176:  -1     -2     -3      1      2      3      0      0
208:   5     -5     -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      0
-----

```

Cycle:68

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R4, 220(R10)]

Entry 1:

## Post\_MEM Queue:

Entry 0: [LW R3, 176(R10)]

## Registers

```

R00:  0      7      0      5      0      1      -1      0
R08:  0      0     28      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

Entry

```

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
    Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
    Entry
0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,0,6)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000001>]
Set 3: LRU=0
    Entry
0: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]
    Entry
1: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]

```

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	5	-5	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	7

-----  
Cycle:69

## Pre-Issue Buffer:

```

    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:

```

## Pre\_ALU Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_ALU Queue:

```

    Entry 0:

```

## Pre\_MEM Queue:

```

    Entry 0:      [LW      R4, 220(R10)]
    Entry 1:

```

## Post\_MEM Queue:

```

    Entry 0:

```

## Registers

R00:	0	7	0	0	0	1	-1	0
R08:	0	0	28	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

```

    Entry

```

```

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

```

```

    Entry

```

```

1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

```

Set 1: LRU=1

```

    Entry

```

```

0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]

```

```

    Entry

```

```

1: [(1,0,6)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 2: LRU=1

```

    Entry

```

```

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

```

```

    Entry

```

```

1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000001>]

```

Set 3: LRU=0

```

Entry
0: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
Entry
1: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]

```

```

Data
176:  -1      -2      -3      1      2      3      0      0
208:   5      -5      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      7
-----

```

Cycle:70

```

Pre-Issue Buffer:
Entry 0:      [SUB      R6, R4, R5]
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:      [LW      R4, 220(R10)]

```

```

Registers
R00:  0      7      0      0      0      1      -1      0
R08:  0      0      28     0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

Cache

Set 0: LRU=0

```

Entry
0: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

```

Set 1: LRU=1

```

Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,0,6)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 2: LRU=1

```

Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
Entry
1: [(1,1,6)<11111111111111111111111111111111,00000000000000000000000000000001>]

```

Set 3: LRU=1

```

Entry
0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Entry
1: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]

```

```

Data
176:  -1      -2      -3      1      2      3      0      0
208:   5      -5      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      7
-----

```

Cycle:71

```

Pre-Issue Buffer:
Entry 0:

```

```

Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:      [SUB      R6, R4, R5]
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      7      0      0      0      1      -1      0
R08:  0      0      28     0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=0
Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,0,6)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
Entry
0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Entry
1: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]

Data
176:  -1      -2      -3      1      2      3      0      0
208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      7
-----
Cycle:72

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:      [SUB      R6, R4, R5]
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

```

## Registers

R00:	0	7	0	0	0	1	-1	0
R08:	0	0	28	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,0,6)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	7

-----  
Cycle:73

## Pre-Issue Buffer:

Entry 0: [SW R6, 176(R10)]

Entry 1: [ADDI R1, R1, #-1]

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	7	0	0	0	1	-1	0
R08:	0	0	28	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

```

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,0,6)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
    Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
    Entry
0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
    Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	7

-----  
Cycle:74

## Pre-Issue Buffer:

```

    Entry 0:      [SW      R1, 268(R0)]
    Entry 1:
    Entry 2:
    Entry 3:

```

## Pre\_ALU Queue:

```

    Entry 0:      [ADDI    R1, R1, #-1]
    Entry 1:

```

## Post\_ALU Queue:

```

    Entry 0:

```

## Pre\_MEM Queue:

```

    Entry 0:      [SW      R6, 176(R10)]
    Entry 1:

```

## Post\_MEM Queue:

```

    Entry 0:

```

## Registers

R00:	0	7	0	0	0	1	-1	0
R08:	0	0	28	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

```

    Entry

```

```

0: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]

```

```

    Entry

```

```

1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

```

Set 1: LRU=1

```

    Entry

```

```

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

```

```

    Entry

```

```

1: [(1,0,6)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Set 2: LRU=0

```

    Entry

```

```

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

```

```

    Entry

```

```

1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]

```

Set 3: LRU=0

```

    Entry

```

```

0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

    Entry

```

```

1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```
Data
176:  -1    -2    -3    1    2    3    0    0
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    7
```

-----  
Cycle:75

Pre-Issue Buffer:

```
Entry 0:      [SW    R1, 268(R0)]
Entry 1:      [LW    R1, 268(R0)]
Entry 2:
Entry 3:
```

Pre\_ALU Queue:

```
Entry 0:
Entry 1:
```

Post\_ALU Queue:

```
Entry 0:      [ADDI   R1, R1, #-1]
```

Pre\_MEM Queue:

```
Entry 0:
Entry 1:
```

Post\_MEM Queue:

```
Entry 0:
```

Registers

```
R00:  0    7    0    0    0    1    -1    0
R08:  0    0   28    0    0    0    0    0
R16:  0    0    0    0    0    0    0    0
R24:  0    0    0    0    0    0    0    0
```

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

Entry

1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,6)<00000000000000000000000000000000,11111111111111111111111111111111>]

Set 2: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

Entry

1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]

Set 3: LRU=0

Entry

0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]

Data

```
176:  -1    -2    -3    1    2    3    0    0
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    7
```

-----  
Cycle:76

Pre-Issue Buffer:

```
Entry 0:
Entry 1:
Entry 2:
Entry 3:
```

Pre\_ALU Queue:

```
Entry 0:
```



```

Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [SW      R1, 268(R0)]
Entry 1:      [LW      R1, 268(R0)]
Post_MEM Queue:
Entry 0:

Registers
R00:  0      6      0      0      0      1      -1      0
R08:  0      0     28      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,5)<10101100000000010000000100001100,10001000000000000000000000011100>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,6)<00000000000000000000000000000000,1111111111111111111111111111111>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
Entry
1: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
Entry
0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Data
176:  -1     -2     -3      1      2      3      0      0
208:  -1      1     -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      7
-----
Cycle:77

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [SW      R1, 268(R0)]
Entry 1:      [LW      R1, 268(R0)]
Post_MEM Queue:
Entry 0:

Registers
R00:  0      6      0      0      0      1      -1      0
R08:  0      0     28      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

```

Cache
Set 0: LRU=1
    Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
    Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
    Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,1,6)<00000000000000000000000000000000,11111111111111111111111111111111>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
    Entry
0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
    Entry
1: [(1,0,4)<101011010100011000000000010110000,10100000001000011111111111111111>]

Data
176:  -1    -2    -3     1     2     3     0     0
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     7
-----
Cycle:78

Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:          [LW      R1, 268(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:

Registers
R00:  0     6     0     0     0     1    -1     0
R08:  0     0    28     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

Cache
Set 0: LRU=1
    Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
    Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
    Entry
0: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000110>]
    Entry
1: [(1,1,6)<00000000000000000000000000000000,11111111111111111111111111111111>]
Set 2: LRU=1
    Entry

```

```

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
    Entry
0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
    Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     7
-----

```

Cycle:79

```

Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:          [LW      R1, 268(R0)]

```

```

Registers
R00:  0     6     0     0     0     1    -1     0
R08:  0     0    28     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=1
    Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
    Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
    Entry
0: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000110>]
    Entry
1: [(1,1,6)<00000000000000000000000000000000,11111111111111111111111111111111>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
    Entry
0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
    Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     7
-----

```

Cycle:80

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	6	0	0	0	1	-1	0
R08:	0	0	28	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

0: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000110&gt;]

Entry

1: [(1,1,6)&lt;00000000000000000000000000000000,11111111111111111111111111111111&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000000100110,1000000100001010011000000100000&gt;]

Set 3: LRU=0

Entry

0: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,4)&lt;101011010100011000000000010110000,10100000001000011111111111111111&gt;]

Data

176:	-1	-2	-3	1	2	3	0	0
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	7

Cycle:81

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:  
Post\_MEM Queue:  
Entry 0:

## Registers

R00:	0	6	0	0	0	1	-1	0
R08:	0	0	28	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

0: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000110&gt;]

Entry

1: [(1,1,6)&lt;00000000000000000000000000000000,11111111111111111111111111111111&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,1000000100001010011000000100000&gt;]

Set 3: LRU=0

Entry

0: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,4)&lt;101011010100011000000000010110000,10100000001000011111111111111111&gt;]

## Data

176:	-1	-2	-3	1	2	3	0	0
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	7

-----  
Cycle:82

## Pre-Issue Buffer:

Entry 0:	[SLL	R10, R1, #2]
Entry 1:	[LW	R3, 176(R10)]
Entry 2:		
Entry 3:		

## Pre\_ALU Queue:

Entry 0:  
Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:  
Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	6	0	0	0	1	-1	0
R08:	0	0	28	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Data								
176:	-1	-2	-3	1	2	3	0	0
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	7

```
Post_MEM Queue:
    Entry 0:
```

```
Cache
Set 0: LRU=0
    Entry
0: [(1,0,5)<101011000000000010000000100001100,1000100000000000000000000000000011100>]
    Entry
1: [(1,0,4)<1000110101000100000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
    Entry
0: [(1,1,8)<00000000000000000000000000000001,0000000000000000000000000000000000110>]
    Entry
1: [(1,1,6)<00000000000000000000000000000000,11111111111111111111111111111111>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<100011000000000010000000100001100,10000100001000000000000000000001100>]
    Entry
1: [(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
    Entry
```

```

0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,0,4)<101011010100011000000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     7
-----

```

Cycle:84

```

Pre-Issue Buffer:
    Entry 0:      [LW      R3, 176(R10)]
    Entry 1:      [LW      R4, 220(R10)]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:      [SLL      R10, R1, #2]
Pre_MEM Queue:
    Entry 0:      [LW      R5, 264(R0)]
    Entry 1:
Post_MEM Queue:
    Entry 0:

```

```

Registers
R00:   0     6     0     0     0     1    -1     0
R08:   0     0    28     0     0     0     0     0
R16:   0     0     0     0     0     0     0     0
R24:   0     0     0     0     0     0     0     0

```

Cache

Set 0: LRU=0

```

    Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
    Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

```

Set 1: LRU=1

```

    Entry
0: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000110>]
    Entry
1: [(1,1,6)<00000000000000000000000000000000,11111111111111111111111111111111>]

```

Set 2: LRU=1

```

    Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]

```

Set 3: LRU=1

```

    Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,0,4)<101011010100011000000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     0     0
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     7
-----

```

Cycle:85

```

Pre-Issue Buffer:
    Entry 0:
    Entry 1:

```

```

Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R3, 176(R10)]
Entry 1:      [LW      R4, 220(R10)]
Post_MEM Queue:
Entry 0:      [LW      R5, 264(R0)]

Registers
R00:  0      6      0      0      0      1      -1      0
R08:  0      0     24      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=0
Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
Entry
0: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000110>]
Entry
1: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]

Data
176:  -1     -2     -3      1      2      3      0     -1
208:  -1      1     -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      7
-----
Cycle:86

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R3, 176(R10)]
Entry 1:      [LW      R4, 220(R10)]
Post_MEM Queue:
Entry 0:

Registers

```



```

R00:  0      6      0      0      0      1      -1      0
R08:  0      0     24      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,1,8)&lt;00000000000000000000000000000001,000000000000000000000000000000110&gt;]

Entry

1: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;100010000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

## Data

```

176:  -1     -2     -3      1      2      3      0     -1
208:  -1      1     -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      7
-----

```

Cycle:87

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R4, 220(R10)]

Entry 1:

## Post\_MEM Queue:

Entry 0: [LW R3, 176(R10)]

## Registers

```

R00:  0      6      0      0      0      1      -1      0
R08:  0      0     24      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,6)&lt;00000000000000000000000000000000,11111111111111111111111111111111&gt;]

```

      Entry
1: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Set 2: LRU=1
      Entry
0: [(1,0,3)<100011000000000010000000100001100,1000010000100000000000000000001100>]
      Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     0    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     6
-----

```

Cycle:88

Pre-Issue Buffer:

```

      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:

```

Pre\_ALU Queue:

```

      Entry 0:
      Entry 1:

```

Post\_ALU Queue:

```

      Entry 0:

```

Pre\_MEM Queue:

```

      Entry 0:      [LW      R4, 220(R10)]
      Entry 1:

```

Post\_MEM Queue:

```

      Entry 0:

```

Registers

```

R00:  0     6     0     0     0     1    -1     0
R08:  0     0    24     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

Cache

Set 0: LRU=0

```

      Entry

```

```

0: [(1,0,5)<101011000000000010000000100001100,10001000000000000000000000000011100>]

```

```

      Entry

```

```

1: [(1,0,4)<1000110101000100000000000011011100,10001100000001010000000100001000>]

```

Set 1: LRU=0

```

      Entry

```

```

0: [(1,0,6)<00000000000000000000000000000000,11111111111111111111111111111111>]

```

```

      Entry

```

```

1: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

```

Set 2: LRU=1

```

      Entry

```

```

0: [(1,0,3)<100011000000000010000000100001100,1000010000100000000000000000001100>]

```

```

      Entry

```

```

1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]

```

Set 3: LRU=1

```

      Entry

```

```

0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]

```

```

      Entry

```

```

1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

Data

176:	-1	-2	-3	1	2	3	0	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	6

-----  
Cycle:89

Pre-Issue Buffer:

Entry 0: [SUB R6, R4, R5]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0: [LW R4, 220(R10)]

Registers

R00:	0	6	0	0	0	1	-1	0
R08:	0	0	24	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,6)&lt;00000000000000000000000000000000,11111111111111111111111111111111&gt;]

Entry

1: [(1,0,4)&lt;100001000110000000000000000000010,10000000100001010011000000100010&gt;]

Set 2: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,10000100001000000000000000001100&gt;]

Entry

1: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

Data

176:	-1	-2	-3	1	2	3	0	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	6

-----  
Cycle:90

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0: [SUB R6, R4, R5]

Entry 1:

Post\_ALU Queue:  
 Entry 0:  
 Pre\_MEM Queue:  
 Entry 0:  
 Entry 1:  
 Post\_MEM Queue:  
 Entry 0:

## Registers

R00:	0	6	0	0	0	1	-1	0
R08:	0	0	24	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;1010110000000001000000100001100,100010000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,6)&lt;00000000000000000000000000000000,11111111111111111111111111111111&gt;]

Entry

1: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Set 2: LRU=1

Entry

0: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Entry

1: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

## Data

176:	-1	-2	-3	1	2	3	0	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	6

-----  
Cycle:91

## Pre-Issue Buffer:

Entry 0: [SW R6, 176(R10)]

Entry 1: [ADDI R1, R1, #-1]

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0: [SUB R6, R4, R5]

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	6	0	0	0	1	-1	0
R08:	0	0	24	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

```

Cache
Set 0: LRU=0
  Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
  Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
  Entry
0: [(1,0,6)<00000000000000000000000000000000,11111111111111111111111111111111>]
  Entry
1: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
Set 2: LRU=1
  Entry
0: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]
  Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
  Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
  Entry
1: [(1,0,4)<101011010100011000000000010110000,10100000001000011111111111111111>]

Data
176:  -1    -2    -3     1     2     3     0    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     6
-----
Cycle:92

Pre-Issue Buffer:
  Entry 0:      [SW      R1, 268(R0)]
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:      [ADDI    R1, R1, #-1]
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:      [SW      R6, 176(R10)]
  Entry 1:
Post_MEM Queue:
  Entry 0:

Registers
R00:   0     6     0     0     0     1    -1     0
R08:   0     0    24     0     0     0     0     0
R16:   0     0     0     0     0     0     0     0
R24:   0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=1
  Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
  Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
  Entry
0: [(1,0,6)<00000000000000000000000000000000,11111111111111111111111111111111>]
  Entry
1: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
Set 2: LRU=1
  Entry
0: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]

```

```

Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     0    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     6
-----

```

Cycle:93

```

Pre-Issue Buffer:
Entry 0:      [SW      R1, 268(R0)]
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:      [ADDI    R1, R1, #-1]
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

```

```

Registers
R00:  0     6     0     0     0     1    -1     0
R08:  0     0    24     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=1
Entry
0: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
Entry
0: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]
Entry
1: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Set 2: LRU=1
Entry
0: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 3: LRU=0
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     0    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     6
-----

```

Cycle:94

Pre-Issue Buffer:

Entry 0: [LW R1, 268(R0)]  
 Entry 1:  
 Entry 2:  
 Entry 3:

Pre\_ALU Queue:

Entry 0:  
 Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [SW R1, 268(R0)]  
 Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	5	0	0	0	1	-1	0
R08:	0	0	24	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

0: [(1,1,6)&lt;11111111111111111111111111111111,11111111111111111111111111111111&gt;]

Entry

1: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Entry

1: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Set 3: LRU=0

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

Data

176:	-1	-2	-3	1	2	3	0	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	6

-----  
Cycle:95

Pre-Issue Buffer:

Entry 0:  
 Entry 1:  
 Entry 2:  
 Entry 3:

Pre\_ALU Queue:

Entry 0:  
 Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [SW R1, 268(R0)]  
 Entry 1: [LW R1, 268(R0)]

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	5	0	0	0	1	-1	0
R08:	0	0	24	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

0: [(1,1,6)&lt;11111111111111111111111111111111,11111111111111111111111111111111&gt;]

Entry

1: [(1,0,4)&lt;100001000110000000000000000000010,10000000100001010011000000100010&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;10001000000000000000000000000100110,10000000100001010011000000100000&gt;]

Entry

1: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Set 3: LRU=0

Entry

0: [(1,0,3)&lt;1000000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;101011010100011000000000010110000,10100000001000011111111111111111&gt;]

Data

176:	-1	-2	-3	1	2	3	0	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	6

-----  
Cycle:96

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R1, 268(R0)]

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	5	0	0	0	1	-1	0
R08:	0	0	24	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry



```

1: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
    Entry
0: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]
    Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000101>]
Set 2: LRU=0
    Entry
0: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
    Entry
1: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000001100>]
Set 3: LRU=0
    Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]

```

## Data

176:	-1	-2	-3	1	2	3	0	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	6

-----  
Cycle:97

## Pre-Issue Buffer:

```

    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:

```

## Pre\_ALU Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_ALU Queue:

```

    Entry 0:

```

## Pre\_MEM Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_MEM Queue:

```

    Entry 0:          [LW      R1, 268(R0)]

```

## Registers

R00:	0	5	0	0	0	1	-1	0
R08:	0	0	24	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,100010000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,1,6)&lt;11111111111111111111111111111111,11111111111111111111111111111111&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000101&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Entry

1: [(1,0,3)&lt;100011000000000010000000100001100,100001000010000000000000000001100&gt;]

Set 3: LRU=0

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry  
1: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]

Data  
176:   -1       -2       -3       1       2       3       0       -1  
208:   -1       1       -1       0       0       0       0       0  
240:   0       0       0       0       0       0       1       6

-----  
Cycle:98

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:   0       5       0       0       0       1       -1       0  
R08:   0       0       24      0       0       0       0       0  
R16:   0       0       0       0       0       0       0       0  
R24:   0       0       0       0       0       0       0       0

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]

Entry

1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

Set 1: LRU=0

Entry

0: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000101>]

Set 2: LRU=0

Entry

0: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]

Entry

1: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]

Set 3: LRU=0

Entry

0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]

Entry

1: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]

Data

176:   -1       -2       -3       1       2       3       0       -1  
208:   -1       1       -1       0       0       0       0       0  
240:   0       0       0       0       0       0       1       6

-----  
Cycle:99

Pre-Issue Buffer:

Entry 0:       [SLL    R10, R1, #2]  
Entry 1:       [LW    R3, 176(R10)]  
Entry 2:

```

Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      5      0      0      0      1      -1      0
R08:  0      0     24      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
Entry
0: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000101>]
Set 2: LRU=0
Entry
0: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]
Entry
1: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Set 3: LRU=1
Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]

Data
176:  -1     -2     -3      1      2      3      0     -1
208:  -1      1     -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      6
-----
Cycle:100

Pre-Issue Buffer:
Entry 0:      [LW      R3, 176(R10)]
Entry 1:      [LW      R4, 220(R10)]
Entry 2:      [LW      R5, 264(R0)]
Entry 3:
Pre_ALU Queue:
Entry 0:      [SLL      R10, R1, #2]
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      5      0      0      0      1      -1      0

```

```

R08:  0      0      24      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,1,6)&lt;11111111111111111111111111111111,11111111111111111111111111111111&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000101&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;10001000000000000000000000000100110,10000000100001010011000000100000&gt;]

Entry

1: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

## Data

```

176:  -1      -2      -3      1      2      3      0      -1
208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      6
-----

```

Cycle:101

## Pre-Issue Buffer:

Entry 0: [LW R3, 176(R10)]

Entry 1: [LW R4, 220(R10)]

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0: [SLL R10, R1, #2]

## Pre\_MEM Queue:

Entry 0: [LW R5, 264(R0)]

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

```

R00:  0      5      0      0      0      1      -1      0
R08:  0      0      24      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=0

Entry

0: [(1,1,6)&lt;11111111111111111111111111111111,11111111111111111111111111111111&gt;]

Entry

```

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000101>]
Set 2: LRU=0
    Entry
0: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
    Entry
1: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000001100>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     0    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     6
-----

```

Cycle:102

```

Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:      [LW    R3, 176(R10)]
    Entry 1:      [LW    R4, 220(R10)]
Post_MEM Queue:
    Entry 0:      [LW    R5, 264(R0)]

```

```

Registers
R00:  0     5     0     0     0     1    -1     0
R08:  0     0    20     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=0
    Entry
0: [(1,0,5)<101011000000000010000000100001100,100010000000000000000000000011100>]
    Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
    Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000101>]
Set 2: LRU=0
    Entry
0: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
    Entry
1: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000001100>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3    -1    -1

```

```

208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      6
-----

```

Cycle:103

Pre-Issue Buffer:

```

Entry 0:
Entry 1:
Entry 2:
Entry 3:

```

Pre\_ALU Queue:

```

Entry 0:
Entry 1:

```

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

```

Entry 0:      [LW      R3, 176(R10)]
Entry 1:      [LW      R4, 220(R10)]

```

Post\_MEM Queue:

Entry 0:

Registers

```

R00:  0      5      0      0      0      1      -1      0
R08:  0      0      20     0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,4)&lt;100011010100010000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000101&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;100010000000000000000000000100110,10000000100001010011000000100000&gt;]

Entry

1: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

Data

```

176:  -1      -2      -3      1      2      3      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      6
-----

```

Cycle:104

Pre-Issue Buffer:

```

Entry 0:
Entry 1:
Entry 2:
Entry 3:

```

Pre\_ALU Queue:

```

Entry 0:
Entry 1:

```

Post\_ALU Queue:

```

Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R4, 220(R10)]
Entry 1:
Post_MEM Queue:
Entry 0:      [LW      R3, 176(R10)]

Registers
R00:  0      5      0      0      0      1      -1      0
R08:  0      0      20     0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,6)<00000000000000000000000000000010,00000000000000000000000000000011>]
Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000101>]
Set 2: LRU=0
Entry
0: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Entry
1: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Set 3: LRU=1
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Data
176:  -1      -2      -3      1      2      3      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      6
-----
Cycle:105

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R4, 220(R10)]
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      5      0      3      0      1      -1      0
R08:  0      0      20     0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache

```

```

Set 0: LRU=1
      Entry
0: [(1,0,6)<00000000000000000000000000000010,00000000000000000000000000000011>]
      Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
      Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000101>]
Set 2: LRU=0
      Entry
0: [(1,0,4)<100010000000000000000000000000100110,10000000100001010011000000100000>]
      Entry
1: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000001100>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<1000000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     6
-----

```

Cycle:106

```

Pre-Issue Buffer:
      Entry 0:      [SUB    R6, R4, R5]
      Entry 1:
      Entry 2:
      Entry 3:
Pre_ALU Queue:
      Entry 0:
      Entry 1:
Post_ALU Queue:
      Entry 0:
Pre_MEM Queue:
      Entry 0:
      Entry 1:
Post_MEM Queue:
      Entry 0:      [LW     R4, 220(R10)]

```

```

Registers
R00:  0     5     0     3     0     1    -1     0
R08:  0     0    20     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=1
      Entry
0: [(1,0,6)<00000000000000000000000000000010,00000000000000000000000000000011>]
      Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
      Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000101>]
Set 2: LRU=1
      Entry
0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry

```



```

1: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000001100>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<1000000000000000010101000010000000,100011010100001100000000010110000>]
      Entry
1: [(1,0,4)<101011010100011000000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     6
-----

```

Cycle:107

Pre-Issue Buffer:

```

      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:

```

Pre\_ALU Queue:

```

      Entry 0:      [SUB    R6, R4, R5]
      Entry 1:

```

Post\_ALU Queue:

```

      Entry 0:

```

Pre\_MEM Queue:

```

      Entry 0:
      Entry 1:

```

Post\_MEM Queue:

```

      Entry 0:

```

Registers

```

R00:   0     5     0     3     0     1    -1     0
R08:   0     0    20     0     0     0     0     0
R16:   0     0     0     0     0     0     0     0
R24:   0     0     0     0     0     0     0     0

```

Cache

Set 0: LRU=1

Entry

```

0: [(1,0,6)<00000000000000000000000000000010,0000000000000000000000000000011>]

```

Entry

```

1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

```

Set 1: LRU=1

Entry

```

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

```

Entry

```

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000101>]

```

Set 2: LRU=0

Entry

```

0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Entry

```

1: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]

```

Set 3: LRU=1

Entry

```

0: [(1,0,3)<1000000000000000010101000010000000,100011010100001100000000010110000>]

```

Entry

```

1: [(1,0,4)<101011010100011000000000010110000,1010000000100001111111111111111>]

```

Data

```

176:  -1    -2    -3     1     2     3     -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     6
-----

```

Cycle:108

```

Pre-Issue Buffer:
    Entry 0:      [SW      R6, 176(R10)]
    Entry 1:      [ADDI    R1, R1, #-1]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:      [SUB      R6, R4, R5]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

```

```

Registers
R00:  0      5      0      3      0      1      -1      0
R08:  0      0     20      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

```

Cache
Set 0: LRU=1
    Entry
0: [(1,0,6)<00000000000000000000000000000010,00000000000000000000000000000011>]
    Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
    Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000101>]
Set 2: LRU=0
    Entry
0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
    Entry
1: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
    Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]

```

```

Data
176:  -1     -2     -3      1      2      3      -1     -1
208:  -1      1     -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      6
-----

```

Cycle:109

```

Pre-Issue Buffer:
    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:      [ADDI    R1, R1, #-1]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:      [SW      R6, 176(R10)]
    Entry 1:
Post_MEM Queue:

```

Entry 0:

Registers

R00:	0	5	0	3	0	1	-1	0
R08:	0	0	20	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,6)&lt;00000000000000000000000000000010,000000000000000000000000000011&gt;]

Entry

1: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000101&gt;]

Set 2: LRU=0

Entry

0: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=0

Entry

0: [(1,0,3)&lt;1000000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

Data

176:	-1	-2	-3	1	2	3	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	6

-----  
Cycle:110

Pre-Issue Buffer:

Entry 0: [SW R1, 268(R0)]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0: [ADDI R1, R1, #-1]

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	5	0	3	0	1	-1	0
R08:	0	0	20	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,1,6)&lt;00000000000000000000000000000010,11111111111111111111111111111111&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,100010000000000000000000000011100&gt;]

```

Set 1: LRU=1
      Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000101>]
Set 2: LRU=0
      Entry
0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     6
-----

```

Cycle:111

Pre-Issue Buffer:

```

      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:

```

Pre\_ALU Queue:

```

      Entry 0:
      Entry 1:

```

Post\_ALU Queue:

```

      Entry 0:

```

Pre\_MEM Queue:

```

      Entry 0:      [SW      R1, 268(R0)]
      Entry 1:

```

Post\_MEM Queue:

```

      Entry 0:

```

Registers

```

R00:  0     4     0     3     0     1     -1     0
R08:  0     0    20     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

Cache

Set 0: LRU=0

Entry

```

0: [(1,1,6)<00000000000000000000000000000010,1111111111111111111111111111111>]

```

Entry

```

1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]

```

Set 1: LRU=1

Entry

```

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

```

Entry

```

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000101>]

```

Set 2: LRU=0

Entry

```

0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

Entry

```

1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]

```

Set 3: LRU=0

Entry

```

0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]

```

Entry

1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Data								
176:	-1	-2	-3	1	2	3	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	6

-----  
Cycle:112

Pre-Issue Buffer:  
 Entry 0: [LW R1, 268(R0)]  
 Entry 1:  
 Entry 2:  
 Entry 3:  
 Pre\_ALU Queue:  
 Entry 0:  
 Entry 1:  
 Post\_ALU Queue:  
 Entry 0:  
 Pre\_MEM Queue:  
 Entry 0:  
 Entry 1:  
 Post\_MEM Queue:  
 Entry 0:

Registers								
R00:	0	4	0	3	0	1	-1	0
R08:	0	0	20	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache  
 Set 0: LRU=0  
 Entry  
 0: [(1,1,6)<00000000000000000000000000000010,1111111111111111111111111111111>]  
 Entry  
 1: [(1,0,5)<101011000000000010000000100001100,1000100000000000000000000000011100>]  
 Set 1: LRU=0  
 Entry  
 0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]  
 Entry  
 1: [(1,1,8)<000000000000000000000000000000001,000000000000000000000000000000100>]  
 Set 2: LRU=1  
 Entry  
 0: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000001100>]  
 Entry  
 1: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]  
 Set 3: LRU=0  
 Entry  
 0: [(1,0,3)<1000000000000000010101000010000000,10001101010000110000000010110000>]  
 Entry  
 1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Data								
176:	-1	-2	-3	1	2	3	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	6

-----  
Cycle:113

Pre-Issue Buffer:  
 Entry 0:  
 Entry 1:  
 Entry 2:  
 Entry 3:

```

Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:      [LW      R1, 268(R0)]
  Entry 1:
Post_MEM Queue:
  Entry 0:

Registers
R00:  0      4      0      3      0      1      -1      0
R08:  0      0      20     0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=0
  Entry
0: [(1,1,6)<00000000000000000000000000000010,11111111111111111111111111111111>]
  Entry
1: [(1,0,5)<101011000000000010000000100001100,10001000000000000000000000000011100>]
Set 1: LRU=0
  Entry
0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
  Entry
1: [(1,1,8)<000000000000000000000000000000001,000000000000000000000000000000100>]
Set 2: LRU=1
  Entry
0: [(1,0,3)<100011000000000010000000100001100,1000010000100000000000000000001100>]
  Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
  Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
  Entry
1: [(1,0,4)<101011010100011000000000010110000,10100000001000011111111111111111>]

Data
176:  -1      -2      -3      1      2      3      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      6
-----
Cycle:114

Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:      [LW      R1, 268(R0)]

Registers
R00:  0      4      0      3      0      1      -1      0
R08:  0      0      20     0      0      0      0      0

```

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Cache

Entry

Entry

Set 1: LRU=0

$$0: [(1, 0, 4) < 10]$$
$$1 : [(1, 1, 8) < 00]$$

Entr

Entry

Set 3: LRU=0

```
0: [(1, 0, 3) < 10
```

```
1: [(1,0,4)<10
```

## Data

208: -1

-----

Cycle: 113

Pre-Issue Bul.  
Entry

Entry

```

      ENTRY
  Proc ALL Queue

```

Entry  
EntryPost\_ALU Queue  
EnterPre\_MEM Queue  
FutureEntry  
Post MEM Quay

Entry

Registers  
R00: 0

```
R08:      0
R16:      0
```

R24: 0

Cache

Entry

Entry

Set 1: LRU=0

```
0: [(1, 0, 4) < 10
```

```
1: [(1,1,8)<00
```

---

```

Set 2: LRU=1
      Entry
0: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000000001100>]
      Entry
1: [(1,0,4)<10001000000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<101011010100011000000000010110000,10100000001000011111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     6
-----

```

Cycle:116

```

Pre-Issue Buffer:
      Entry 0:      [SLL    R10, R1, #2]
      Entry 1:      [LW     R3, 176(R10)]
      Entry 2:
      Entry 3:

```

```

Pre_ALU Queue:
      Entry 0:
      Entry 1:

```

```

Post_ALU Queue:
      Entry 0:

```

```

Pre_MEM Queue:
      Entry 0:
      Entry 1:

```

```

Post_MEM Queue:
      Entry 0:

```

```

Registers
R00:   0     4     0     3     0     1    -1     0
R08:   0     0    20     0     0     0     0     0
R16:   0     0     0     0     0     0     0     0
R24:   0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=0
      Entry
0: [(1,1,6)<00000000000000000000000000000010,11111111111111111111111111111111>]
      Entry
1: [(1,0,5)<101011000000000010000000100001100,1000100000000000000000000000000011100>]
Set 1: LRU=0
      Entry
0: [(1,0,4)<1000010001100000000000000000000010,100000001000010100110000001000010>]
      Entry
1: [(1,1,8)<0000000000000000000000000000000001,00000000000000000000000000000000100>]
Set 2: LRU=1
      Entry
0: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000000001100>]
      Entry
1: [(1,0,4)<10001000000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<101011010100011000000000010110000,10100000001000011111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     3     -1    -1
208:  -1     1    -1     0     0     0     0     0

```



```
240:    0        0        0        0        0        0        1        6
```

```
-----
Cycle:117
```

```
Pre-Issue Buffer:
```

```
Entry 0:    [LW    R3, 176(R10)]
Entry 1:
Entry 2:
Entry 3:
```

```
Pre_ALU Queue:
```

```
Entry 0:    [SLL    R10, R1, #2]
Entry 1:
```

```
Post_ALU Queue:
```

```
Entry 0:
```

```
Pre_MEM Queue:
```

```
Entry 0:
```

```
Entry 1:
```

```
Post_MEM Queue:
```

```
Entry 0:
```

```
Registers
```

```
R00:    0        4        0        3        0        1        -1        0
R08:    0        0       20        0        0        0        0        0
R16:    0        0        0        0        0        0        0        0
R24:    0        0        0        0        0        0        0        0
```

```
Cache
```

```
Set 0: LRU=0
```

```
Entry
```

```
0: [(1,1,6)<00000000000000000000000000000010,11111111111111111111111111111111>]
```

```
Entry
```

```
1: [(1,0,5)<101011000000000010000000100001100,100010000000000000000000000011100>]
```

```
Set 1: LRU=0
```

```
Entry
```

```
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
```

```
Entry
```

```
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000100>]
```

```
Set 2: LRU=1
```

```
Entry
```

```
0: [(1,0,3)<100011000000000010000000100001100,10000100001000000000000000001100>]
```

```
Entry
```

```
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
```

```
Set 3: LRU=1
```

```
Entry
```

```
0: [(1,0,3)<1000000000000000010101000010000000,10001101010000110000000010110000>]
```

```
Entry
```

```
1: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]
```

```
Data
```

```
176:    -1       -2       -3        1        2        3       -1       -1
208:    -1        1       -1        0        0        0        0        0
240:     0        0        0        0        0        0        1        6
```

```
-----
Cycle:118
```

```
Pre-Issue Buffer:
```

```
Entry 0:    [LW    R3, 176(R10)]
Entry 1:    [LW    R4, 220(R10)]
Entry 2:    [LW    R5, 264(R0)]
Entry 3:
```

```
Pre_ALU Queue:
```

```
Entry 0:
```

```
Entry 1:
```

```
Post_ALU Queue:
```

```
Entry 0:    [SLL    R10, R1, #2]
```

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	4	0	3	0	1	-1	0
R08:	0	0	20	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,000000000000000000000000000000100&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,1010000000100001111111111111111&gt;]

Data

176:	-1	-2	-3	1	2	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	6

Cycle:119

Pre-Issue Buffer:

Entry 0: [LW R5, 264(R0)]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R3, 176(R10)]

Entry 1: [LW R4, 220(R10)]

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	4	0	3	0	1	-1	0
R08:	0	0	16	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

```

Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
Entry
1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Set 1: LRU=1
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,000000000000000000000000000000100>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,1000010000100000000000000000001100>]
Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2    -1    -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     6
-----

```

Cycle:120

```

Pre-Issue Buffer:
Entry 0:      [LW      R5, 264(R0)]
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R3, 176(R10)]
Entry 1:      [LW      R4, 220(R10)]
Post_MEM Queue:
Entry 0:

```

```

Registers
R00:  0     4     0     3     0     1    -1     0
R08:  0     0    16     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=1
Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
Entry
1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Set 1: LRU=1
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,000000000000000000000000000000100>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]

```

```

Set 3: LRU=1
      Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]

```

```

Data
176:  -1    -2    -3    1    2    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    6
-----

```

Cycle:121

```

Pre-Issue Buffer:
      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:
Pre_ALU Queue:
      Entry 0:
      Entry 1:
Post_ALU Queue:
      Entry 0:
Pre_MEM Queue:
      Entry 0:      [LW      R4, 220(R10)]
      Entry 1:      [LW      R5, 264(R0)]
Post_MEM Queue:
      Entry 0:      [LW      R3, 176(R10)]

```

```

Registers
R00:  0    4    0    3    0    1    -1    0
R08:  0    0   16    0    0    0    0    0
R16:  0    0    0    0    0    0    0    0
R24:  0    0    0    0    0    0    0    0

```

```

Cache
Set 0: LRU=0
      Entry
0: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
      Entry
1: [(1,0,6)<00000000000000000000000000000010,111111111111111111111111111111>]
Set 1: LRU=1
      Entry
0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000001,0000000000000000000000000000100>]
Set 2: LRU=1
      Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
      Entry
1: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]

```

```

Data
176:  -1    -2    -3    1    2    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    6
-----

```

Cycle:122

Pre-Issue Buffer:

```

Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R4, 220(R10)]
Entry 1:      [LW      R5, 264(R0)]
Post_MEM Queue:
Entry 0:

Registers
R00:  0      4      0      2      0      1      -1      0
R08:  0      0      16     0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=0
Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
Entry
1: [(1,0,6)<00000000000000000000000000000010,11111111111111111111111111111111>]
Set 1: LRU=1
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000100>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]

Data
176:  -1      -2      -3      1      2      -1      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      6
-----
Cycle:123

Pre-Issue Buffer:
Entry 0:      [SUB      R6, R4, R5]
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R5, 264(R0)]
Entry 1:
Post_MEM Queue:
Entry 0:      [LW      R4, 220(R10)]

```

## Registers

R00:	0	4	0	2	0	1	-1	0
R08:	0	0	16	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,6)&lt;00000000000000000000000000000010,11111111111111111111111111111111&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,10000100001000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

## Data

176:	-1	-2	-3	1	2	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	4

-----  
Cycle:124

## Pre-Issue Buffer:

Entry 0: [SUB R6, R4, R5]

Entry 1: [SW R6, 176(R10)]

Entry 2: [ADDI R1, R1, #-1]

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R5, 264(R0)]

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	4	0	2	0	1	-1	0
R08:	0	0	16	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,6)&lt;00000000000000000000000000000010,11111111111111111111111111111111&gt;]

Set 1: LRU=1

```

Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3    1    2    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    4
-----

```

Cycle:125

```

Pre-Issue Buffer:
Entry 0:      [SUB    R6, R4, R5]
Entry 1:      [SW     R6, 176(R10)]
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:      [ADDI   R1, R1, #-1]
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:      [LW     R5, 264(R0)]

```

```

Registers
R00:  0    4    0    2    0    1    -1    0
R08:  0    0   16    0    0    0    0    0
R16:  0    0    0    0    0    0    0    0
R24:  0    0    0    0    0    0    0    0

```

```

Cache
Set 0: LRU=0
Entry
0: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Entry
1: [(1,0,6)<00000000000000000000000000000010,1111111111111111111111111111111>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,0,8)<00000000000000000000000000000001,00000000000000000000000000000100>]
Set 2: LRU=0
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```
Data
176:  -1    -2    -3    1    2    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    4
-----
```

Cycle:126

```
Pre-Issue Buffer:
    Entry 0:      [SW      R6, 176(R10)]
    Entry 1:      [SW      R1, 268(R0)]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:      [SUB      R6, R4, R5]
    Entry 1:
Post_ALU Queue:
    Entry 0:      [ADDI     R1, R1, #-1]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:
```

```
Registers
R00:   0    4    0    2    0    1    -1    0
R08:   0    0   16    0    0    0    0    0
R16:   0    0    0    0    0    0    0    0
R24:   0    0    0    0    0    0    0    0
```

Cache

```
Set 0: LRU=1
    Entry
0: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]
    Entry
1: [(1,0,6)<00000000000000000000000000000010,11111111111111111111111111111111>]
Set 1: LRU=0
    Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,0,8)<00000000000000000000000000000001,00000000000000000000000000000100>]
Set 2: LRU=0
    Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
    Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
    Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]
```

```
Data
176:  -1    -2    -3    1    2    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    4
-----
```

Cycle:127

```
Pre-Issue Buffer:
    Entry 0:      [SW      R6, 176(R10)]
    Entry 1:      [SW      R1, 268(R0)]
    Entry 2:      [LW      R1, 268(R0)]
    Entry 3:
Pre_ALU Queue:
```



```

Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:      [SUB      R6, R4, R5]
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      3      0      2      0      1      -1      0
R08:  0      0     16      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Entry
1: [(1,0,6)<00000000000000000000000000000010,11111111111111111111111111111111>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,0,8)<00000000000000000000000000000001,00000000000000000000000000000100>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]

Data
176:  -1      -2      -3      1      2      -1      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      4
-----
Cycle:128

Pre-Issue Buffer:
Entry 0:      [SW      R1, 268(R0)]
Entry 1:      [LW      R1, 268(R0)]
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [SW      R6, 176(R10)]
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      3      0      2      0      1      -1      0
R08:  0      0     16      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0

```

R24: 0 0 0 0 0 0 0 0 0

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

Entry

1: [(1,0,6)<00000000000000000000000000000010,11111111111111111111111111111111>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,0,8)<00000000000000000000000000000001,00000000000000000000000000000100>]

Set 2: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

Entry

1: [(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]

Set 3: LRU=0

Entry

0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]

Entry

1: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]

Data

176: -1 -2 -3 1 2 -1 -1 -1

208: -1 1 -1 0 0 0 0 0

240: 0 0 0 0 0 0 1 4

-----  
Cycle:129

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [SW R1, 268(R0)]

Entry 1: [LW R1, 268(R0)]

Post\_MEM Queue:

Entry 0:

Registers

R00: 0 3 0 2 0 1 -1 0

R08: 0 0 16 0 0 0 0 0

R16: 0 0 0 0 0 0 0 0

R24: 0 0 0 0 0 0 0 0

Cache

Set 0: LRU=0

Entry

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

Entry

1: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,0,8)<00000000000000000000000000000001,00000000000000000000000000000100>]

Set 2: LRU=1

```

Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<101011010100011000000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     -1     -1     -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     4
-----

```

Cycle:130

Pre-Issue Buffer:

```

Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R1, 268(R0)]
Entry 1:
Post_MEM Queue:
Entry 0:

```

Registers

```

R00:  0     3     0     2     0     1     -1     0
R08:  0     0    16     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

Cache

```

Set 0: LRU=0
Entry
0: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000001100>]
Entry
1: [(1,1,6)<11111111111111111111111111111111,1111111111111111111111111111111>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000011>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<101011010100011000000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     -1     -1     -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     4

```

-----  
Cycle:131

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0: [LW R1, 268(R0)]

Registers

R00:	0	3	0	2	0	1	-1	0
R08:	0	0	16	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

Entry

1: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]

Set 1: LRU=0

Entry

0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000011>]

Set 2: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

Entry

1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]

Set 3: LRU=0

Entry

0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]

Entry

1: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]

Data

176:	-1	-2	-3	1	2	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	4

-----  
Cycle:132

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:  
Post\_MEM Queue:  
Entry 0:

## Registers

R00:	0	3	0	2	0	1	-1	0
R08:	0	0	16	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,1,6)&lt;11111111111111111111111111111111,11111111111111111111111111111111&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;100001000110000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000011&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;10001000000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=0

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

## Data

176:	-1	-2	-3	1	2	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	4

-----  
Cycle:133

## Pre-Issue Buffer:

Entry 0: [SLL R10, R1, #2]  
Entry 1: [LW R3, 176(R10)]  
Entry 2:  
Entry 3:

## Pre\_ALU Queue:

Entry 0:  
Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:  
Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	3	0	2	0	1	-1	0
R08:	0	0	16	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

```

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
    Entry
1: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]
Set 1: LRU=0
    Entry
0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000011>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    -3     1     2     -1     -1     -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     4
-----

```

Cycle:134

```

Pre-Issue Buffer:
    Entry 0:          [LW      R3, 176(R10)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:          [SLL      R10, R1, #2]
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

```

```

Registers
R00:  0     3     0     2     0     1     -1     0
R08:  0     0    16     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=0
    Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
    Entry
1: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]
Set 1: LRU=0
    Entry
0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000011>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1

```

```

Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]

```

```

Data
176:  -1    -2    -3    1    2    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    4
-----

```

Cycle:135

```

Pre-Issue Buffer:
Entry 0:      [LW    R3, 176(R10)]
Entry 1:      [LW    R4, 220(R10)]
Entry 2:      [LW    R5, 264(R0)]
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:      [SLL    R10, R1, #2]
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

```

```

Registers
R00:  0    3    0    2    0    1    -1    0
R08:  0    0    16   0    0    0    0    0
R16:  0    0    0    0    0    0    0    0
R24:  0    0    0    0    0    0    0    0

```

Cache

Set 0: LRU=1

```

Entry
0: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Entry
1: [(1,1,6)<11111111111111111111111111111111,1111111111111111111111111111>]

```

Set 1: LRU=0

```

Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,000000000000000000000000000011>]

```

Set 2: LRU=1

```

Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
Entry
1: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]

```

Set 3: LRU=1

```

Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]

```

```

Data
176:  -1    -2    -3    1    2    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    4
-----

```

Cycle:136

```

Pre-Issue Buffer:
Entry 0:      [LW    R5, 264(R0)]

```

```

Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R3, 176(R10)]
Entry 1:      [LW      R4, 220(R10)]
Post_MEM Queue:
Entry 0:

```

## Registers

R00:	0	3	0	2	0	1	-1	0
R08:	0	0	12	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

```

Entry
0: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

```

```

Entry
1: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]

```

Set 1: LRU=1

```

Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

```

```

Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000011>]

```

Set 2: LRU=1

```

Entry
0: [(1,0,3)<10001100000000010000000100001100,1000010000100000000000000000001100>]

```

```

Entry
1: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]

```

Set 3: LRU=1

```

Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]

```

```

Entry
1: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]

```

## Data

176:	-1	-2	-3	1	2	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	4

-----  
Cycle:137

## Pre-Issue Buffer:

```

Entry 0:      [LW      R5, 264(R0)]
Entry 1:
Entry 2:
Entry 3:

```

## Pre\_ALU Queue:

```

Entry 0:
Entry 1:

```

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

```

Entry 0:      [LW      R3, 176(R10)]
Entry 1:      [LW      R4, 220(R10)]

```

## Post\_MEM Queue:

Entry 0:



## Registers

R00:	0	3	0	2	0	1	-1	0
R08:	0	0	12	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,1,6)&lt;11111111111111111111111111111111,11111111111111111111111111111111&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000011&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,1000010000100000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;100010000000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

## Data

176:	-1	-2	-3	1	2	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	4

-----  
Cycle:138

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R4, 220(R10)]

Entry 1: [LW R5, 264(R0)]

## Post\_MEM Queue:

Entry 0: [LW R3, 176(R10)]

## Registers

R00:	0	3	0	2	0	1	-1	0
R08:	0	0	12	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,1,6)&lt;11111111111111111111111111111111,11111111111111111111111111111111&gt;]

Set 1: LRU=1

Entry

```

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000011>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000100001100,1000010000100000000000000000001100>]
    Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
    Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,0,5)<11111111111111111111111111111101,0000000000000000000000000000001>]

```

## Data

176:	-1	-2	-3	1	2	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	4

-----  
Cycle:139

## Pre-Issue Buffer:

```

    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:

```

## Pre\_ALU Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_ALU Queue:

```

    Entry 0:

```

## Pre\_MEM Queue:

```

    Entry 0:      [LW      R4, 220(R10)]
    Entry 1:      [LW      R5, 264(R0)]

```

## Post\_MEM Queue:

```

    Entry 0:

```

## Registers

R00:	0	3	0	1	0	1	-1	0
R08:	0	0	12	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

```

    Entry

```

```

0: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

```

```

    Entry

```

```

1: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]

```

Set 1: LRU=1

```

    Entry

```

```

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

```

```

    Entry

```

```

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000011>]

```

Set 2: LRU=1

```

    Entry

```

```

0: [(1,0,3)<10001100000000010000000100001100,1000010000100000000000000000001100>]

```

```

    Entry

```

```

1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]

```

Set 3: LRU=0

```

    Entry

```

```

0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]

```

```

    Entry

```

```

1: [(1,0,5)<11111111111111111111111111111101,0000000000000000000000000000001>]

```

```
Data
176:  -1    -2    -3    1    2    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    4
```

-----  
Cycle:140

Pre-Issue Buffer:

```
Entry 0:      [SUB    R6, R4, R5]
Entry 1:
Entry 2:
Entry 3:
```

Pre\_ALU Queue:

```
Entry 0:
Entry 1:
```

Post\_ALU Queue:

```
Entry 0:
```

Pre\_MEM Queue:

```
Entry 0:      [LW     R5, 264(R0)]
Entry 1:
```

Post\_MEM Queue:

```
Entry 0:      [LW     R4, 220(R10)]
```

Registers

```
R00:  0    3    0    1    0    1    -1    0
R08:  0    0   12    0    0    0    0    0
R16:  0    0    0    0    0    0    0    0
R24:  0    0    0    0    0    0    0    0
```

Cache

Set 0: LRU=1

Entry

```
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
```

Entry

```
1: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]
```

Set 1: LRU=1

Entry

```
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
```

Entry

```
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
```

Set 2: LRU=0

Entry

```
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
```

Entry

```
1: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]
```

Set 3: LRU=0

Entry

```
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
```

Entry

```
1: [(1,0,5)<11111111111111111111111111111101,00000000000000000000000000000001>]
```

Data

```
176:  -1    -2    -3    1    2    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    3
```

-----  
Cycle:141

Pre-Issue Buffer:

```
Entry 0:      [SUB    R6, R4, R5]
Entry 1:
Entry 2:
Entry 3:
```

Pre\_ALU Queue:

```
Entry 0:
```

```

Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R5, 264(R0)]
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      3      0      1      0      1      -1      0
R08:  0      0     12      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
Entry
1: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]
Set 1: LRU=1
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 2: LRU=0
Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
Entry
1: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,5)<11111111111111111111111111111101,00000000000000000000000000000001>]

Data
176:  -1      -2      -3      1      2      -1      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      3
-----
Cycle:142

Pre-Issue Buffer:
Entry 0:      [SUB      R6, R4, R5]
Entry 1:      [SW       R6, 176(R10)]
Entry 2:      [ADDI     R1, R1, #-1]
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:      [LW       R5, 264(R0)]

Registers
R00:  0      3      0      1      0      1      -1      0
R08:  0      0     12      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

```

Cache
Set 0: LRU=1
    Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
    Entry
1: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]
Set 1: LRU=0
    Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,0,8)<00000000000000000000000000000001,00000000000000000000000000000011>]
Set 2: LRU=0
    Entry
0: [(1,0,3)<10001100000000010000000100001100,1000010000100000000000000000001100>]
    Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
    Entry
0: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]
    Entry
1: [(1,0,5)<11111111111111111111111111111101,00000000000000000000000000000001>]

Data
176:  -1    -2    -3     1     2    -1    -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     3
-----
Cycle:143

Pre-Issue Buffer:
    Entry 0:      [SW      R6, 176(R10)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:      [SUB      R6, R4, R5]
    Entry 1:      [ADDI     R1, R1, #-1]
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

Registers
R00:  0     3     0     1     0     1    -1     0
R08:  0     0    12     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=1
    Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
    Entry
1: [(1,1,6)<11111111111111111111111111111111,11111111111111111111111111111111>]
Set 1: LRU=0
    Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,0,8)<00000000000000000000000000000001,00000000000000000000000000000011>]
Set 2: LRU=0
    Entry

```

```

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
    Entry
0: [(1,0,4)<101011010100011000000000010110000,1010000000100001111111111111111>]
    Entry
1: [(1,0,5)<111111111111111111111111111111101,00000000000000000000000000000001>]

```

```

Data
176:  -1    -2    -3     1     2    -1    -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     3
-----

```

Cycle:144

```

Pre-Issue Buffer:
    Entry 0:      [SW      R6, 176(R10)]
    Entry 1:      [SW      R1, 268(R0)]
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:      [ADDI    R1, R1, #-1]
    Entry 1:
Post_ALU Queue:
    Entry 0:      [SUB     R6, R4, R5]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

```

```

Registers
R00:  0     3     0     1     0     1    -1     0
R08:  0     0    12     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=0
    Entry
0: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
    Entry
1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000001100>]
Set 1: LRU=0
    Entry
0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,0,8)<000000000000000000000000000000001,000000000000000000000000000000011>]
Set 2: LRU=0
    Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
    Entry
1: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
    Entry
0: [(1,0,4)<101011010100011000000000010110000,1010000000100001111111111111111>]
    Entry
1: [(1,0,5)<111111111111111111111111111111101,00000000000000000000000000000001>]

```

```

Data
176:  -1    -2    -3     1    -1    -1    -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     3
-----

```

Cycle:145

Pre-Issue Buffer:

Entry 0: [SW R1, 268(R0)]  
 Entry 1: [LW R1, 268(R0)]  
 Entry 2:  
 Entry 3:

Pre\_ALU Queue:

Entry 0:  
 Entry 1:

Post\_ALU Queue:

Entry 0: [ADDI R1, R1, #-1]

Pre\_MEM Queue:

Entry 0: [SW R6, 176(R10)]  
 Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	3	0	1	0	1	-1	0
R08:	0	0	12	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,0,8)&lt;00000000000000000000000000000001,00000000000000000000000000000011&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,4)&lt;10101101010001100000000010110000,1010000000100001111111111111111&gt;]

Entry

1: [(1,0,5)&lt;11111111111111111111111111111101,00000000000000000000000000000001&gt;]

Data

176:	-1	-2	-3	1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

Cycle:146

Pre-Issue Buffer:

Entry 0:  
 Entry 1:  
 Entry 2:  
 Entry 3:

Pre\_ALU Queue:

Entry 0:  
 Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [SW R1, 268(R0)]

Entry 1: [LW R1, 268(R0)]  
 Post\_MEM Queue:  
 Entry 0:

## Registers

R00:	0	2	0	1	0	1	-1	0
R08:	0	0	12	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,0,8)&lt;00000000000000000000000000000001,00000000000000000000000000000011&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=0

Entry

0: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

Entry

1: [(1,1,5)&lt;11111111111111111111111111111101,11111111111111111111111111111111&gt;]

## Data

176:	-1	-2	-3	1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:147

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue: [LW R1, 268(R0)]

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	2	0	1	0	1	-1	0
R08:	0	0	12	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]



```

Entry
1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000010>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000000001100>]
Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
Entry
0: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]
Entry
1: [(1,1,5)<11111111111111111111111111111101,1111111111111111111111111111111>]

```

## Data

176:	-1	-2	-3	1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:148

## Pre-Issue Buffer:

```

Entry 0:
Entry 1:
Entry 2:
Entry 3:

```

## Pre\_ALU Queue:

```

Entry 0:
Entry 1:

```

## Post\_ALU Queue:

```

Entry 0:

```

## Pre\_MEM Queue:

```

Entry 0:
Entry 1:

```

## Post\_MEM Queue:

```

Entry 0:          [LW      R1, 268(R0)]

```

## Registers

R00:	0	2	0	1	0	1	-1	0
R08:	0	0	12	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

```

Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
Entry

```

```

1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Set 1: LRU=0
Entry

```

```

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry

```

```

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000010>]
Set 2: LRU=1
Entry

```

```

0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000000001100>]
Entry

```

```

1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
Entry

```

```

0: [(1,0,4)<101011010100011000000000010110000,101000000010000111111111111111>]
    Entry
1: [(1,1,5)<11111111111111111111111111111101,1111111111111111111111111111>]

```

```

Data
176:  -1    -2    -3     1    -1    -1    -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     3
-----

```

Cycle:149

Pre-Issue Buffer:

```

    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:

```

Pre\_ALU Queue:

```

    Entry 0:
    Entry 1:

```

Post\_ALU Queue:

```

    Entry 0:

```

Pre\_MEM Queue:

```

    Entry 0:
    Entry 1:

```

Post\_MEM Queue:

```

    Entry 0:

```

Registers

```

R00:   0     2     0     1     0     1    -1     0
R08:   0     0    12     0     0     0     0     0
R16:   0     0     0     0     0     0     0     0
R24:   0     0     0     0     0     0     0     0

```

Cache

Set 0: LRU=0

Entry

```

0: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

```

Entry

```

1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

```

Set 1: LRU=0

Entry

```

0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]

```

Entry

```

1: [(1,1,8)<000000000000000000000000000000001,00000000000000000000000000000010>]

```

Set 2: LRU=1

Entry

```

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

```

Entry

```

1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]

```

Set 3: LRU=0

Entry

```

0: [(1,0,4)<101011010100011000000000010110000,101000000010000111111111111111>]

```

Entry

```

1: [(1,1,5)<11111111111111111111111111111101,1111111111111111111111111111>]

```

```

Data
176:  -1    -2    -3     1    -1    -1    -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     3
-----

```

Cycle:150

Pre-Issue Buffer:

```

    Entry 0:
    Entry 1:

```

```

Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      2      0      1      0      1      -1      0
R08:  0      0     12      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=0
Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
Entry
1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000010>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,1000010000100000000000000000001100>]
Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
Entry
0: [(1,0,4)<101011010100011000000000010110000,1010000000100001111111111111111>]
Entry
1: [(1,1,5)<11111111111111111111111111111101,111111111111111111111111111111>]

Data
176:  -1     -2     -3      1     -1     -1     -1     -1
208:  -1      1     -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      3
-----
Cycle:151

Pre-Issue Buffer:
Entry 0:      [SLL    R10, R1, #2]
Entry 1:      [LW     R3, 176(R10)]
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers

```

R00:	0	2	0	1	0	1	-1	0
R08:	0	0	12	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000010&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;100010000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,1,5)&lt;11111111111111111111111111111101,11111111111111111111111111111111&gt;]

## Data

176:	-1	-2	-3	1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:152

## Pre-Issue Buffer:

Entry 0: [LW R3, 176(R10)]

Entry 1: [LW R4, 220(R10)]

Entry 2: [LW R5, 264(R0)]

Entry 3:

## Pre\_ALU Queue:

Entry 0: [SLL R10, R1, #2]

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	2	0	1	0	1	-1	0
R08:	0	0	12	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Data

176:	-1	-2	-3	1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:154

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R3, 176(R10)]

Entry 1: [LW R4, 220(R10)]

Post\_MEM Queue:

Entry 0: [LW R5, 264(R0)]

Registers

R00:	0	2	0	1	0	1	-1	0
R08:	0	0	8	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,100010000000000000000000000011100&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000010&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,10000100001000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;100000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,1,5)&lt;11111111111111111111111111111101,11111111111111111111111111111111&gt;]

Data

176:	-1	-2	-3	1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:155

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

```

Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:      [LW      R4, 220(R10)]
  Entry 1:
Post_MEM Queue:
  Entry 0:      [LW      R3, 176(R10)]

Registers
R00:  0      2      0      1      0      1      -1      0
R08:  0      0      8      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
  Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
  Entry
1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Set 1: LRU=1
  Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
  Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000010>]
Set 2: LRU=1
  Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
  Entry
1: [(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
  Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
  Entry
1: [(1,1,5)<11111111111111111111111111111101,1111111111111111111111111111111>]

Data
176:  -1      -2      -3      1      -1      -1      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:  0      0      0      0      0      0      1      3
-----
Cycle:156

Pre-Issue Buffer:
  Entry 0:
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:      [LW      R4, 220(R10)]
  Entry 1:
Post_MEM Queue:
  Entry 0:

Registers
R00:  0      2      0     -3      0      1      -1      0
R08:  0      0      8      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

```

Cache
Set 0: LRU=1
  Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
  Entry
1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Set 1: LRU=1
  Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
  Entry
1: [(1,1,8)<000000000000000000000000000000001,00000000000000000000000000000010>]
Set 2: LRU=1
  Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
  Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
  Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
  Entry
1: [(1,1,5)<11111111111111111111111111111101,11111111111111111111111111111111>]

```

```

Data
176:  -1    -2    -3     1     -1     -1     -1     -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     3
-----

```

Cycle:157

```

Pre-Issue Buffer:
  Entry 0:          [ADD    R6, R4, R5]
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:          [LW     R4, 220(R10)]

```

```

Registers
R00:  0     2     0    -3     0     1    -1     0
R08:  0     0     8     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=0
  Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
  Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=1
  Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
  Entry
1: [(1,1,8)<000000000000000000000000000000001,00000000000000000000000000000010>]
Set 2: LRU=0
  Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

```



Cycle:159

```

Pre-Issue Buffer:
    Entry 0:      [SW      R6, 176(R10)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:      [ADDI    R1, R1, #-1]
    Entry 1:
Post_ALU Queue:
    Entry 0:      [ADD     R6, R4, R5]
Pre_MEM Queue:
    Entry 0:
    Entry 1:
Post_MEM Queue:
    Entry 0:

```

## Registers

R00:	0	2	0	-3	0	1	-1	0
R08:	0	0	8	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

```

Set 0: LRU=0
    Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
    Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=1
    Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000010>]
Set 2: LRU=0
    Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
    Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
    Entry
0: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
    Entry
1: [(1,1,5)<1111111111111111111111111111101,1111111111111111111111111111>]

```

## Data

176:	-1	-2	-3	1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:160

```

Pre-Issue Buffer:
    Entry 0:      [SW      R1, 268(R0)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:      [ADDI    R1, R1, #-1]
Pre_MEM Queue:
    Entry 0:      [SW      R6, 176(R10)]
    Entry 1:

```

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	2	0	-3	0	1	1	0
R08:	0	0	8	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000010&gt;]

Set 2: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,10000100001000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=1

Entry

0: [(1,0,4)&lt;10101101010001100000000010110000,1010000000100001111111111111111&gt;]

Entry

1: [(1,1,5)&lt;1111111111111111111111111111101,1111111111111111111111111111111&gt;]

Data

176:	-1	-2	-3	1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:161

Pre-Issue Buffer:

Entry 0: [LW R1, 268(R0)]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [SW R1, 268(R0)]

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	1	0	-3	0	1	1	0
R08:	0	0	8	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

```

1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=1
  Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
  Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000010>]
Set 2: LRU=1
  Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
  Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
  Entry
0: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]
  Entry
1: [(1,1,5)<00000000000000000000000000000001,1111111111111111111111111111111>]

```

## Data

176:	-1	-2	-3	1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:162

## Pre-Issue Buffer:

```

Entry 0:
Entry 1:
Entry 2:
Entry 3:

```

## Pre\_ALU Queue:

```

Entry 0:
Entry 1:

```

## Post\_ALU Queue:

```

Entry 0:

```

## Pre\_MEM Queue:

```

Entry 0:      [LW      R1, 268(R0)]
Entry 1:

```

## Post\_MEM Queue:

```

Entry 0:

```

## Registers

R00:	0	1	0	-3	0	1	1	0
R08:	0	0	8	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,100010000000000000000000000011100&gt;]

Entry

1: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,0000000000000000000000000000001&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=0

Entry

0: [(1,0,4)&lt;10101101010001100000000010110000,1010000000100001111111111111111&gt;]

Entry  
1: [(1,1,5)<00000000000000000000000000000001,1111111111111111111111111111111>]

Data  
176:    -1       -2       -3       1       -1       -1       -1       -1  
208:    -1       1       -1       0       0       0       0       0  
240:    0       0       0       0       0       0       1       3

-----  
Cycle:163

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:            [LW       R1, 268(R0)]

Registers

R00:    0       1       0       -3       0       1       1       0  
R08:    0       0       8       0       0       0       0       0  
R16:    0       0       0       0       0       0       0       0  
R24:    0       0       0       0       0       0       0       0

Cache

Set 0: LRU=1

Entry

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

Entry

1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000001>]

Set 2: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

Entry

1: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]

Set 3: LRU=0

Entry

0: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Entry

1: [(1,1,5)<00000000000000000000000000000001,1111111111111111111111111111111>]

Data  
176:    -1       -2       -3       1       -1       -1       -1       -1  
208:    -1       1       -1       0       0       0       0       0  
240:    0       0       0       0       0       0       1       3

-----  
Cycle:164

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:

```

Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      1      0      -3      0      1      1      0
R08:  0      0      8      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000001>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=0
Entry
0: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]
Entry
1: [(1,1,5)<00000000000000000000000000000001,1111111111111111111111111111111>]

Data
176:  -1      -2      -3      1      -1      -1      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      3
-----
Cycle:165

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      1      0      -3      0      1      1      0

```

```

R08:  0      0      8      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,4)&lt;1000100000000000000000000000100110,10000000100001010011000000100000&gt;]

Set 3: LRU=0

Entry

0: [(1,0,4)&lt;10101101010001100000000010110000,1010000000100001111111111111111&gt;]

Entry

1: [(1,1,5)&lt;00000000000000000000000000000001,1111111111111111111111111111111&gt;]

## Data

```

176:  -1      -2      -3      1      -1      -1      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      3
-----

```

Cycle:166

## Pre-Issue Buffer:

Entry 0: [SLL R10, R1, #2]

Entry 1: [LW R3, 176(R10)]

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

```

R00:  0      1      0      -3      0      1      1      0
R08:  0      0      8      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

## Cache

Set 0: LRU=1

Entry

0: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Entry

1: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

```

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000001>]
Set 2: LRU=1
  Entry
0: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000001100>]
  Entry
1: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
  Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
  Entry
1: [(1,1,5)<000000000000000000000000000000001,11111111111111111111111111111111>]

```

```

Data
176:  -1    -2    -3     1     -1     -1     -1     -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     3
-----

```

Cycle:167

```

Pre-Issue Buffer:
  Entry 0:      [LW      R3, 176(R10)]
  Entry 1:
  Entry 2:
  Entry 3:
Pre_ALU Queue:
  Entry 0:      [SLL      R10, R1, #2]
  Entry 1:
Post_ALU Queue:
  Entry 0:
Pre_MEM Queue:
  Entry 0:
  Entry 1:
Post_MEM Queue:
  Entry 0:

```

```

Registers
R00:  0     1     0    -3     0     1     1     0
R08:  0     0     8     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=1
  Entry
0: [(1,0,5)<101011000000000010000000100001100,1000100000000000000000000000011100>]
  Entry
1: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Set 1: LRU=0
  Entry
0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
  Entry
1: [(1,1,8)<000000000000000000000000000000001,00000000000000000000000000000001>]
Set 2: LRU=1
  Entry
0: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000001100>]
  Entry
1: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
  Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
  Entry
1: [(1,1,5)<000000000000000000000000000000001,11111111111111111111111111111111>]

```

```

Data
176:  -1    -2    -3     1     -1     -1     -1     -1

```



```

208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      3
-----

```

Cycle:168

Pre-Issue Buffer:

```

Entry 0:      [LW      R3, 176(R10)]
Entry 1:      [LW      R4, 220(R10)]
Entry 2:      [LW      R5, 264(R0)]
Entry 3:

```

Pre\_ALU Queue:

```

Entry 0:
Entry 1:

```

Post\_ALU Queue:

```

Entry 0:      [SLL      R10, R1, #2]

```

Pre\_MEM Queue:

```

Entry 0:
Entry 1:

```

Post\_MEM Queue:

```

Entry 0:

```

Registers

```

R00:  0      1      0      -3      0      1      1      0
R08:  0      0      8      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

```

Cache

Set 0: LRU=0

Entry

```

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

```

Entry

```

1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

```

Set 1: LRU=0

Entry

```

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

```

Entry

```

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000001>]

```

Set 2: LRU=1

Entry

```

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

```

Entry

```

1: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]

```

Set 3: LRU=1

Entry

```

0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]

```

Entry

```

1: [(1,1,5)<00000000000000000000000000000001,11111111111111111111111111111111>]

```

Data

```

176:  -1      -2      -3      1      -1      -1      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      3
-----

```

Cycle:169

Pre-Issue Buffer:

```

Entry 0:      [LW      R5, 264(R0)]
Entry 1:
Entry 2:
Entry 3:

```

Pre\_ALU Queue:

```

Entry 0:
Entry 1:

```

Post\_ALU Queue:

```

Entry 0:
Pre_MEM Queue:
    Entry 0:      [LW      R3, 176(R10)]
    Entry 1:      [LW      R4, 220(R10)]
Post_MEM Queue:
    Entry 0:

Registers
R00:   0      1      0      -3      0      1      1      0
R08:   0      0      4      0      0      0      0      0
R16:   0      0      0      0      0      0      0      0
R24:   0      0      0      0      0      0      0      0

Cache
Set 0: LRU=0
    Entry
0: [(1,0,5)<1010110000000001000000100001100,100010000000000000000000000011100>]
    Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
    Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000001>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000100001100,1000010000100000000000000000001100>]
    Entry
1: [(1,0,4)<100010000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
    Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
    Entry
1: [(1,1,5)<00000000000000000000000000000001,11111111111111111111111111111111>]

Data
176:   -1      -2      -3      1      -1      -1      -1      -1
208:   -1      1      -1      0      0      0      0      0
240:    0      0      0      0      0      0      1      3
-----
Cycle:170

Pre-Issue Buffer:
    Entry 0:      [LW      R5, 264(R0)]
    Entry 1:
    Entry 2:
    Entry 3:
Pre_ALU Queue:
    Entry 0:
    Entry 1:
Post_ALU Queue:
    Entry 0:
Pre_MEM Queue:
    Entry 0:      [LW      R3, 176(R10)]
    Entry 1:      [LW      R4, 220(R10)]
Post_MEM Queue:
    Entry 0:

Registers
R00:   0      1      0      -3      0      1      1      0
R08:   0      0      4      0      0      0      0      0
R16:   0      0      0      0      0      0      0      0
R24:   0      0      0      0      0      0      0      0

Cache

```

```

Set 0: LRU=0
      Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
      Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
      Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000001>]
Set 2: LRU=1
      Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000000001100>]
      Entry
1: [(1,0,4)<1000100000000000000000000000000100110,10000000100001010011000000100000>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,1,5)<00000000000000000000000000000001,11111111111111111111111111111111>]

```

```

Data
176:  -1    -2    -3     1     -1     -1     -1     -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     3
-----

```

Cycle:171

Pre-Issue Buffer:

```

      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:

```

Pre\_ALU Queue:

```

      Entry 0:
      Entry 1:

```

Post\_ALU Queue:

```

      Entry 0:

```

Pre\_MEM Queue:

```

      Entry 0:      [LW      R4, 220(R10)]
      Entry 1:      [LW      R5, 264(R0)]

```

Post\_MEM Queue:

```

      Entry 0:      [LW      R3, 176(R10)]

```

Registers

```

R00:  0     1     0    -3     0     1     1     0
R08:  0     0     4     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

Cache

Set 0: LRU=0

Entry

```

0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

```

Entry

```

1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

```

Set 1: LRU=1

Entry

```

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

```

Entry

```

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000001>]

```

Set 2: LRU=0

Entry

```

0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000000001100>]

```

Entry

```

1: [(1,0,5)<11111111111111111111111111111111,11111111111111111111111111111110>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,1,5)<00000000000000000000000000000001,11111111111111111111111111111111>]

```

```

Data
176:  -1    -2    -3     1    -1    -1    -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     3
-----

```

Cycle:172

```

Pre-Issue Buffer:
      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:
Pre_ALU Queue:
      Entry 0:
      Entry 1:
Post_ALU Queue:
      Entry 0:
Pre_MEM Queue:
      Entry 0:      [LW      R4, 220(R10)]
      Entry 1:      [LW      R5, 264(R0)]
Post_MEM Queue:
      Entry 0:

```

```

Registers
R00:   0     1     0    -2     0     1     1     0
R08:   0     0     4     0     0     0     0     0
R16:   0     0     0     0     0     0     0     0
R24:   0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=0
      Entry
0: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000011100>]
      Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=1
      Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000001>]
Set 2: LRU=0
      Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
      Entry
1: [(1,0,5)<11111111111111111111111111111111,11111111111111111111111111111110>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,1,5)<00000000000000000000000000000001,11111111111111111111111111111111>]

```

```

Data
176:  -1    -2    -3     1    -1    -1    -1    -1
208:  -1     1    -1     0     0     0     0     0
240:   0     0     0     0     0     0     1     3
-----

```

Cycle:173

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [LW R5, 264(R0)]  
Entry 1:

Post\_MEM Queue:

Entry 0: [LW R4, 220(R10)]

Registers

R00:	0	1	0	-2	0	1	1	0
R08:	0	0	4	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=1

Entry

0: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Set 2: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,0,5)&lt;11111111111111111111111111111111,11111111111111111111111111111110&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,1,5)&lt;00000000000000000000000000000001,11111111111111111111111111111111&gt;]

Data

176:	-1	-2	-3	1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:174

Pre-Issue Buffer:

Entry 0: [ADD R6, R4, R5]  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0: [LW R5, 264(R0)]

## Registers

R00:	0	1	0	-2	0	1	1	0
R08:	0	0	4	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000001>]

Set 2: LRU=1

Entry

0: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]

Entry

1: [(1,0,5)<11111111111111111111111111111111,11111111111111111111111111111110>]

Set 3: LRU=1

Entry

0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]

Entry

1: [(1,1,5)<00000000000000000000000000000001,1111111111111111111111111111111>]

## Data

176:	-1	-2	-3	1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:175

## Pre-Issue Buffer:

Entry 0: [SW R6, 176(R10)]

Entry 1: [ADDI R1, R1, #-1]

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0: [ADD R6, R4, R5]

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	1	0	-2	0	1	1	0
R08:	0	0	4	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]

```

Set 1: LRU=0
      Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000001>]
Set 2: LRU=1
      Entry
0: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
      Entry
1: [(1,0,5)<11111111111111111111111111111111,11111111111111111111111111111110>]
Set 3: LRU=0
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    1    -1    -1    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    3
-----

```

Cycle:176

```

Pre-Issue Buffer:
      Entry 0:      [SW      R6, 176(R10)]
      Entry 1:
      Entry 2:
      Entry 3:
Pre_ALU Queue:
      Entry 0:      [ADDI    R1, R1, #-1]
      Entry 1:
Post_ALU Queue:
      Entry 0:      [ADD     R6, R4, R5]
Pre_MEM Queue:
      Entry 0:
      Entry 1:
Post_MEM Queue:
      Entry 0:

```

```

Registers
R00:  0    1    0    -2    0    1    1    0
R08:  0    0    4    0    0    0    0    0
R16:  0    0    0    0    0    0    0    0
R24:  0    0    0    0    0    0    0    0

```

```

Cache
Set 0: LRU=1
      Entry
0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
      Entry
1: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Set 1: LRU=0
      Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000001>]
Set 2: LRU=1
      Entry
0: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
      Entry
1: [(1,0,5)<11111111111111111111111111111111,11111111111111111111111111111110>]
Set 3: LRU=0
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry

```

1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Data								
176:	-1	-2	1	-1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:177

Pre-Issue Buffer:  
 Entry 0: [SW R1, 268(R0)]  
 Entry 1:  
 Entry 2:  
 Entry 3:

Pre\_ALU Queue:  
 Entry 0:  
 Entry 1:

Post\_ALU Queue:  
 Entry 0: [ADDI R1, R1, #-1]

Pre\_MEM Queue:  
 Entry 0: [SW R6, 176(R10)]  
 Entry 1:

Post\_MEM Queue:  
 Entry 0:

Registers								
R00:	0	1	0	-2	0	1	1	0
R08:	0	0	4	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache  
 Set 0: LRU=0  
 Entry  
 0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]  
 Entry  
 1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]  
 Set 1: LRU=0  
 Entry  
 0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]  
 Entry  
 1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000001>]  
 Set 2: LRU=1  
 Entry  
 0: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]  
 Entry  
 1: [(1,0,5)<11111111111111111111111111111111,11111111111111111111111111111110>]  
 Set 3: LRU=0  
 Entry  
 0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]  
 Entry  
 1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Data								
176:	-1	-2	1	-1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:178

Pre-Issue Buffer:  
 Entry 0:  
 Entry 1:  
 Entry 2:  
 Entry 3:



Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0: [SW R1, 268(R0)]

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	0	-2	0	1	1	0
R08:	0	0	4	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Set 2: LRU=0

Entry

0: [(1,0,4)&lt;100010000000000000000000000100110,10000000100001010011000000100000&gt;]

Entry

1: [(1,1,5)&lt;11111111111111111111111111111111,00000000000000000000000000000001&gt;]

Set 3: LRU=0

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;101011010100011000000000010110000,1010000000100001111111111111111&gt;]

Data

176:	-1	-2	1	-1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:179

Pre-Issue Buffer:

Entry 0: [LW R1, 268(R0)]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	0	-2	0	1	1	0
R08:	0	0	4	0	0	0	0	0

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Cache

Entry

Entry

LRU=0

$$, 4) < 10$$
$$, 8) < 00$$

Entry

Entry

LRU=0

$$, 3) < 10$$
$$, 4) < 10$$

```
208:      -1      1      -1      0      0      0      0      0
```

Cycle:180

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Entry 0:

Entry 1:

```
Entry 0:
```

Queue:

Entry 1:

M Queue:

Entry 0:

```
R00: 0
```

```
R08:      0      0      4      0      0      0      0      0
```

```
R16:      0      0      0      0      0      0      0      0
```

```
R24:      0      0      0      0      0      0      0      0
```

Set 0

Entry

$$, 7) < 00$$
$$, 5) < 10$$

LRU=0

$$, 4) < 10$$
$$, 8) < 00$$

---

```

Set 2: LRU=1
      Entry
0: [(1,0,3)<100011000000000010000000100001100,100001000010000000000000000000001100>]
      Entry
1: [(1,1,5)<11111111111111111111111111111111,000000000000000000000000000000001>]
Set 3: LRU=0
      Entry
0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1      -2      1      -1      -1      -1      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:   0      0      0      0      0      0      1      3
-----

```

Cycle:181

Pre-Issue Buffer:

```

      Entry 0:
      Entry 1:
      Entry 2:
      Entry 3:

```

Pre\_ALU Queue:

```

      Entry 0:
      Entry 1:

```

Post\_ALU Queue:

```

      Entry 0:

```

Pre\_MEM Queue:

```

      Entry 0:
      Entry 1:

```

Post\_MEM Queue:

```

      Entry 0:          [LW      R1, 268(R0)]

```

Registers

```

R00:   0      0      0      -2      0      1      1      0
R08:   0      0      4      0      0      0      0      0
R16:   0      0      0      0      0      0      0      0
R24:   0      0      0      0      0      0      0      0

```

Cache

Set 0: LRU=0

```

      Entry

```

```

0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

```

```

      Entry

```

```

1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]

```

Set 1: LRU=0

```

      Entry

```

```

0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]

```

```

      Entry

```

```

1: [(1,1,8)<000000000000000000000000000000001,00000000000000000000000000000000>]

```

Set 2: LRU=1

```

      Entry

```

```

0: [(1,0,3)<10001100000000010000000100001100,1000010000100000000000000000001100>]

```

```

      Entry

```

```

1: [(1,1,5)<11111111111111111111111111111111,00000000000000000000000000000001>]

```

Set 3: LRU=0

```

      Entry

```

```

0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]

```

```

      Entry

```

```

1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

Data

```

176:  -1      -2      1      -1      -1      -1      -1      -1
208:  -1      1      -1      0      0      0      0      0

```

240: 0 0 0 0 0 0 1 3

-----  
Cycle:182

Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00: 0 0 0 -2 0 1 1 0

R08: 0 0 4 0 0 0 0 0

R16: 0 0 0 0 0 0 0 0

R24: 0 0 0 0 0 0 0 0

Cache

Set 0: LRU=0

Entry

0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]

Entry

1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<000000000000000000000000000000001,00000000000000000000000000000000>]

Set 2: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

Entry

1: [(1,1,5)<11111111111111111111111111111111,00000000000000000000000000000001>]

Set 3: LRU=0

Entry

0: [(1,0,3)<100000000000000010101000010000000,10001101010000110000000010110000>]

Entry

1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

Data

176: -1 -2 1 -1 -1 -1 -1 -1

208: -1 1 -1 0 0 0 0 0

240: 0 0 0 0 0 0 1 3

-----  
Cycle:183

Pre-Issue Buffer:

Entry 0: [SLL R10, R1, #2]

Entry 1: [LW R3, 176(R10)]

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0:

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	0	-2	0	1	1	0
R08:	0	0	4	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,7)&lt;00000000000000000000000000000000,00000000000000000000000000000000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000000&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,1,5)&lt;11111111111111111111111111111111,00000000000000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,1010000000100001111111111111111&gt;]

Data

176:	-1	-2	1	-1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:184

Pre-Issue Buffer:

Entry 0: [LW R3, 176(R10)]

Entry 1:

Entry 2:

Entry 3:

Pre\_ALU Queue:

Entry 0: [SLL R10, R1, #2]

Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:

Entry 1:

Post\_MEM Queue:

Entry 0:

Registers

R00:	0	0	0	-2	0	1	1	0
R08:	0	0	4	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

```

Entry
0: [(1,0,7)<00000000000000000000000000000000,00000000000000000000000000000000>]
Entry
1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000000>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,1,5)<11111111111111111111111111111111,00000000000000000000000000000001>]
Set 3: LRU=1
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]

```

```

Data
176:  -1    -2    1    -1    -1    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    3
-----

```

Cycle:185

Pre-Issue Buffer:

```

Entry 0:      [LW      R3, 176(R10)]
Entry 1:      [LW      R4, 220(R10)]
Entry 2:      [LW      R5, 264(R0)]
Entry 3:

```

Pre\_ALU Queue:

```

Entry 0:
Entry 1:

```

Post\_ALU Queue:

```

Entry 0:      [SLL      R10, R1, #2]

```

Pre\_MEM Queue:

```

Entry 0:
Entry 1:

```

Post\_MEM Queue:

```

Entry 0:

```

Registers

```

R00:  0    0    0    -2    0    1    1    0
R08:  0    0    4    0    0    0    0    0
R16:  0    0    0    0    0    0    0    0
R24:  0    0    0    0    0    0    0    0

```

Cache

Set 0: LRU=1

Entry

```

0: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]

```

Entry

```

1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

```

Set 1: LRU=0

Entry

```

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

```

Entry

```

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000000>]

```

Set 2: LRU=1

Entry

```

0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]

```

Entry

```

1: [(1,1,5)<11111111111111111111111111111111,00000000000000000000000000000001>]

```

```
Set 3: LRU=1
      Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
```

```
Data
176:  -1    -2    1    -1    -1    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    3
-----
```

Cycle:186

```
Pre-Issue Buffer:
      Entry 0:      [LW      R5, 264(R0)]
      Entry 1:
      Entry 2:
      Entry 3:
Pre_ALU Queue:
      Entry 0:
      Entry 1:
Post_ALU Queue:
      Entry 0:
Pre_MEM Queue:
      Entry 0:      [LW      R3, 176(R10)]
      Entry 1:      [LW      R4, 220(R10)]
Post_MEM Queue:
      Entry 0:
```

```
Registers
R00:  0    0    0    -2    0    1    1    0
R08:  0    0    0    0    0    0    0    0
R16:  0    0    0    0    0    0    0    0
R24:  0    0    0    0    0    0    0    0
```

```
Cache
Set 0: LRU=1
      Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
      Entry
1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000011100>]
Set 1: LRU=1
      Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
      Entry
1: [(1,1,8)<00000000000000000000000000000001,000000000000000000000000000000>]
Set 2: LRU=1
      Entry
0: [(1,0,3)<10001100000000010000000100001100,10000100001000000000000000001100>]
      Entry
1: [(1,1,5)<11111111111111111111111111111111,00000000000000000000000000000001>]
Set 3: LRU=1
      Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
      Entry
1: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
```

```
Data
176:  -1    -2    1    -1    -1    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    3
-----
```

Cycle:187

```
Pre-Issue Buffer:
```

```

Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R4, 220(R10)]
Entry 1:      [LW      R5, 264(R0)]
Post_MEM Queue:
Entry 0:      [LW      R3, 176(R10)]

Registers
R00:  0      0      0      -2      0      1      1      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=1
Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
Entry
1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]
Set 1: LRU=1
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000000>]
Set 2: LRU=0
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,1,5)<11111111111111111111111111111111,00000000000000000000000000000001>]
Set 3: LRU=1
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]

Data
176:  -1      -2      1      -1      -1      -1      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:  0      0      0      0      0      0      1      3
-----
Cycle:188

Pre-Issue Buffer:
Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R4, 220(R10)]
Entry 1:      [LW      R5, 264(R0)]
Post_MEM Queue:
Entry 0:

```



## Registers

R00:	0	0	0	-1	0	1	1	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Set 1: LRU=1

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,00000000000000000000000000000000&gt;]

Set 2: LRU=0

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,100001000010000000000000000001100&gt;]

Entry

1: [(1,1,5)&lt;11111111111111111111111111111111,00000000000000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,3)&lt;10000000000000010101000010000000,10001101010000110000000010110000&gt;]

Entry

1: [(1,0,4)&lt;10101101010001100000000010110000,10100000001000011111111111111111&gt;]

## Data

176:	-1	-2	1	-1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:189

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [LW R5, 264(R0)]

Entry 1:

## Post\_MEM Queue:

Entry 0: [LW R4, 220(R10)]

## Registers

R00:	0	0	0	-1	0	1	1	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=1

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,1000100000000000000000000000011100&gt;]

Set 1: LRU=1

```

Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000000>]
Set 2: LRU=0
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,1,5)<11111111111111111111111111111111,00000000000000000000000000000001>]
Set 3: LRU=0
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

```

```

Data
176:  -1    -2    1    -1    -1    -1    -1    -1
208:  -1     1   -1     0     0     0     0     0
240:   0     0    0     0     0     0     1     3
-----

```

Cycle:190

```

Pre-Issue Buffer:
Entry 0:      [ADD    R6, R4, R5]
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:      [LW     R5, 264(R0)]

```

```

Registers
R00:  0     0     0    -1     0     1     1     0
R08:  0     0     0     0     0     0     0     0
R16:  0     0     0     0     0     0     0     0
R24:  0     0     0     0     0     0     0     0

```

```

Cache
Set 0: LRU=1
Entry
0: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
Entry
1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000000>]
Set 2: LRU=1
Entry
0: [(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]
Entry
1: [(1,1,5)<11111111111111111111111111111111,00000000000000000000000000000001>]
Set 3: LRU=0
Entry
0: [(1,0,3)<10000000000000010101000010000000,10001101010000110000000010110000>]
Entry
1: [(1,0,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

```

```
Data
176:  -1    -2    1    -1    -1    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    3
-----
```

Cycle:191

```
Pre-Issue Buffer:
    Entry 0:      [SW      R6, 176(R10)]
    Entry 1:      [ADDI    R1, R1, #-1]
    Entry 2:
    Entry 3:
```

```
Pre_ALU Queue:
    Entry 0:      [ADD     R6, R4, R5]
    Entry 1:
```

```
Post_ALU Queue:
    Entry 0:
```

```
Pre_MEM Queue:
    Entry 0:
    Entry 1:
```

```
Post_MEM Queue:
    Entry 0:
```

Registers

```
R00:   0    0    0    -1    0    1    1    0
R08:   0    0    0    0    0    0    0    0
R16:   0    0    0    0    0    0    0    0
R24:   0    0    0    0    0    0    0    0
```

Cache

Set 0: LRU=1

```
    Entry
0: [(1,0,4)<100011010100010000000000011011100,10001100000001010000000100001000>]
```

```
    Entry
1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
```

Set 1: LRU=0

```
    Entry
0: [(1,0,4)<100001000110000000000000000000010,10000000100001010011000000100010>]
```

```
    Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000000>]
```

Set 2: LRU=1

```
    Entry
0: [(1,0,4)<10001000000000000000000000000100110,10000000100001010011000000100000>]
```

```
    Entry
1: [(1,1,5)<11111111111111111111111111111111,00000000000000000000000000000001>]
```

Set 3: LRU=1

```
    Entry
0: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
```

```
    Entry
1: [(1,0,6)<11111111111111111111111111111111,00000000000000000000000000000000>]
```

```
Data
176:  -1    -2    1    -1    -1    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    3
-----
```

Cycle:192

```
Pre-Issue Buffer:
    Entry 0:      [SW      R6, 176(R10)]
    Entry 1:      [SW      R1, 268(R0)]
    Entry 2:
    Entry 3:
```

```
Pre_ALU Queue:
```

```

Entry 0:      [ADDI   R1, R1, #-1]
Entry 1:
Post_ALU Queue:
Entry 0:      [ADD    R6, R4, R5]
Pre_MEM Queue:
Entry 0:
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      0      0      -1      0      1      1      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0
R24:  0      0      0      0      0      0      0      0

Cache
Set 0: LRU=0
Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
Entry
1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000000>]
Set 2: LRU=1
Entry
0: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]
Entry
1: [(1,1,5)<11111111111111111111111111111111,00000000000000000000000000000001>]
Set 3: LRU=1
Entry
0: [(1,0,4)<10101101010001100000000010110000,1010000000100001111111111111111>]
Entry
1: [(1,0,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

Data
176:  -1      -2      1      -1      -1      -1      -1      -1
208:  -1      1      -1      0      0      0      0      0
240:  0      0      0      0      0      0      1      3
-----
Cycle:193

Pre-Issue Buffer:
Entry 0:      [SW      R1, 268(R0)]
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:      [ADDI   R1, R1, #-1]
Pre_MEM Queue:
Entry 0:      [SW      R6, 176(R10)]
Entry 1:
Post_MEM Queue:
Entry 0:

Registers
R00:  0      0      0      -1      0      1      1      0
R08:  0      0      0      0      0      0      0      0
R16:  0      0      0      0      0      0      0      0

```

R24: 0 0 0 0 0 0 0 0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]

Entry

1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000000>]

Set 2: LRU=1

Entry

0: [(1,0,4)<1000100000000000000000000000100110,10000000100001010011000000100000>]

Entry

1: [(1,1,5)<11111111111111111111111111111111,00000000000000000000000000000001>]

Set 3: LRU=1

Entry

0: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]

Entry

1: [(1,0,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

## Data

176: -1 -2 1 -1 -1 -1 -1 -1

208: -1 1 -1 0 0 0 0 0

240: 0 0 0 0 0 0 1 3

-----  
Cycle:194

## Pre-Issue Buffer:

Entry 0: [LW R1, 268(R0)]

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0: [SW R1, 268(R0)]

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00: 0 -1 0 -1 0 1 1 0

R08: 0 0 0 0 0 0 0 0

R16: 0 0 0 0 0 0 0 0

R24: 0 0 0 0 0 0 0 0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]

Entry

1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,00000000000000000000000000000000>]

Set 2: LRU=1

```

Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,1,5)<00000000000000000000000000000001,00000000000000000000000000000001>]
Set 3: LRU=1
Entry
0: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
Entry
1: [(1,0,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

```

```

Data
176:  -1    -2    1    -1    -1    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    3
-----

```

Cycle:195

Pre-Issue Buffer:

```

Entry 0:
Entry 1:
Entry 2:
Entry 3:
Pre_ALU Queue:
Entry 0:
Entry 1:
Post_ALU Queue:
Entry 0:
Pre_MEM Queue:
Entry 0:      [LW      R1, 268(R0)]
Entry 1:
Post_MEM Queue:
Entry 0:

```

```

Registers
R00:  0    -1    0    -1    0    1    1    0
R08:  0    0    0    0    0    0    0    0
R16:  0    0    0    0    0    0    0    0
R24:  0    0    0    0    0    0    0    0

```

Cache

```

Set 0: LRU=0
Entry
0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
Entry
1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000001100>]
Set 1: LRU=0
Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
Entry
1: [(1,1,8)<00000000000000000000000000000001,111111111111111111111111111111>]
Set 2: LRU=1
Entry
0: [(1,0,3)<10001100000000010000000100001100,100001000010000000000000000001100>]
Entry
1: [(1,1,5)<00000000000000000000000000000001,00000000000000000000000000000001>]
Set 3: LRU=1
Entry
0: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
Entry
1: [(1,0,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

```

```

Data
176:  -1    -2    1    -1    -1    -1    -1    -1
208:  -1    1    -1    0    0    0    0    0
240:   0    0    0    0    0    0    1    3

```

-----  
Cycle:196

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:

Post\_MEM Queue:

Entry 0: [LW R1, 268(R0)]

Registers

R00:	0	-1	0	-1	0	1	1	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

Cache

Set 0: LRU=0

Entry

0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]

Entry

1: [(1,0,5)<10101100000000010000000100001100,100010000000000000000000000011100>]

Set 1: LRU=0

Entry

0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]

Entry

1: [(1,1,8)<00000000000000000000000000000001,11111111111111111111111111111111>]

Set 2: LRU=1

Entry

0: [(1,0,3)<10001100000000010000000100001100,1000010000100000000000000000001100>]

Entry

1: [(1,1,5)<00000000000000000000000000000001,00000000000000000000000000000001>]

Set 3: LRU=1

Entry

0: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]

Entry

1: [(1,0,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

Data

176:	-1	-2	1	-1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:197

Pre-Issue Buffer:

Entry 0:  
Entry 1:  
Entry 2:  
Entry 3:

Pre\_ALU Queue:

Entry 0:  
Entry 1:

Post\_ALU Queue:

Entry 0:

Pre\_MEM Queue:

Entry 0:  
Entry 1:  
Post\_MEM Queue:  
Entry 0:

## Registers

R00:	0	-1	0	-1	0	1	1	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry

0: [(1,0,4)&lt;10001101010001000000000011011100,10001100000001010000000100001000&gt;]

Entry

1: [(1,0,5)&lt;10101100000000010000000100001100,100010000000000000000000000011100&gt;]

Set 1: LRU=0

Entry

0: [(1,0,4)&lt;10000100011000000000000000000010,10000000100001010011000000100010&gt;]

Entry

1: [(1,1,8)&lt;00000000000000000000000000000001,1111111111111111111111111111111&gt;]

Set 2: LRU=1

Entry

0: [(1,0,3)&lt;10001100000000010000000100001100,1000010000100000000000000000001100&gt;]

Entry

1: [(1,1,5)&lt;00000000000000000000000000000001,00000000000000000000000000000001&gt;]

Set 3: LRU=1

Entry

0: [(1,0,4)&lt;10101101010001100000000010110000,1010000000100001111111111111111&gt;]

Entry

1: [(1,0,6)&lt;11111111111111111111111111111111,00000000000000000000000000000000&gt;]

## Data

176:	-1	-2	1	-1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:198

## Pre-Issue Buffer:

Entry 0:

Entry 1:

Entry 2:

Entry 3:

## Pre\_ALU Queue:

Entry 0:

Entry 1:

## Post\_ALU Queue:

Entry 0:

## Pre\_MEM Queue:

Entry 0:

Entry 1:

## Post\_MEM Queue:

Entry 0:

## Registers

R00:	0	-1	0	-1	0	1	1	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

Entry



```

0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]
    Entry
1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]
Set 1: LRU=0
    Entry
0: [(1,0,4)<10000100011000000000000000000010,10000000100001010011000000100010>]
    Entry
1: [(1,1,8)<00000000000000000000000000000001,11111111111111111111111111111111>]
Set 2: LRU=1
    Entry
0: [(1,0,3)<10001100000000010000000100001100,1000010000100000000000000000001100>]
    Entry
1: [(1,1,5)<00000000000000000000000000000001,00000000000000000000000000000001>]
Set 3: LRU=1
    Entry
0: [(1,0,4)<10101101010001100000000010110000,10100000001000011111111111111111>]
    Entry
1: [(1,0,6)<11111111111111111111111111111111,00000000000000000000000000000000>]

```

## Data

176:	-1	-2	1	-1	-1	-1	-1	-1
208:	-1	1	-1	0	0	0	0	0
240:	0	0	0	0	0	0	1	3

-----  
Cycle:199

## Pre-Issue Buffer:

```

    Entry 0:
    Entry 1:
    Entry 2:
    Entry 3:

```

## Pre\_ALU Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_ALU Queue:

```

    Entry 0:

```

## Pre\_MEM Queue:

```

    Entry 0:
    Entry 1:

```

## Post\_MEM Queue:

```

    Entry 0:

```

## Registers

R00:	0	-1	0	-1	0	1	1	0
R08:	0	0	0	0	0	0	0	0
R16:	0	0	0	0	0	0	0	0
R24:	0	0	0	0	0	0	0	0

## Cache

Set 0: LRU=0

```

    Entry

```

```

0: [(1,0,4)<10001101010001000000000011011100,10001100000001010000000100001000>]

```

```

    Entry

```

```

1: [(1,0,5)<10101100000000010000000100001100,1000100000000000000000000000011100>]

```

Set 1: LRU=1

```

    Entry

```

```

0: [(1,0,5)<00000000000000000000000000000000,1000000000000000000000000000001101>]

```

```

    Entry

```

```

1: [(1,0,8)<00000000000000000000000000000001,11111111111111111111111111111111>]

```

Set 2: LRU=1

```

    Entry

```

```

0: [(1,0,3)<10001100000000010000000100001100,1000010000100000000000000000001100>]

```

```

    Entry

```

```

1: [(1,0,5)<00000000000000000000000000000001,00000000000000000000000000000001>]

```

Set 3: LRU=1

```
Entry
0: [(1,0,4)<10101101010001100000000010110000,101000000010000111111111111111>]
Entry
1: [(1,0,6)<1111111111111111111111111111,00000000000000000000000000000000>]

Data
176:  1      1      1      -1      -1      -1      -1      -1
208: -1      1     -1      0      0      0      0      0
240:  0      0      0      0      0      0      1     -1
```