[CS M51A F14] Homework 6

Due: Friday 12/12/2014

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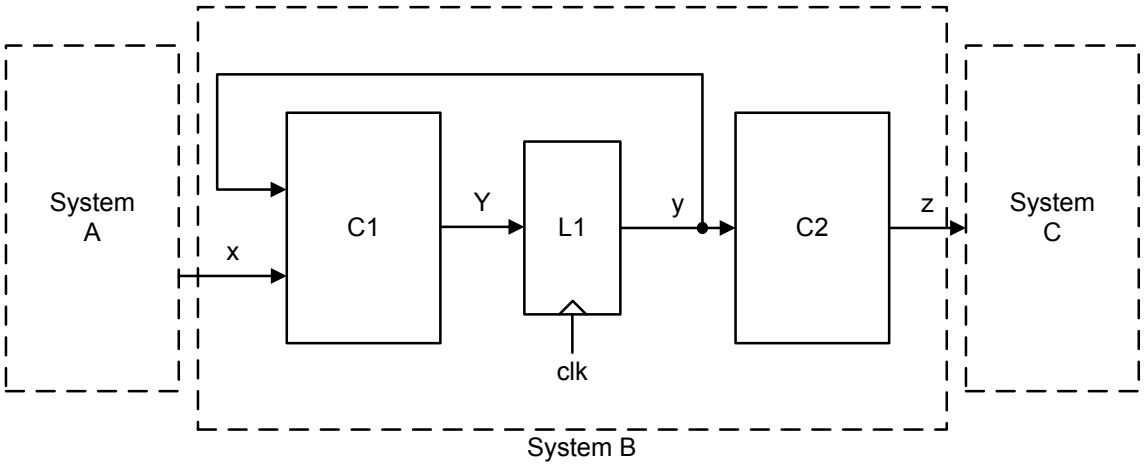
Homework Problems (30 points total)

Exercises

From the book: 9.5, 9.15, 10.7, 10.11, 11.11, 11.13

Problem 1 (6 points)

We would like to analyze the timing required for the following sequential system. All registers in the system are positive edge triggered flip-flops. Propagation delays of all registers are equal at $t_p = 1.5$ ns, and setup times for all registers are also fixed at $t_{su} = 0.4$ ns.



For System A, the delay from the output of the state register to signal x is $d2_A = 2.5$ ns.

For System B, the delay with respect to input x is $d1^x = 3.5$ ns, the delay with respect to state register value y is $d1^y = 4.5$ ns, and the delay of the output combinational logic is $d2_B = 2.5$ ns.

For System C, the delay for signal z to reach the state register of System C is $d1^z = 2.7$ ns.

1. Assume no clock skew for the three systems. What is the minimum clock period required in regard to signal x?
2. What is the minimum clock period required in regard to signal y?
3. What is the minimum clock period required in regard to signal z?
4. Considering all the three previous values, what is the minimum clock period required for the whole system?

5. Now, increased distance between the three systems has caused clock skew, and we need to take it into consideration. System C is the closest to the clock source, and the clock arrives at System C the fastest. The clock arrives at System B 0.3 ns later than it arrives at System C, and it arrives at System A 0.6 ns later than System C.

   Of the three clock periods related to signals x, y and z, calculate the adjusted minimum clock period of the affected signals. Also, what is the minimum clock period for the whole system with clock skew?

Problem 2 (6 points)

Complete the following table for the given representations in each part.

	Signed integer x (in decimal)	Representation x_R (in decimal)	Bit-vector $\underline{x}$
a	-25		
b		37	
c			110110

The 'Signed integer' column shows the actual value of the signed integer, and the 'Representation' column holds the value of the bit-vector representation. Assume that any bit vector that is shorter than the given bit length has leading 0s.

1. Two's complement, $n = 7$ bits
2. Two's complement, $n = 6$ bits
3. Ones' complement, $n = 6$ bits

Problem 3 (6 points)

We would like to identify the working signals of an arithmetic unit at work, namely the two's-complement arithmetic unit shown in the textbook at Figure 10.12 (page 297). For the system, fill in the table below according to the given computation in each part. c_0, K_x and K_y are control signals, and z, c_{out}, ovf, $zero$ and sgn are result signals.

1. $z = x + y$

x	y	c_0	K_x	K_y	z	c_{out}	ovf	$zero$	sgn
00000000	00000000								
10101010	10100101								
10110110	00110011								

2. $z = x - y$

x	y	c_0	K_x	K_y	z	c_{out}	ovf	$zero$	sgn
00100010	00100010								
10010010	01000011								
00010011	00110011								

Problem 4 (6 points)

Using a modulo-16 binary counter with parallel inputs explained in the textbook (p. 321) along with logic gates, we would like to implement the following counters.

For each design, minimize the gate logic for the input signals and load signal as much as possible using K-maps.

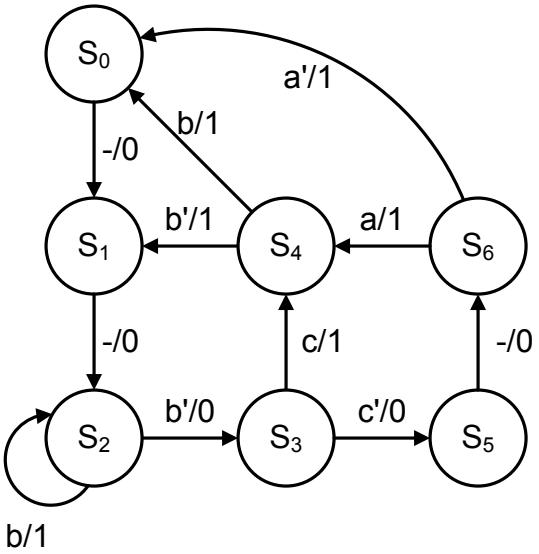
1. A modulo-10 counter.

2. A 5-to-14 counter.

3. A counter which counts in the following sequence: 0, 1, 2, 3, 4, 8, 9, 10, 13, 14, 15

Problem 5 (6 points)

Implement a sequential system using the standard modulo-16 binary counter with parallel input. The system has three binary inputs a, b, c and one binary output z. The transition and the output functions are specified by the state diagram shown below.



1. Setting $LD = CNT'$, obtain the expression for the input CNT in terms of states (S_0 to S_6) and input signals.

2. Find all load input combinations that we need for this system. For each combination, write the input conditions in terms of states (S_0 to S_6) and input signals. Simplify the conditions as much as possible.

3. Using K-maps, obtain the minimal expressions for I_3 to I_0 and the output z, in terms of counter outputs (Q_3 to Q_0) and input signals.