Chapter 3 (September 24, 2003)

Exercise 3.1 (a) logic values

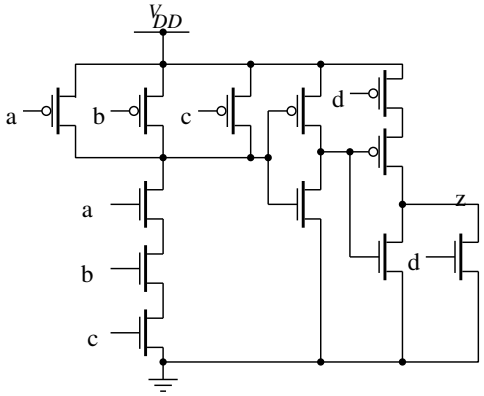
Voltage (V)	Positive Logic	Negative Logic
1.0	0	1
4.5	1	0
2.0	undefined	undefined
-1.0	undefined	undefined

(b) module has the following behavior (voltage levels):

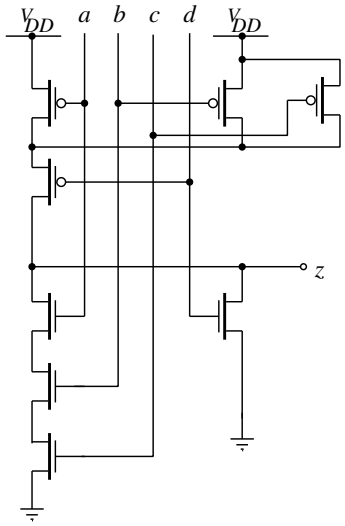
			Positive Logic			Negative Logic		
x_1	x_0	z	x_1	x_0	z	x_1	x_0	z
0.3	0.2	0.5	0	0	0	1	1	1
0.3	4.5	4.4	0	1	1	1	0	0
4.5	0.2	4.4	1	0	1	0	1	0
4.5	4.5	0.2	1	1	0	0	0	1

For positive logic, the module is a XOR gate. $z = x_0 \oplus x_1$.
For negative logic, the module is a XNOR gate. $z = (x_0 \oplus x_1)'$.

Exercise 3.3 The network on Figure 3.21 of the book corresponds to the expression: $(abc+d)'$. This function is implemented using AND and NOR circuits and also complex gates approach as shown in Figure 3.1.



(a) using AND and NOR circuits



(b) using complex gate approach

Figure 3.1: Function $(abc + d)'$ – Exercise 3.3

Exercise 3.5 The circuit is similar to the one presented as an example for a transmission gate (Figure 3.8 of the textbook).

When $s = 1$, the transmission gate in the bottom is *ON* and the transmission gate at the top is *OFF*. When $s = 0$, the opposite happens. So, a switching expression for the circuit is:

$$z = b.s + a.s'$$

Exercise 3.7 Based on the figure, and knowing that the propagation delay is measured based on 50% of the voltage level transition (input to output), the propagation delay time is:

$$\begin{aligned} t_{pHL}(\text{NOR}) &= 4.5ns \\ t_{pLH}(\text{NOR}) &= 4.0ns \end{aligned}$$

Exercise 3.9 (a) For a load factor of $L = 70$ the propagation delays are:

$$\begin{aligned} t_{pHL} &= 0.43 + 0.15 * 70 = 10.93ns \\ t_{pLH} &= 0.35 + 0.25 * 70 = 17.85ns \end{aligned}$$

(b) Using a buffer with load factor of 2 and propagation time given by $t_{pHL}(\text{buffer}) = t_{pLH}(\text{buffer}) = 0.6 + 0.02L(ns)$, the network consisting of a gate followed by the buffer has a delay:

$$\begin{aligned} t_{pHL}(\text{gate\&buffer}) &= 0.43 + 0.15 * 2 + 0.6 + 0.02 * 70 = 2.73ns \\ t_{pLH}(\text{gate\&buffer}) &= 0.35 + 0.25 * 2 + 0.6 + 0.02 * 70 = 2.85ns \end{aligned}$$

(c) using two buffers we get:

$$\begin{aligned} t_{pHL}(\text{gate\&2-buffers}) &= 0.43 + 0.15 * 4 + 0.6 + 0.02 * 35 = 2.33ns \\ t_{pLH}(\text{gate\&2-buffers}) &= 0.35 + 0.25 * 4 + 0.6 + 0.02 * 35 = 2.65ns \end{aligned}$$

(d) Optimum number of buffers can be obtained by the generalization of the delay equation, considering n as the number of buffers:

$$\begin{aligned} t_{pHL}(\text{gate\&n-buffers}) &= 0.43 + 0.15 * 2n + 0.6 + 0.02 * \lceil 70/n \rceil = 1.03 + 0.3n + 0.02 * \lceil 70/n \rceil \\ t_{pLH}(\text{gate\&n-buffers}) &= 0.35 + 0.25 * 2n + 0.6 + 0.02 * \lceil 70/n \rceil = 0.95 + 0.5n + 0.02 * \lceil 70/n \rceil \end{aligned}$$

The function has a minimum. We can see that for $n = 3$, the delays increase to $t_{pHL} = 2.41$ and $t_{pLH} = 2.93$, when compared to delays for $n = 2$. So, the best number of buffers is 2, and the load should be distributed in only 2 sets.

Exercise 3.11 Noise margins are defined as:

$$V_{Hmin}(OUT) - V_{Hmin}(IN)$$

and

$$V_{Lmax}(OUT) - V_{Lmax}(IN)$$

Based on the values

$$\begin{aligned} e \leq V_H(OUT) \leq f, \\ a \leq V_H(IN) \leq b, \\ g \leq V_L(OUT) \leq h, \\ c \leq V_L(IN) \leq d \end{aligned}$$

we obtain the noise margins:

$$V_{Hmin}(OUT) - V_{Hmin}(IN) = e - a$$

and

$$V_{Lmax}(OUT) - V_{Lmax}(IN) = h - d$$