[CS M51A F14] Solution to Quiz 2

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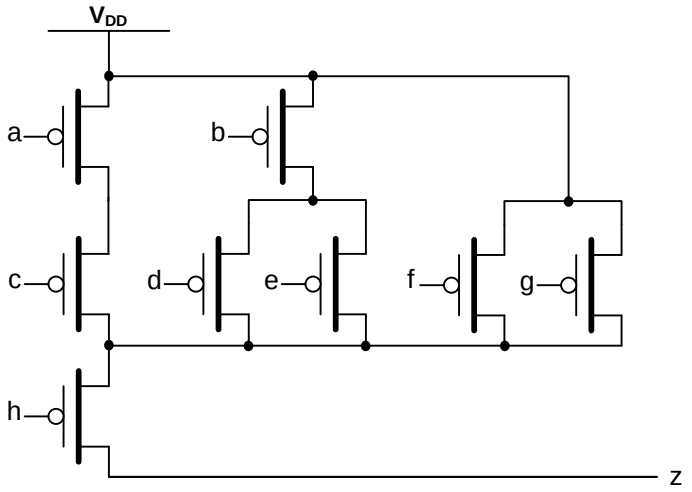
Quiz Problems (50 points total)

Problem 1 (20 points)

The following pull-up network is part of a complex CMOS gate that we wish to implement.



1. **(10 points)** Write the expression for the pull-up network. From this, derive the expression for the pull-down network using switching algebra. Make sure the inverts are on the correct variables.

   Solution From the given network we can directly write for the pull-up network

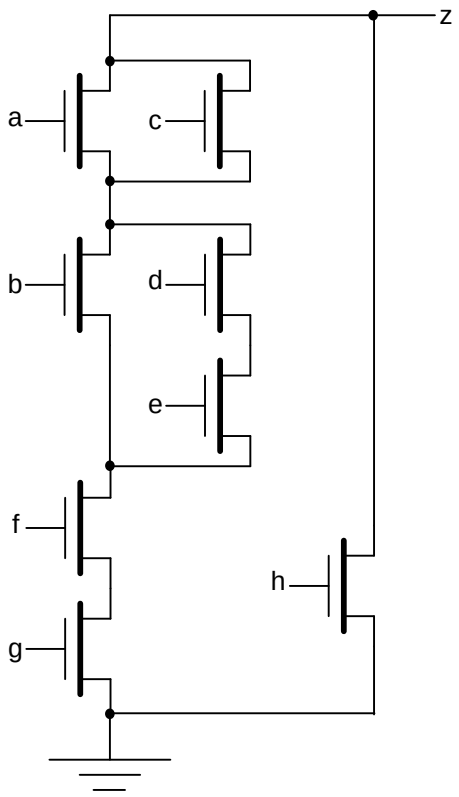
   $$z = (a'c' + b'(d' + e') + (f' + g'))h'$$

   Therefore, the expression for the pull-down network is

   $$\begin{aligned} z' &= \left[(a'c' + b'(d' + e') + (f' + g'))h'\right]' \\ &= (a'c' + b'(d' + e') + (f' + g'))' + h \\ &= (a + c)(b + (d' + e')')fg + h \\ &= (a + c)(b + de)fg + h \end{aligned}$$

2. **(10 points)** Draw the pull-down network of NMOS transistors that correspond to the expression and completes the CMOS gate that drives output z. To keep it minimal, only use one NMOS transistor for each input variable.

Solution Using the expression for z', we can create the circuit as shown.

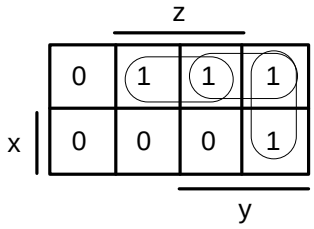


Problem 2 (10 points)

Answer the following questions on the given switching expression.

$$E(x, y, z) = \sum m(1, 2, 3, 6)$$

1. **(5 points)** Using K-maps, find all the prime implicants for $E(x, y, z)$.
   Solution

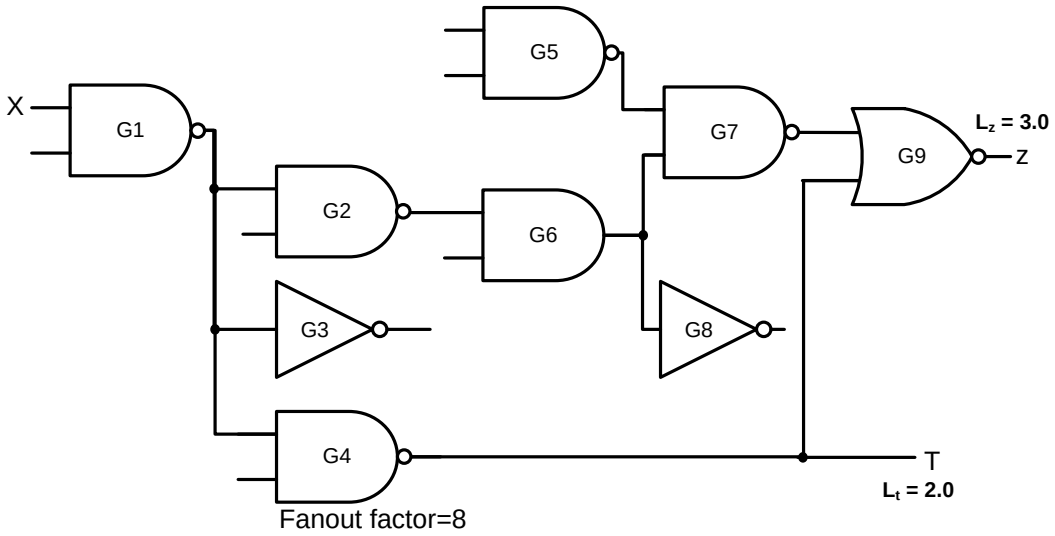


   The equivalent product terms are x'z, x'y, and yz'.

2. **(5 points)** Which of these prime implicants are **not** essential?
   Solution x'y does not have any squares that it covers alone, therefore it is not essential.

Problem 3 (20 points)

Given the circuit shown below,



show the items below for the worst case path.

The necessary gate characteristics are listed in the following table.

Gate Type	Fan-in	Propagation Delays (ns) t_{pLH}	Propagation Delays (ns) t_{pHL}	Load Factor I
AND	2	$0.20 + 0.038L$	$0.18 + 0.018L$	1.0
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$	1.0
NAND	2	$0.05 + 0.038L$	$0.08 + 0.027L$	1.0
NOR	2	$0.06 + 0.075L$	$0.07 + 0.016L$	1.0

1. **(20 points)** For $t_{pLH}(x \to z)$, fill in the blanks with the appropriate information. For the Delay section, write down the equation from the table with the proper L value shown. You do not need to obtain the final delay value for full credit.

   Solution Looking at the circuit, we can get:

   Gate type: G1: NAND2 → G2: NAND2 → G6: AND2 → G7: NAND2 → G9: NOR2

   & fan-in LH / HL: G1: HL → G2: LH → G6: LH → G7: HL → G9: LH

   Total load: G1: 3 → G2: 1 → G6: 2 → G7: 1 → G9: 3

   Delay: G1: $0.08 + 0.027 \times 3$ → G2: $0.05 + 0.038 \times 1$ → G6: $0.20 + 0.038 \times 2$ → G7: $0.08 + 0.027 \times 1$ → G9: $0.06 + 0.075 \times 3$