[CS M51A Fall 14] Assignment 1

Due: 10/17/14

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Rules of Engagement: Homework problems must be submitted on the specified due date in discussion. Please write legibly and follow directions.

Homework Problems (70 points total)

Problem 1 (10 points)

Find x and y such that the following conditions are satisfied and show all the steps of your work.

1. $(EC76)_{16} = (x)_8$
2. $(465)_7 + (383)_9 = (y)_{11}$

Problem 2 (10 points)

Show that the following holds using the postulates of Boolean algebra.

1. $x'y'z' + x'y'z + x'yz + xy'z + xyz = x'y' + z$
2. $xy' + xzw + yw = xy' + yw$

Problem 3 (10 points)

We would like to convert the given switching expression into the specified form.

$$E(x_3, x_2, x_1, x_0) = (((x_3 + x_2 + x_2'x_1')x_1 + x_0)' + x_3x_2')'$$

1. Convert the given expression into a simplified sum of products form.
2. Convert the sum of products form into a sum of minterms form.

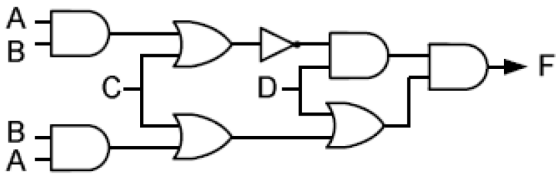
Problem 4 (10 points)

Convert the following truth table to a switching expression (Boolean Algebra) and simplify the expression as much as possible.

x	y	z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Problem 5 (10 points)

For the following diagrams, give the simplified POS expressions and show the corresponding two-level gate network.



Problem 6 (20 points)

Your goal is to design a module which adds two digits x and y belonging to the set $\{-1, 0, 1\}$ to produce an output in the set $\{-2, -1, 0, 1, 2\}$. The inputs x and y are encoded via two bits, $x_p x_n$ and $y_p y_n$ with values given by $x_p - x_n$ (i.e. setting $x_p = 0$ and $x_n = 1$ encodes -1, with zero having two possible encodings 00 and 11). The outputs are encoded via three bits z_s, z_1, z_0, whose value is interpreted via $(-1)^{z_s}(2\, z_1 + z_0)$.

1. Write the switching functions for the three output bits z_s, z_1, z_0 in tabular form.
2. Obtain the minterm expressions (in m-notation) of z_s, z_1 and z_0 respectively.
3. Obtain the maxterm expressions (in M-notation) of z_s, z_1 and z_0 respectively.
4. Does any of the switching functions have a dc-set? If so, which one?
5. Implement z_1 as a two-level AND-OR gate network. Note that NOT gates do not count as the two levels, so include them as needed.