[CS M51A W13] Solutions for Midterm exam

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Problem 1 (10 points)

The following questions are based on the function shown here.

$$f(x,y,z) = (xy + z')(x' + y)$$

1. **(5 points)** Obtain the minimal sum of products form for $f(x,y,z)$ using the identities of Boolean algebra (shown on page 14). Show all the steps in your derivation.

   Solution

$$\begin{aligned} f(x,y,z) &= (xy + z')(x' + y) \\ &= xx'y + x'z' + xyy + yz' \\ &= x'z' + xy + yz' \\ &= x'z' + xy + (x + x')yz' \\ &= x'z' + xy + xyz' + x'yz' \\ &= x'z'(1 + y) + xy(1 + z') \\ &= x'z' + xy \end{aligned}$$

2. **(5 points)** Due to the characteristics of the system, the inputs x and z will never be both 1 at the same time.

   Write the zero-set, one-set and dc-set for $f(x,y,z)$.

   Solution Since x and z will never be 1 at the same time, $f(1,0,1)$ and $f(1,1,1)$ are don't-cares. The function in tabular form is shown:

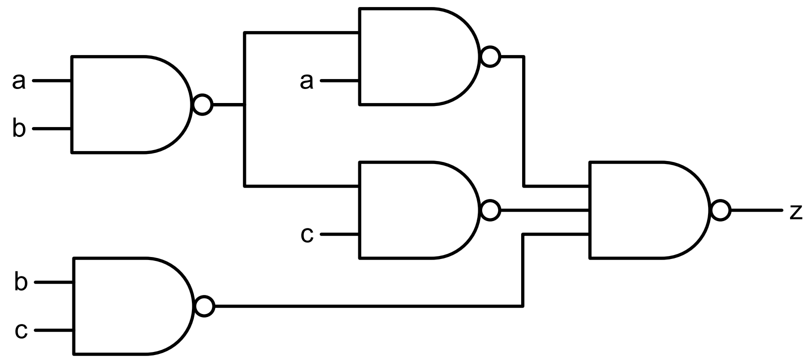
	x	y	z	$f(x,y,z)$
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	–
6	1	1	0	1
7	1	1	1	–

   So the sets will be:

   zero-set (1,3,4), one-set (0,2,6), dc-set (5,7)

Problem 2 (11 points)

The set {NOR} is a universal set and thus, any combinational network can be implemented using only NOR gates. Convert the following network of NAND gates into a NOR network by following the steps given below.



1. **(6 points)** Obtain the minimal product of sums form for z using network analysis and identities. Show all steps.

   Solution From the circuit, we can obtain:

$$\begin{aligned}
z &= \left[((ab)'a)' \cdot ((ab)'c)' \cdot (bc)'\right]' \\
&= (ab)'a + (ab)'c + bc \\
&= (a' + b')a + (a' + b')c + bc \\
&= aa' + ab' + a'c + b'c + bc \\
&= ab' + a'c + b'c + bc \\
&= ab' + c(a' + b' + b) \\
&= ab' + c(a' + 1) \\
&= ab' + c \\
&= (a + c)(b' + c)
\end{aligned}$$

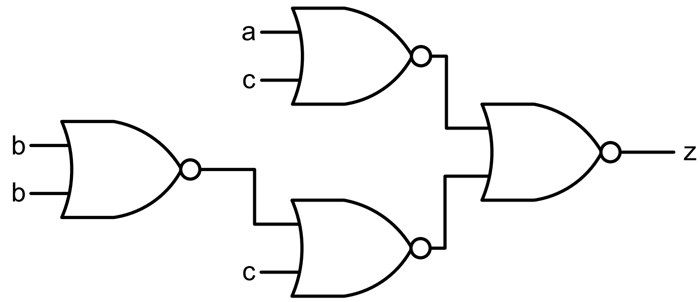
2. **(5 points)** Using the expression obtained from the previous step, obtain the NOR network that uses **ONLY** NOR gates. Inverted inputs are not available, and no constant inputs are allowed. (*Hint: A product of sums form can be converted into a NOR operation by using DeMorgan's Law, where* $(\cdots)(\cdots) = [(\cdots)' + (\cdots)']'$.)

   Which of the following circuits is the correct NOR network?

   Solution Using DeMorgan's Law, we can write:

$$\begin{aligned}
z &= (a + c)(b' + c) \\
&= \left[(a + c)' + (b' + c)'\right]' \\
&= \left[(a + c)' + ((b + b)' + c)'\right]' \\
&= \mathrm{NOR}\left[\mathrm{NOR}(a, c), \mathrm{NOR}(\mathrm{NOR}(b, b), c)\right]
\end{aligned}$$

   Converting this into a circuit, we get:



This is equivalent to (c).

Problem 3 (15 points)

Given the following simplification of a boolean expression, answer the following.

$$
\begin{aligned}
E_1(a,b,c,d) &= ((ab'+c')(b'+c)+b+cd)' && (1)\\
&= ((ab'+c')(b'+c))'(b+cd)' && (2)\\
&= ((ab'+c')(b'+c))'(b'c'+d') && (3)\\
&= ((ab'+c')'+(b'+c)')(b'c'+d') && (4)\\
&= ((a'+bc)+(bc'))(b'c'+d') && (5)\\
&= (a'+bc+bc')(b'c'+d') && (6)\\
&= (a'+b(c+c'))(b'c'+d') && (7)\\
&= (a'+b(0))(b'c'+d') && (8)\\
&= a'(b'c'+d') && (9)\\
&= a'b'c'+ad' && (10)
\end{aligned}
$$

1. **(6 points)** There is **at least one** error in the simplifying process. Find all wrong steps and briefly explain what is wrong for each error.

   (For example, (11)→(12), wrong application of the Identity rule)

   Solution The wrong steps are

   (2)→(3) (wrong application of DeMorgan's Law)

   (4)→(5) (wrong application of DeMorgan's Law)

   (7)→(8) ($c+c'$ should be 1 not 0)

   (9)→(10) (missing invert sign at ad', should be $a'd'$)

2. **(9 points)** Given that $E_2(a,b,c,d) = a'(d'(abd+b'c+a'd)+((a'+c')(a'+b'+cd))'+ac'd')$, which of the following switching expressions represents the function corresponding to the expression $E_1(a,b,c,d) + {E_2}'(a,b,c,d)$?

Solution The correct simplification for each expression is shown below.

$$
\begin{aligned}
E_1(a,b,c,d) &= ((ab'+c')(b'+c)+b+cd)' \\
&= ((ab'+c')(b'+c))'(b+cd)' \\
&= ((ab'+c')'+(b'+c)')b'(cd)' \\
&= ((ab')'c+bc')b'(c'+d') \\
&= ((a'+b)c+bc')b'(c'+d') \\
&= (a'c+bc+bc')b'(c'+d') \\
&= (a'c+b(c+c'))b'(c'+d') \\
&= (a'c+b)b'(c'+d') \\
&= (a'b'c+bb')(c'+d') \\
&= a'b'c(c'+d') \\
&= a'b'cc'+a'b'cd' \\
&= a'b'cd'
\end{aligned}
$$

For long expressions such as E_2, one should simplify it as much as possible before applying DeMorgan's law on it (for the invert). So we work to simplify E_2 first. Luckily, there are a lot of terms that we can remove here.

$$
\begin{aligned}
E_2(a,b,c,d) &= a'(d'(abd+b'c+a'd)+((a'+c')(a'+b'+cd))'+ac'd') \\
&= a'((abdd'+b'cd'+a'dd')+(a'+c')'+(a'+b'+cd)'+ac'd') \\
&= a'((b'cd')+ac+(ab(cd)')+ac'd') \\
&= a'b'cd'+aa'c+aa'b(cd)'+aa'c'd' \\
&= a'b'cd' \\
&= E_1
\end{aligned}
$$

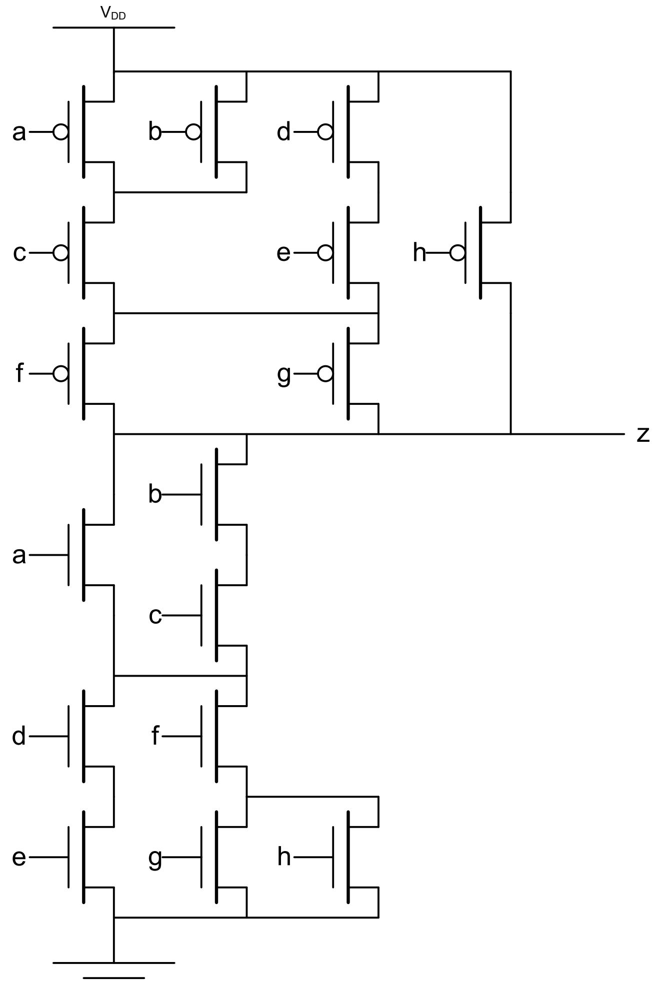
Therefore,

$$E_1(a,b,c,d)+{E_2}'(a,b,c,d) = E_1+{E_1}' = 1$$

This is equal to (a).

Problem 4 (13 points)

Answer the following questions on the given CMOS complex gate.



1. **(3 points)** There is a problem with this complex gate. When $f = 0$, $g = 0$ and $h = 1$, there exists at least one combination of signals that activates both the pull-up and pull-down networks and forms a direct path from V_{DD} to ground. Show any single combination of values that makes this happen.

   Solution For the pull-up network:

$$z = ((a' + b')c' + d'e')(f' + g') + h'$$

   For the pull-down network:

$$z' = (a + bc)(de + f(g + h))$$

   For a direct path to form from V_{DD} to ground, both networks need to be connected.

   With $f = 0$, $de = 1$ otherwise the pull-down network would be inactive. Therefore $d = e = 1$. This in turn implies $c = 0$ as this is the last possible path that can be active and connect z to V_{DD}. This cuts off the right path in the top part of the pull-down network, and $a = 1$. $b = 0$ to finalize the path in the pull-up network.

   The resulting signal values are: $a = 1$, $b = 0$, $c = 0$, $d = 1$ and $e = 1$.

2. **(5 points)** Assuming that the pull-up network has the correct functionality that we want, obtain the expression for the corresponding pull-down network. Show all your work. Which one of the following is the expression equivalent to? (each letter in the diagram stands for an NMOS transistor)

Solution

$$\begin{aligned}
z &= ((a'+b')c'+d'e')(f'+g')+h' \\
z' &= \left[((a'+b')c'+d'e')(f'+g')+h'\right]' \\
&= \left[((a'+b')c'+d'e')(f'+g')\right]' h \\
&= \left[((a'+b')c'+d'e')'+(f'+g')'\right] h \\
&= \left[((a'+b')c'+d'e')'+fg\right] h \\
&= \left[((a'+b')c')'(d'e')'+fg\right] h \\
&= \left[((a'+b')c')'(d+e)+fg\right] h \\
&= \left[((a'+b')'+c)(d+e)+fg\right] h \\
&= ((ab+c)(d+e)+fg)h
\end{aligned}$$

This is equivalent to (b).

3. **(5 points)** Assuming that the pull-down network has the correct functionality that we want, obtain the expression for the corresponding pull-up network. Show all your work. Which one of the following is the expression equivalent to? (each letter in the diagram stands for a PMOS transistor)

Solution

$$\begin{aligned}
z' &= (a+bc)(de+f(g+h)) \\
z &= [(a+bc)(de+f(g+h))]' \\
&= (a+bc)'+(de+f(g+h))' \\
&= a'(bc)'+(de)'(f(g+h))' \\
&= a'(b'+c')+(d'+e')(f'+(g+h)') \\
&= a'(b'+c')+(d'+e')(f'+g'h')
\end{aligned}$$

This is equivalent to (a).

Problem 5 (10 points)

$$E(a,b,c,d) = ac'd + bc'd + ab' + a'd + b'cd'$$

Prove that $E(a,b,c,d)$ is a universal function.

Specify the pre-established universal set you are using, and explicitly show the implementation for each element in the set. You can use either constant 1 or 0 as an input, but not both (For example, you cannot implement an AND using constant 1 inputs and implement a NOT using constant 0 inputs).

Solution Plugging in different input combinations, we can find some inputs that implements a NAND function.

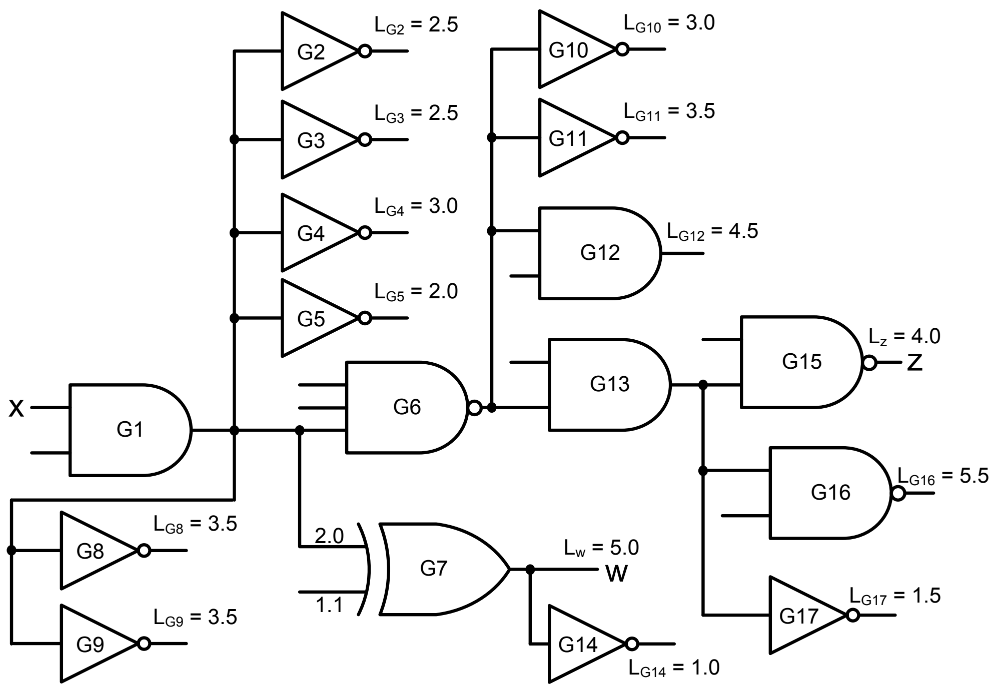
$$\begin{aligned}
E(1,b,c,1) &= c'+bc'+b' = b'+c' = (bc)' \\
E(a,1,c,1) &= ac'+c'+a' = a'+c' = (ac)' \\
E(a,b,1,1) &= ab'+a'+b' = a'+b' = (ab)'
\end{aligned}$$

Since $\{\text{NAND}\}$ is a pre-established universal set and we can use $E(a,b,c,d)$ to implement all elements in the set, $E(a,b,c,d)$ is universal.

Problem 6 (20 points)

Determine the propagation delay of the gate network shown. The outputs are z and w, and the input signal that we are interested in is x. The related gate characteristics are given in the table below.

Gate Type	Fan-in	Propagation Delays (ns) t_{pLH}	t_{pHL}	Load Factor I
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$	1.0
AND	2	$0.15 + 0.037L$	$0.16 + 0.017L$	1.0
NAND	2	$0.05 + 0.038L$	$0.08 + 0.027L$	1.0
NAND	3	$0.07 + 0.038L$	$0.09 + 0.039L$	1.0
XOR	2	$0.30 + 0.036L$	$0.30 + 0.021L$	1.1
		$0.16 + 0.036L$	$0.15 + 0.020L$	2.0



1. **(9 points)** Find the worst case value of $t_{pLH}(x \to z)$. Fill in the blanks below with the appropriate values.

Solution

Gate type & fan-in	G1: AND2 $\to$ G6: NAND3 $\to$ G13: AND2 $\to$ G15: NAND2
LH / HL	G1: LH $\to$ G6: HL $\to$ G13: HL $\to$ G15: LH
Total load L	G1: 9.0 $\to$ G6: 4.0 $\to$ G13: 3.0 $\to$ G15: 4.0

For the propagational delay values:

$$\begin{aligned} \text{G1:}\quad & 0.15 + 0.037 \cdot 9.0 = 0.483 \\ \text{G6:}\quad & 0.09 + 0.039 \cdot 4.0 = 0.246 \\ \text{G13:}\quad & 0.16 + 0.017 \cdot 3.0 = 0.211 \\ \text{G15:}\quad & 0.05 + 0.038 \cdot 4.0 = 0.202 \end{aligned}$$

$t_{pLH}(x \to z) = 0.483 + 0.246 + 0.211 + 0.202 = 1.142$ (ns)

2. **(9 points)** Unlike other gates, a low to high input for an XOR gate can cause the output to transition both from low to high and from high to low, depending on the value of the other input gate.

x	y	XOR
0	0	0
0	1	1
1	0	1
1	1	0

From the table, when $x = 0$, a low to high ($0 \to 1$) transition at input y will cause the output to move from low to high, but when $x = 1$, the same low to high transition at y will cause the output to move from high to low.

Taking this into consideration, find the worst case value of $t_{pLH}(x \to w)$.

Because G7 is an XOR gate, we need to consider both low to high and high to low transitions at the output of G1, and select the worst case. Fill in the blanks below with the appropriate values.

Solution

Gate type & fan-in	G1: AND2 $\to$ G7: XOR2
Total load L	G1: 9.0 $\to$ G7: 6.0
LH / HL	G7: LH

For the propagational delay values:

$$\begin{aligned} \text{G7:} &\quad 0.16 + 0.036 \cdot 6.0 = 0.376 \\ \text{G1(LH):} &\quad 0.15 + 0.037 \cdot 9.0 = 0.483 \\ \text{G1(HL):} &\quad 0.16 + 0.017 \cdot 9.0 = 0.313 \end{aligned}$$

3. **(2 points)** What is the worst case value of $t_{pLH}(x \to w)$?

Solution For gate G1, LH has the higher delay. Therefore, the worst case value of $t_{pLH}(x \to w)$ is $0.376 + 0.483 = 0.859$ (ns).

Problem 7 (21 points)

For the switching function $f(x_3, x_2, x_1, x_0)$, we are given the information below for the dc-set and zero-set.

$$\text{dc-set} = (11, 12)$$

$$\text{zero-set} = \text{zero-set of function } (x_3 + x_2 + x_1 + x_0)(x_3 + x_2 + x_1' + x_0')(x_3 + x_2' + x_1 + x_0)(x_3 + x_2' + x_1' + x_0)(x_3 + x_2' + x_1' + x_0')(x_3' + x_2' + x_1' + x_0)(x_3' + x_2' + x_1' + x_0')$$

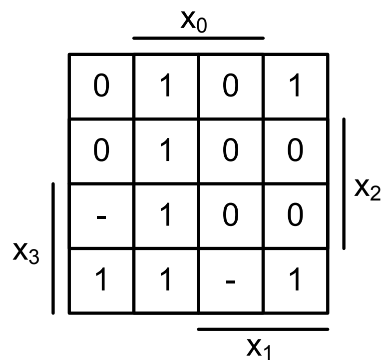
1. **(3 points)** Fill out the following K-map.

Solution From the given equation, we can get

$$\begin{aligned} \text{zero-set} &= \text{zero-set of function} \prod(0, 3, 4, 6, 7, 14, 15) \\ &= (0, 3, 4, 6, 7, 14, 15) \end{aligned}$$

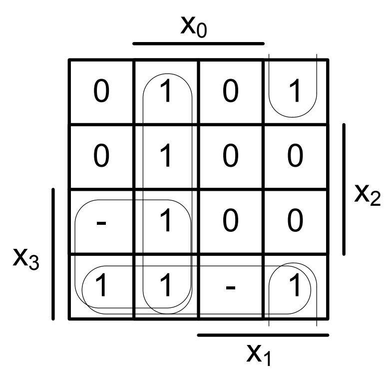
And since the dc-set is given, we can deduce the one-set.

The completed K-map is shown:



2. **(4 points)** Which of the given expressions are prime implicants of the function given above? Circle **all** that apply. Do not circle implicants that are not prime.

   Solution The prime implicants are shown in the K-map.



   The equivalent product terms are $x_1'x_0$ (not listed), x_3x_1' (not listed), x_3x_2' (b), $x_2'x_1x_0'$ (g).

3. **(3 points)** Write down the complete set of **essential** prime implicants. It is possible that not all essential primes were listed in the previous problem.

   Solution The 1 squares with single coverage are 1, 2, and 5. So we have two essential implicants, $x_1'x_0$ (covering 1, 5) and $x_2'x_1x_0'$ (covering 2).

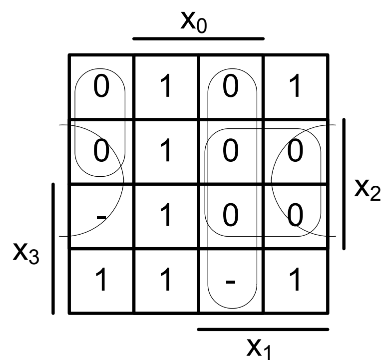
   x_3x_1' and x_3x_2' are not essential, since all 1 squares that they cover are also being covered by other prime implicants.

4. **(2 points)** Write **ALL** minimal sum of products expressions for f.

   Solution Since index 8 is not covered by the essential primes, we need either x_3x_1' or x_3x_2' to cover it. Therefore, the minimal SOP expression is either $x_1'x_0 + x_2'x_1x_0' + x_3x_1'$ or $x_1'x_0 + x_2'x_1x_0' + x_3x_2'$.

5. **(4 points)** Which of the given expressions are prime implicates of the function given above? Circle **all** that apply. Do not circle implicates that are not prime.

   Solution The prime implicates are shown in the K-map.



The equivalent sum terms are $(x_3 + x_1 + x_0)$ (h), $(x_2' + x_1')$ (not listed), $(x_1' + x_0')$ (f) and $(x_2' + x_0)$ (not listed).

6. **(3 points)** Write down the complete set of **essential** prime implicates. It is possible that not all essential primes were listed in the previous problem.

   Solution The 0 squares with single coverage are 0, and 3. So we have two essential implicates, $(x_3+x_1+x_0)$ (covering 0) and $(x_1' + x_0')$ (covering 3).

   $(x_2'+x_1')$ and $(x_2'+x_0)$ are not essential, since all 0 squares that they cover are also being covered by other prime implicates.

7. **(2 points)** Write **ALL** minimal product of sums expressions for f.

   Solution Since index 6 and 14 are not covered by the essential primes, we need either $(x_2' + x_1')$ or $(x_2'+x_0)$ to cover them. Therefore, the minimal POS expression is either $(x_3+x_1+x_0)(x_1'+x_0')(x_2'+x_1')$ or $(x_3 + x_1 + x_0)(x_1' + x_0')(x_2' + x_0)$.