[CSM51A Fall 2014] Solution to Assignment 2

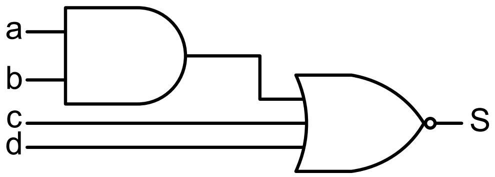
Due: 10/31/14

TA: Yang Lu (yangluphil@gmail.com)

Homework Problems (45 points total)

Problem 1 (5 points)

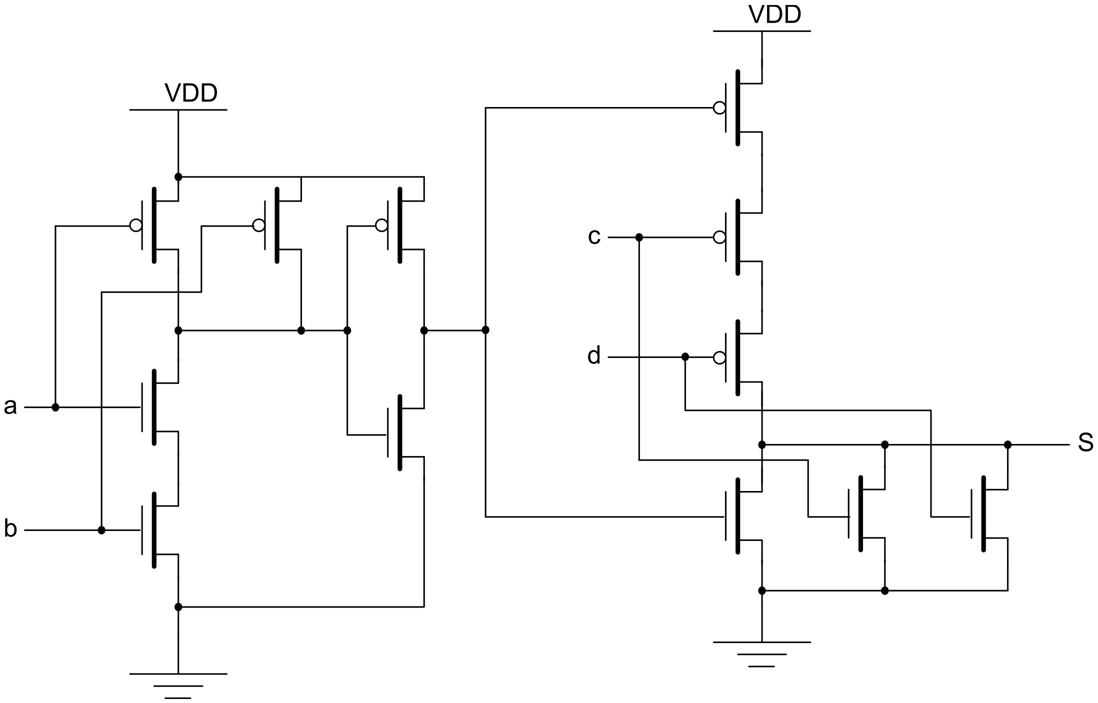
Draw the CMOS circuit implementations for the function given by the gate network shown in the figure below,



using:

1. **(2 points)** Separate AND and NOR gate implementations.

   Solution We simply connect the CMOS implementations of an AND gate and NOR gate as shown.



2. **(3 points)** A single complex gate.

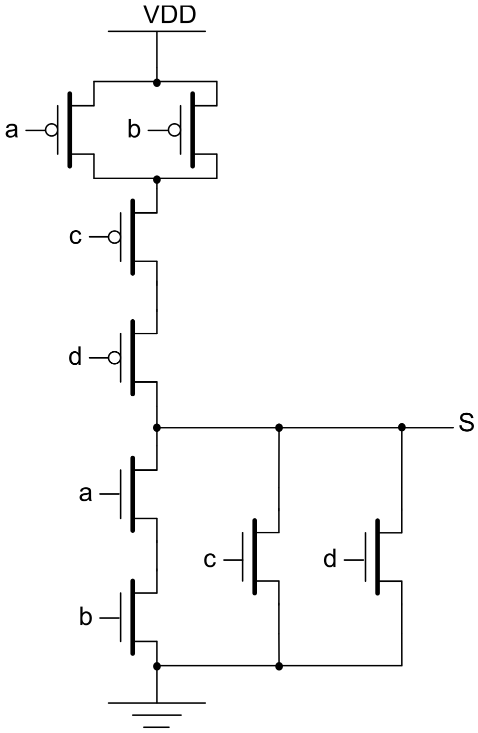
Solution For the pull-up network we need

$$\begin{aligned} S &= (ab + c + d)' \\ &= (ab)'c'd' \\ &= (a' + b')c'd' \end{aligned}$$

and for the pull-down network we need

$$\begin{aligned} S' &= (ab + c + d)'' \\ &= ab + c + d \end{aligned}$$

Using these expressions, the complex gate implementation looks like

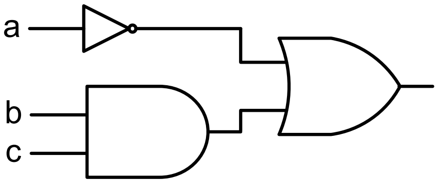


Problem 2 (10 points)

We would like to implement the logic $a' + bc$ using a CMOS circuit. We will try to save circuit area by reducing the number of transistors. To do this, we first consider the gate implementations.

1. **(1 points)** Draw the gate implementation of the circuit using NOT, AND and OR gates. How many transistors do we need for this implementation?

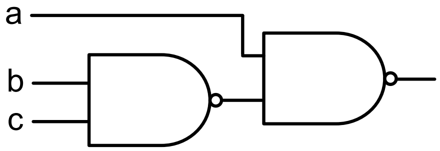
   Solution:



The number of transistors we need is 2(NOT gate) + 6(AND gate) + 6(OR gate) = 14 transistors.

2. **(2 points)** Find an alternative implementation that uses only NAND gates. Show the switching expression. (*Hint: Use Involution and DeMorgan's Law*)
   Solution: $a' + bc = ((a')'(bc)')' = (a(bc)')'$

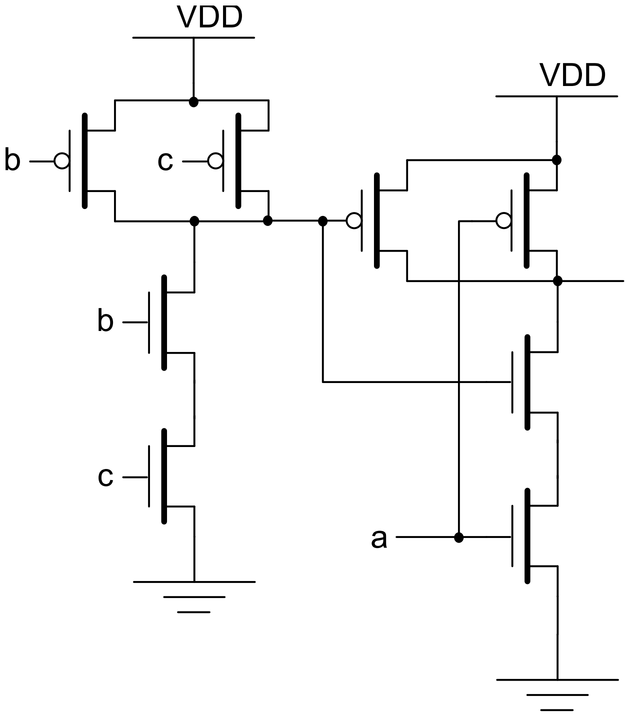
3. **(2 point)** Draw the gate implementation from 2. How many transistors do we need for this implementation?
   Solution:



   The number of transistors we need is 4(NAND gate) * 2 = 8 transistors.

4. **(5 points)** Of the above two cases, which implementation uses fewer transistors? Draw the CMOS implementation circuit.

   Solution: Clearly, the NAND gate implementation requires fewer transistors. The CMOS implementation for this is as shown.



Problem 3 (5 points)

We would like to design a function S with four input bits a, b, c, and d. The output z is 1 when exactly three inputs are 1, and 0 otherwise.

1. **(2 points)** Fill in the table below that shows the switching function $S(a, b, c, d)$.

   Solution

a	b	c	d	$S(a,b,c,d)$
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

2. **(3 points)** Is the function $S(a, b, c, d)$ universal? If it is, provide proof. You are allowed to set any input to a constant value.

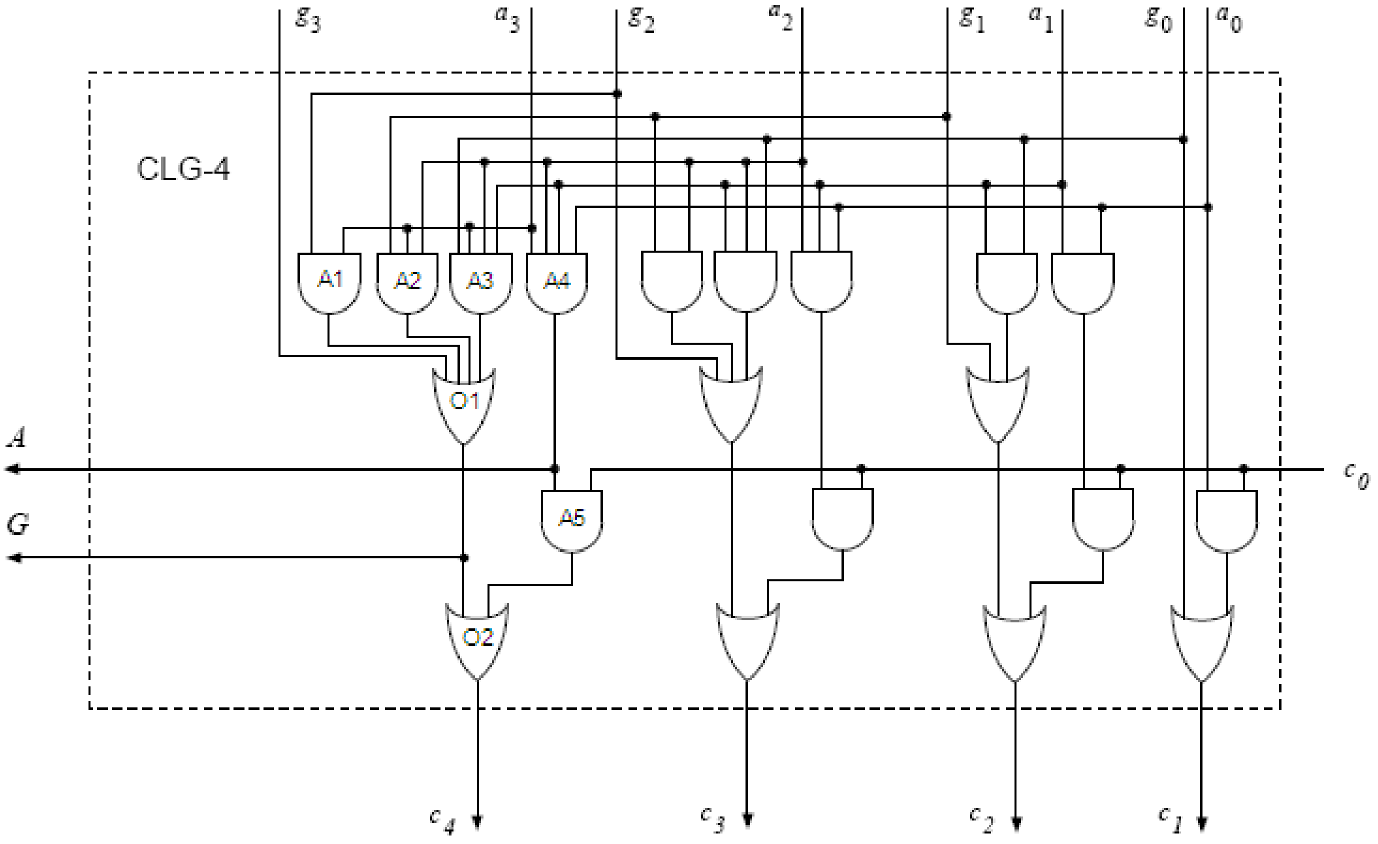
   Solution From the table, we can write $S(a, b, c, d) = a'bcd + ab'cd + abc'd + abcd'$. Now, we show that

   $S(a, b, 1, 0) = ab$: AND gate

   $S(a, 1, 1, 1) = a'$: NOT gate

   Since the set {AND, NOT} forms a universal set, the function S is universal.

Problem 4 (10 points)



We are given the above network and the following load values.

$$\begin{aligned} L_A &= 2.0 \\ L_G &= 6.0 \\ L_{c_4} &= 4.0 \end{aligned}$$

Using this information and Table 4.1 from the textbook, we would like to determine:

1. **(5 points)** The total load of each input signal. Calculate the total load of a_0, a_1, a_2, a_3, g_0, g_1, g_2, g_3, and c_0.

   Solution All gates in this diagram have its load factor values at 1.0. So calculating the total load of an input is equivalent to counting the number of gates it drives.

   The load values are:

a_0	4	g_0	4	c_0	4
a_1	6	g_1	3		
a_2	6	g_2	2		
a_3	4	g_3	1		

2. **(5 points)** Of the possible paths, which ones likely have the worst case delay to the output signal c_4? Find the worst case value of $t_{pHL}(c_4)$.

   Solution Looking at the circuit, the path with the worst delay would be either $A4 \rightarrow A5 \rightarrow O2$ or $A3 \rightarrow O1 \rightarrow O2$. The two gates, $A2$ and $A1$, have fewer inputs and equal or less load, thus the paths that go through these gates will be faster than the ones going through $A3$ or $A4$, and therefore do not need to be considered.

We calculate the delay of these two paths and compare them to find the worst case value of t_{pLH}. The total load values we need are $L_{A3} = 1$, $L_{A4} = L_A + 1 = 3$, $L_{O1} = L_G + 1 = 7$, $L_{A5} = 1$ and $L_{O2} = L_{c_4} = 4$.

$$\begin{aligned} t_{pHL}(c_4) &= t_{pHL}(O2) + t_{pHL}(A5) + t_{pHL}(A4) \\ &\text{or} \quad t_{pHL}(O2) + t_{pHL}(O1) + t_{pHL}(A3) \end{aligned}$$

$$\begin{aligned} & t_{pHL}(O2) + t_{pHL}(A5) + t_{pHL}(A4) \\ = \;& 0.20 + 0.019L_{O2} + 0.16 + 0.017L_{A5} + 0.21 + 0.019L_{A4} \\ = \;& 0.21 + 0.019 \cdot 4 + 0.16 + 0.017 + 0.20 + 0.019 \cdot 3 \\ = \;& 0.72 \text{ (ns)} \end{aligned}$$

$$\begin{aligned} & t_{pHL}(O2) + t_{pHL}(O1) + t_{pHL}(A3) \\ = \;& 0.20 + 0.019L_{O2} + 0.45 + 0.025L_{O1} + 0.21 + 0.019L_{A3} \\ = \;& 0.20 + 0.019 \cdot 4 + 0.45 + 0.025 \cdot 7 + 0.21 + 0.019 \\ = \;& 1.13 \text{ (ns)} \end{aligned}$$

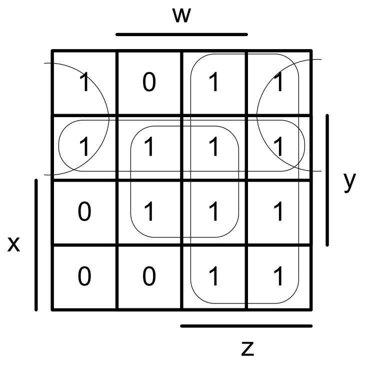
We can see that the second path is the slower of the two. The worst t_{pHL} delay path to c_4 is $A3 \rightarrow O1 \rightarrow O2$ and the delay value is 1.13 ns.

Problem 5 (6 points)

For $f(x, y, z, w) = \prod M(1, 8, 9, 12)$

1. Using K-maps, find all the prime implicants.

   Solution The prime implicants are shown in the K-map.



1	0	1	1
1	1	1	1
0	1	1	1
0	0	1	1

   The equivalent product terms are z, yw, $x'w'$ and $x'y$.

2. Which of these prime implicants are essential?

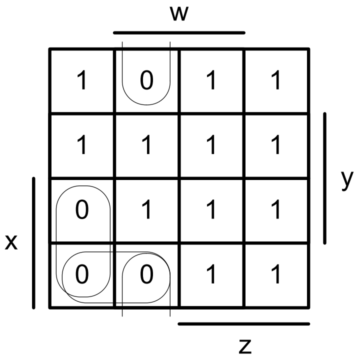
   Solution $x'y$ does not have any squares that it covers alone, therefore it is not essential.

3. Write the minimal sum of products for f.

   Solution Excluding the non-essential prime, we get $z + yw + x'w'$.

4. Find all the prime implicates.

   Solution



1	0	1	1
1	1	1	1
0	1	1	1
0	0	1	1

The equivalent sum terms are $(x' + z + w)$, $(y + z + w')$ and $(x' + y + z)$.

5. Which of these prime implicates are essential?

   Solution $(x' + y + z)$ does not have any squares that it covers alone, therefore it is not essential.

6. Write the minimal product of sums for f.

   Solution Excluding the non-essential prime, we get $(x' + z + w)(y + z + w')$.

Problem 6 (9 points)

We are given a module with four input bits, x_1, x_0, y_1, y_0 and three output bits, z_2, z_1, z_0, which are:

$$\begin{aligned} z_2 &= \sum m(7, 10, 11, 13, 14, 15) \\ z_1 &= \sum m(2, 3, 5, 6, 8, 9, 12, 15) \\ z_0 &= \sum m(1, 3, 4, 6, 9, 11, 12, 14) \end{aligned}$$

1. **(1 point)** Fill in the table.

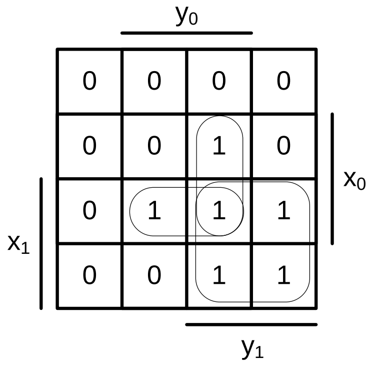
   Solution

x_1	x_0	y_1	y_0	z_2	z_1	z_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

2. **(3 points)** Draw K-maps for each output bit. Find the prime implicants.

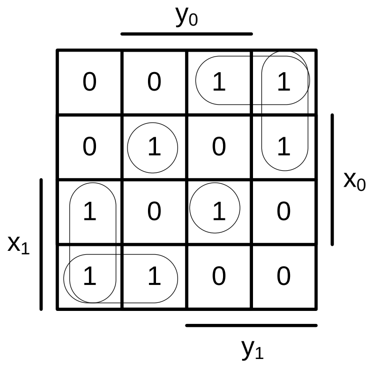
Solution The input bits are x_1, x_0, y_1, y_0 with x_1 being the most significant bit. The K-maps for each bit is as shown below.

Prime implicants for z_2: x_1y_1, $x_1x_0y_0$, $x_0y_1y_0$



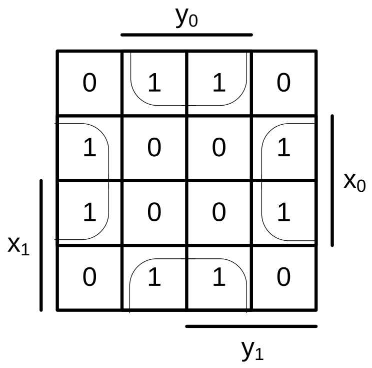
0	0	0	0
0	0	1	0
0	1	1	1
0	0	1	1

Prime implicants for z_1: $x_1y_1'y_0'$, $x_1x_0'y_1'$, $x_1'x_0y_1'y_0$, $x_1x_0y_1y_0$, $x_1'x_0'y_1$, $x_1'y_1y_0'$



0	0	1	1
0	1	0	1
1	0	1	0
1	1	0	0

Prime implicants for z_0: x_0y_0', $x_0'y_0$



0	1	1	0
1	0	0	1
1	0	0	1
0	1	1	0

3. **(3 points)** Write the minimal sum of products expression for each z bit.

Solution All prime implicants for the outputs are essential here. Therefore the minimal SoPs are:

$$\begin{aligned} z_2 &= x_1y_1 + x_1x_0y_0 + x_0y_1y_0 \\ z_1 &= x_1y_1'y_0' + x_1x_0'y_1' + x_1'x_0y_1'y_0 + x_1x_0y_1y_0 + x_1'x_0'y_1 + x_1'y_1y_0' \\ z_0 &= x_0y_0' + x_0'y_0 \end{aligned}$$

4. **(2 points)** Looking back at the table, can you identify the high-level function of the module?

   Solution Looking at the inputs as separate binary values of x and y, we can see that the resulting z is a sum of x and y. The module is an adder which adds the two inputs x and y.