[CSM51A Fall 2014] Homework 2

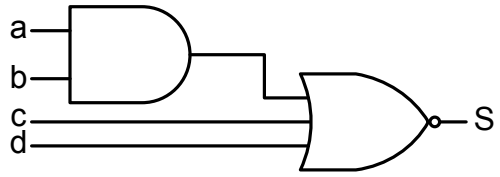
Due: 10/31/14

TA: Yang Lu (yangluphil@gmail.com)

Homework Problems (45 points total)

Problem 1 (5 points)

Draw the CMOS circuit implementations for the function given by the gate network shown in the figure below,



using:

1. **(2 points)** Separate AND and NOR gate implementations.
2. **(3 points)** A single complex gate.

Problem 2 (10 points)

We would like to implement the logic $a' + bc$ using a CMOS circuit. We will try to save circuit area by reducing the number of transistors. To do this, we first consider the gate implementations.

1. **(1 points)** Draw the gate implementation of the circuit using NOT, AND and OR gates. How many transistors do we need for this implementation?
2. **(2 points)** Find an alternative implementation that uses only NAND gates. Show the switching expression. (*Hint: Use Involution and DeMorgan's Law*)
3. **(2 point)** Draw the gate implementation from 2. How many transistors do we need for this implementation?
4. **(5 points)** Of the above two cases, which implementation uses fewer transistors? Draw the CMOS implementation circuit.

Problem 3 (5 points)

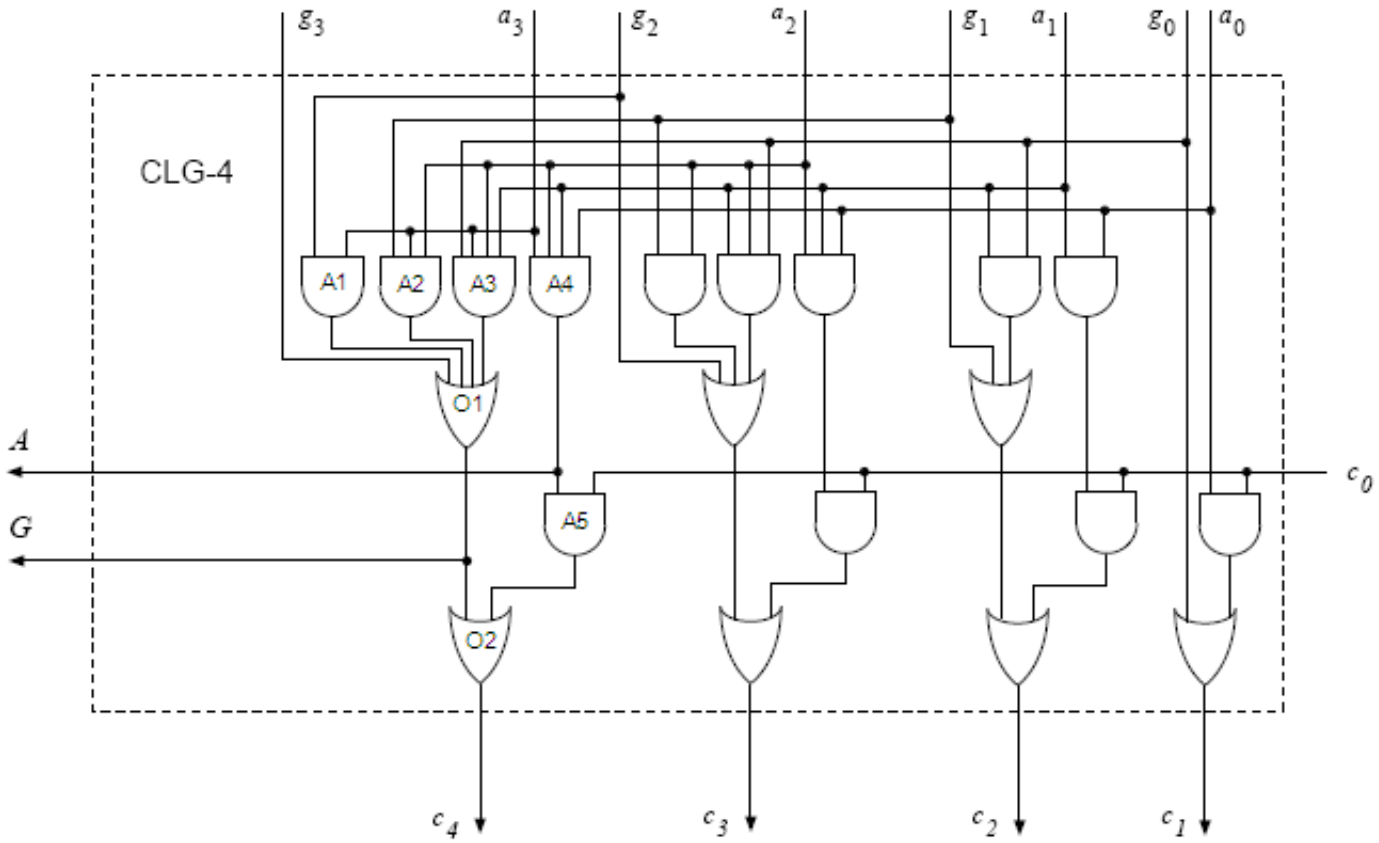
We would like to design a function S with four input bits a, b, c, and d. The output z is 1 when exactly three inputs are 1, and 0 otherwise.

1. **(2 points)** Fill in the table below that shows the switching function $S(a, b, c, d)$.

a	b	c	d	$S(a,b,c,d)$
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

2. **(3 points)** Is the function $S(a,b,c,d)$ universal? If it is, provide proof. You are allowed to set any input to a constant value.

Problem 4 (10 points)



We are given the above network and the following load values.

$$\begin{aligned} L_A &= 2.0 \\ L_G &= 6.0 \\ L_{c_4} &= 4.0 \end{aligned}$$

Using this information and Table 4.1 from the textbook, we would like to determine:

1. **(5 points)** The total load of each input signal. Calculate the total load of a_0, a_1, a_2, a_3, g_0, g_1, g_2, g_3, and c_0.
2. **(5 points)** Of the possible paths, which ones likely have the worst case delay to the output signal c_4? Find the worst case value of $t_{pHL}(c_4)$.

Problem 5 (6 points)

For $f(x, y, z, w) = \prod M(1, 8, 9, 12)$

1. Using K-maps, find all the prime implicants.
2. Which of these prime implicants are essential?
3. Write the minimal sum of products for f.
4. Find all the prime implicates.
5. Which of these prime implicates are essential?
6. Write the minimal product of sums for f.

Problem 6 (9 points)

We are given a module with four input bits, x_1, x_0, y_1, y_0 and three output bits, z_2, z_1, z_0, which are:

$$\begin{aligned} z_2 &= \sum m(7, 10, 11, 13, 14, 15) \\ z_1 &= \sum m(2, 3, 5, 6, 8, 9, 12, 15) \\ z_0 &= \sum m(1, 3, 4, 6, 9, 11, 12, 14) \end{aligned}$$

1. **(1 point)** Fill in the table.

x_1	x_0	y_1	y_0	z_2	z_1	z_0
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

2. **(3 points)** Draw K-maps for each output bit. Find the prime implicants.
3. **(3 points)** Write the minimal sum of products expression for each z bit.
4. **(2 points)** Looking back at the table, can you identify the high-level function of the module?