# LMV3xx Low-Voltage Rail-to-Rail Output Operational Amplifier

## 1 Features

- For an upgraded version - refer to **LMV321A, LMV324A, and LMV358A**
- 2.7-V and 5-V performance
- –40°C to +125°C operation
- No crossover distortion
- Low supply current
  - LMV321: 130 µA (typical)
  - LMV358: 210 µA (typical)
  - LMV324: 410 µA (typical)
- Rail-to-rail output swing
- ESD protection exceeds JESD 22
  - 2000-V human-body model
  - 1000-V charged-device model

## 2 Applications

- Desktop PCs
- HVAC: heating, ventilating, and air conditioning
- Motor control: AC induction
- Netbooks
- Portable media players
- Power: telecom DC/DC module: digital
- Professional audio mixers
- Refrigerators
- Washing machines: high-end and low-end

## 3 Description

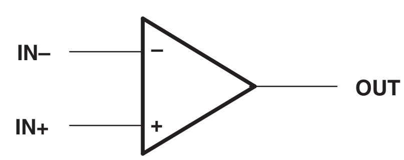
For an upgraded version with enhanced performance, please refer to **LMV321A, LMV324A, and LMV358A**.

The LMV321, LMV358, and LMV324 devices are single, dual, and quad low-voltage (2.7 V to 5.5 V) operational amplifiers with rail-to-rail output swing. These devices are the most cost-effective solutions for applications where low-voltage operation, space saving, and low cost are needed. These amplifiers are designed specifically for low-voltage (2.7 V to 5 V) operation, with performance specifications meeting or exceeding the LM358 and LM324 devices that operate from 5 V to 30 V. With package sizes down to one-half the size of the DBV (SOT-23) package, these devices can be used for a variety of applications.

**Device Information(1)**

| PART NUMBER | PACKAGE (PIN) | BODY SIZE |
|---|---|---|
| LMV321 | SOT-23 (5) | 2.90 mm × 1.60 mm |
| | SC-70 (5) | 2.00 mm × 1.25 mm |
| LMV358 | SOIC (8) | 4.90 mm × 3.90 mm |
| | VSSOP (8) | 2.30 mm × 2.00 mm |
| | VSSOP (8) | 3.00 mm × 4.40 mm |
| | TSSOP (8) | 3.00 mm × 3.00 mm |
| LMV324 | SOIC (14) | 8.65 mm × 3.91 mm |
| | TSSOP (14) | 5.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



# Table of Contents



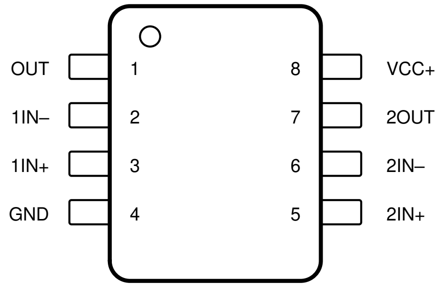
# 4 Revision History

**Changes from Revision W (October 2014) to Revision X** — **Page**

- Deleted LMV324S mentions on the front page of the data sheet .......... 1
- Added end equipment links in *Application* section .......... 1
- Added recommended device notice for LMV321A, LMV358A, and LMV324A .......... 1
- Changed *Device Information* table to sort devices by channel count in ascending order .......... 1
- Changed *Pin Configuration and Functions* section by dividing the Pin Functions table into separate tables per device .......... 3
- Deleted LMV324S pinout information .......... 4
- Changed HBM ESD voltage from 2500 V to 2000 V .......... 5
- Changed CDM ESD voltage from 1500 V to 1000 V .......... 5
- Deleted Shutdown voltage threshold for LMV324S .......... 5
- Changed *Thermal Information* section by dividing the *Thermal Information* table into separate tables per device .......... 5
- Changed Thermal Information for LMV321 .......... 5
- Deleted LMV324S Thermal Information .......... 5
- Changed Thermal Information for LMV324 .......... 5
- Changed Thermal Information for LMV358 .......... 6
- Deleted LMV324S test condition for supply current .......... 7
- Changed output short-circuit current for sourcing from 60 mA to 40 mA .......... 8
- Changed output short-circuit current for sinking from 160 mA to 40 mA .......... 8
- Deleted LMV324S test condition for supply current .......... 8
- Added assured by characterization table notes to output short-circuit current, output swing, and input bias current specifications .......... 8
- Changed Source Current Vs Output Voltage $V_{CC}$=2.7V plot with Output Voltage vs Output Current (Claw) plot in *Typical Characteristics* section .......... 10
- Deleted plots Source Current Vs Output Voltage $V_{CC}$= 5V, Sinking Current vs Output Voltage $V_{CC}$=2.7V, Sinking Current vs Output Voltage $V_{CC}$=5V, Short-Circuit Current vs Temperature in *Typical Characteristics* section .......... 10
- Changed Open-Loop Output Impedance Vs Frequency plot in *Typical Characteristics* section .......... 12
- Added *Receiving Notification* and *Support Resources* sections to the *Device and Documentation Support* section .......... 23

# 5 Pin Configuration and Functions

**D, DDU, DGK, and PW Packages**
**8-Pin SOIC, VSSOP and TSSOP**
**Top View**

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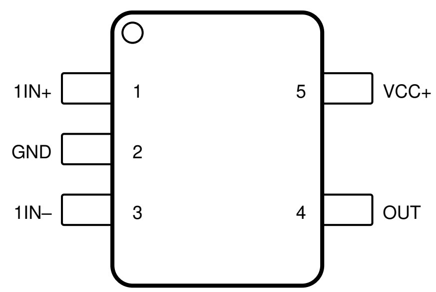
**Pin Functions: LMV358**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1IN+ | 3 | I | Noninverting input |
| 1IN– | 2 | I | Inverting input |
| 2IN+ | 5 | I | Noninverting input |
| 2IN– | 6 | I | Inverting input |
| 2OUT | 7 | O | Output |
| GND | 4 | — | Negative supply |
| OUT | 1 | O | Output |
| VCC+ | 8 | — | Positive supply |

**DBV and DCK Packages**
**5-Pin SOT-23 and SC-70**
**Top View**

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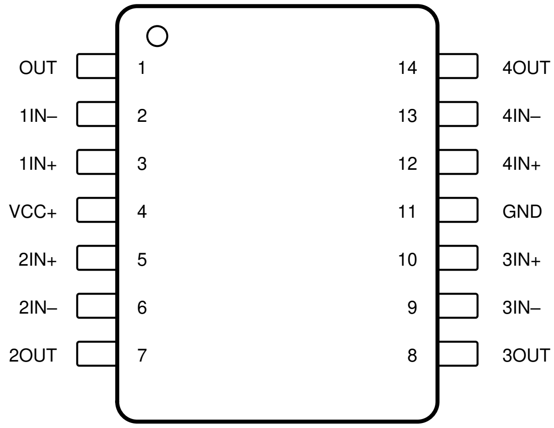
**Pin Functions: LMV321**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1IN+ | 1 | I | Noninverting input |
| 1IN– | 3 | I | Inverting input |
| GND | 2 | — | Negative supply |
| OUT | 4 | O | Output |
| VCC+ | 5 | — | Positive supply |

**D and PW Packages
14-Pin SOIC and TSSOP
Top View**

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### Pin Functions: LMV324

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 3/4 SHDN | — | I | Shutdown (logic low ) / enable (logic high) |
| 1/2 SHDN | — | I | Shutdown (logic low) / enable (logic high) |
| 1IN+ | 3 | I | Noninverting input |
| 1IN– | 2 | I | Inverting input |
| 2IN+ | 5 | I | Noninverting input |
| 2IN– | 6 | I | Inverting input |
| 2OUT | 7 | O | Output |
| 3IN+ | 10 | I | Noninverting input |
| 3IN– | 9 | I | Inverting input |
| 3OUT | 8 | O | Output |
| 4IN+ | 12 | I | Noninverting input |
| 4IN– | 13 | I | Inverting input |
| 4OUT | 14 | O | Output |
| GND | 11 | — | Negative supply |
| OUT | 1 | O | OUT |
| VCC+ | 4 | — | Positive supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage [2] | | | 5.5 | V |
| $V_{ID}$ | Differential input voltage [3] | | –5.5 | 5.5 | V |
| $V_I$ | Input voltage (either input) | | –0.2 | 5.7 | V |
| | Duration of output short circuit (one amplifier) to ground [4] | At or below $T_A$ = 25°C, $V_{CC} \le 5.5$ V | Unlimited | | |
| $T_J$ | Operating virtual junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and $V_{CC}$ specified for the measurement of $I_{OS}$) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to $V_{CC}$ can cause excessive heating and eventual destruction.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins [2] | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions [1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage (single-supply operation) | | 2.7 | 5.5 | V |
| $T_A$ | Operating free-air temperature | I temperature (LMV321, LMV358, LMV324, LMV321IDCK) | –40 | 125 | °C |
| | | Q temperature | –40 | 125 | |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*.

## 6.4 Thermal Information: LMV321

| THERMAL METRIC [1] | | LMV321 DBV (SOT-23) 5 PINS | LMV321 DCK (SC-70) 5 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 232.9 | 239.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Thermal Information: LMV324

| THERMAL METRIC [1] | | LMV324 D (SOIC) 14 PINS | LMV324 PW (TSSOP) 14 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 102.1 | 148.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.6 Thermal Information: LMV358

| THERMAL METRIC[1] | | LMV358 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | D (SOIC) | DGK (VSSOP) | DDU (VSSOP) | PW (TSSOP) | |
| | | 8 PINS | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 207.9 | 201.2 | 210 | 200.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.7 Electrical Characteristics: $V_{CC}+ = 2.7$ V

$V_{CC+} = 2.7$ V, $T_A = 25°C$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP[(1)] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | | | | 1.7 | 7 | mV |
| $\alpha_{VIO}$ | Average temperature coefficient of input offset voltage | | | | 5 | | µV/°C |
| $I_{IB}$ | Input bias current | | | | 11 | 250 | nA |
| $I_{IO}$ | Input offset current | | | | 5 | 50 | nA |
| CMRR | Common-mode rejection ratio | $V_{CM} = 0$ to 1.7 V | | 50 | 63 | | dB |
| $k_{SVR}$ | Supply-voltage rejection ratio | $V_{CC} = 2.7$ V to 5 V, $V_O = 1$ V | | 50 | 60 | | dB |
| $V_{ICR}$ | Common-mode input voltage range | CMRR ≥ 50 dB | | 0 | –0.2 | | V |
| | | | | | 1.9 | 1.7 | |
| $V_O$ | Output swing | $R_L = 10$ kΩ to 1.35 V | High level | $V_{CC} – 100$ | $V_{CC} – 10$ | | mV |
| | | | Low level | | 60 | 180 | |
| $I_{CC}$ | Supply current | LMV321I | | | 80 | 170 | µA |
| | | LMV358I (both amplifiers) | | | 140 | 340 | |
| | | LMV324I (all four amplifiers) | | | 260 | 680 | |
| $B_1$ | Unity-gain bandwidth | $C_L = 200$ pF | | | 1 | | MHz |
| $\Phi_m$ | Phase margin | | | | 60 | | ° |
| $G_m$ | Gain margin | | | | 10 | | dB |
| $V_n$ | Equivalent input noise voltage | f = 1 kHz | | | 46 | | $nV/\sqrt{Hz}$ |
| $I_n$ | Equivalent input noise current | f = 1 kHz | | | 0.17 | | $pA/\sqrt{Hz}$ |

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

## 6.8 Electrical Characteristics: $V_{CC}+ = 5$ V

$V_{CC+}$ = 5 V, at specified free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP[(1)] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $T_A$ = 25°C | | 1.7 | 7 | mV |
| | | $T_A$ = –40°C to +125°C | | | 9 | |
| $\alpha_{VIO}$ | Average temperature coefficient of input offset voltage | $T_A$ = 25°C | | 5 | | µV/°C |
| $I_{IB}$ | Input bias current | $T_A$ = 25°C | | 15 | 250[(2)] | nA |
| | | $T_A$ = –40°C to +125°C | | | 500[(2)] | |
| $I_{IO}$ | Input offset current | $T_A$ = 25°C | | 5 | 50[(2)] | nA |
| | | $T_A$ = –40°C to +125°C | | | 150[(2)] | |
| CMRR | Common-mode rejection ratio | $V_{CM}$ = 0 to 4 V<br>$T_A$ = 25°C | 50 | 65 | | dB |
| $k_{SVR}$ | Supply-voltage rejection ratio | $V_{CC}$ = 2.7 V to 5 V, $V_O$ = 1 V, $V_{CM}$ = 1 V<br>$T_A$ = 25°C | 50 | 60 | | dB |
| $V_{ICR}$ | Common-mode input voltage range | CMRR ≥ 50 dB, $T_A$ = 25°C | 0 | –0.2 | | V |
| | | | | 4.2 | 4 | |
| $V_O$ | Output swing | $R_L$ = 2 kΩ to 2.5 V, high level, $T_A$ = 25°C | $V_{CC}$ – 300 | $V_{CC}$ – 40 | | mV |
| | | $R_L$ = 2 kΩ to 2.5 V, high level, $T_A$ = –40°C to +125°C | $V_{CC}$ – 400[(2)] | | | |
| | | $T_A$ = 25°C, low level | | 120 | 300 | |
| | | $T_A$ = –40°C to +125°C, low level | | | 400[(2)] | |
| | | $R_L$ = 10 kΩ to 2.5 V, high level, $T_A$ = 25°C | $V_{CC}$ – 100 | $V_{CC}$ – 10 | | |
| | | $R_L$ = 10 kΩ to 2.5 V, high level, $T_A$ = –40°C to +125°C | $V_{CC}$ – 200[(2)] | | | |
| | | $T_A$ = 25°C, low level | | 65 | 180 | |
| | | $T_A$ = –40°C to +125°C, low level | | | 280[(2)] | |
| $A_{VD}$ | Large-signal differential voltage gain | $R_L$ = 2 kΩ, $T_A$ = 25°C | 15 | 100 | | V/mV |
| | | $R_L$ = 2 kΩ, $T_A$ = –40°C to +125°C | 10[(2)] | | | |
| $I_{OS}$ | Output short-circuit current | Sourcing, $V_O$ = 0 V, $T_A$ = 25°C | 5[(2)] | 40 | | mA |
| | | Sinking, $V_O$ = 5 V, $T_A$ = 25°C | 10[(2)] | 40 | | |
| $I_{CC}$ | Supply current | LMV321I, $T_A$ = 25°C | | 130 | 250 | µA |
| | | LMV321I, $T_A$ = –40°C to +125°C | | | 350 | |
| | | LMV358I (both amplifiers), $T_A$ = 25°C | | 210 | 440 | |
| | | LMV358I (both amplifiers), $T_A$ = –40°C to +125°C | | | 615 | |
| | | LMV324I (all four amplifiers), $T_A$ = 25°C | | 410 | 830 | |
| | | LMV324I (all four amplifiers), $T_A$ = –40°C to +125°C | | | 1160 | |
| $B_1$ | Unity-gain bandwidth | $C_L$ = 200 pF, $T_A$ = 25°C | | 1 | | MHz |
| $\Phi_m$ | Phase margin | $T_A$ = 25°C | | 60 | | ° |
| $G_m$ | Gain margin | $T_A$ = 25°C | | 10 | | dB |
| $V_n$ | Equivalent input noise voltage | f = 1 kHz, $T_A$ = 25°C | | 39 | | nV/√Hz |
| $I_n$ | Equivalent input noise current | f = 1 kHz, $T_A$ = 25°C | | 0.21 | | pA/√Hz |
| SR | Slew rate | $T_A$ = 25°C | | 1 | | V/µs |

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) Assured by characterization. Not production tested.

## 6.9 Typical Characteristics

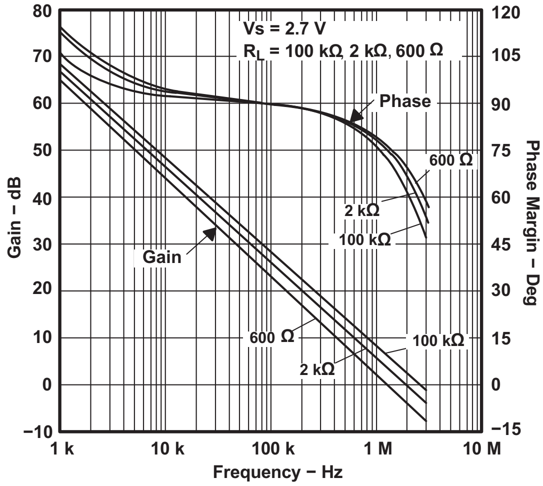



Figure 1. LMV321 Frequency Response vs Resistive Load

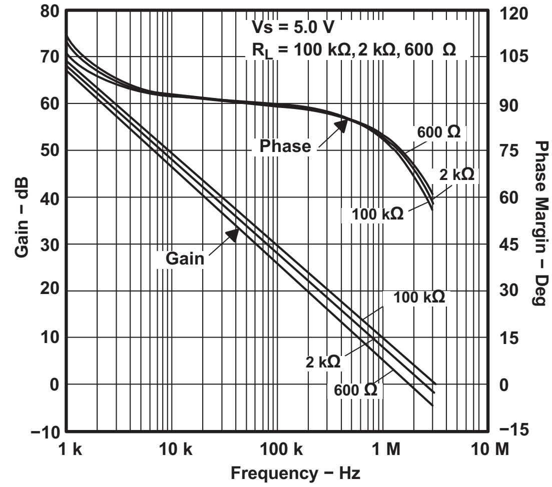



Figure 2. LMV321 Frequency Response vs Resistive Load

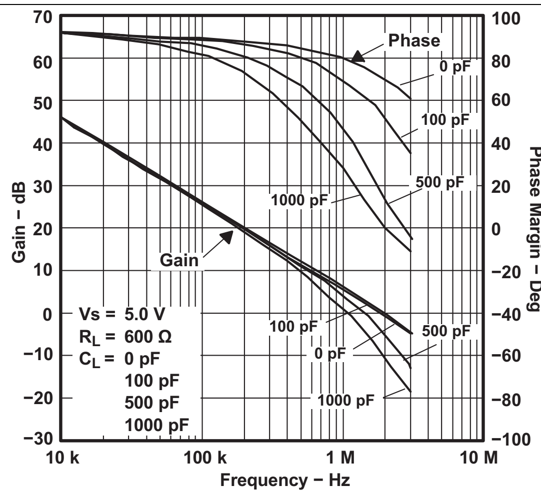



Figure 3. LMV321 Frequency Response vs Capacitive Load

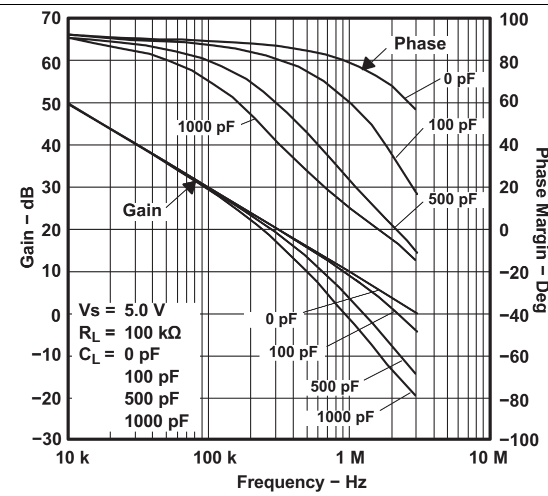



Figure 4. LMV321 Frequency Response vs Capacitive Load

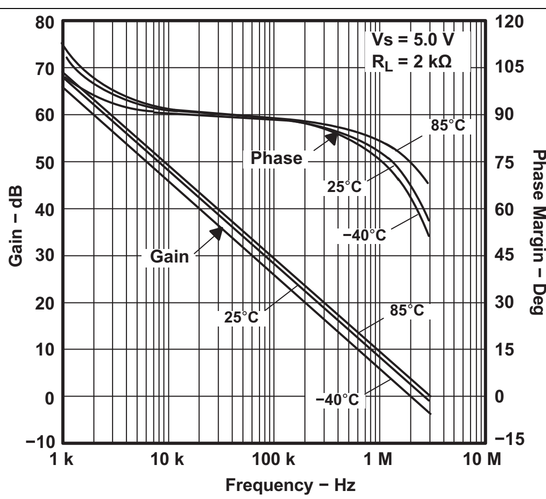



Figure 5. LMV321 Frequency Response vs Temperature

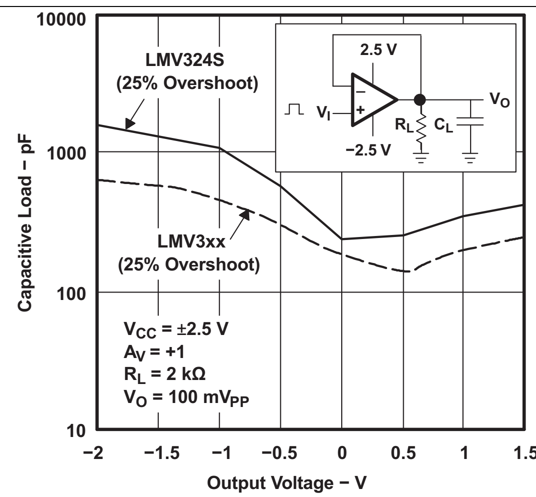



Figure 6. Stability vs Capacitive Load

## Typical Characteristics (continued)

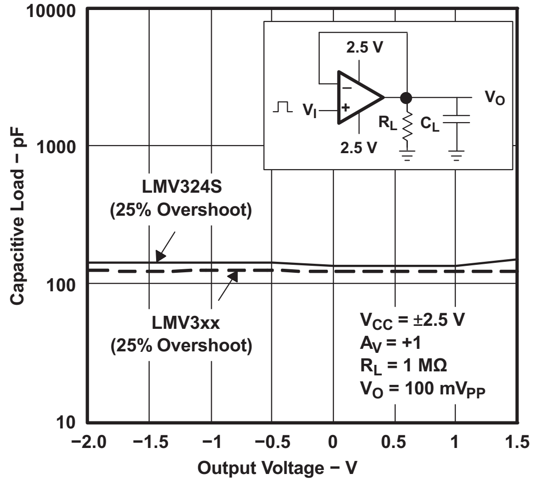



**Figure 7. Stability vs Capacitive Load**

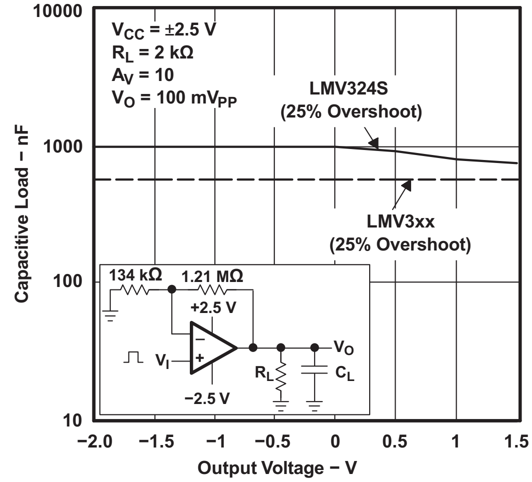



**Figure 8. Stability vs Capacitive Load**

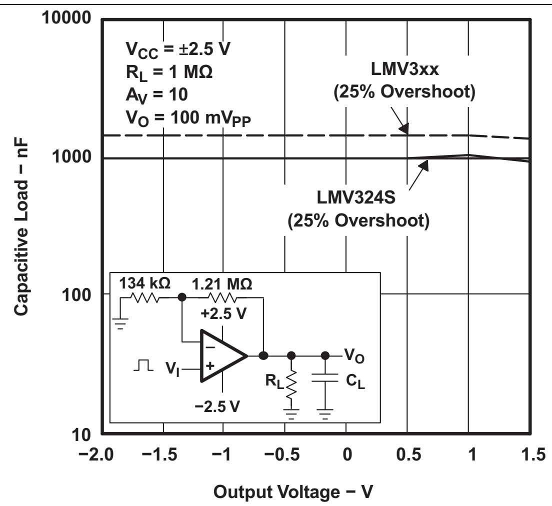



**Figure 9. Stability vs Capacitive Load**

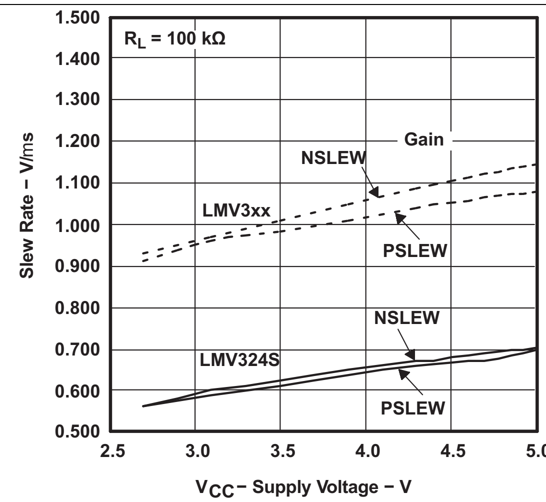



**Figure 10. Slew Rate vs Supply Voltage**

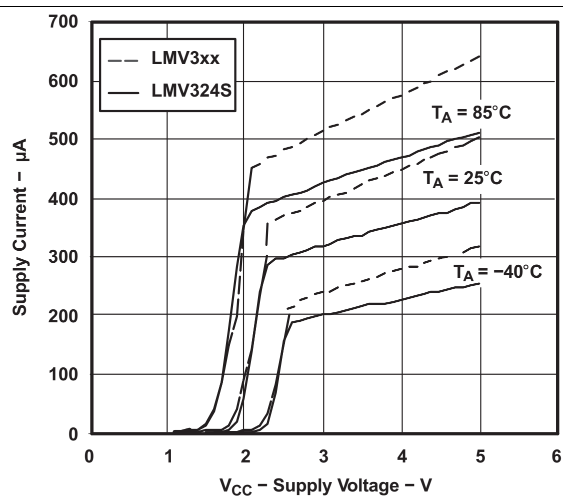



**Figure 11. Supply Current vs Supply Voltage: Quad Amplifier**

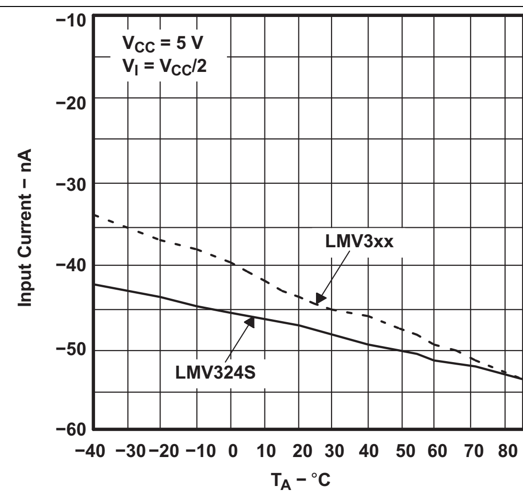



**Figure 12. Input Current vs Temperature**

## Typical Characteristics (continued)

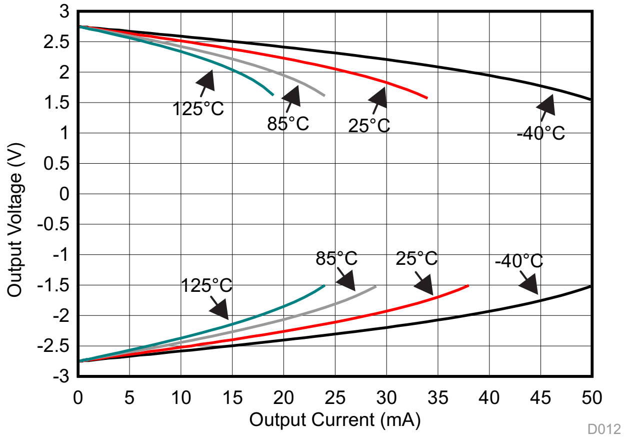



Figure 13. Output Voltage vs Output Current (Claw)

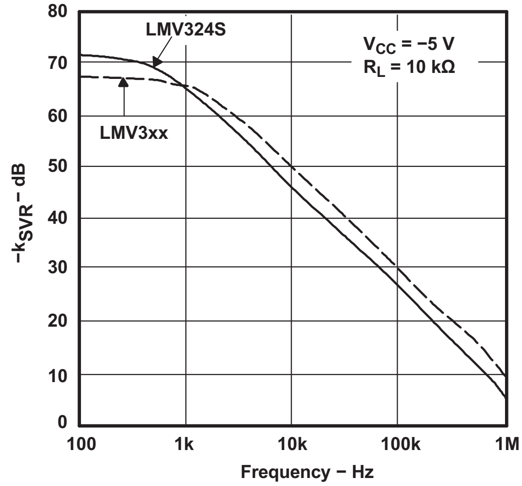



Figure 14. $-k_{SVR}$ vs Frequency

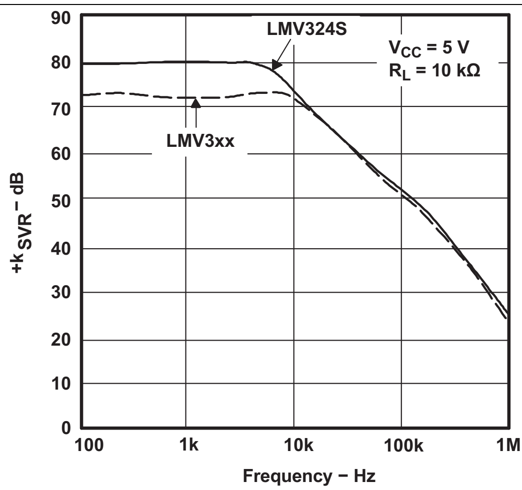



Figure 15. $+k_{SVR}$ vs Frequency

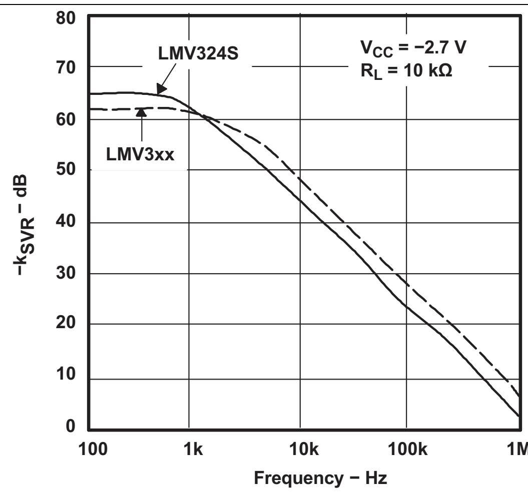



Figure 16. $-k_{SVR}$ vs Frequency

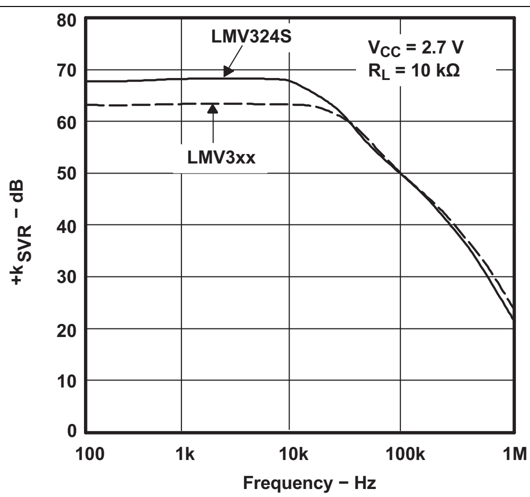



Figure 17. $+k_{SVR}$ vs Frequency

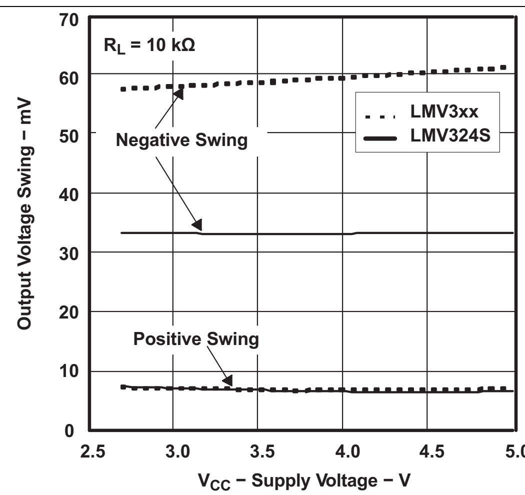



Figure 18. Output Voltage Swing From Rails vs Supply Voltage

## Typical Characteristics (continued)

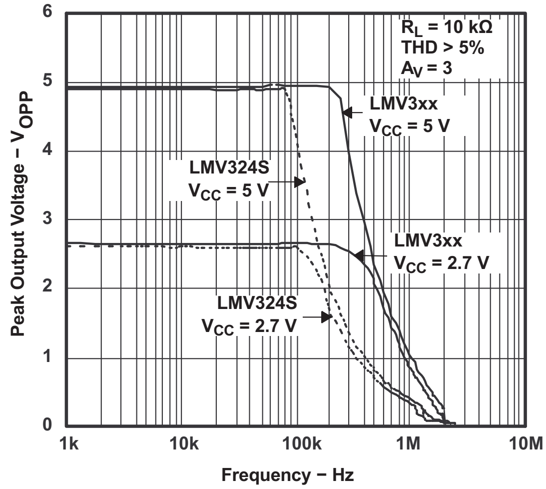



Figure 19. Output Voltage vs Frequency

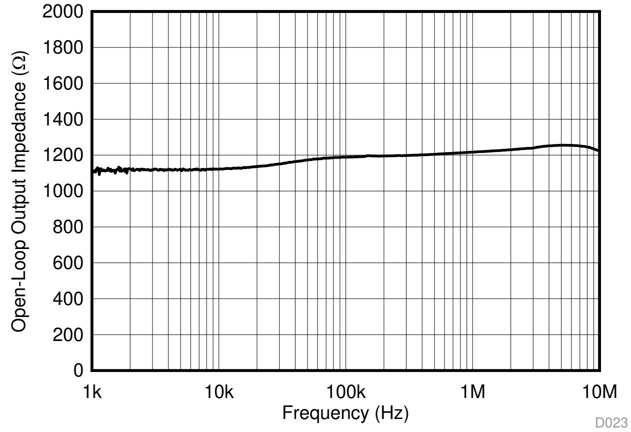



Figure 20. Open-Loop Output Impedance vs Frequency

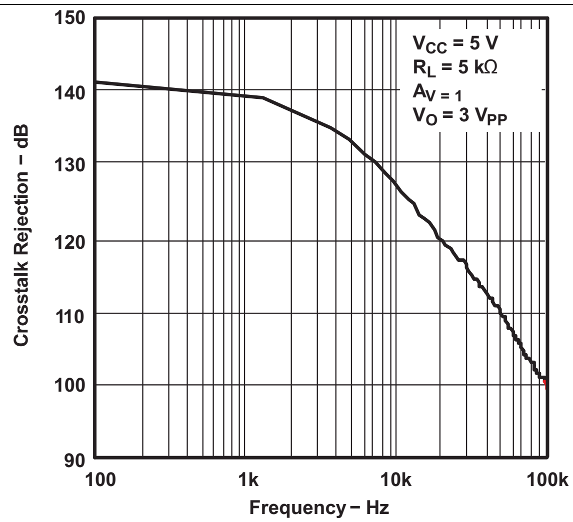



Figure 21. Cross-Talk Rejection vs Frequency

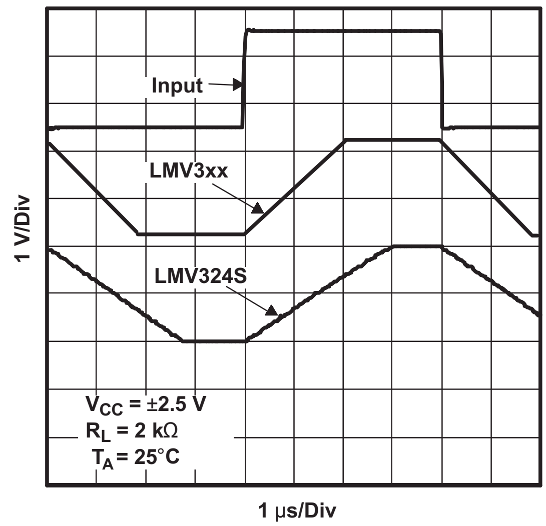



Figure 22. Noninverting Large-Signal Pulse Response

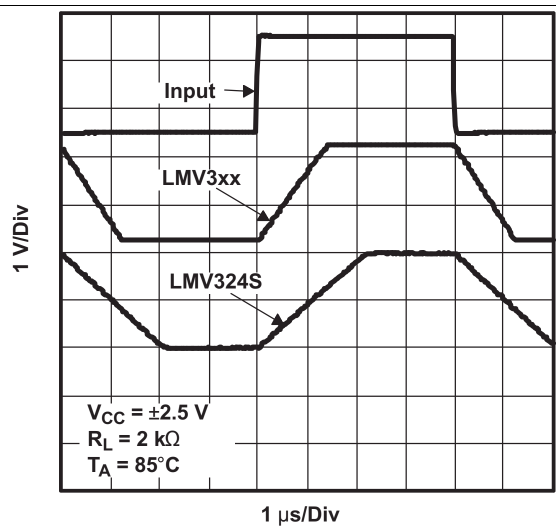



Figure 23. Noninverting Large-Signal Pulse Response

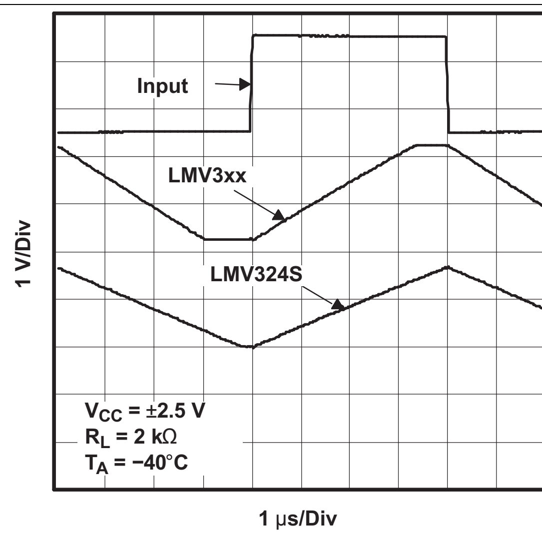



Figure 24. Noninverting Large-Signal Pulse Response

## Typical Characteristics (continued)

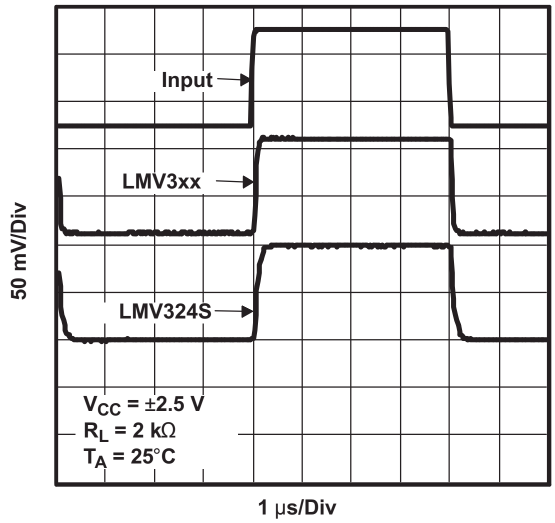



Figure 25. Noninverting Small-Signal Pulse Response

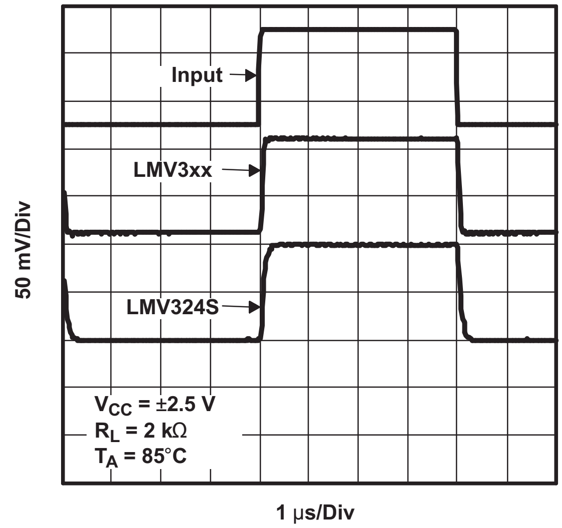



Figure 26. Noninverting Small-Signal Pulse Response

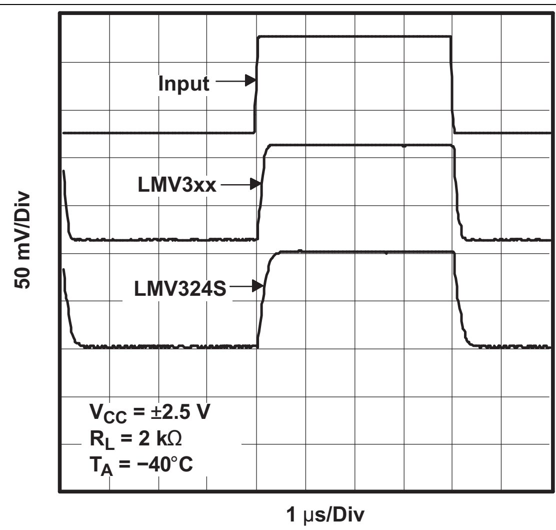



Figure 27. Noninverting Small-Signal Pulse Response

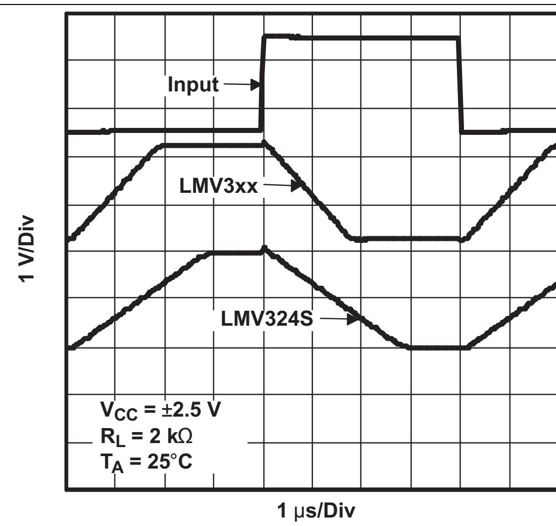



Figure 28. Inverting Large-Signal Pulse Response

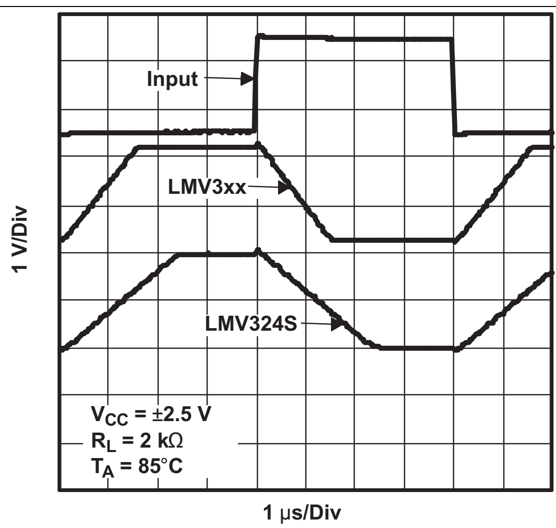



Figure 29. Inverting Large-Signal Pulse Response

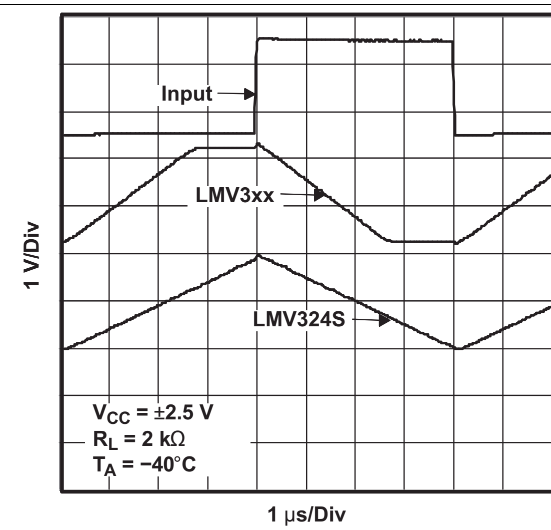



Figure 30. Inverting Large-Signal Pulse Response

## Typical Characteristics (continued)

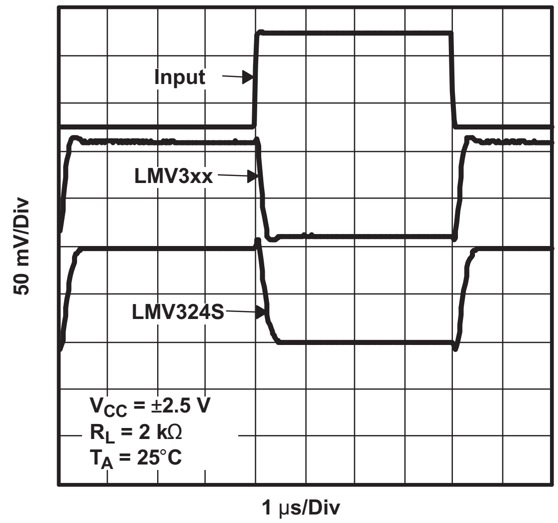



Figure 31. Inverting Small-Signal Pulse Response

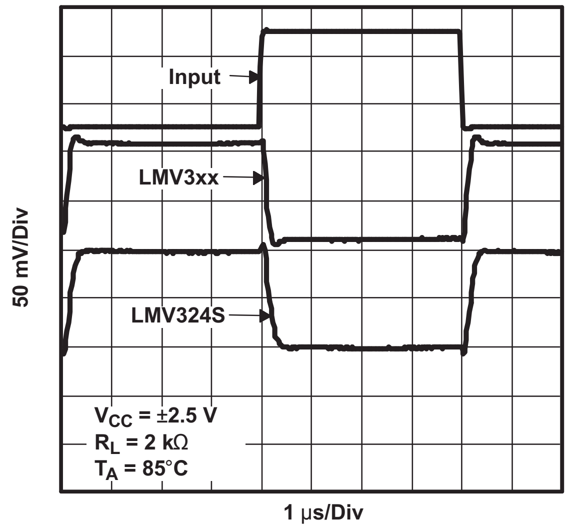



Figure 32. Inverting Small-Signal Pulse Response

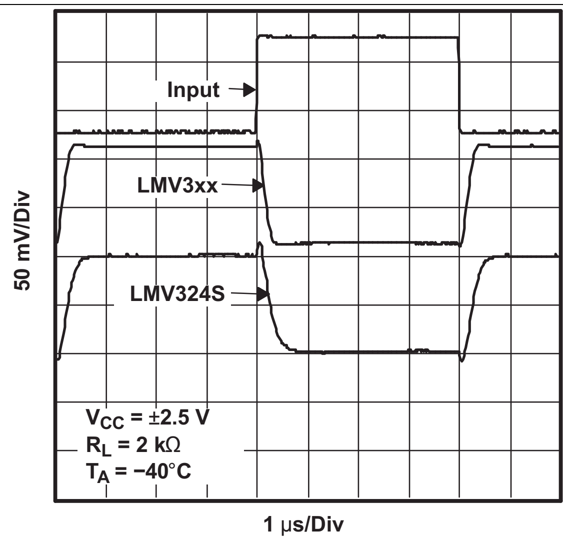



Figure 33. Inverting Small-Signal Pulse Response

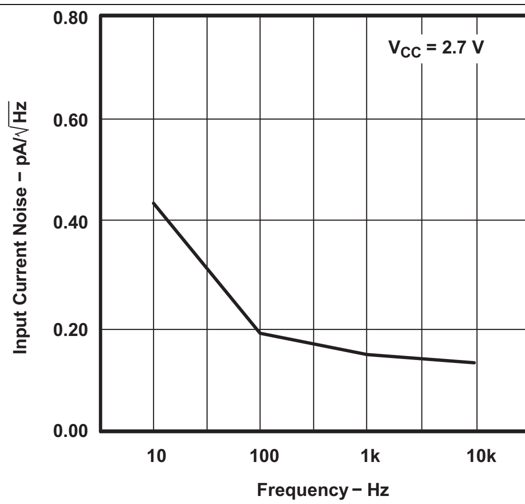



Figure 34. Input Current Noise vs Frequency

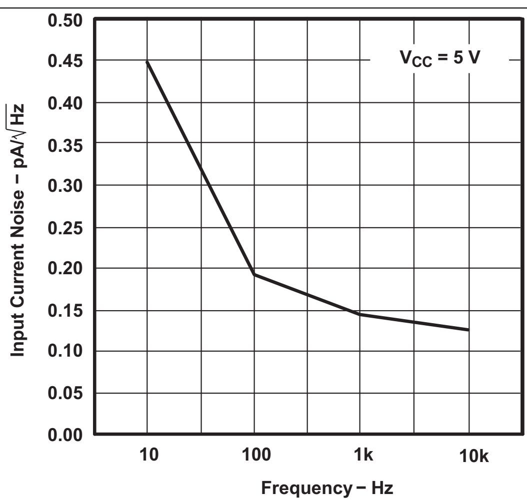



Figure 35. Input Current Noise vs Frequency

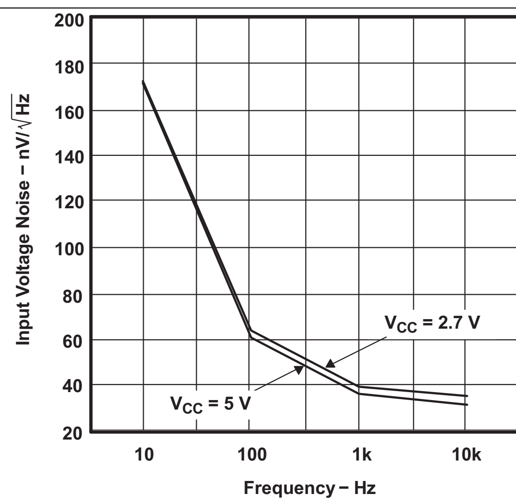



Figure 36. Input Voltage Noise vs Frequency

## Typical Characteristics (continued)

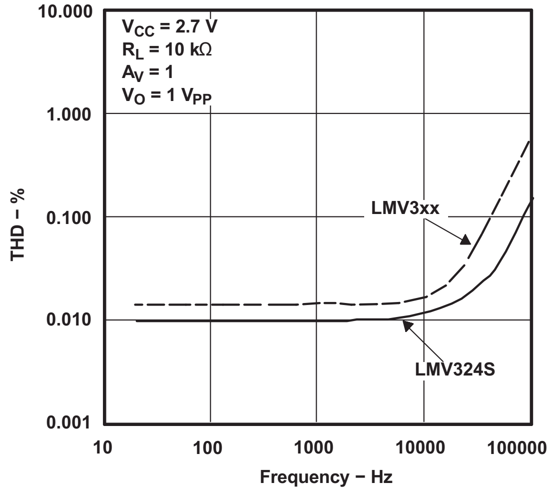



Figure 37. THD + N vs Frequency

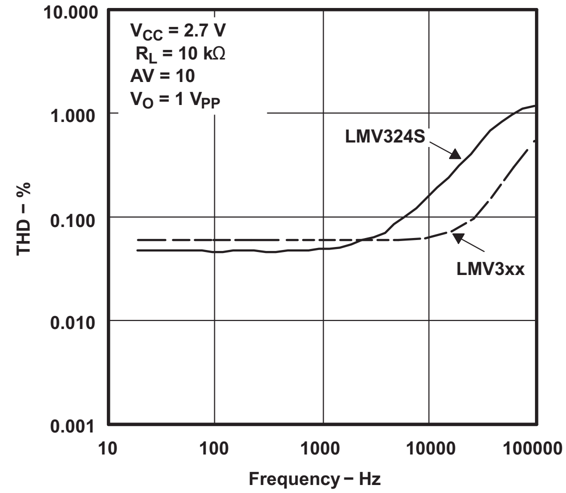



Figure 38. THD + N vs Frequency

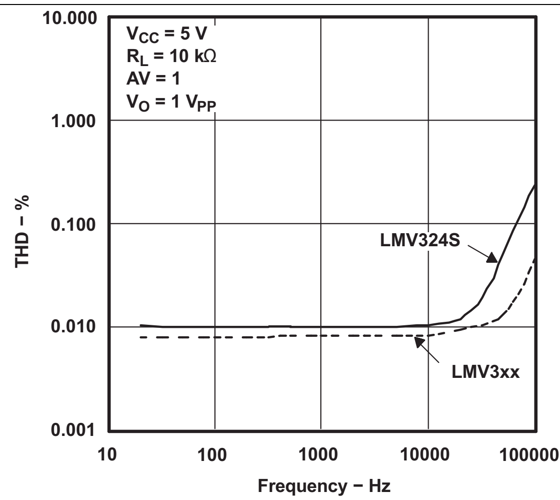



Figure 39. THD + N vs Frequency

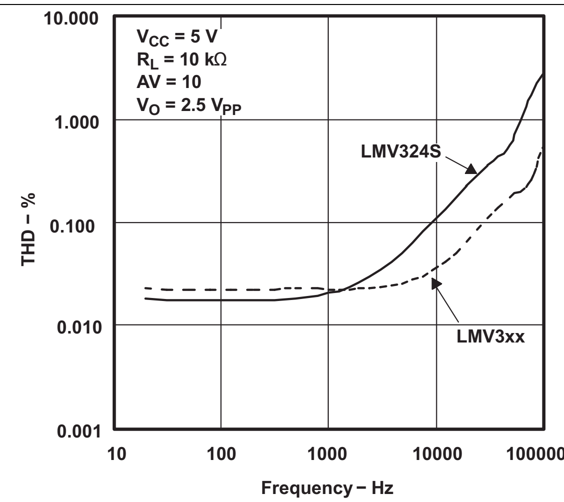



Figure 40. THD + N vs Frequency

# 7 Detailed Description

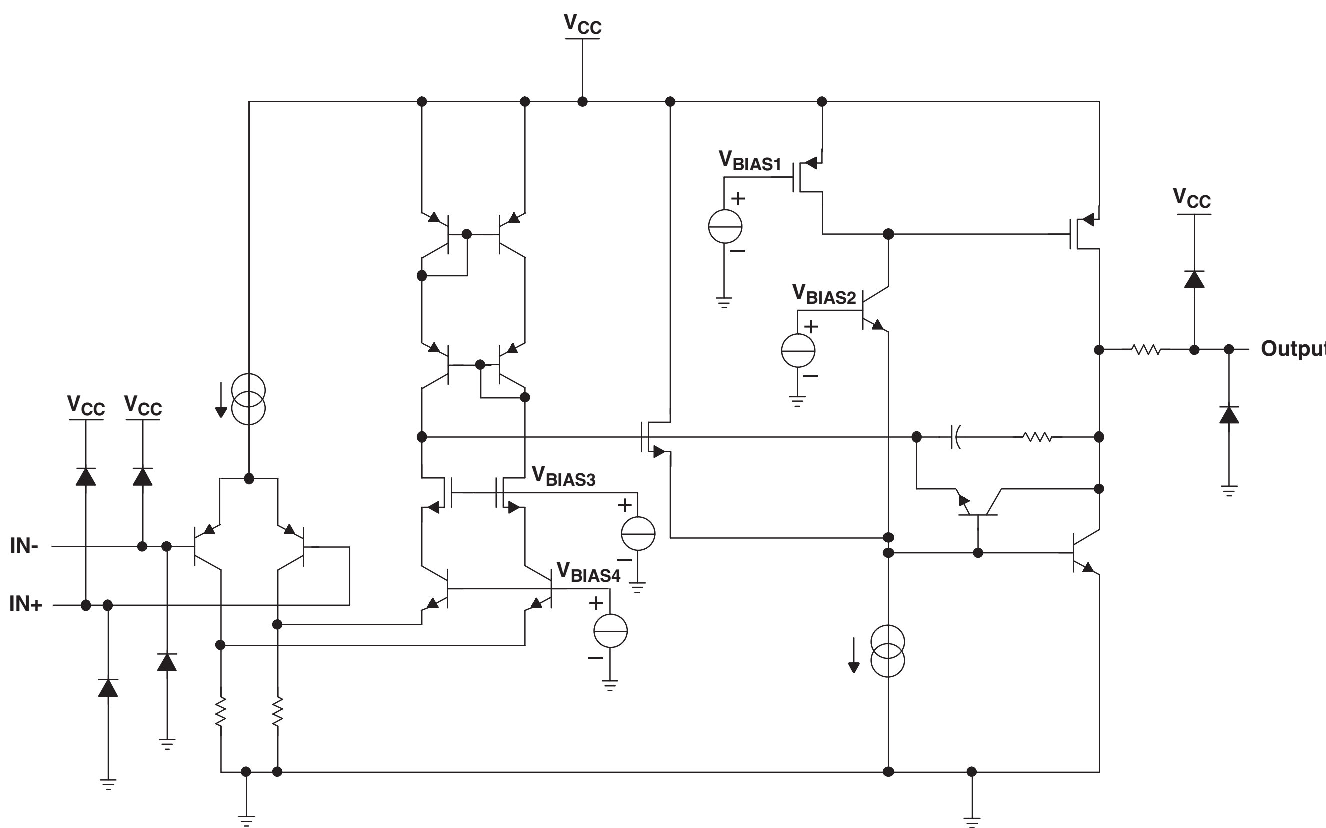
## 7.1 Overview

The LMV321, LMV358, and LMV324 devices are single, dual, and quad low-voltage (2.7 V to 5.5 V) operational amplifiers with rail-to-rail output swing.

The LMV321, LMV358, and LMV324 devices are the most cost-effective solutions for applications where low-voltage operation, space saving, and low cost are needed. These amplifiers are designed specifically for low-voltage (2.7 V to 5 V) operation, with performance specifications meeting or exceeding the LM358 and LM324 devices that operate from 5 V to 30 V. Additional features of the LMV3xx devices are a common-mode input voltage range that includes ground, 1-MHz unity-gain bandwidth, and 1-V/μs slew rate.

The LMV321 device is available in the ultra-small package, which is approximately one-half the size of the DBV (SOT-23) package. This package saves space on printed circuit boards and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Operating Voltage

The LMV321, LMV358, LMV324 devices are fully specified and ensured for operation from 2.7 V to 5 V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* graphs.

### 7.3.2 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The LMV321, LMV358, LMV324 devices have a 1-MHz unity-gain bandwidth.

### 7.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The LMV321, LMV358, LMV324 devices have a 1-V/μs slew rate.

## 7.4 Device Functional Modes

The LMV321, LMV358, LMV324 devices are powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Typical Application

Some applications require differential signals. Figure 41 shows a simple circuit to convert a single-ended input of 0.5 to 2 V into differential output of ±1.5 V on a single 2.7-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, $V_{OUT+}$. The second amplifier inverts the input and adds a reference voltage to generate $V_{OUT-}$. Both $V_{OUT+}$ and $V_{OUT-}$ range from 0.5 to 2 V. The difference, $V_{DIFF}$, is the difference between $V_{OUT+}$ and $V_{OUT-}$. The LMV358 was used to build this circuit.

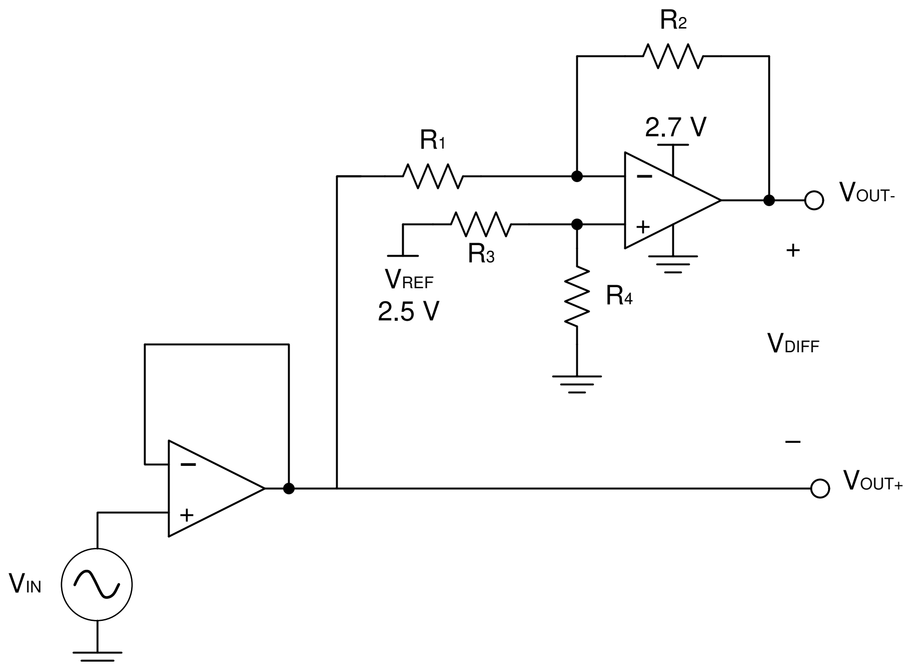



**Figure 41. Schematic for Single-Ended Input to Differential Output Conversion**

## Typical Application (continued)

### 8.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 2.7 V
- Reference voltage: 2.5 V
- Input: 0.5 to 2 V
- Output differential: ±1.5 V

### 8.1.2 Detailed Design Procedure

The circuit in Figure 41 takes a single-ended input signal, $V_{IN}$, and generates two output signals, $V_{OUT+}$ and $V_{OUT-}$ using two amplifiers and a reference voltage, $V_{REF}$. $V_{OUT+}$ is the output of the first amplifier and is a buffered version of the input signal, $V_{IN}$ (see Equation 1). $V_{OUT-}$ is the output of the second amplifier which uses $V_{REF}$ to add an offset voltage to $V_{IN}$ and feedback to add inverting gain. The transfer function for $V_{OUT-}$ is Equation 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT-} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) - V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

The differential output signal, $V_{DIFF}$, is the difference between the two single-ended output signals, $V_{OUT+}$ and $V_{OUT-}$. Equation 3 shows the transfer function for $V_{DIFF}$. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the $V_{REF}$. The differential output range is $2 \times V_{REF}$. Furthermore, the common mode voltage will be one half of $V_{REF}$ (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) \tag{3}$$

$$V_{OUT+} = V_{IN} \tag{4}$$

$$V_{OUT-} = V_{REF} - V_{IN} \tag{5}$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \tag{6}$$

$$V_{cm} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2} V_{REF} \tag{7}$$

#### *8.1.2.1 Amplifier Selection*

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Because LMV358 has a bandwidth of 1 MHz, this circuit will only be able to process signals with frequencies of less than 1 MHz.

#### *8.1.2.2 Passive Component Selection*

Because the transfer function of $V_{OUT-}$ is heavily reliant on resistors ($R_1$, $R_2$, $R_3$, and $R_4$), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 kΩ with tolerances measured to be within 2%. If the noise of the system is a key parameter, the user can select smaller resistance values (6 kΩ or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

## Typical Application (continued)

### 8.1.3 Application Curves

The measured transfer functions in Figure 42, Figure 43, and Figure 44 were generated by sweeping the input voltage from 0 V to 2.5 V. However, this design should only be used between 0.5 V and 2 V for optimum linearity.

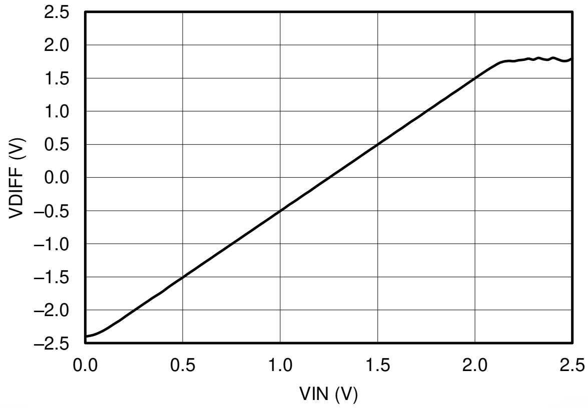



**Figure 42. Differential Output Voltage vs Input Voltage**

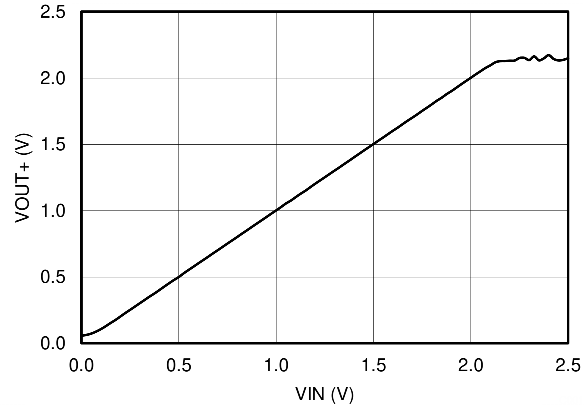



**Figure 43. Positive Output Voltage Node vs Input Voltage**

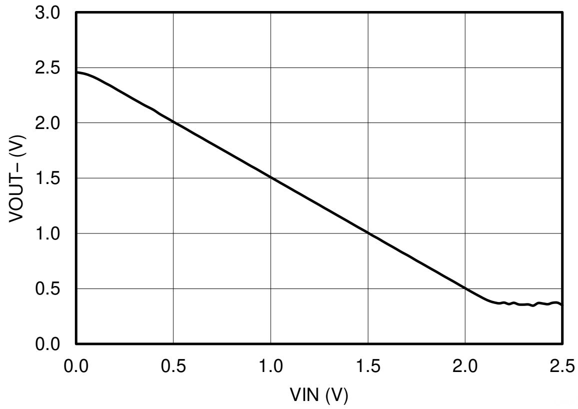



**Figure 44. Positive Output Voltage Node vs Input Voltage**

# 9 Power Supply Recommendations

The LMV321, LMV358, LMV324 devices are specified for operation from 2.7 to 5 V; many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

**CAUTION**

Supply voltages larger than 5.5 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout*.

# 10 Layout

## 10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 10.2 Layout Example

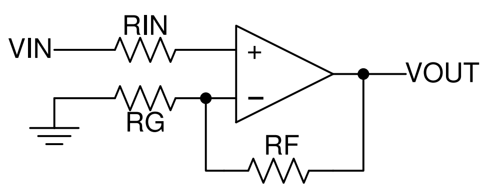



**Figure 45. Operational Amplifier Schematic for Noninverting Configuration**

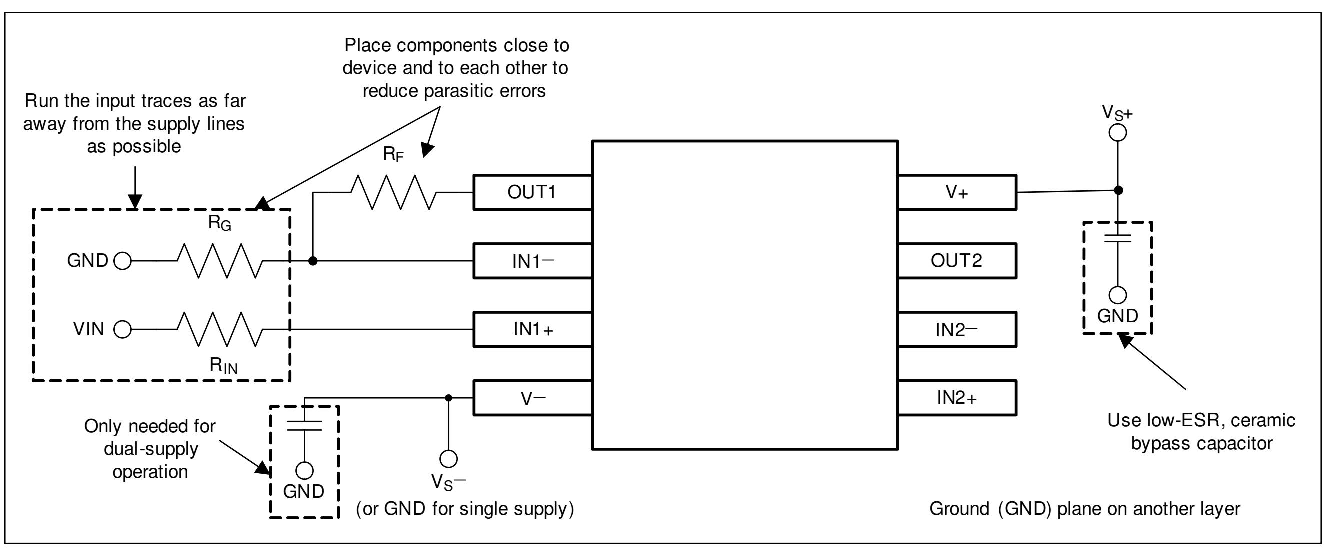



**Figure 46. Operational Amplifier Board Layout for Noninverting Configuration**

# 11 Device and Documentation Support

## 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| LMV321 | Click here | Click here | Click here | Click here | Click here |
| LMV358 | Click here | Click here | Click here | Click here | Click here |
| LMV324 | Click here | Click here | Click here | Click here | Click here |

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMV321IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RC1F, RC1K) | Samples |
| LMV321IDBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RC1F, RC1K) | Samples |
| LMV321IDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RC1F, RC1K) | Samples |
| LMV321IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RC1F, RC1K) | Samples |
| LMV321IDCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU \| SN \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | (R3F, R3K, R3O, R3 R, R3Z) | Samples |
| LMV321IDCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | (R3F, R3K, R3O, R3 R, R3Z) | Samples |
| LMV321IDCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU \| SN \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | (R3C, R3F, R3R) | Samples |
| LMV324ID | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324I | Samples |
| LMV324IDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LMV324I | Samples |
| LMV324IDRE4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324I | Samples |
| LMV324IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324I | Samples |
| LMV324IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | MV324I | Samples |
| LMV324IPWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV324I | Samples |
| LMV324IPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV324I | Samples |
| LMV324QD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324Q | Samples |
| LMV324QDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324Q | Samples |
| LMV324QDRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324Q | Samples |
| LMV324QPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV324Q | Samples |
| LMV324QPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | MV324Q | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMV324QPWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 125 | MV324Q | Samples |
| LMV358ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IDDUR | ACTIVE | VSSOP | DDU | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | RA5R | Samples |
| LMV358IDDURG4 | ACTIVE | VSSOP | DDU | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | RA5R | Samples |
| LMV358IDG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | (R5B, R5Q, R5R) | Samples |
| LMV358IDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | (R5B, R5Q, R5R) | Samples |
| LMV358IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IDRE4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IPW | ACTIVE | TSSOP | PW | 8 | 150 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IPWG4 | ACTIVE | TSSOP | PW | 8 | 150 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | MV358I | Samples |
| LMV358IPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358QD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358Q | Samples |
| LMV358QDDUR | ACTIVE | VSSOP | DDU | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | RAHR | Samples |
| LMV358QDG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358Q | Samples |
| LMV358QDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | (RHO, RHR) | Samples |
| LMV358QDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | (RHO, RHR) | Samples |
| LMV358QDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358Q | Samples |
| LMV358QPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | MV358Q | Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

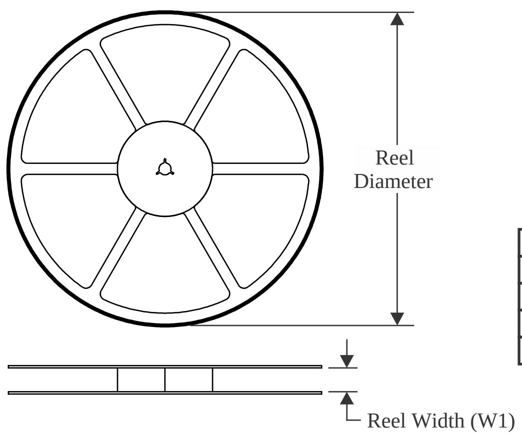
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

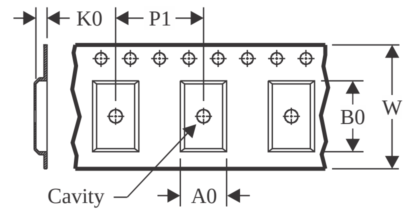
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

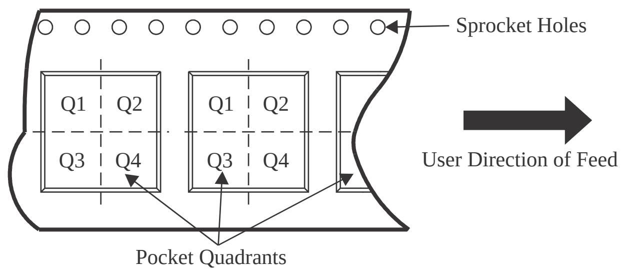



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

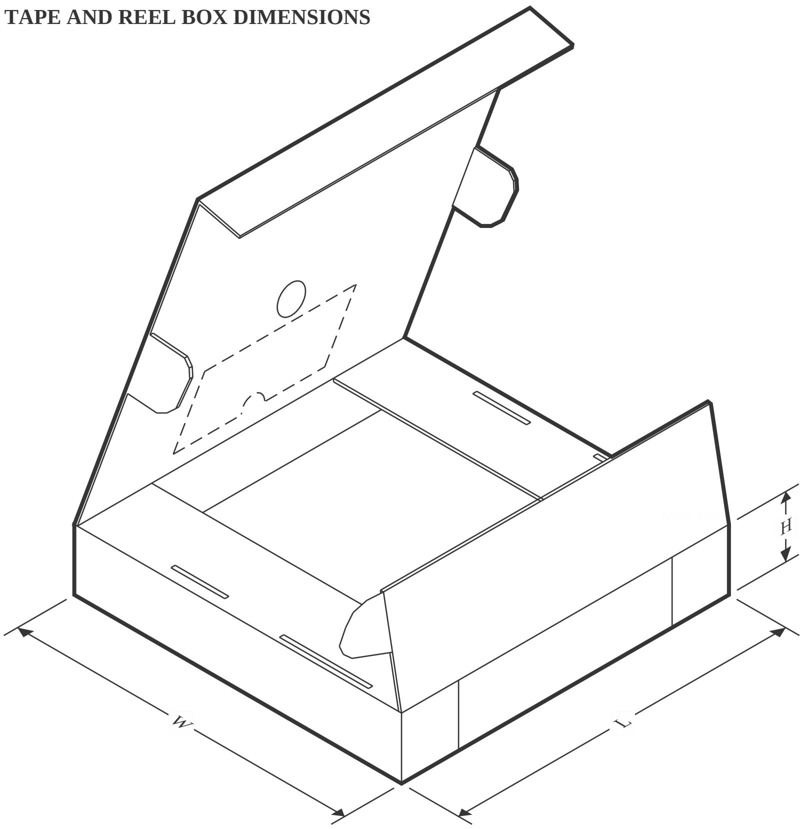



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMV321IDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| LMV321IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMV321IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMV321IDBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| LMV321IDCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| LMV321IDCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| LMV321IDCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| LMV321IDCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| LMV324IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LMV324IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LMV324IDR | SOIC | D | 14 | 2500 | 330.0 | 16.8 | 6.5 | 9.5 | 2.1 | 8.0 | 16.0 | Q1 |
| LMV324IDRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LMV324IDRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LMV324IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LMV324IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LMV324IPWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMV324QDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LMV324QPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LMV324QPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LMV358IDDUR | VSSOP | DDU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| LMV358IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMV358IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMV358IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMV358IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LMV358IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LMV358IDR | SOIC | D | 8 | 2500 | 330.0 | 12.8 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LMV358IDRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LMV358IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LMV358IPWRG4 | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LMV358QDDUR | VSSOP | DDU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| LMV358QDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMV358QDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMV358QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LMV358QPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

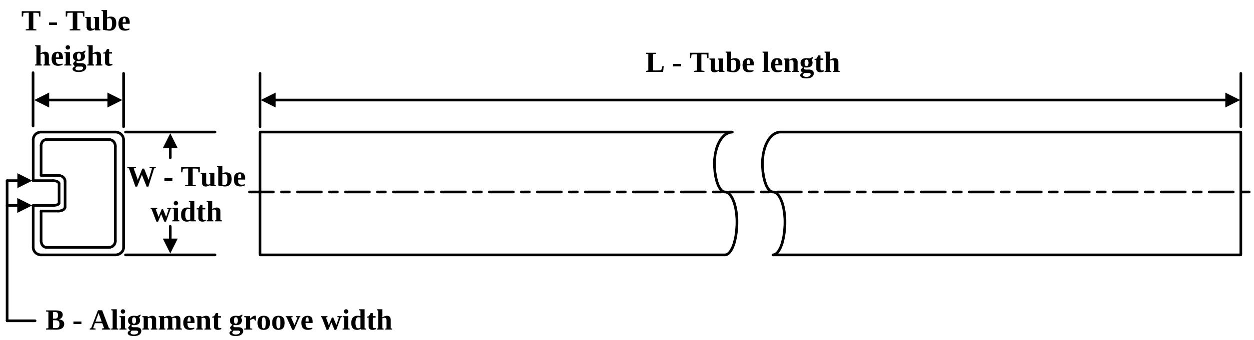



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMV321IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| LMV321IDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LMV321IDBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| LMV321IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| LMV321IDCKR | SC70 | DCK | 5 | 3000 | 190.0 | 190.0 | 30.0 |
| LMV321IDCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| LMV321IDCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| LMV321IDCKT | SC70 | DCK | 5 | 250 | 190.0 | 190.0 | 30.0 |
| LMV324IDR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| LMV324IDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| LMV324IDR | SOIC | D | 14 | 2500 | 364.0 | 364.0 | 27.0 |
| LMV324IDRG4 | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| LMV324IDRG4 | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| LMV324IPWR | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| LMV324IPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| LMV324IPWRG4 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| LMV324QDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| LMV324QPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |

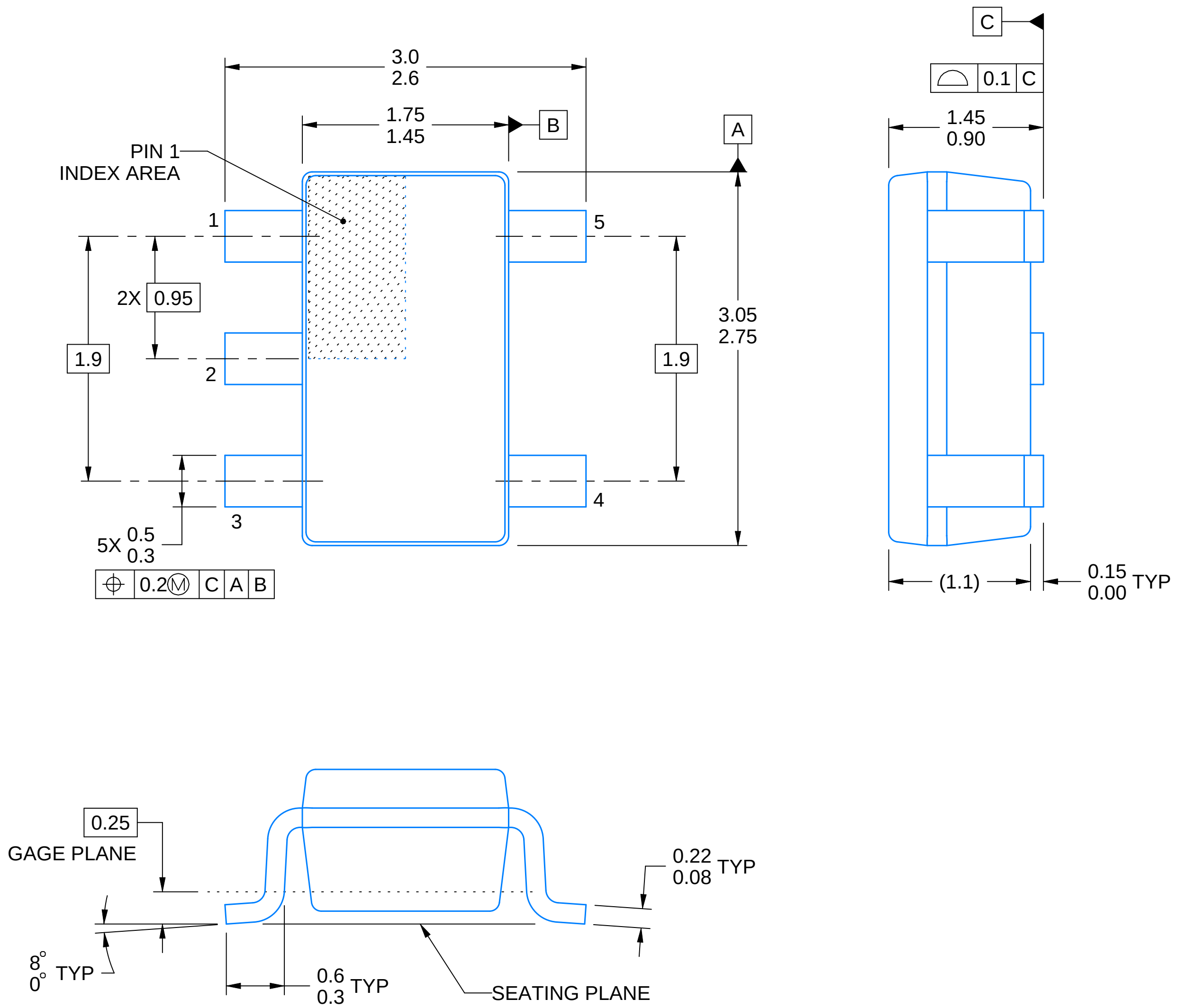
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMV324QPWR | TSSOP | PW | 14 | 2000 | 366.0 | 364.0 | 50.0 |
| LMV358IDDUR | VSSOP | DDU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| LMV358IDGKR | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| LMV358IDGKR | VSSOP | DGK | 8 | 2500 | 370.0 | 355.0 | 55.0 |
| LMV358IDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| LMV358IDR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| LMV358IDR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| LMV358IDR | SOIC | D | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| LMV358IDRG4 | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| LMV358IPWR | TSSOP | PW | 8 | 2000 | 366.0 | 364.0 | 50.0 |
| LMV358IPWRG4 | TSSOP | PW | 8 | 2000 | 356.0 | 356.0 | 35.0 |
| LMV358QDDUR | VSSOP | DDU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| LMV358QDGKR | VSSOP | DGK | 8 | 2500 | 370.0 | 355.0 | 55.0 |
| LMV358QDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| LMV358QDR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| LMV358QPWR | TSSOP | PW | 8 | 2000 | 366.0 | 364.0 | 50.0 |

## TUBE




*All dimensions are nominal

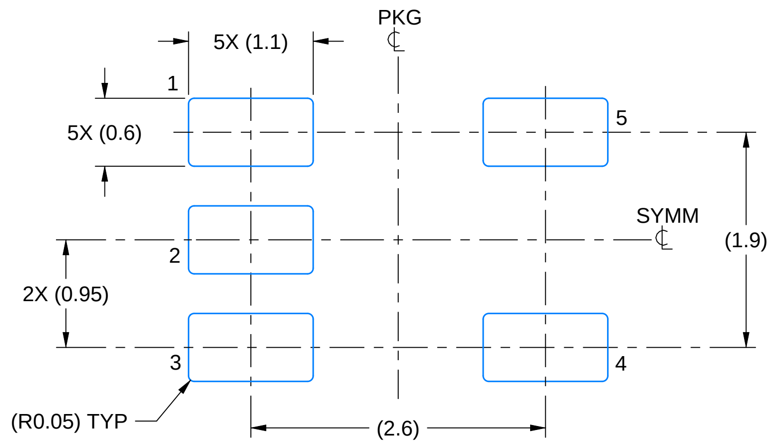
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LMV324ID | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| LMV324QD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| LMV324QPW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| LMV358ID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| LMV358ID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| LMV358IDG4 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| LMV358IDG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| LMV358IPW | PW | TSSOP | 8 | 150 | 530 | 10.2 | 3600 | 3.5 |
| LMV358IPWG4 | PW | TSSOP | 8 | 150 | 530 | 10.2 | 3600 | 3.5 |
| LMV358QD | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| LMV358QDG4 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |



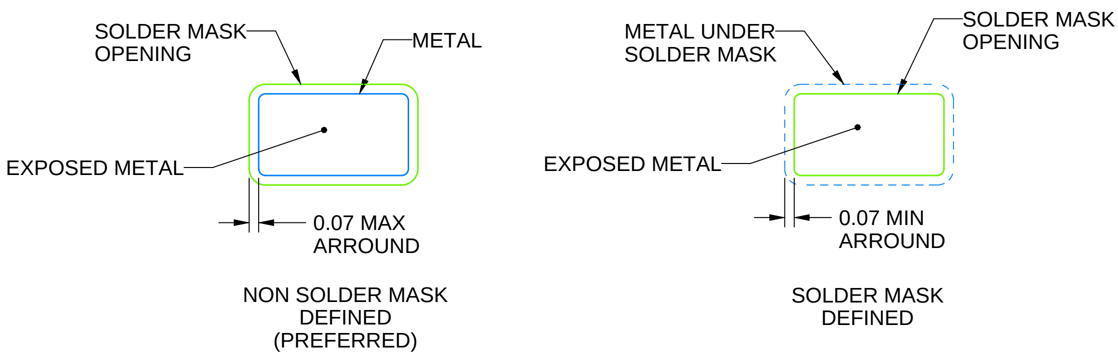

4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

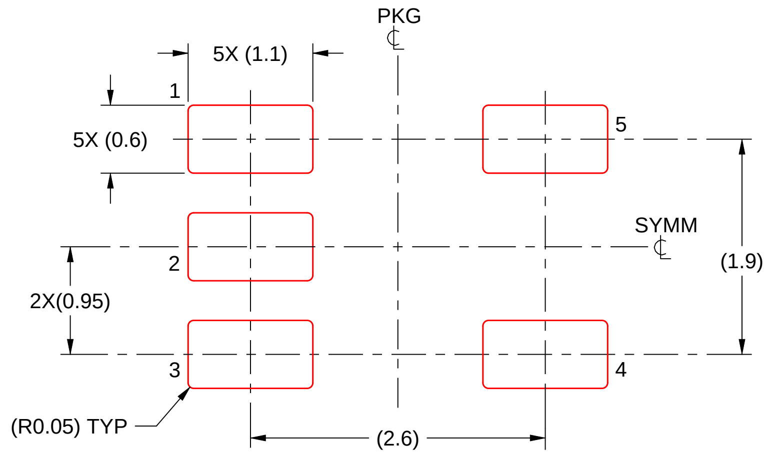



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



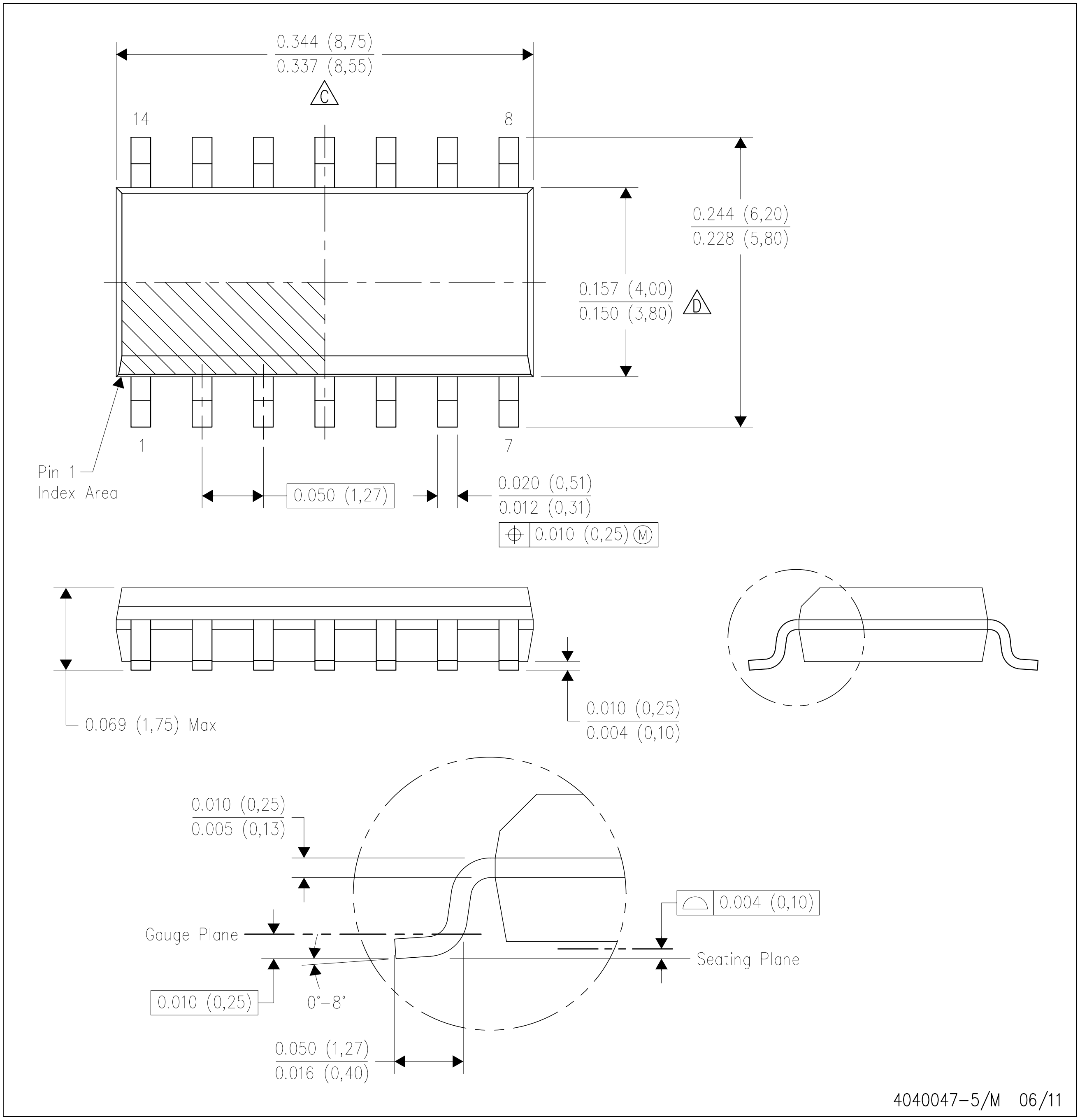

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

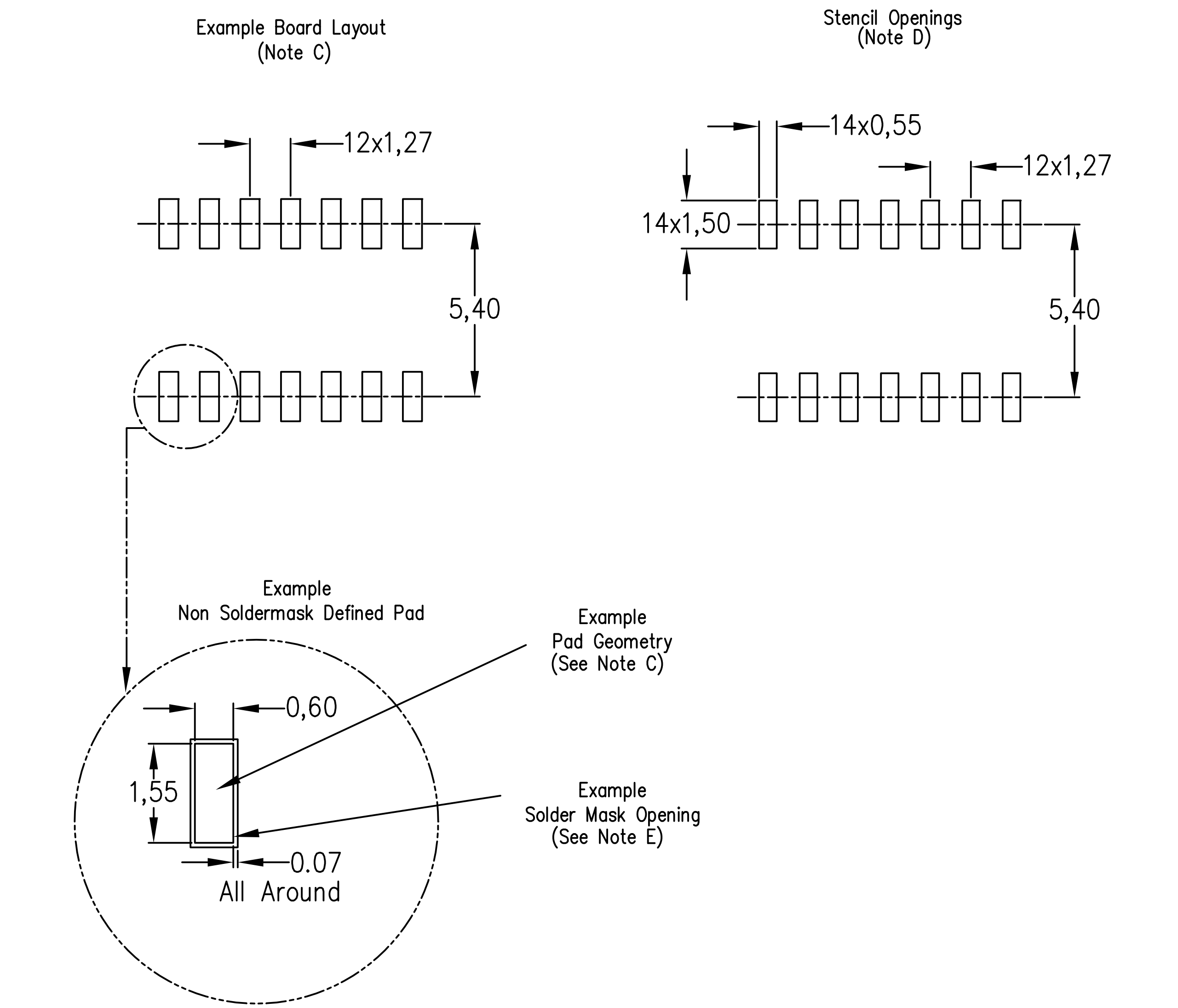
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE




NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

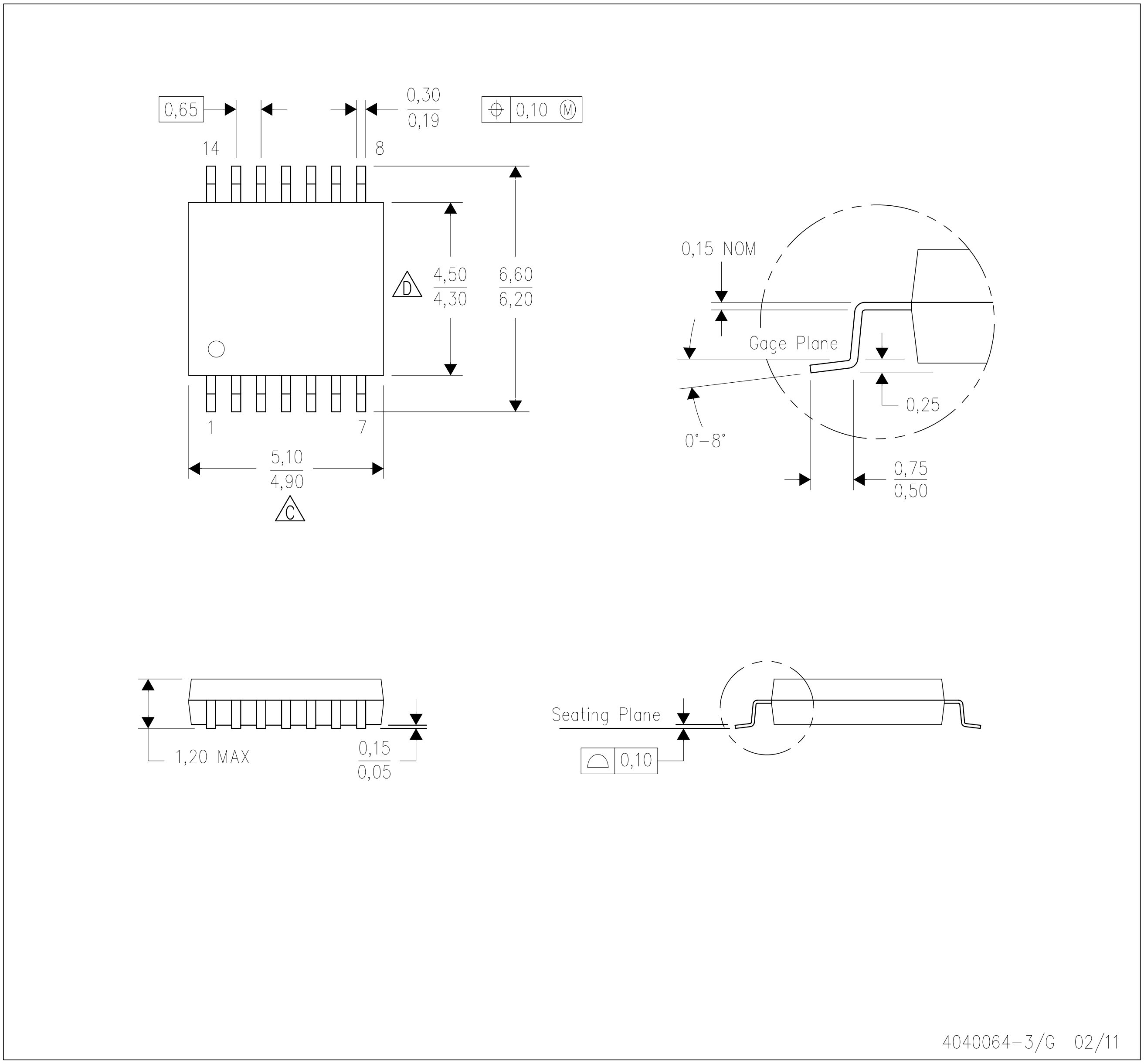
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4211283–3/E 08/12

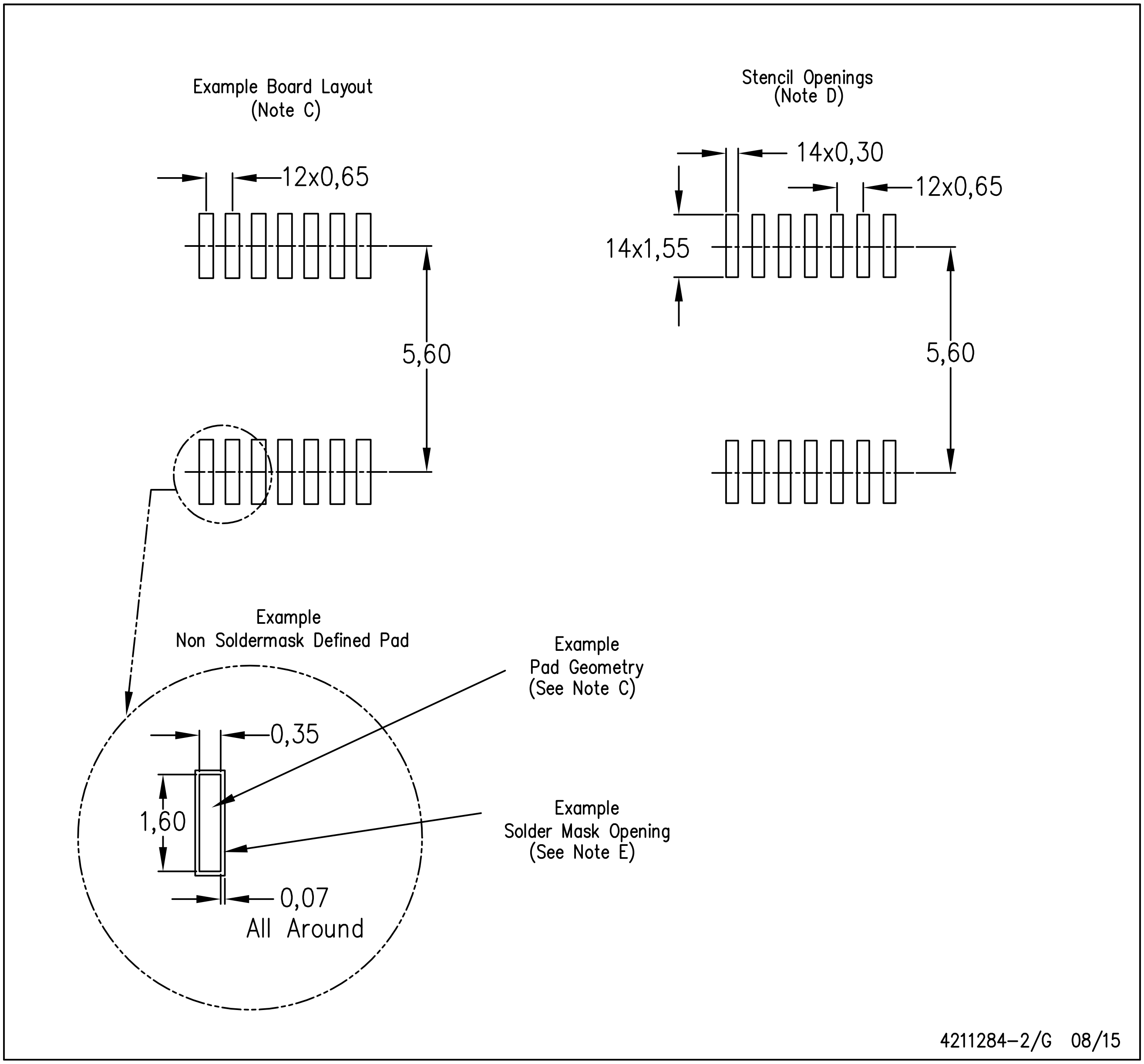
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

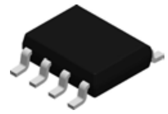



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

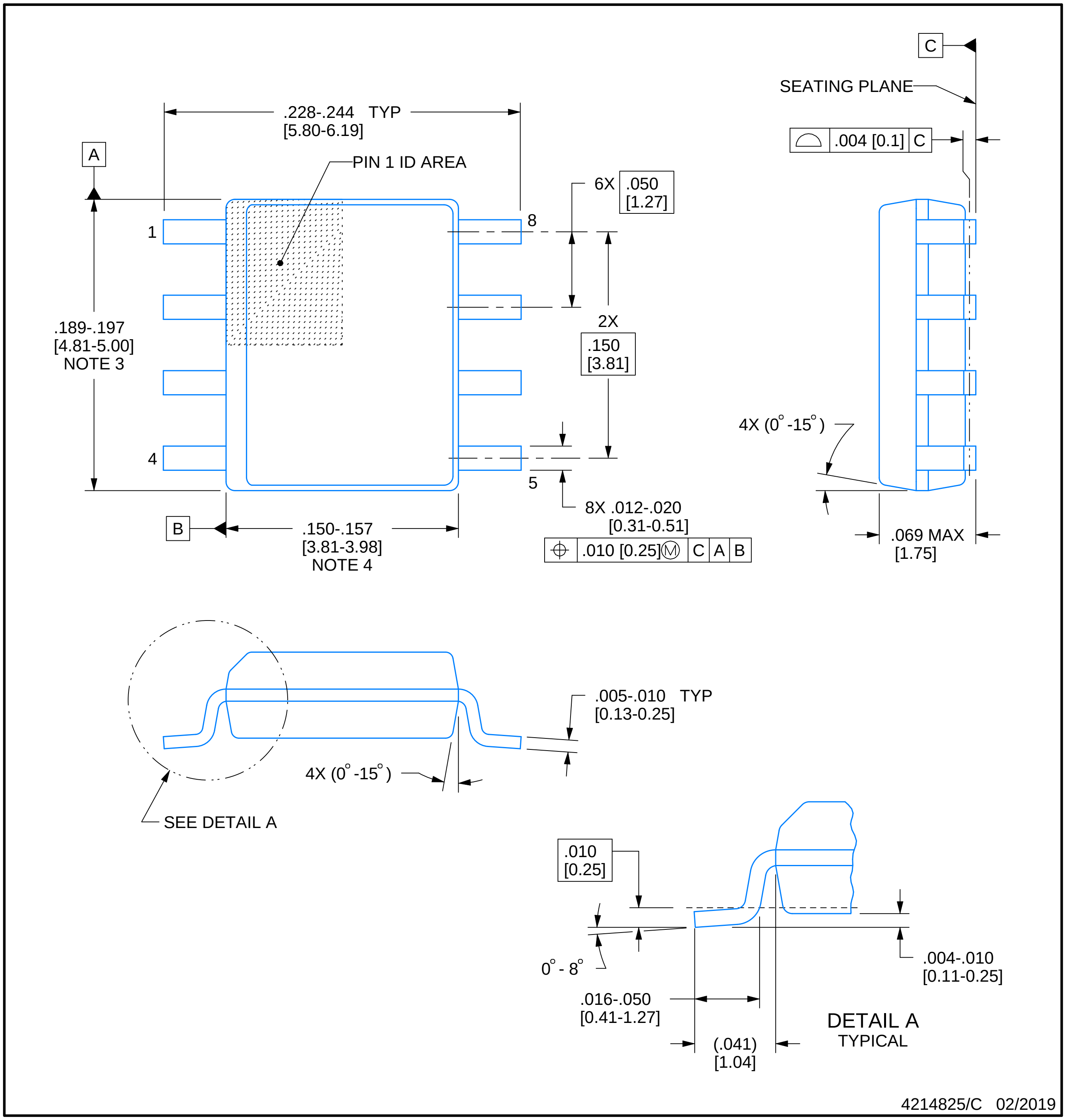


# PACKAGE OUTLINE

## D0008A

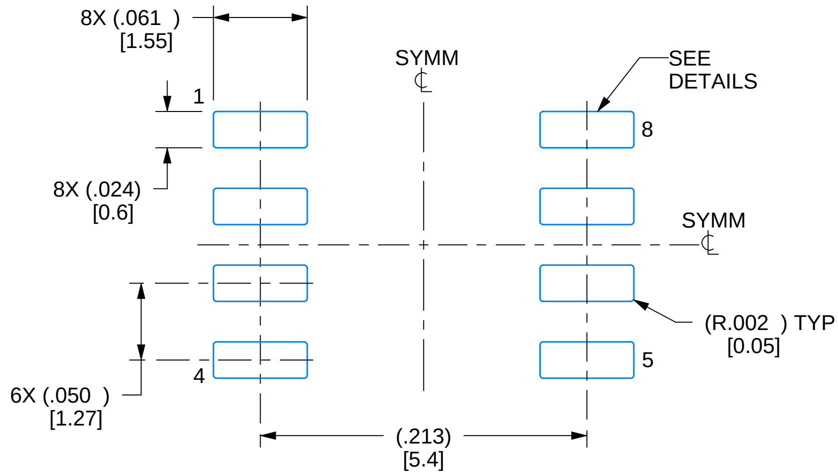
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

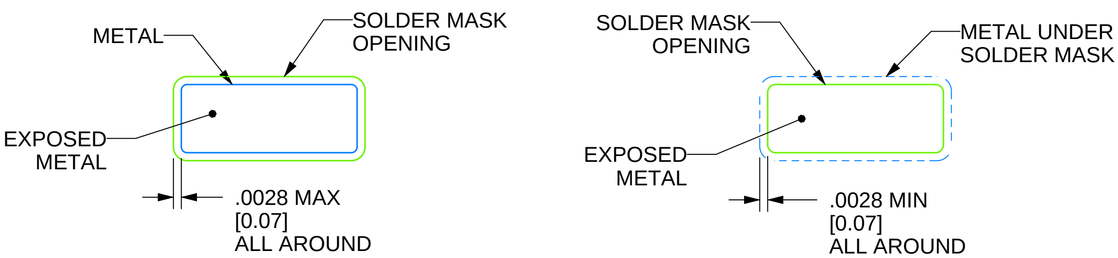



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




NON SOLDER MASK
DEFINED

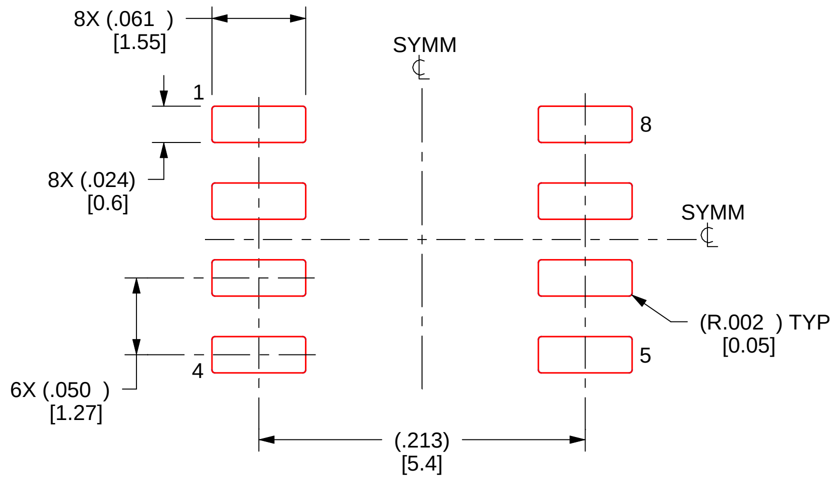
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



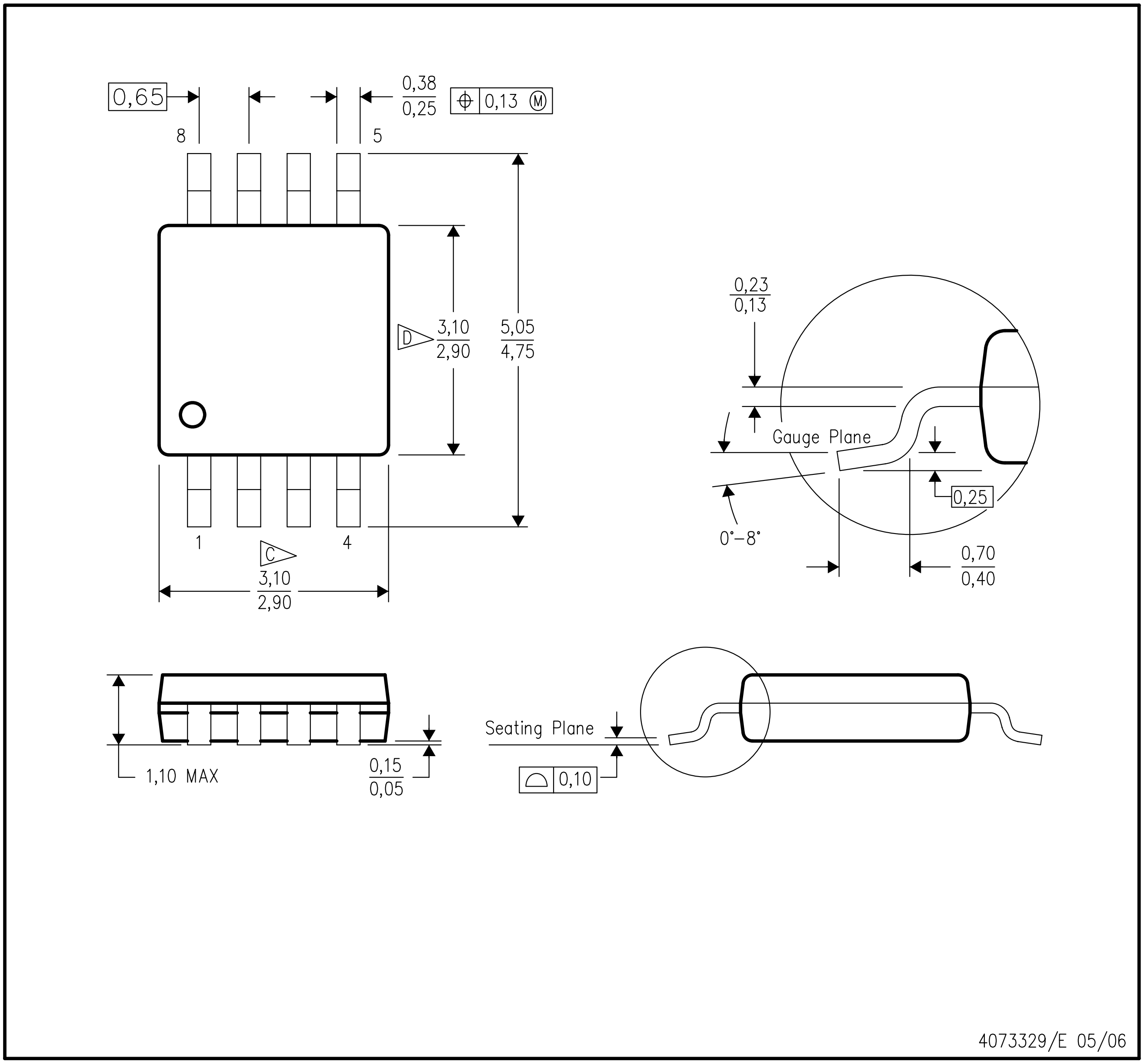

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

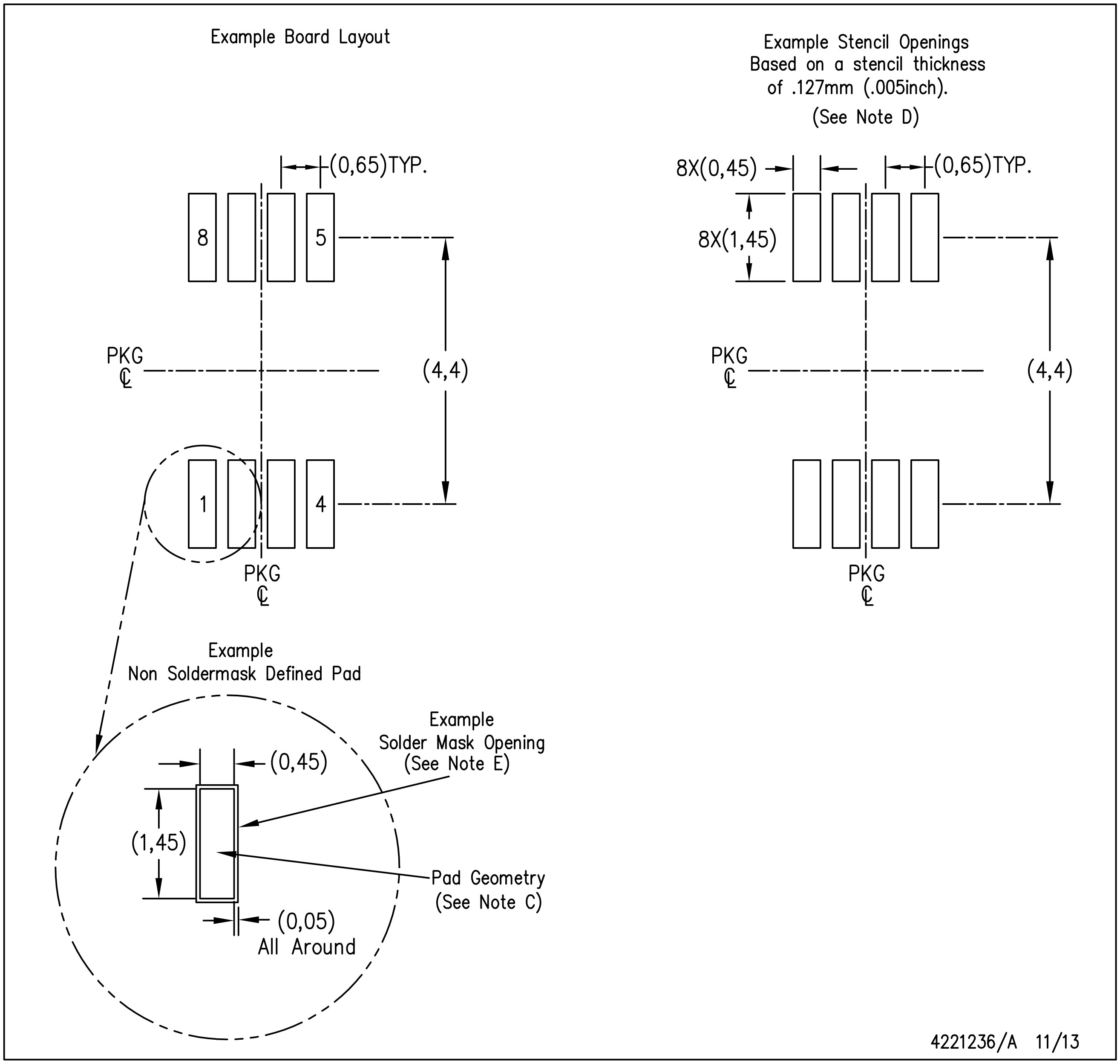
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE

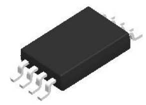



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



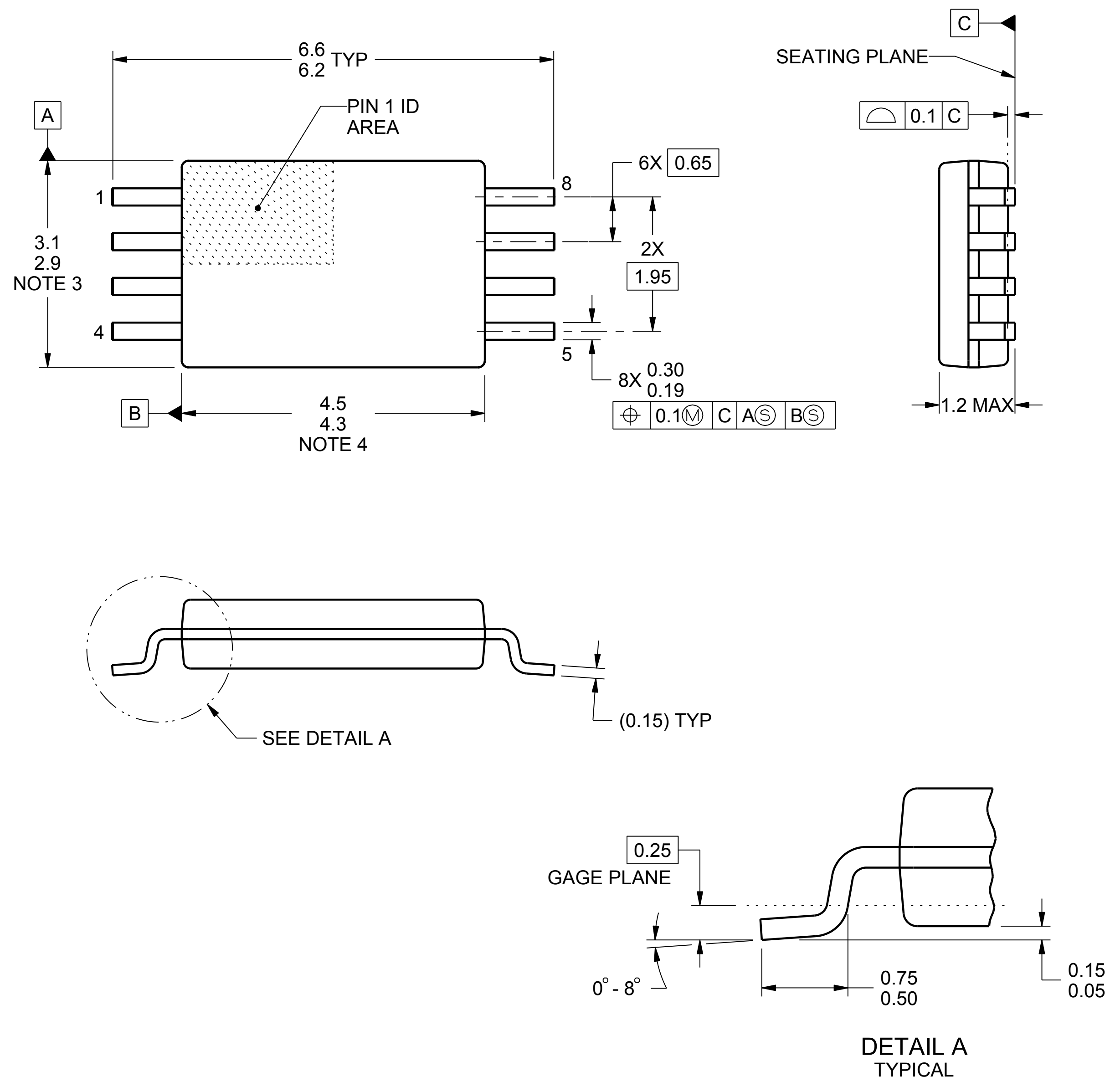

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

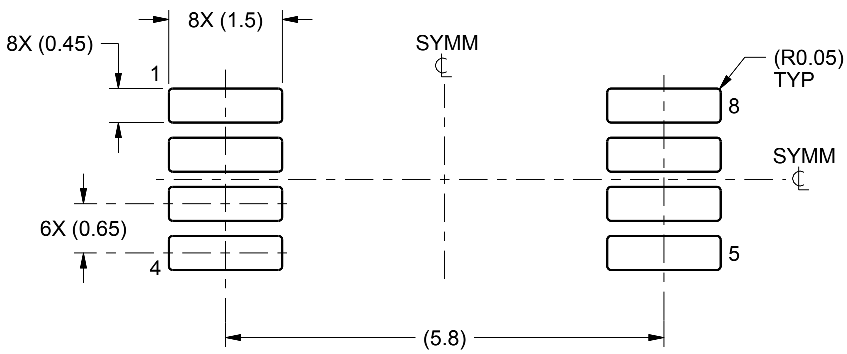
SMALL OUTLINE PACKAGE



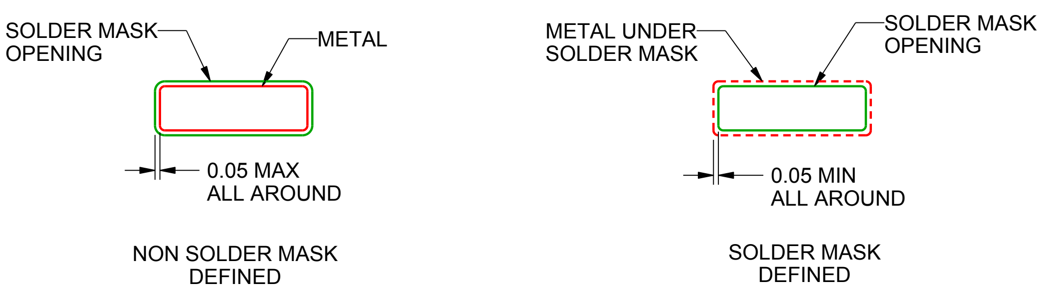

4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.




LAND PATTERN EXAMPLE
SCALE:10X

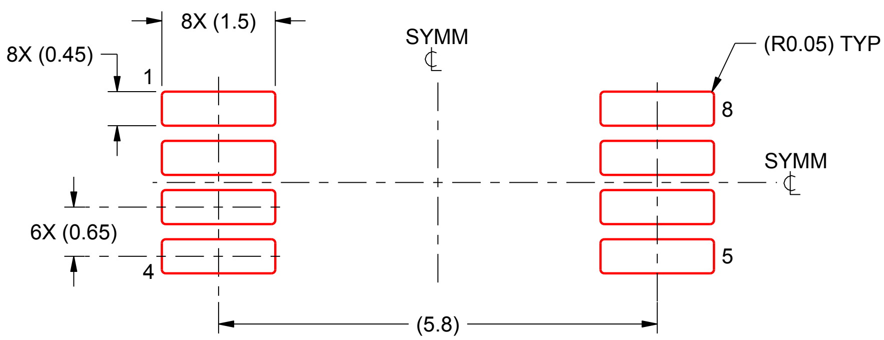



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



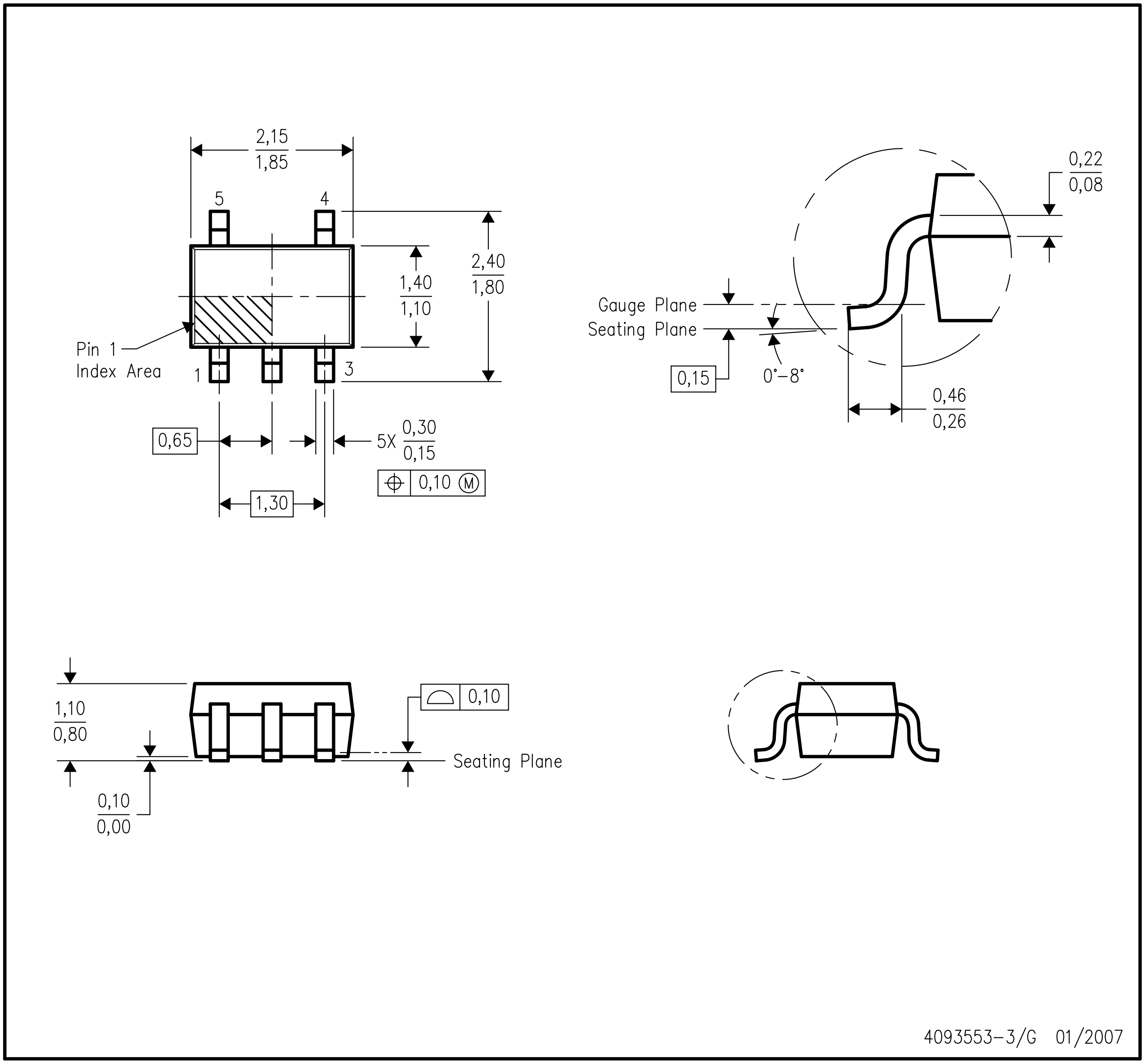

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

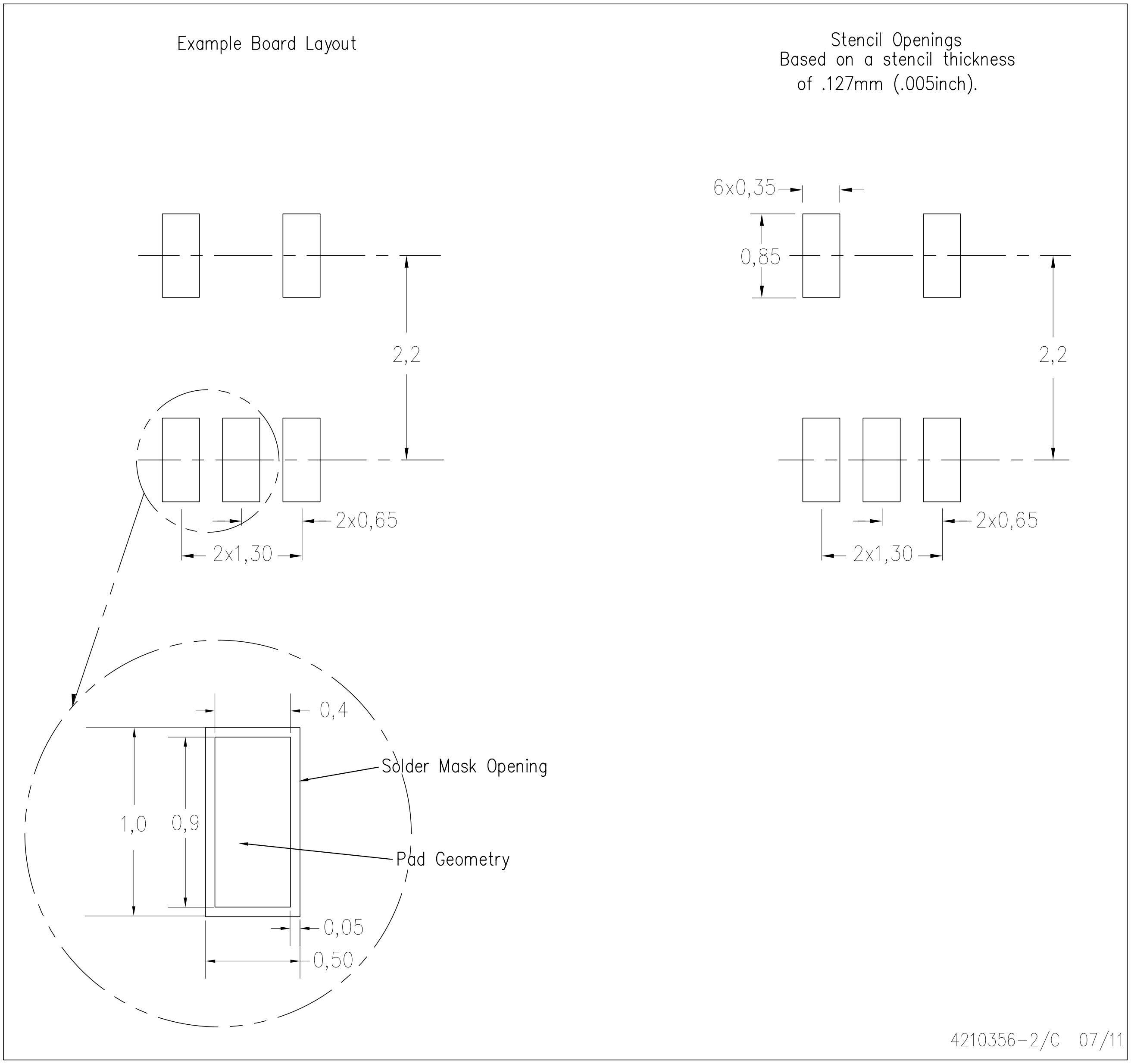
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



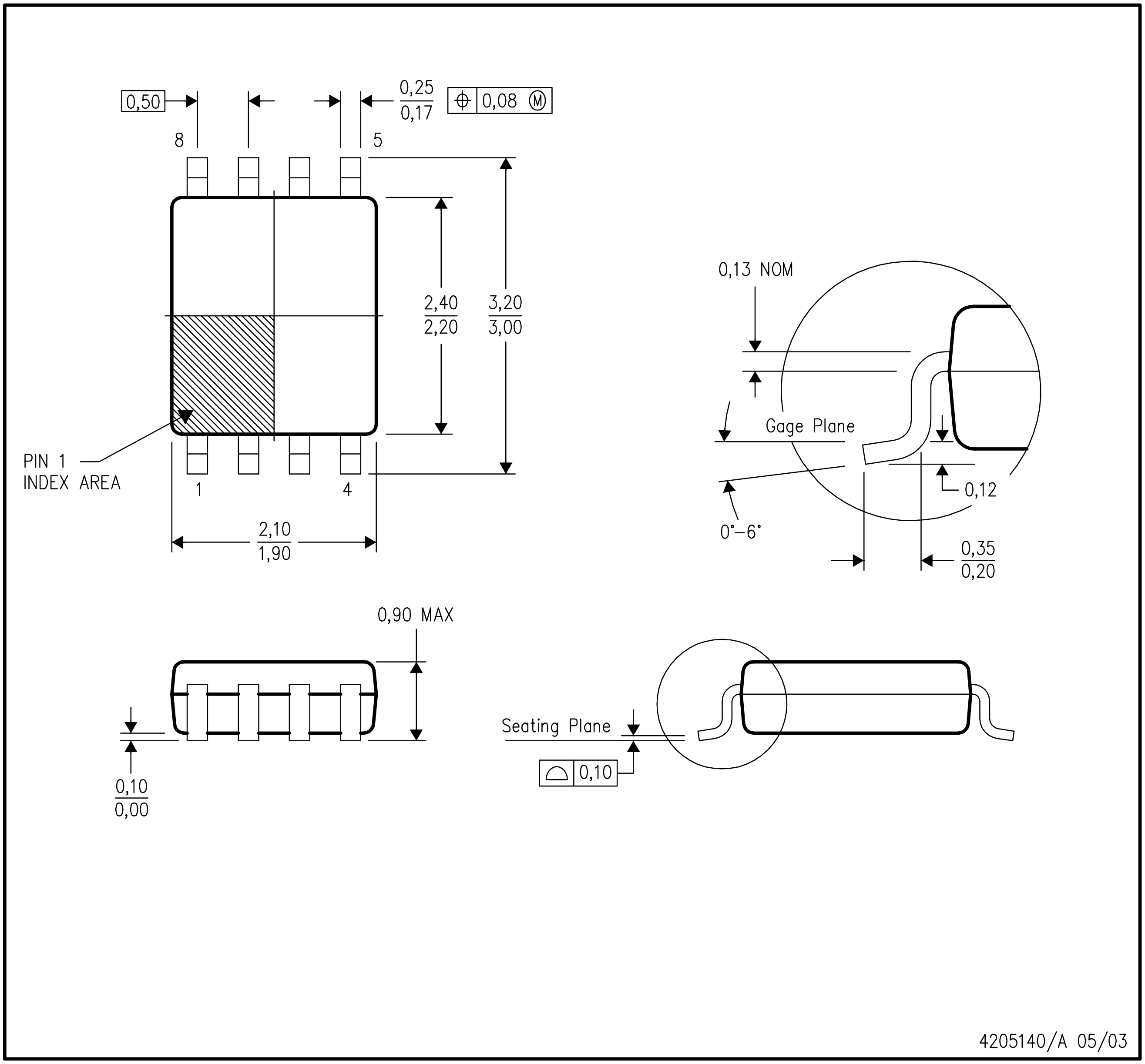

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



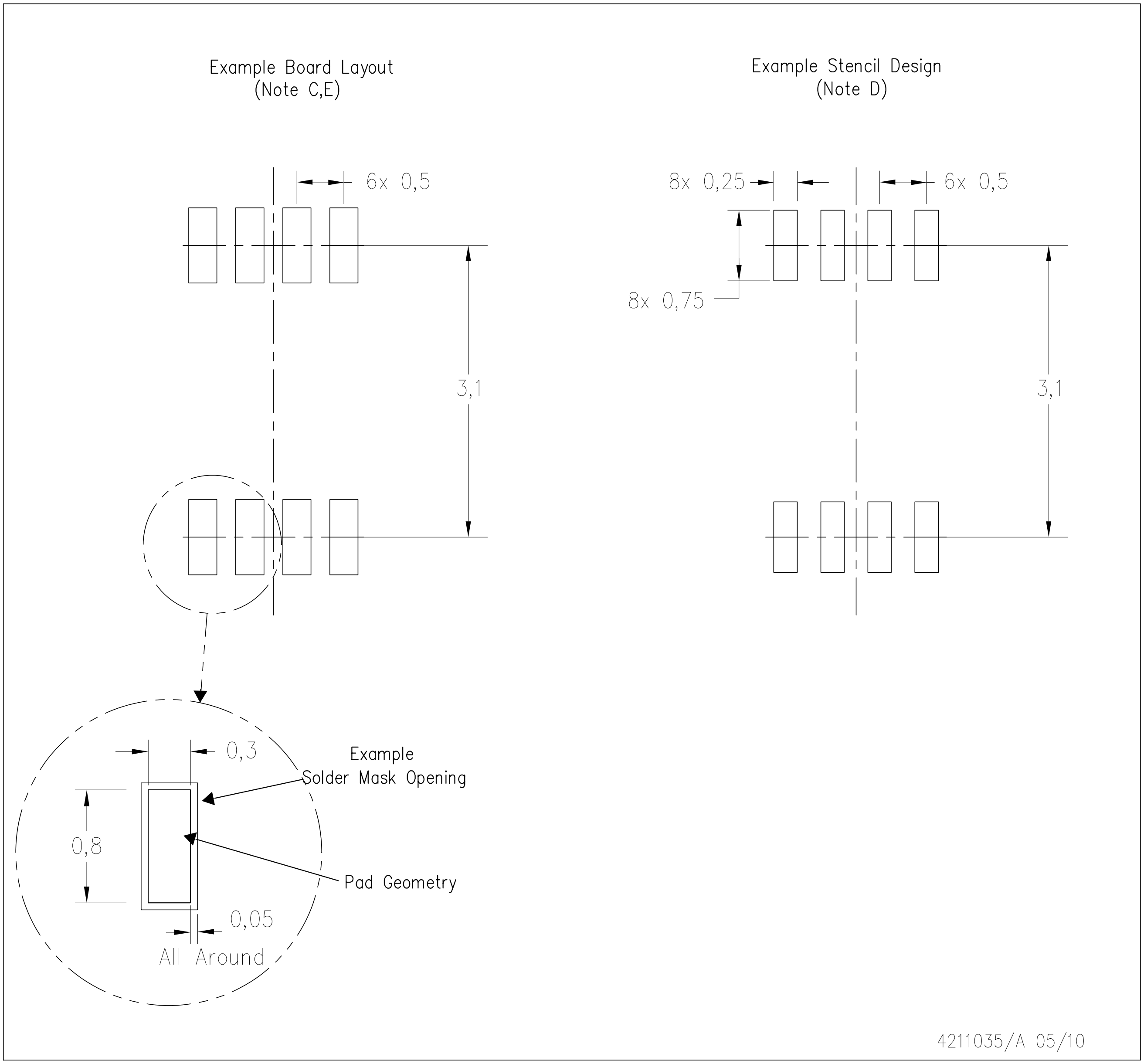

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DDU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation CA.

DDU (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE (DIE UP)




NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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