Table H.1 (H.11.12.7 of edition 3) – Acceptable measures to address fault/errors [a] *(1 of 6)*

Component [b]	Fault/error	Software class		Example of acceptable measures [c d e]	Definitions
		B	C		
1. CPU					
1.1					
Registers	Stuck at	rq		Functional test, or	H.2.16.5
				periodic self-test using either:	H.2.16.6
				– **static memory test**, or	H.2.19.6
				– **word protection with single bit redundancy**	H.2.19.8.2
	DC **fault**		rq	Comparison of redundant CPUs by either:	
				– **reciprocal comparison**	H.2.18.15
				– **independent** hardware **comparator**, or	H.2.18.3
				internal error detection, or	H.2.18.9
				redundant memory with comparison, or	H.2.19.5
				periodic self-tests using either	
				– **walkpat memory test**	H.2.19.7
				– **Abraham test**	H.2.19.1
				– **transparent GALPAT test**; or	H.2.19.2.1
				word protection with multi-bit redundancy, or	H.2.19.8.1
				static memory test and word protection	H.2.19.6
				with single bit redundancy	H.2.19.8.2
1.2					
Instruction	Wrong		rq	Comparison of redundant CPUs by either:	
decoding and	decoding			– **reciprocal comparison**	H.2.18.15
execution	and execution			– **independent** hardware **comparator**, or	H.2.18.3
				internal error detection, or	H.2.18.9
				periodic self-test using **equivalence class test**	H.2.18.5
1.3				Functional test, or	H.2.16.5
Programme	Stuck at	rq		periodic self-test, or	H.2.16.6
counter				**independent time-slot monitoring of the program sequence**, or	H.2.18.10.4
				logical monitoring of the programme sequence	H.2.18.10.2
				Periodic self-test and monitoring using either:	H.2.16.7
	DC **fault**		rq	– **independent time-slot and logical monitoring**	H.2.18.10.3
				– **internal error detection**, or	H.2.18.9
				comparison of redundant functional channels by either:	
				– **reciprocal comparison**	H.2.18.15
				– **independent** hardware **comparator**	H.2.18.3

Table H.1 *(2 of 6)*

Component [b]	Fault/error	Software class		Example of acceptable measures [c d e]	Definitions
		B	C		
1.4 Addressing	DC **fault**		rq	Comparison of redundant CPUs by either: – **reciprocal comparison** – **independent** hardware **comparator**; or **Internal error detection**; or periodic self-test using a **testing pattern** of the address lines; or **full bus redundancy**, or **multi-bit bus parity**	 H.2.18.15 H.2.18.3 H.2.18.9 H.2.16.7 H.2.18.22 H.2.18.1.1 H.2.18.1.2
1.5 Data paths instruction decoding	DC **fault** and execution		rq	Comparison of redundant CPUs by either: **reciprocal comparison**, or **independent** hardware **comparator**, or **Internal error detection**, or periodic self-test using a **testing pattern**, or **data redundancy**, or **multi-bit bus parity**	 H.2.18.15 H.2.18.3 H.2.18.9 H.2.16.7 H.2.18.2.1 H.2.18.1.2
2. Interrupt handling and execution	No interrupt or too frequent interrupt	rq		Functional test; or time-slot monitoring	H.2.16.5 H.2.18.10.4
	No interrupt or too frequent interrupt related to different sources		rq	Comparison of redundant functional channels by either **reciprocal comparison**, **independent** hardware **comparator**, or **Independent time-slot and logical monitoring**	 H.2.18.15 H.2.18.3 H.2.18.10.3

Table H.1 *(3 of 6)*

Component [b]	Fault/error	Software class		Example of acceptable measures [c d e]	Definitions
		B	C		
3. Clock		rq		**Frequency monitoring**, or	H.2.18.10.1
				time slot monitoring	H.2.18.10.4
	Wrong frequency (for quartz synchronized clock: harmonics/ subharmonics only)		rq	**Frequency monitoring**, or	H.2.18.10.1
				time-slot monitoring, or	H.2.18.10.4
				comparison of redundant functional channels by either:	
				– **reciprocal comparison**	H.2.18.15
				– **independent** hardware **comparator**	H.2.18.3
4. Memory					
4.1 **Invariable memory**	All single bit **faults**	rq		Periodic **modified checksum**; or	H.2.19.3.1
				multiple checksum, or	H.2.19.3.2
				word protection with single bit redundancy	H.2.19.8.2
	99,6 % coverage of all information errors		rq	Comparison of redundant CPUs by either:	
				– **reciprocal comparison**	H.2.18.15
				– **independent** hardware **comparator**, or	H.2.18.3
				redundant memory with comparison, or	H.2.19.5
				periodic cyclic redundancy check, either	
				– single word	H.2.19.4.1
				– double word, or	H.2.19.4.2
				word protection with multi-bit redundancy	H.2.19.8.1
4.2 Variable memory	DC **fault**	rq		Periodic **static memory test**, or	H.2.19.6
				word protection with single bit redundancy	H.2.19.8.2
	DC **fault** and dynamic cross links		rq	Comparison of redundant CPUs by either:	
				– **reciprocal comparison**	H.2.18.15
				– **independent** hardware **comparator**, or	H.2.18.3
				redundant memory with comparison, or	H.2.19.5
				periodic self-tests using either:	
				– **walkpat memory test**	H.2.19.7
				– **Abraham test**	H.2.19.1
				– **transparent GALPAT test**, or	H.2.19.2.1
				word protection with multi-bit redundancy	H.2.19.8.1

Table H.1 *(4 of 6)*

Component [b]	Fault/error	Software class		Example of acceptable measures [c d e]	Definitions
		B	C		
4.3 Addressing (relevant to **variable memory** and **invariable memory**)	Stuck at	rq		**Word protection with single bit redundancy** including the address, or	H.2.19.18.2
	DC **fault**		rq	comparison of redundant CPUs by either:	
				– **reciprocal comparison**, or	H.2.18.15
				– **independent** hardware **comparator**, or	H.2.18.3
				full bus redundancy	H.2.18.1.1
				Testing pattern, or	
				periodic cyclic redundancy check, either:	H.2.18.22
				– single word	H.2.19.4.1
				– double word, or	H.2.19.4.2
				word protection with multi-bit redundancy including the address	H.2.19.8.1
5. Internal data path					
5.1 Data	Stuck at	rq		**Word protection with single bit redundancy**	H.2.19.8.2
	DC **fault**		rq	Comparison of redundant CPUs by either:	
				– **reciprocal comparison**	H.2.18.15
				– **independent** hardware **comparator**, or	H.2.18.3
				word protection with multi-bit redundancy	H.2.19.8.1
				including the address, or **data redundancy**, or	H.2.18.2.1
				testing pattern, or	H.2.18.22
				protocol test	H.2.18.14
5.2 Addressing	Wrong address	rq		**Word protection with single bit redundancy** including the address	H.2.19.8.2
	Wrong		rq	Comparison of redundant CPUs by:	
	address and			– **reciprocal comparison**	H.2.18.15
	multiple			– **independent** hardware **comparator**, or	H.2.18.3
	addressing			**word protection with multi-bit redundancy**, including the address, or **full bus redundancy**; or **testing pattern** including the address	H.2.19.8.1 H.2.18.1.1 H.2.18.22
6 External communication	**Hamming distance** 3	rq		**Word protection with multi-bit redundancy**, or **CRC – single word** , or	H.2.19.8.1 H.2.19.4.1
				transfer redundancy, or	H.2.18.2.2
				protocol test	H.2.18.14

Table H.1 *(5 of 6)*

Component [b]	Fault/error	Software class		Example of acceptable measures [c d e]	Definitions
		B	C		
6.1 Data	**Hamming distance** 4		rq	**CRC – double word**, or	H.2.19.4.2
				data redundancy or comparison of redundant functional channels by either:	H.2.18.2.1
				– **reciprocal comparison**	H.2.18.15
				– **independent** hardware **comparator**	H.2.18.3
6.2 Addressing	Wrong address	rq		**Word protection with multi-bit redundancy**, including the address, or **CRC – single word** including the addresses, or	H.2.19.8.1 H.2.19.4.1
				transfer redundancy or	H.2.18.2.2
				protocol test	H.2.18.14
	Wrong and multiple addressing		rq	**CRC – double word**, including the address, or **full bus redundancy** of data and address, or comparison of redundant communication channels by either:	H.2.19.4.2 H.2.18.1.1
				– **reciprocal comparison**	H.2.18.15
				– **independent** hardware **comparator**	H.2.18.3
6.3 Timing	Wrong point in time	rq		Time-slot monitoring, or **scheduled transmission**	H.2.18.10.4 H.2.18.18
			rq	**Time-slot and logical monitoring**, or comparison of redundant communication channels by either:	H.2.18.10.3
				– **reciprocal comparison**	H.2.18.15
				– **independent** hardware **comparator**	H.2.18.3
	Wrong sequence	rq		Logical monitoring, or time-slot monitoring, or **scheduled transmission**	H.2.18.10.2 H.2.18.10.4 H.2.18.18
			rq	(same options as for wrong point in time)	
7. Input/output periphery 7.1 Digital I/O	**Fault** conditions specified in Clause H.27	rq		**Plausibility check**	H.2.18.13
			rq	Comparison of redundant CPUs by either:	
				– **reciprocal comparison**	H.2.18.15
				– **independent** hardware **comparator**, or	H.2.18.3
				input comparison, or	H.2.18.8
				multiple parallel outputs; or	H.2.18.11
				output verification, or	H.2.18.12
				testing pattern, or	H.2.18.22
				code safety	H.2.18.2

Table H.1 *(6 of 6)*

Component [b]	Fault/error	Software class		Example of acceptable measures [c d e]	Definitions
		B	C		
7.2 Analog I/O					
7.2.1 A/D- and	**Fault** conditions	rq		**Plausibility check**	H.2.18.13
D/A- convertor	specified in Clause H.27		rq	Comparison of redundant CPUs by either:	
				– **reciprocal comparison**	H.2.18.15
				– **independent** hardware **comparator**, or	H.2.18.3
				input comparison, or	H.2.18.8
				multiple parallel outputs, or	H.2.18.11
				output verification, or	H.2.18.12
				testing pattern	H.2.18.22
7.2.2 Analog multiplexer	Wrong addressing	rq		**Plausibility check**	H.2.18.13
			rq	Comparison of redundant CPUs by either:	
				– **reciprocal comparison**	H.2.18.15
				– **independent** hardware **comparator**, or	H.2.18.3
				input comparison or	H.2.18.8
				testing pattern	H.2.18.22
8. Monitoring devices and **comparators**	Any output outside the static and dynamic functional specification		rq	**Tested monitoring**, or **redundant monitoring** and comparison, or **error recognizing means**	H.2.18.21 H.2.18.17 H.2.18.6
9. Custom chips [f] for example, ASIC, GAL, Gate array	Any output outside the static and dynamic functional specification	rq		Periodic self-test	H.2.16.6
			rq	Periodic self-test and monitoring, or	H.2.16.7
				dual channel (diverse) with comparison, or	H.2.16.2
				error recognizing means	H.2.18.6

CPU: Central programmation unit

rq: Coverage of the **fault** is required for the indicated software class.

[a] Table H.1 is applied according to the requirements of H.11.12 to H.11.12.2.12 inclusive.

[b] For **fault**/error assessment, some components are divided into their subfunctions.

[c] For each subfunction in the table, the software class C measure will cover the software class B **fault**/error.

[d] It is recognized that some of the acceptable measures provide a higher level of assurance than is required by this standard.

[e] Where more than one measure is given for a subfunction, these are alternatives.

[f] To be divided as necessary by the manufacturer into subfunctions.

H.11.12.2.5 Measures others than those specified in H.11.12.2.4 are permitted if they can be shown to satisfy the requirements listed in Table H.1.