LTC6813 Safety Manual

18 Cell Battery Stack Monitor

December 12, 2019 **Status: Release**

Contents

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1 Introduction

Analog Devices[1] is a supplier of high-performance analog integrated circuits (ICs) to major OEM and tier 1 automotive customers worldwide. Our commitment to the automotive industry is underscored by our exemplary dedication to quality, reliability and customer service:

- We were among the first semiconductor companies to become certified to the TS16949 standard, a distinction we have maintained since 2003.
- We are committed to the goal of zero defects as required by automotive customers.
- We have developed proprietary automotive process flows. To learn more about our unique automotive flows, please contact the sales office in your area:

  http://www.analog.com/en/about-adi/contact-us.html

This same focus has been applied to the recently published ISO 26262 road vehicle functional safety standard and our next generation LTC68xx family of battery stack monitor ICs. This document is the safety manual for the LTC6813 multicell battery stack monitor.

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2 Revision History

Previous Version	Current Version	Version Description	Date
N/A	1.0	Initial release	7/6/2018
1.0	1.1	• updated diagnosability of VREF2 SM for both ATSRs • removed cell voltages within 1V AoU and SM • removed VREG input voltage must be between 4.5-5.5V AoU • clarified AoU2 and AoU3 • re-worded AoU requiring DCP=0 to indicate that it may be ignored if using external discharge and the parasitic I*R drop is small • re-worded internal die temp SM to confirm that the die temperature is within datasheet limits • changed frequency for internal die temp SM from FTTI to "As needed by system" • changed frequency for send bad CRC SM from FTTI to MPFDI • added SPFM, LFM metrics for both ATSRs • added PMHF and other detailed FIT rates for both ATSRs • replaced instances of "Safety Measure" with "Safety Mechanism"	8/13/2018
1.1	1.2	Added voltage ranges to diagnosability of VREF2 SM for both ATSRs	8/14/2018
1.2	1.3	• Clarified AoU7 • Removed middle conversion from open wire checker safety mechanism • Updated LFM metrics • Updated formatting	9/7/2018
1.3	1.4	• Updated ATSR-1 such that TME is specified up to 4.5V of cell voltage for two different T_J ranges • Updated ATSR2 for two different T_J ranges • ADOW, ADOL, and ADCVSC are added to AoU6 • ADAXD and ADSTATD are recommended over ADAX and ADSTAT for SM2 and SM3 as they run with SM5 applied • Added fault detection threshold to SM23 Sum of Cell measurement • Changed the name of SM26 • SM8 and SM23 are not relevant for ATSR2 in summary of safety mechanisms table. • Changed Frequency of SM11 in summary of safety mechanisms table. • Added 9.13 Considerations of Soft Errors	10/17/2018

Previous Version	Current Version	Version Description	Date
1.4	1.5	• Modified SM5 and SM13 to add procedure to ensure all cells and GPIO's are processed with the redundant digital filter. • Removed SM17, command verification methods. • Edited SM20 to add GPIO range. • Edited SM29 and SM31, modified the threshold when comparing open wire to regular conversion. • Revised SM30 to perform conversions to check for GPIO shorts. • Modified procedure in SM32, removed step 12. • Edited table in 9.11.2 to reflect changes in SM29 and SM31. • Added AoU11 • Updated SPF/LF metrics	11/20/2018
1.5	1.6	• Added AoU12 • Modified SM4 algorithm • Modified SM5 and SM13 procedure • Expanded SM21 description. • Fixed title of table 8	12/12/2018
1.6	1.7	• Expanded HRS's in section 9 and mapping table. • Revised Metric Calculations as DC=60% is claimed for leaky pads and V+ to C18 short FM.	12/20/2018
1.7	1.8	• Added AoU13 • Removed incorrect timing numbers from Table 6 • Added fast mode codes footnote to Table 6 • Updated SM29 • SM29 is not relevant for ATSR2 in summary of safety mechanisms table • Updated SM30 in summary table • Added SM33 • Updated SPF/LF metrics	1/30/2019
1.8	1.9	• Updated SM14 • Updated SM27 • Updated temperature measurements section • Updated Figure 15	3/1/2019
1.9	2.0	• Reworded AoU7 • Updated description of SM14, SM18, SM27, SM29, and SM31 • Updated Temperature Measurements section • Updated Figure 15 • Updated SPF/LF metrics	3/8/2019
2.0	2.1	• Revised ATSR-2 such that 2 application cases of NTC pull-up voltage are addressed. • Revised Table 7 for SM8. • Reworded SM20. • Revised SM21 and HSR21 for GPIO open-wire detection. • Range of digital redundancy fault code is explicitly stated in SM5, SM13, SM18, and SM26.	07/18/2019

Previous Version	Current Version	Version Description	Date
2.1	2.2	• Revised SM6 and SM9 descriptions in Table 1 by removing requirements for reading back the register contents. • Updated SM27 • Updated SM31 • Removed SM12 • Updated HSR20 • Updated SPF/LF metrics	9/24/2019
2.2	2.3	• Revised SM4 algorithm to include open C0 and top C pin fault by the inequality.	11/25/2019
2.3	2.4	• Added $CELL_{PD}(N) = 0$ condition to C(N) open wire fault detection criteria in SM4 • Updated SM21 • Removed SM31 as it is covered by SM29 • Updated SPF/LF metrics	12/10/2019

3 Product Overview

The LTC6813 is a fourth generation multicell battery stack monitor that can measure up to 18 series connected battery cells with a total measurement error of 2.2mV or less. The cell measurement range of 0V to 5V makes the LTC6813 suitable for most battery chemistries. All 18 cells can be measured in approximately 290µs, and lower data acquisition rates can be selected for high noise reduction.

Multiple LTC6813 devices can be connected in series, permitting simultaneous cell monitoring of high voltage battery strings. Each LTC6813 has an isoSPI interface for high speed, RF-immune, long distance communications.

Two communication options are available: using the LTC6813-1, multiple devices are connected in a daisy-chain with one host processor connection for all devices. Using the LTC6813-2, multiple devices are connected in parallel to the host processor, with each device individually addressed.

Additional features include passive balancing for each cell, an onboard 5V regulator, and nine general purpose I/O lines. In sleep mode, current consumption is reduced to around 6µA. The LTC6813 can be powered directly from the battery or from an isolated supply. Block diagrams showing the major functional blocks of LTC6813-1 and LTC6813-2 are shown Figure 1 and Figure 2 respectively.

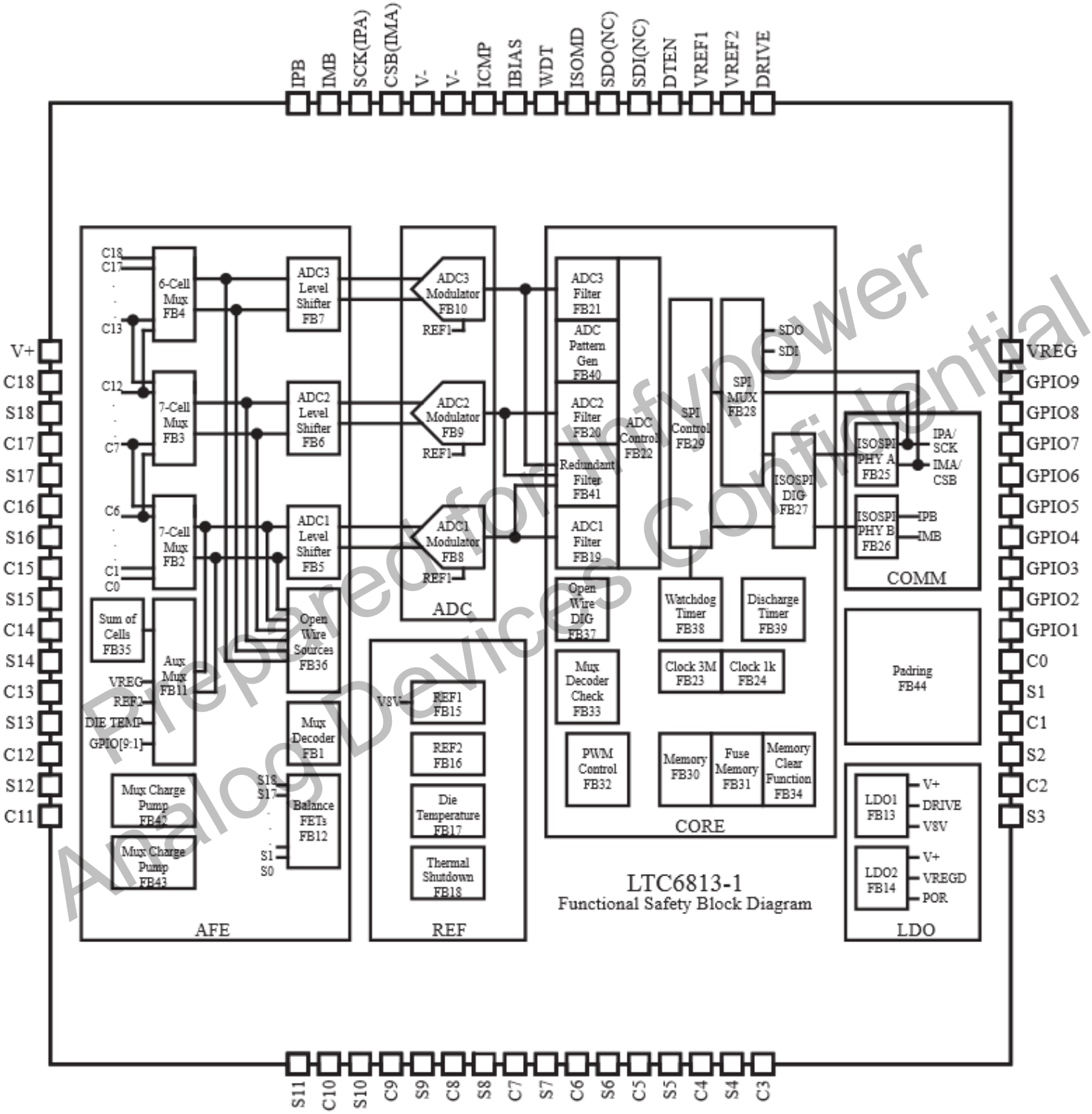

Figure 1. Block Diagram of the LTC6813-1

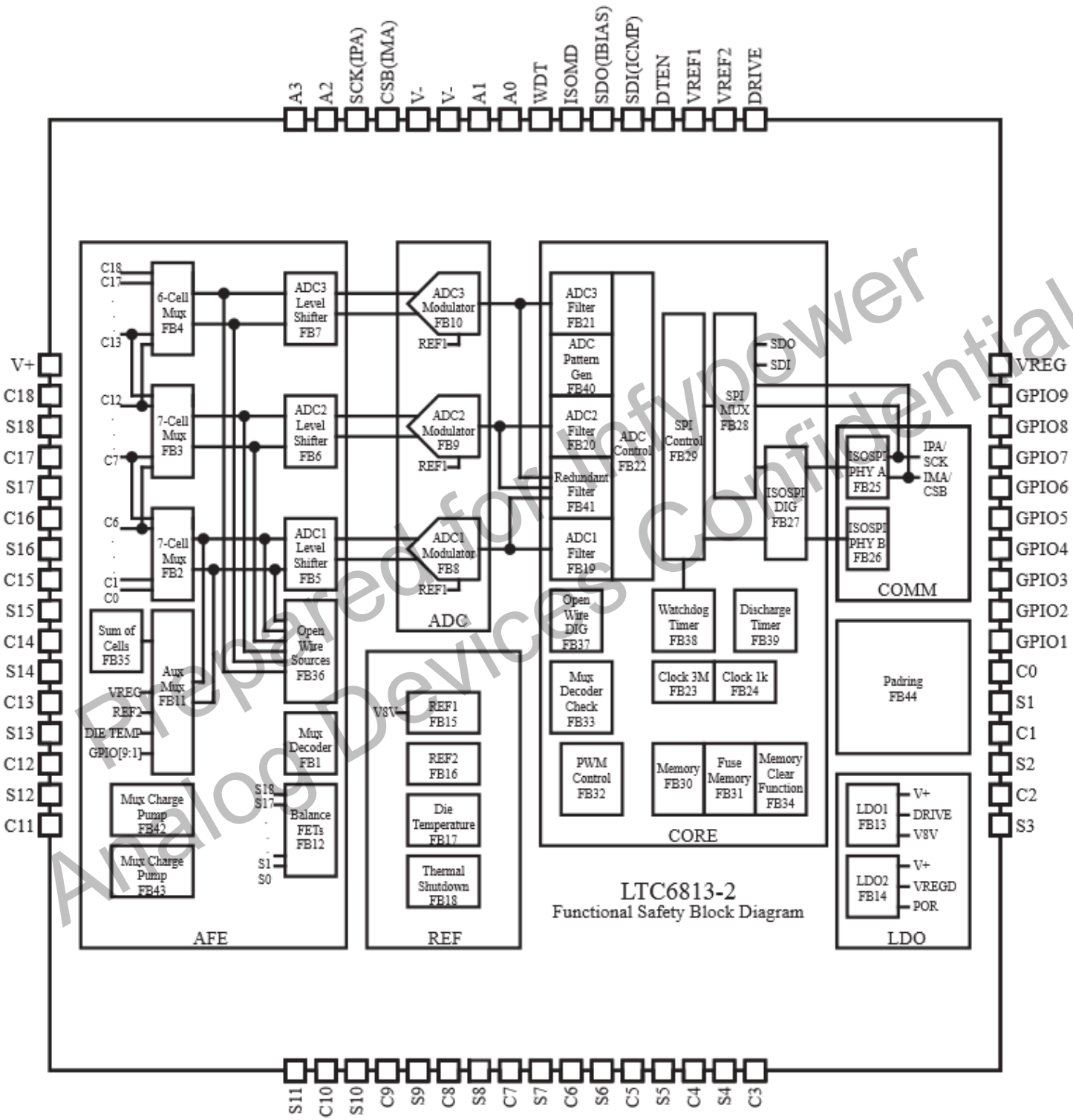

Figure 2. Block Diagram of the LTC6813-2

4 Typical Usage Assumptions

The LTC6813 is a commercial off-the-shelf (COTS) product, designed to be part of a broad product catalog. The LTC6813 was developed with ISO 26262 in mind as a safety element out of context (SEooC). The LTC6813 is intended to monitor battery cells in electric and hybrid electric vehicles. Figure 3 is a high level schematic view of such an application.

5 Assumed System Safety Goal

A battery pack system is the assumed top-level item which defines the safety goal. It is assumed that the battery pack system utilizes the LTC6813 to reliably measure battery cell voltages and temperatures to achieve its safety goal. The LTC6813 is one element of a battery pack system; its technical safety requirements are determined by the battery pack system. If proper operation of the LTC6813 is not required for the system to achieve a safety goal, then the LTC6813 is not a safety element and the requirements of ISO 26262 do not apply.

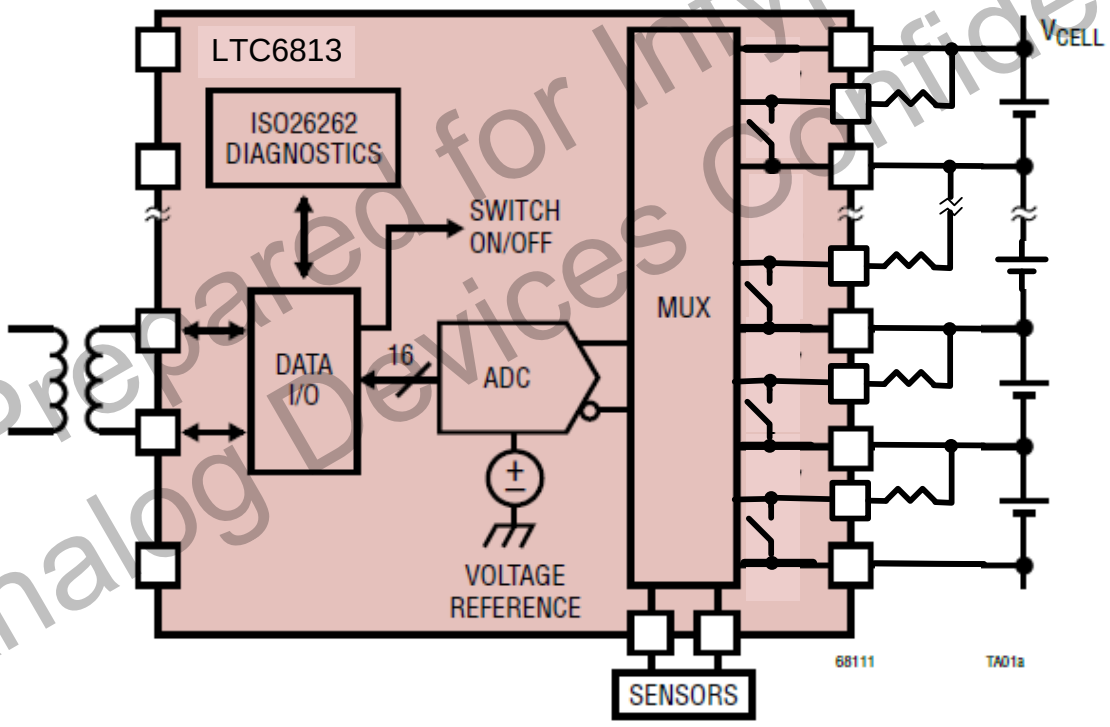

Figure 3. Typical Application

If proper operation of the LTC6813 is required for the system to meet a safety goal, the ASIL of the system will cascade down to the LTC6813. The LTC6813 was designed, developed, produced and tested for ISO 26262 compliant systems.

5.1 Assumed Functional Safety Requirements (AFSR) for the System

ID	Assumed Functional Safety Requirement[1)]	ASIL
AFSR-1	Charge or discharge of a battery shall be regulated per manufacturer's specifications based on cell voltage measurement.	ASIL C
AFSR-2	Charge or discharge of a battery shall be regulated per manufacturer's specifications based on cell temperature measurement.	ASIL C

1) The host controller shall be responsible for putting the system in a safe state by reading and interpreting fault status of the LTC6813 within FTTI defined in system level. The LTC6813 does not take any action to put the system in a safe state.

5.1.1 Assumed Technical Safety Requirements

ID	Assumed Technical Safety Requirement	ASIL
ATSR-1	Ensure that all cell voltage measurement up to 4.5V are within a minimum accuracy of ±20mV for T_J=-40°C to 85°C and ±25.5mV for T_J=-40°C to 125°C.	ASIL C
ATSR-2[1]	Ensure that all GPIO measurements up to 3.0V used to measure thermistor voltage are within a minimum accuracy of ±17mV[2] or ±30mV[3] for T_J = -40°C to 125°C.	ASIL C
ATSR-3	The LTC6813 shall implement apparatus that detect errors in serial communication with the host controller.	ASIL C

1) Thermistor is pulled up to bias voltage, V_{PU} via a pull-up resistor in fixed value as shown in Figure 16. Ratiometric measurement of $\frac{V_{PU}}{V_{NTC}}$ is used to calculate thermistor resistance, $R_{NTC} = \frac{R_{PU}}{\frac{V_{PU}}{V_{NTC}}-1}$.
2) Applicable to circuit configuration where VREF2 is directly used for V_{PU}.
3) Applicable to circuit configuration where buffered VREF2 is used for V_{PU}.

5.2 Assumptions of Use

AoU1 Each LTC6813 will be used to monitor up to 18 battery cells in series.

AoU2 Cells are connected between C-pins via an RC filter. The values of the resistor and capacitor will influence cell measurement accuracy (see datasheet for details). It is assumed that the system will be tolerant of any additional measurement error.

AoU3 Cells will also be connected to the S-pins either via a series discharge resistor of at least 10Ω or an external discharge MOSFET circuit.

AoU4 Temperature measurements will be made using a simple thermistor and resistor combination connected to the VREF2 pin and one of the GPIO inputs.

AoU5 The LTC6813 is always operated within the limits specified in the datasheet Absolute Maximum (ABS MAX) table.

AoU6 Discharge permit, DCP in the ADCV, ADOW, ADOL and ADCVSC command codes, shall be set to 0 (cells will not be discharged during a measurement). This AoU may be ignored if external MOSFETs are used for discharge and the parasitic I*R drop is less than the voltage accuracy of ATSR-1 or accuracy required by system.

AoU7 Unless directed by a safety mechanism all DCC bits will be set to 0 (MUTE command can be used for this) during cell measurements.

AoU8 The REFON bit in Configuration Register Group A shall be asserted prior to cell or temperature measurements.

AoU9 The STSCTRL command shall not be used. The S pins are used for cell balancing only.

AoU10 The listed safety mechanism shall be used at least once within each FTTI or MPFDI defined in the item level.

AoU11 If using internal discharge with single-ended filtering, the filter resistance may be no more than 10X the discharge resistance.

AoU12 System shall assume any one measurement in the FTTI could be corrupted due to low-probability transient faults and shall be designed to tolerate such events.

AoU13 All ADC measurements should be done in Normal Mode unless otherwise noted.

5.3 Safety Mechanisms

Table 1 Summary of Safety Mechanisms

Safety Mechanism Number	Safety Mechanism Name	Safety Mechanism Description	Relevant ATSR	Addressed Failure Mode	Frequency (FTTI, Key, Continuous)	System Level Overhead
SM1	Mux Decoder Check	Using DIAGN command, exercise mux control circuits through a measurement sequence and check for proper operation with a digital checker circuit.	ATSR-1, ATSR-2	SPF	FTTI	Read the MUXFAIL Flag
SM2	Reference Check	Using ADAXD command, measure VREF2 with ADC1 to diagnose VREF1 and VREF2.	ATSR-1, ATSR-2	SPF	FTTI	Measure / Compare

Safety Mechanism Number	Safety Mechanism Name	Safety Mechanism Description	Relevant ATSR	Addressed Failure Mode	Frequency (FTTI, Key, Continuous)	System Level Overhead
SM3	Supply Voltage ADC Check	Use the ADSTATD command. Check that both the regulator voltages VREG and VREGD are above the minimum voltages.	ATSR-1, ATSR-2	SPF	FTTI	Measure / Compare
SM4	Cell Open-wire Check	Use ADOW command to check for cell voltage measurement path opens by turning on pull up or pull down currents during an ADC measurement to check how much change was induced. Follow procedure in datasheet.	ATSR-1	SPF	FTTI	Measure / Compare
SM5	Cell Sinc Filter Check	Performing ADC conversions with digital filter redundancy.	ATSR-1, ATSR-2	SPF	FTTI	Measure / Compare
SM6	Clear Cell Results	Use the CLRCELL command prior to any ADC measurement start commands.	ATSR-1, ATSR-3	SPF	FTTI	1 SPI command prior to conversion commands.
SM7	Cell Register Check	Use the CVST command with both options ST=0b01 and ST=0b10. Check the registers used for cell measurement. The register contents should match the datasheet.	ATSR-1	SPF	FTTI	Compare results to known pattern
SM8	ADC Overlap Check	Use ADOL command to measure CELL7 with both ADC1 and ADC2 and CELL13 with both ADC2 and ADC3. Measurement results should match to within a tolerance dependent on the conversion mode.	ATSR-1	SPF	FTTI	Measure / Compare

Safety Mechanism Number	Safety Mechanism Name	Safety Mechanism Description	Relevant ATSR	Addressed Failure Mode	Frequency (FTTI, Key, Continuous)	System Level Overhead
SM9	Clear Aux Results	Use the CLRAUX command prior to the ADAX/ADAXD command.	ATSR-2, ATSR-3	SPF	FTTI	1 SPI command
SM11	Aux Register Check	Use the AXST command with both options ST=0b01 and ST=0b10. Check the registers used for aux measurement. The register contents should match the datasheet.	ATSR-2	SPF	FTTI	Compare results to known pattern
SM13	Aux Sinc Filter Check	Measure GPIOs using the ADAXD command. A result greater than 0xFF00 indicates a fault was detected due to mismatch between the ADC1 filter (FB19) and the redundant filter (FB41). SM13 provides digital redundancy to SM2.	ATSR-2	SPF	FTTI	Measure / Compare
SM14	Redundant Thermistor Circuits	Redundant thermistor circuits and GPIO inputs mitigate open circuit and leakage faults for these circuits.	ATSR-2	SPF	FTTI	Measure / Compare
SM16	Communication Check	Read data from the IC to confirm that communication is functional. Any operation that satisfies this requirement, such as another safety mechanism, is sufficient. No specific communication command is needed.	ATSR-3	SPF	FTTI	1 SPI command
SM18	Cell result range check	Check the cell measurement result vs the valid cell voltage range.	ATSR-1	SPF	FTTI	Measure / Compare

Safety Mechanism Number	Safety Mechanism Name	Safety Mechanism Description	Relevant ATSR	Addressed Failure Mode	Frequency (FTTI, Key, Continuous)	System Level Overhead
SM19	Send bad CRC	Send command with bad CRC and/or a register write command with a bad data CRC.	ATSR-3	LF	MPFDI	1 SPI command
SM20	Thermistor measurement range check	Check that the thermistor measurement result is in the valid range.	ATSR-2	SPF	FTTI	Measure / Compare
SM21	GPIO open wire	Activate the internal pull-down switch to ground the GPIO pins. Release the switch and measure the voltages to detect open fault at the GPIO pins or on trace.	ATSR-2	SPF	FTTI	Measure / Compare
SM22	Die Temperature Measurement	Confirm that die temperature is within datasheet limits.	ATSR-1, ATSR-2		As needed by system	Measure / Compare
SM23	Sum of Cells Check	Use the ADSTATD or ADCVSC command to measure the “Sum of Cells”. Compare the “sum of cells” value to the sum of the cell measurements from the ADCV or ADCVSC commands. All discharge bits must be set to 0 when measuring the individual cells.	ATSR-1	SPF	FTTI	Measure / Compare

Safety Mechanism Number	Safety Mechanism Name	Safety Mechanism Description	Relevant ATSR	Addressed Failure Mode	Frequency (FTTI, Key, Continuous)	System Level Overhead
SM26	Diagnostic test on digital redundancy	For setting PS=00 or setting PS=01, run an all channel aux measurement with digital redundancy (ADAXD) and an all channel cell measurement (ADCV), both with FDRF=1. Then clear the registers and run an overlap measurement (ADOL) with FDRF=1. For setting PS=10 and setting PS=11, run an all channel cell measurement (ADCV) with FDRF=1. Then clear the registers and run an overlap measurement (ADOL) with FDRF=1. Confirm that digital redundancy fault codes are written to the expected registers after each measurement.	ATSR-1, ATSR-2	LF	MPFDI	PS=00 or 01: 1. WRFG Cmd with FDRF Asserted. 2. Issue ADAXD Cmd 3. Read Aux Reg 4. Clear Aux Reg 5. Issue ADCV Cmd 6. Read Cell Reg 7. Clear Cell Reg 8. Issue ADOL Cmd 9. Read Cell Reg PS=10 or 11: 1. WRFG Cmd with FDRF Asserted 2. Issue ADCV Cmd 3. Read Cell Reg 4. Clear Cell Reg 5. Issue ADOL Cmd 6. Read Cell Reg
SM27	Discharge verification algorithm	Measure difference in ADC readings (DCP=1) between discharge off and discharge on for each cell, using circuit/algorithm shown in the safety manual.	ATSR-1	SPF	FTTI	Measure / Compare

Safety Mechanism Number	Safety Mechanism Name	Safety Mechanism Description	Relevant ATSR	Addressed Failure Mode	Frequency (FTTI, Key, Continuous)	System Level Overhead
SM29	Verify that open wire currents not stuck on or off during cell measurements	Compare Cell 1 measurement results with ADOW (PUP=0) and ADCV to diagnose pull down current sources. For pull up current sources, compare Cell N (top cell) measurement results with ADOW (PUP=1) and ADCV.	ATSR-1 ATSR-2	SPF	FTTI	Measure / Compare
SM30	GPIO adjacent short verification	Use an ADAXD command to measure GPIO(n). Write GPIO(n-1) and GPIO(n+1) low and all other GPIOs high with the WRCFGA and WRCFGB commands. Use the ADAXD command to measure GPIO(n) again and compare to the previous result. If GPIO(n) changes significantly or is near 0V then it is shorted to an adjacent GPIO.	ATSR-2	SPF	FTTI	Measure / Compare
SM32	Verify that all clear commands can write all 0s to 1s	Every Key on Cycle: Follow a detailed sequence of self-test, clear, and read commands to ensure that the clear command can write all Cell Voltage Registers, Auxiliary Registers, and stat register bits high. The sequence is described in detail in section 5.2	ATSR-1, ATSR-2	LF	MPFDI	Sequence of commands

Safety Mechanism Number	Safety Mechanism Name	Safety Mechanism Description	Relevant ATSR	Addressed Failure Mode	Frequency (FTTI, Key, Continuous)	System Level Overhead
SM33	Verify that V+ and C18 are not shorted	Check that V+ and C18 are not shorted. Turn on a GPIO pull down that has a 5k resistor in series with a diode connected to DRIVE. This loads DRIVE and V+ with an additional 1mA. Do an ADC conversion of the top cell in this condition and compare it to a normal result. If the measurement with additional load current is more than 25mV lower than the normal measurement, then a short between V+ and C18 is detected.	ATSR-1	SPF	FTTI	Measure / Compare
SM34	Thermistor pull-up reference crosscheck	When buffered VREF2 is used for thermistor pull-up reference compare measurement from GPIO pin against what ADAXD measures to detect faults in the GPIO pin or on PCB trace.	ATSR-2	SPF	FTTI	Measure / Compare

The following safety mechanisms are needed to meet the assumed technical safety requirements listed in 5.1.1 Assumed Technical Safety Requirements:

SM1. Use the DIAGN command, check that the bit MUXFAIL=0.

As shown in the simplified schematic of the LTC6813 multiplexers (Figure 4), 5 address lines are used for the decoder to connect specific inputs to each ADC. This figure illustrates the address line decoding for these multiplexers.

If the inputs to the decoder (A0 – A4) experience a fault, the fault may not be detectable by cell measurements. For example, if line A0 is stuck high and the LTC6813 is commanded to measure 18 battery cells, then 9 cells are measured twice, 9 cells are not measured at all, and 18 measurements are stored in

memory. The DIAGN command and DECODER CHECK circuit ensure proper operation of the digital control of the multiplexers. Use the DIAGN command to force the multiplexer to cycle through every channel. The resulting output of the decoder is monitored by the DECODER CHECK block; if all channels are successfully decoded, the MUXFAIL memory bit is low, and if any of the channels are not decoded, MUXFAIL = 1. The RDSTATB command is used to read the MUXFAIL bit value. To confirm that the MUXFAIL bit value is not stuck low, the CLRSTAT command must be used to force the MUXFAIL bit to 1.

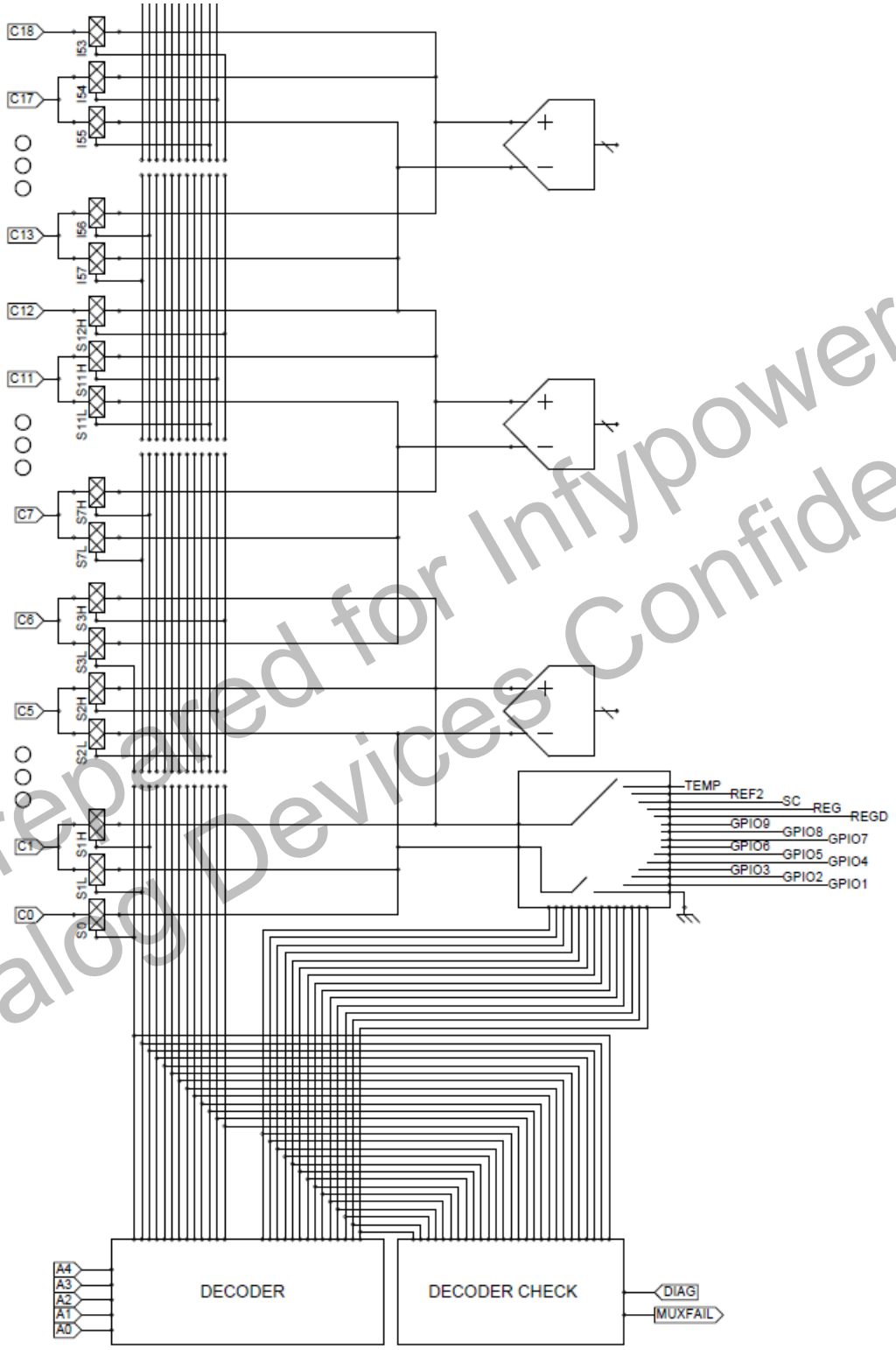

Figure 4. MUX Decoder Check

SM2. Use the ADAXD command to measure the 2nd reference.

An independent 2nd bandgap reference (VREF2) can be used to verify the complete functionality of ADC1 and the accuracy of the 1st reference. Using the measurement system to measure a second independent reference guarantees the accuracy of the measurement system within the second reference's specifications.

The ADAXD command is used to measure the 2nd reference block with digital redundancy (SM5). The RDAUXB command is used to read the result.

The measured VREF2 ranges are listed in Table 2, allowing for variations on VREF2 voltage and ADC TME as well as additional margin to prevent a false fault from being reported. These limits are based on all error sources the system should consider. Measuring the 2nd reference ensures that the assumed diagnostic coverages of SM2 are valid for meeting ATSR-1 and ATSR-2.

Results outside of this range indicate a failure of the 1st reference block, the 2nd reference block or somewhere in the path between the C pins and the output of ADC1. Subsequent cell and GPIO measurements may be inaccurate.

Table 2 Measured VREF2 range to meet ATSR-1 and ATSR-2

T_J	MIN	MAX
-40°C to 85°C	2.992V	3.012V
-40°C to 125°C	2.990V	3.014V

SM3. Use the ADSTATD command. Check that both the regulator voltages VREG and VREGD are above the minimum specified voltages.

Use the ADSTATD command to measure the analog power supply (VREG) and digital power supply (VREGD). The 16-bit ADC value of the analog power supply measurement (VREG) is stored in Status Register Group A. The 16-bit ADC value of the digital power supply measurement (VREGD) is stored in Status Register Group B.

Use the RDSTATA command to read the measurement result for VREG and the RDSTATB command to read the result for VREGD. The results of these power supply measurements are given by:

Analog power supply measurement (VREG) = VA • 100µV

Digital power supply measurement (VREGD) = VD • 100µV

The VREG result should be between 4.5V and 5.5V and the VREGD result should be between 2.7V and 3.6V. Readings outside of this range indicates a failure of the LDO1 block. Subsequent cell and GPIO measurements may be inaccurate.

SM4. Perform the "open wire algorithm" for cells.

The analog switches in the cell multiplexers are checked with the open wire detection algorithm. The ADOW command is used to check for high impedance on any MUX switch or open wires between the ADC inputs inside the LTC6813 and the external battery cells. The ADOW command performs ADC conversions on the C-pin inputs, similar to the ADCV command, except that two internal current sources are used to sink or source current into the two C-pin inputs while they are being measured. Like the ADCV command, the ADOW command is specified with an option to determine the number of channels to measure and the ADC mode. In addition, a specific bit (PUP) of the ADOW command determines whether the current sources are sinking or sourcing 100µA. A simplified schematic of these current sources is shown in Figure 5.

The host controller should perform the following algorithm to check for high MUX impedance or open wires on any of the 19 C-pin Inputs:

1. Execute the ADOW command with PUP= 1 at least twice. Read the cell voltages for cells 1 through N once at the end and store them in array $CELL_{PU}(n)$, n = 1 to N, where N is the number of cells in series.
2. Execute the ADOW command with PUP= 0 at least twice. Read the cell voltages for cells 1 through N once at the end and store them in array $CELL_{PD}(n)$, n = 1 to N, where N is the number of cells in series.
3. Compute the difference between the pull-up and pull-down measurements made in above steps for cells 1 to N:

   $CELL_{\Delta}(n) = CELL_{PU}(n) – CELL_{PD}(n)$
4. For all values of n from 1 to N:

   If $CELL_{\Delta}(n) < –400mV$, then C(n-1) is open.
5. If $CELL_{\Delta}(N) > 400mV$ or $CELL_{PD}(N) = 0$, then C(N) is open.

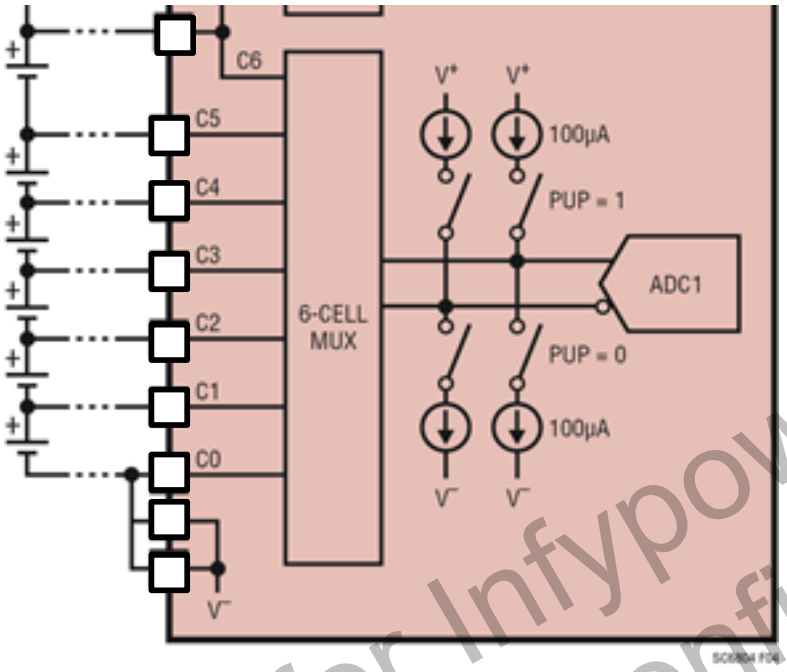

Figure 5. Open Wire Detection

The above algorithm can detect open wires, stuck off MUX channels and MUX channels with high impedances greater than 4k. This algorithm requires that the input capacitance (between the LTC6813 and open wire) be limited to 10nF or less capacitance. If more external capacitance is on the open C-pin input, then more time is required for the conversions (due to the limited 100µA internal current source). To ensure that a measurable voltage difference is created, this algorithm can be used by increasing the number of consecutive ADOW commands in steps 1-4, or by using filtered mode conversions instead of normal mode conversions. Use Table 3 to determine how many conversions are necessary.

Table 3. Number of ADOW Commands for Open Wire Detection

	NUMBER OF ADOW COMMANDS REQUIRED IN STEPS 1-4	
EXTERNAL C-PIN INPUT CAPACITANCE	NORMAL MODE	FILTERED MODE
≤10nF	2	2
100nF	10	2
1µF	100	2
C	1 + ROUNDUP (C/10nF)	2

See SM21 for an open wire diagnostic that can be applied to auxiliary inputs.

SM5. Perform cell conversions using digital redundancy.

The partial block diagram in Figure 6 shows the redundant digital filter (FB41) in the LTC6813. The ADCV, ADOW, ADAXD, ADSTATD, AXOW, ADCVAX, and ADCVSC commands apply the modulator outputs of ADC(n) to a corresponding digital filter. When redundancy is applied to one of the three ADCs, the output of the modulator is processed by both the primary and redundant digital filters, and the output of the two digital filters should be identical. If the filter outputs match, the ADC result is placed in the proper memory register.

If the 2 digital filters produce different readings for a conversion then a fault is indicated. A value between 0xFF01 and 0xFF0F is written to the result register. This value is outside of the clamping range of the ADC and the host should identify this as a fault indication. The last 4 bits are used to indicate which nibble(s) of the result values did not match.

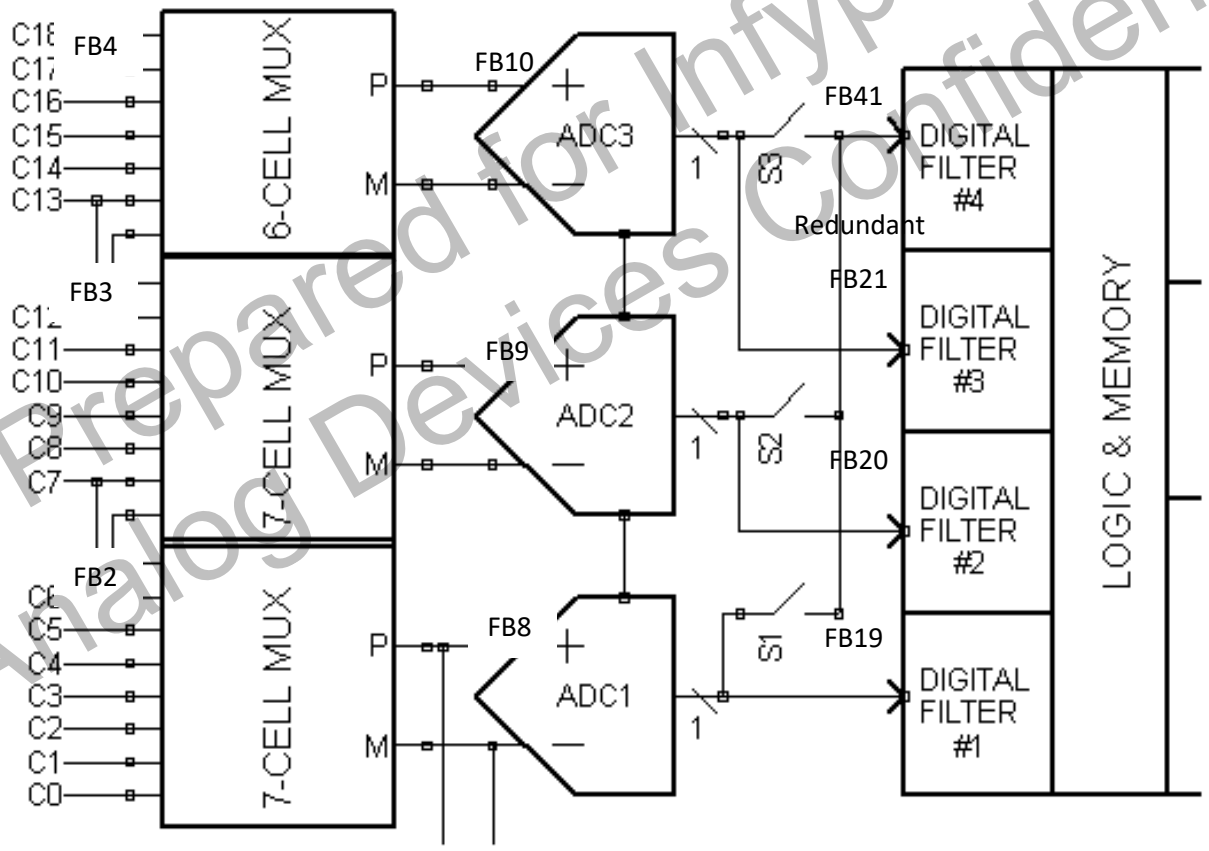

Figure 6. Digital Redundancy

For example, suppose the ADAXD command is executed and the 2 results for the measurement of GPIO1 mismatched. And, suppose the outputs from the 2 digital filters were 0x3A98 & 0x3AAA, corresponding to 1.5000V and 1.5018V. This mismatch would cause the value 0xFF03 to be stored in Auxiliary Register Word [AVAR1,AVAR0]. The “3” in the last nibble indicates that the last 2 nibbles of the results mismatched.

Table 4. Result Registers

RESULT	INDICATION
0b1111_1111_0000_0XXX	No fault detected in bits 15-12
0b1111_1111_0000_1XXX	Fault detected in bits 15-12
0b1111_1111_0000_X0XX	No fault detected in bits 11-8
0b1111_1111_0000_X1XX	Fault detected in bits 11-8
0b1111_1111_0000_XX0X	No fault detected in bits 7-4
0b1111_1111_0000_XX1X	Fault detected in bits 7-4
0b1111_1111_0000_XXX0	No fault detected in bits 3-0
0b1111_1111_0000_XXX1	Fault detected in bits 3-0

The configuration register bits PS[1:0] determine to which ADC redundancy is applied per Table 5.

Table 5. ADC Path Redundancy Selection

	PS[1:0] = 00		PS[1:0] = 01		PS[1:0] = 10		PS[1:0] = 11	
MEASURE	PATH SELECT	REDUNDANT MEASURE	PATH SELECT	REDUNDANT MEASURE	PATH SELECT	REDUNDANT MEASURE	PATH SELECT	REDUNDANT MEASURE
Cells 1, 7, 13	ADC1	Cell 1	ADC1	Cell 1	ADC2	Cell 7	ADC3	Cell 13
Cells 2, 8, 14	ADC2	Cell 8	ADC1	Cell 2	ADC2	Cell 8	ADC3	Cell 14
Cells 3, 9, 15	ADC3	Cell 15	ADC1	Cell 3	ADC2	Cell 9	ADC3	Cell 15
Cells 4, 10, 16	ADC1	Cell 4	ADC1	Cell 4	ADC2	Cell 10	ADC3	Cell 16
Cells 5, 11, 17	ADC2	Cell 11	ADC1	Cell 5	ADC2	Cell 11	ADC3	Cell 17
Cells 6, 12, 18	ADC3	Cell 18	ADC1	Cell 6	ADC2	Cell 12	ADC3	Cell 18
Cell 7 (ADOL)	ADC2	Cell 7	ADC1	Cell 7	ADC2	Cell 7	ADC3	N/A
Cell 13 (ADOL)	ADC2	Cell 13	ADC1	N/A	ADC2	Cell 13	ADC3	Cell 13
GPIO[n]*	ADC1	GPIO[n]	ADC1	GPIO[n]	ADC2	N/A	ADC3	N/A
2nd Reference*	ADC1	2nd Ref	ADC1	2nd Ref	ADC2	N/A	ADC3	N/A
SC*	ADC1	SC	ADC1	SC	ADC2	N/A	ADC3	N/A
ITMP*	ADC1	ITMP	ADC1	ITMP	ADC2	N/A	ADC3	N/A
VA*	ADC1	VA	ADC1	VA	ADC2	N/A	ADC3	N/A
VD*	ADC1	VD	ADC1	VD	ADC2	N/A	ADC3	N/A

To ensure all cells are processed by both the primary and redundant digital filters, every FTTI do the following.

1. Write Config Register with PS[1:0] =01. This will ensure cells 1-6 get processed with a redundant digital when being measured.
2. Issue a cell conversion command.
3. Repeat step 1 with PS[1:0] = 10. This will ensure cells 7-12 get processed with a redundant digital filter when being measured.

4. Issue a cell conversion command.
5. Repeat step 1 with PS[1:0] = 11. This will ensure cells 13-18 get processed with a redundant digital filter when being measured.
6. Issue a cell conversion command.
7. Any mismatch between the primary and redundant digital filter will cause a value between 0xFF01 and 0xFF0F to be written to the respective cell location.

SM6. Use the CLRCELL command prior to any cell measurement commands. This will set all registers to 0xFFFF.

LTC6813 has 3 clear commands: CLRCELL, CLRAUX and CLRSTAT. These commands clear the registers that store all ADC conversion results. Clearing the registers before conversions provides a safety mechanism for the host controller to confirm that new data is being placed in the registers.

- The CLRCELL command clears cell voltage register groups A through F. The 16-bit values in these registers are set to 0xFFFF by CLRCELL command.
- The CLRAUX command clears AUX channel register groups A through D. The 16-bit values in these registers are set to 0xFFFF by CLRAUX command.
- The CLRSTAT command clears status register groups A and B except the REV and RSVD bits in Status Register Group B, byte 5. A readback of REV will return the revision code. RSVD bits always read back 0s. All OV and UV flags, MUXFAIL bit and the THSD bit in Status Register Group B are set to 1 by CLRSTAT command. The 16-bit values of SC, ITMP, VA and VD are all set to 0xFFFF by CLRSTAT command.

SM7. Use the CVST command with both options ST=0b01 and ST=0b10. Check the registers used for cell measurement. The register contents should match the datasheet.

The self-test commands verify the operation of the digital filters and memory. Figure 7 illustrates the operation of the ADC during self-test. The output of the 1-bit pulse density modulator is replaced by a 1-bit test signal. The test signal passes through the digital filter and is converted to a 16-bit value. The 1-bit test signal undergoes the same digital conversion as the regular 1-bit pulse from the modulator, so the conversion time for any self-test command is the same as the corresponding regular ADC conversion command. The 16-bit ADC value is stored in the same register groups as the regular ADC conversion command. The test signals are designed to place alternating one-zero patterns in the registers.

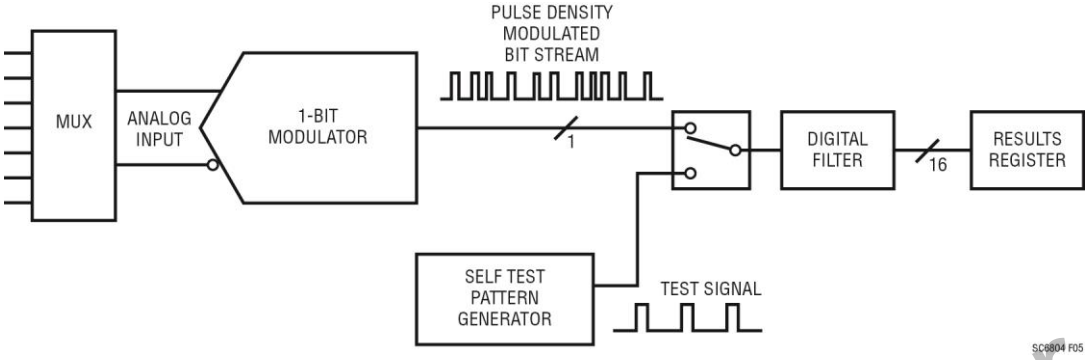

Figure 7. Operation of LTC6813 ADC Self Test

Table 6 is a partial list of the self-test commands. If the digital filters and memory are working properly, then the registers will contain the values shown in Table 6.

Table 6. Self Test Commands

COMMAND	WITH OPTIONS	PLACES PATTERN[1]	IN RESULTS REGISTER
CVST (Cell Voltage Self-Test)	MD1, MD0, ST1, ST0 = 0b1001	0x9555	CVA, CVB, CVC, CVD, CVE, CVF
CVST (Cell Voltage Self-Test)	MD1, MD0, ST1, ST0 = 0b1010	0x6AAA	CVA, CVB, CVC, CVD, CVE, CVF
AXST (AUX Channel Self-Test)	MD1, MD0, ST1, ST0 = 0b1001	0x9555	AUXA, AUXB, AUXC, AUXD
AXST (AUX Channel Self-Test)	MD1, MD0, ST1, ST0 = 0b1010	0x6AAA	AUXA, AUXB, AUXC, AUXD
STATST (Stat Channel Self-Test)	MD1, MD0, ST1, ST0 = 0b1001	0x9555	STATA, STATB
STATST (Stat Channel Self-Test)	MD1, MD0, ST1, ST0 = 0b1010	0x6AAA	STATA, STATB

[1]When using “fast” mode option, the expected patterns are 0x9565 and 0x6A9A instead of 0x9555 and 0x6AAA, respectively.

To verify the results registers, both options of the CVST self-test shown in Table 6 must be used. To speed up the diagnostic, use the CVST command with the “fast” mode option, MD[1:0]=01, CFGAR0[0]=0.

The first step is to send the CVST command with options: ST1, ST0 bits = 0b01. Follow this with the commands RDCVA-RDCVF to read the cell voltage registers. The register values should match the pattern 0x9555 (7kHz – 26Hz modes). The second step is to send the CVST command with options: ST1, ST0 bits = 0b10. Again, follow this with the commands RDCVA-RDCVF to read the cell voltage registers. The register values should match the pattern 0x6AAA (7kHz – 26Hz modes). If there is a pattern mismatch with either of these steps, there is a failure in the digital filters, logic or memory of the LTC6813.

The same procedure applies to the auxiliary and status registers.

SM8. Use ADOL command to measure CELL7 with both ADC1 and ADC2, CELL13 with both ADC2 and ADC3. Measurement results should match to within a tolerance dependent on the conversion mode.

The ADOL command first simultaneously measures CELL7 with both ADC1 and ADC2. Then it simultaneously measures CELL13 with both ADC2 and ADC3. This sequence is shown in Figure 8.

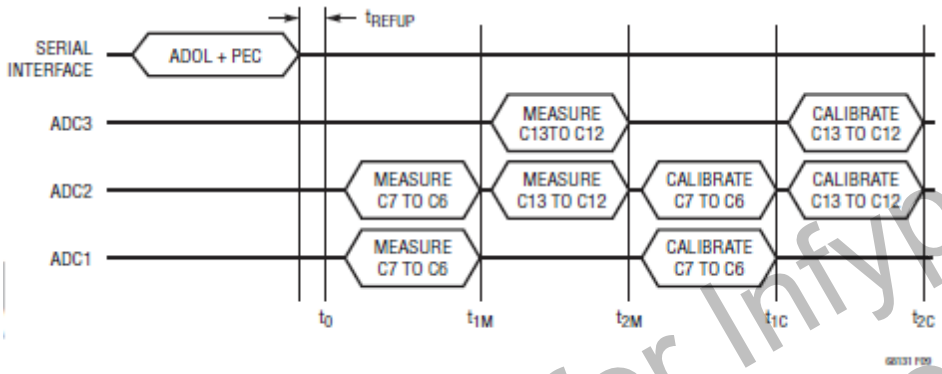

Figure 8. ADOL Command

Once the conversion has completed, the host can read the result values and use the pair of CELL7 results to confirm that ADC2 has accuracy similar to ADC1. Then the host can use the pair of CELL13 results to confirm that ADC3 has accuracy similar to ADC2. When combined with the 2nd reference measurement (SM2) this provides evidence that all three ADCs are operating with accuracy. See the LTC6813 datasheet for the ADOL command format.

The measurements from any 2 ADCs should differ slightly due to noise in the modulators. The measurement difference is reduced by reducing the conversion speed. The measurement difference increases with increased measurement voltage.

Table 7 shows the maximum allowable measurement difference for the various conversion speeds and cell voltages. Differences greater than those inTable 7 indicate a fault.

Table 7. Maximum Allowable Measurement Differences

ADC Mode	Maximum Measurement Difference using ADOL				
	Vcell=0.8V	Vcell=2V	Vcell=3.3V	Vcell=4.2V	Vcell=5V
Normal Mode or Slower OSR settings	1.2mV	2.3mV	3.4mV	4.2mV	7.0mV

SM9. Use the CLRAUX command prior to any AUX measurement commands.

The CLRAUX command clears AUX channel register groups A through D. The 16-bit values in these registers are set to 0xFFFF by CLRAUX command. See SM6 for details.

SM11. Use the AXST command with both options ST=0b01 and ST=0b10. Check the GPIO registers used for thermistor measurements. The register contents should match the datasheet.

The self-test commands verify the operation of the digital filters and memory. See SM7.

SM13. Measure GPIOs and 2nd reference using the ADAXD command. A result between 0xFF01 and 0xFF0F indicates a fault was detected due to mismatch between the ADC1 filter (FB19) and the redundant filter (FB41). SM13 provides digital redundancy to SM2.

The ADAXD command operates similarly to the ADAX command except that an additional diagnostic is performed using digital redundancy. The execution time of ADAX and ADAXD is the same. See SM5.

To ensure that all GPIOs and the REF2 measurement are performed with digital redundancy, every FTTI do the following:

1. Write Config Register with PS[1:0] = 01 or 00. This will ensure that all auxiliary GPIOs and REF2 get processed with a redundant digital filter when being measured.
2. Issue an ADAXD command.
3. Any mismatch between the primary and redundant digital filter will cause a value between 0xFF01 and 0xFF0F to be written to the respective GPIO location.

SM14. Use Redundant thermistor circuits and GPIO inputs for redundant temperature measurements.

The GPIO inputs are measured with ADC1 through AUX MUX. The ADAXD command initiates the measurement of the GPIO inputs. Use the RDAUXA, RDAUXB, RDAUXC and RDAUXD commands to read the results.

For higher ASIL requirement, the system may consider using a redundant thermistor which is measured at a redundant GPIO pin. The redundancy mitigates potential single-point faults attributed to a leaky GPIO pin, leaky external capacitor or faulty thermistor circuitry. The system shall ensure that the GPIO pins used for redundant temperature measurements are not adjacent to each other in order to avoid a latent fault due to potential pin-to-pin short. Temperature measurements that are not similar indicate a failure on one or both measurement paths. SM21 (GPIO Open Wire) and SM30 (GPIO adjacent short verification) are not necessary if redundant GPIOs are used for temperature measurements.

SM16. Read data from the IC to confirm that communication is functional. Check the PEC (packet error code) for all data read from the LTC6813. The LTC6813 will only execute commands with the correct CRC and will only write data to memory with the correct CRC.

The packet error code (PEC) is a 15-bit cyclic redundancy check (CRC) value calculated for all of the bits in a register group in the order they are passed, using the initial PEC value of 000000000010000 and the following characteristic polynomial:

$$x^{15} + x^{14} + x^{10} + x^8 + x^7 + x^4 + x^3 + x^1$$

The PEC prevents erroneous serial data from being interpreted as valid data and guarantees safe communication. A failure in the serial I/O ports will cause erroneous data to be sent or will prevent data from being received. In the case of a write to the device, if the calculated PEC does not match, the received data will be discarded. Data should be read back from the device after write operations to confirm that the write was correctly received. If the data read back does not match what was written, the write should be attempted again. When data is read from the LTC6813, if the PEC calculated by the MCU does not match the transmitted PEC, the data is invalid. In that case, additional reads should be performed until the PEC matches.

The characteristic polynomial is the same as that used in CAN bus communications. For the LTC6813, the data packet length is always 48 bits or less. The Hamming Distance for the CAN polynomial with 48 bits of packet data is 6, which means that any data corruption of 5 bits or fewer would be detected by the CRC (see Koopman, P.; Chakravarty, T., “Cyclic redundancy code (CRC) polynomial selection for embedded networks,” Dependable Systems and Networks, 2004 International Conference on, pp. 145-154, 28 June-1 July 2004).

A typical physical layer interface has primary failure modes of stuck-at-0, stuck-at-1, or floating. The PEC with a non-zero initial seed detects stuck-at-0 and stuck-at-1 faults. Floating data lines and interference can produce random data errors. Because of the large Hamming Distance of the CAN polynomial, the probability of undetected errors is extremely low. The specific probability of undetected errors depends on the system’s communications rate, the bit-error-rate (BER) induced by interference, and the bit error profile.

When the physical interface communicates over cables (like with a twisted pair), then it is assumed that the interface is robust against electromagnetic interference. The isoSPI interface, for example, typically has zero bit errors even under high levels of bulk current injection (BCI). Systems using the LTC6813 should be tested for susceptibility to interference. The measured BER can then be used to estimate the probability of undetected data errors.

If the physical layer interface does not store or interpret the data passing through it, then the assumptions given above are true. This will be the case for the typical interfaces used with the LTC6813: direct connection to a microcontroller (voltage-mode SPI); digital isolators (e.g., opto-couplers); or isoSPI (e.g., LTC6820).

SM18. Check the cell measurement result vs the valid cell voltage range.

System validates all ADC measurement results on cell pins against range deemed plausible. The following internal faults can be detected by SM18.

1. Faults in the redundant digital filter (FB41) may cause false fault detection by SM5, resulting in cell measurements between 0xFF01 and 0xFF0F.
2. Stuck-at faults in Cell Voltage Register Groups can result in implausible cell voltages outside the min and max boundary set by system.
3. Short between V- pin to C or S pin will result in cell voltages below the min value set by system.
4. Short between a C pin and another C pin due to failure in ESD structure can result in implausible cell voltage outside the min and max boundary set by system.

System shall set thresholds for the min and max boundary depending on battery type, hardware configuration, use case, etc.

SM19. Send a command with bad CRC and/or a register write command with a bad CRC. Verify that the LTC6813 rejects these commands.

System runs diagnostic test on CRC engine in SPI Controller (FB29) to make sure there is no fault.

SM20. Check that the thermistor measurement result is in the valid range.

Issue an ADAXD command to measure V_{NTC} at GPIO pins. Verify that the measurement results over temperature are in the valid range that system has calculated based on V_{PU}, R_{NTC}, R_{PU}, etc. in Figure 16.

SM21. Use the internal pull-down switches to check for open circuits on the GPIO inputs.

When a GPIO pin is used to sense a cell temperature via external thermistor circuitry as shown in Figure 9, system can detect open fault at any point (1 to 5) as shown below:

For open fault at 1 or 2,

1. Write 0 to GPIOn configuration bits, n = 1 to N, where N is the number of GPIO inputs used for temperature measurement. This will activate internal pull-down switch at the GPIO pins.
2. Write 1 to GPIOn configuration bits to release the internal pull-down switches. Without open fault, the GPIO pin voltages will rise to the level before activating the pull-down switches with RC time constant defined by external component values.

3. Allow enough time for the GPIO voltages to rise above $V_{GPIO\_OW\_TH}$, where $V_{GPIO\_OW\_TH}$ can be defined at around 50% of minimum GPIO voltage across temperature without any open fault. Run ADAXD command to measure the GPIO voltages, VGPIO(n). For all values of n from 1 to N:

   If VGPIO(n) < $V_{GPIO\_OW\_TH}$, GPIO(n) is open. Else GPIO(n) is not open.

For open fault at 3, VGPIO(n) = 0V and it can be detected by SM20. For open fault at 4 and 5, VGPIO(n) = VREF2 (or whatever pull-up voltage) and it can be also detected by SM20.

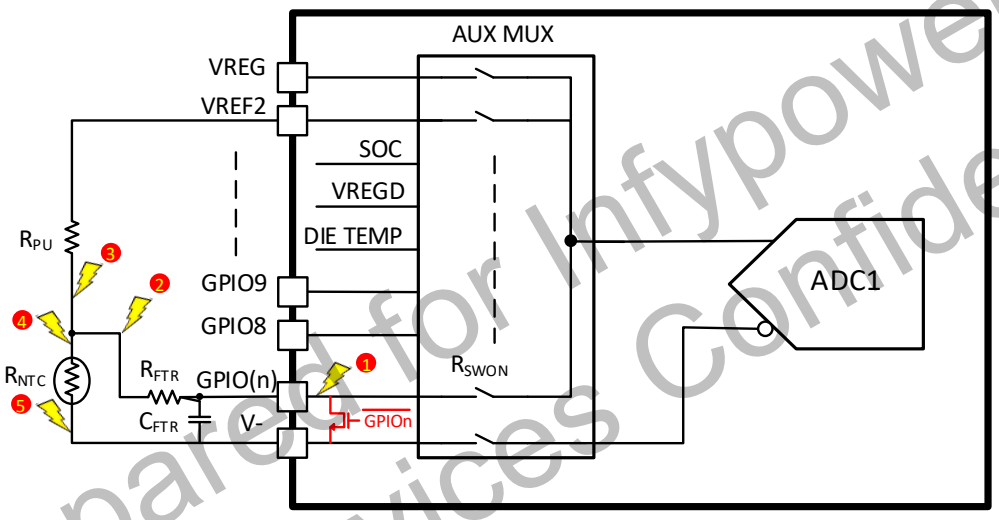

Figure 9 GPIO Open-Wire Detection

SM22. Internal die temperature measurement using the ADSTATD command.

The host controller can use the ADSTATD command as a diagnostic to monitor internal die temperature. The measurement can be utilized to ensure that the abs max temperature ratings are met.

SM23. Use the ADCVSC, ADSTAT or ADSTATD command to measure the Sum of Cells. Compare the result to the individual cell measurements.

The ADSTATD command is a diagnostic command that measures several internal parameters with digital redundancy (SM5): die temperature, Sum of Cells (SC), and the supply voltages.

The Sum of Cells (SC) measurement is the voltage between C18 and C0 with a 30:1 attenuation. The SC measurement is a 16-bit value that is stored in Status Register Group A. The SC result represents the sum of all voltage cell measurements is given by the following formula:

SC measurements = SC_VALUE•30•100µV

To confirm proper multiplexer operation, the SC value shall be compared to the sum of the individual cell measurements. The two quantities should agree within the tolerances of the data sheet.

As cell TME and SC TME in Normal Mode are at ±0.1% and ±0.35%, respectively, difference between the two measurements greater than ±0.45% indicates a failure of either SC measurement path or individual cell measurement path. Subsequent cell measurements and GPIO may be inaccurate.

All discharge bits must be set to 0 when measuring the individual cells.

Figure 10 illustrates how the SC value is measured. The resistor divider and buffer add some error to the measurement. Therefore, the SC value is not as accurate as each individual cell measurement.

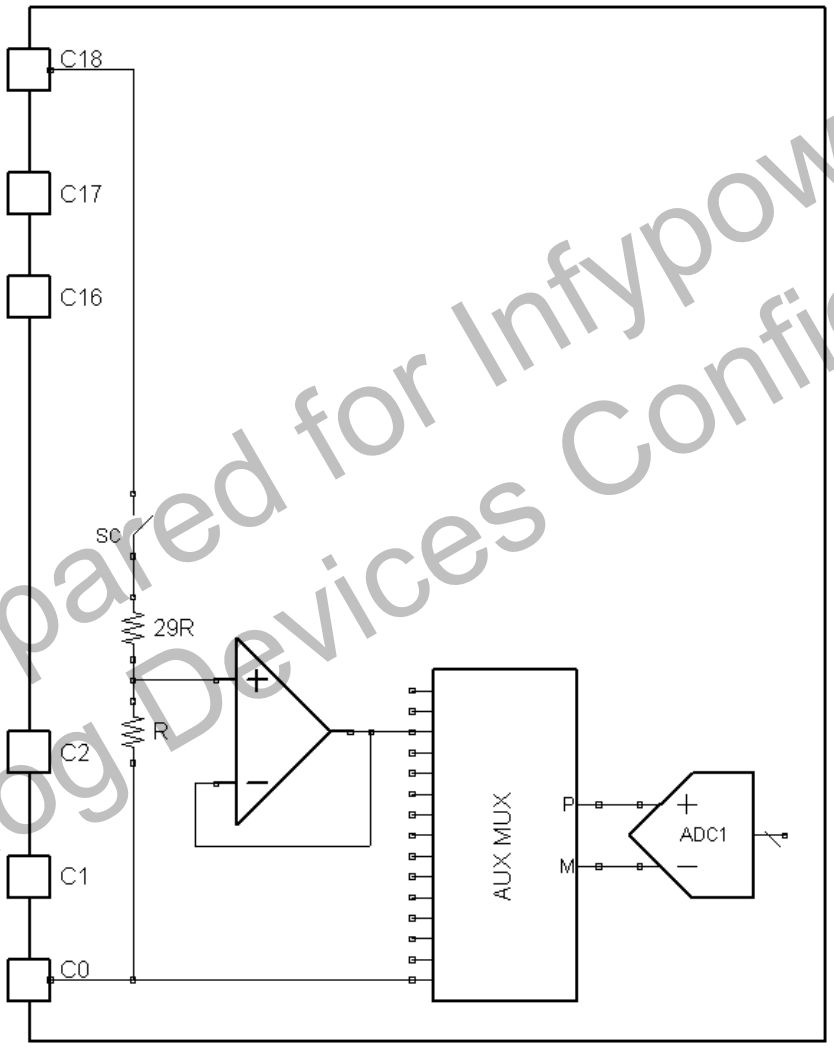

Figure 10. Sum of Cells Measurement

The ADCVSC command can also be used to measure the Sum of Cells. This command measures 9 of the individual cell inputs, then measures SC, then measures the remaining 9 cell inputs. The ADCVSC command reduces the time between measurements (Figure 11) for better noise immunity.

It is recommended multiple SC measurements be taken to get an average value from them as SC measurement is relatively sensitive to noise.

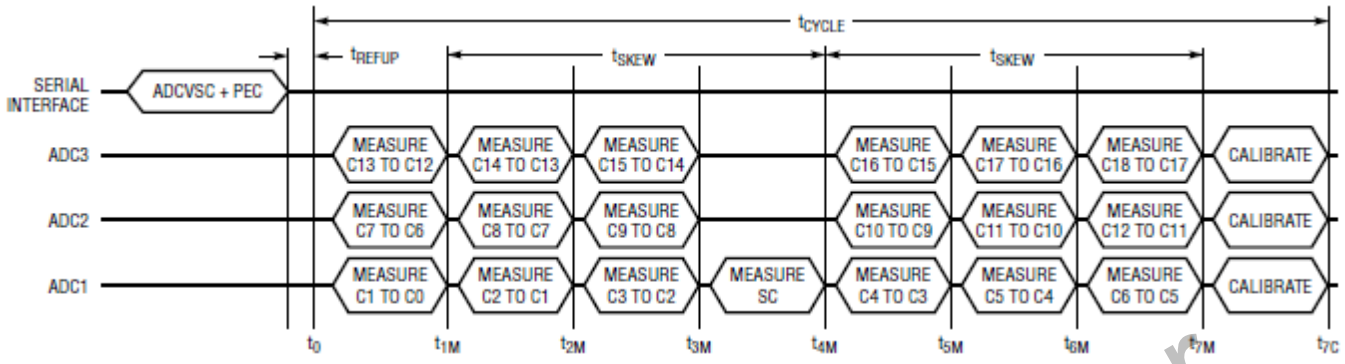

Figure 11. ADCVSC command timing

SM26. Diagnostic test on digital redundancy.

For setting PS=00 or setting PS=01, run an all channel aux measurement with digital redundancy (ADAXD) and an all channel cell measurement (ADCV), both with FDRF=1. Then clear the registers and run an overlap measurement (ADOL) with FDRF=1. For setting PS=10 and setting PS=11, run an all channel cell measurement (ADCV) with FDRF=1. Then clear the registers and run an overlap measurement (ADOL) with FDRF=1. Confirm that fault codes (0xFF01 to 0xFF0F) are written to the expected registers after each measurement.

SM27. Perform the discharge verification algorithm.

When using the internal discharge feature, the ability to verify discharge functionality can be implemented in software. In applications using an external discharge MOSFET, an additional resistor can be added between the battery cell and the source of the discharge MOSFET. This will allow the system to detect faults in discharge circuits.

Both circuits are shown in Figure 12. The functionality of the discharge circuits can be verified by conducting cell measurements and comparing measurements when the discharge is off to measurements when the discharge is on. The measurement taken when the discharge is on requires that the discharge permit bit (DCP) be set. The change in the measurement when the discharge is turned on is calculable based on the resistor values. Care must be taken to ensure that the C0 pin does not exceed the operating maximum of 1V above V- when discharge is on. If C0 exceeds 1V above V-, the measurement results may be inaccurate.

The following algorithm can be used in conjunction with Figure 12 to verify each discharge circuit.

1. Measure all cells with no discharging (all S outputs off) and read and store the results of Cell 1 to Cell N, where N is the number of cells in series. Measurement results of Cell N+1 to Cell 18 are discarded.

For n=1 to 6, repeat steps 2 through 4 below.

2. Turn on S(n), S(n+6) and S(n+12).
3. Measure Cell n, Cell n+6 and Cell n+12.

4. Turn off S(n), S(n+6) and S(n+12).
5. Read the Cell Voltage Register Groups to get the results of Cell 1 to Cell N. Measurement results of Cell N+1 to Cell 18 are discarded.
6. Compare new readings from step 5 with old readings from step 1. Each cell voltage reading should have decreased by a fixed percentage set by $R_{DISCHARGE}$ and R_{FILTER} for internal designs and $R_{DISCHARGE1}$ and $R_{DISCHARGE2}$ for external MOSFET designs. The exact amount of decrease depends on the resistor values and MOSFET characteristics.

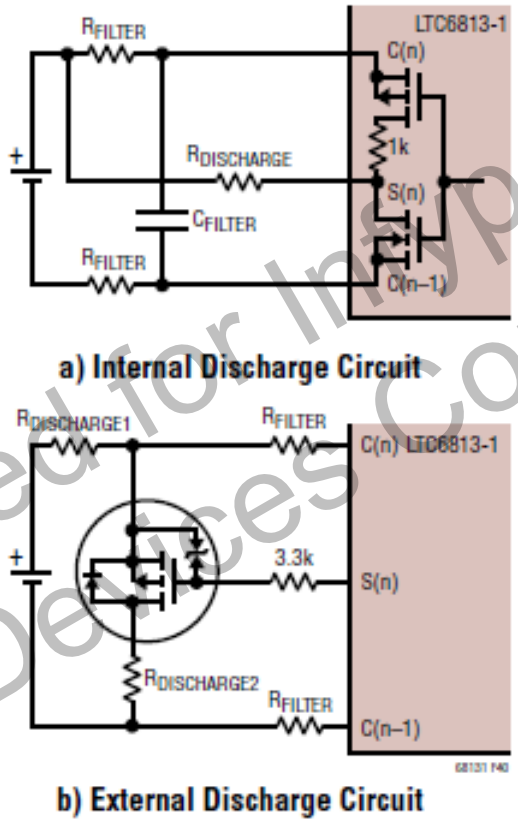

Figure 12. Balancing Self-Test Circuit

SM29. Verify that the open wire current sources are not stuck-on or off during cell measurements.

See SM4 and Figure 5. To ensure that the pull down current sources are not stuck on/off, issue an ADOW command on cell 1 with PUP=0 and compare the ADOW result to the ADCV result. C1 will get pulled down with a 100uA current source. The pull down current source, however, will not be present on C0 due to its compliance limitations (C0=0V). The cell reading will be reduced by 100uA x (R_{FILTER} + R_{SWON_C}), where R_{SWON_C} is C pin mux switch on-resistance. Assuming R_{FILTER} = 100Ω and R_{SWON_C} = 200Ω (nominal value), the ADOW result will be about 30mV lower than the ADCV result. If the current sources are stuck on or off, there will be no difference on cell 1. System can set a threshold at 15mV to detect a fault in pull down current sources. If a fault is detected, the open wire algorithm described in SM4 can no longer be

relied upon to check for open wires.

Similarly, to ensure that the pull up current sources are not stuck on/off, issue an ADOW command on cell N (where N is the number of cells in series) with PUP=1 and compare the ADOW result to the ADCV result. The ADOW result should be at least 15mV lower than the ADCV result as C(N-1) will get pulled up but C(N) will not.

SM30. GPIO adjacent short verification.

If non-adjacent redundant GPIOs are used to measure temperature, SM30 is not necessary. Additionally, if the adjacent GPIO is floating SM30 is not necessary. SM30 is necessary only if the adjacent GPIO is used as an input or output. GPIO(n) is used in conjunction with a thermistor and resistor to measure temperature. The adjacent GPIO's are used as inputs or outputs. If GPIO(n) is outside it's valid range it is possible that it may be shorted to an adjacent GPIO. To determine if a short exists do the following.

1. Measure GPIO(n), it is expected to be within its valid range.
2. Write the adjacent GPIO's low. GPIO(n-1) and GPIO(n+1) will be written low. If GPIO(n-1) or GPIO(n+1) is a digital input, it should be driven low by the system and driven low by writing to the config register.
3. Measure GPIO(n) again, comparing it to the previous result.
    i. If the GPIO(n) result changes significantly or is near 0V then it is shorted to an adjacent GPIO.

SM32. Verify that clear command can write all 0s to 1s.

Every Key on Cycle: Do the following to ensure that the clear command can write all cell register, aux register, and stat register bits high.

1. Issue a CVST option 1 command, normal mode.
2. Issue an AXST option 1 command, normal mode.
3. Issue a STATST option 1 command, normal mode.
4. Issue RDCVA, RDCVB, RDCVC, RDCVD, RDCVE, RDCVF, RDAUXA, RDAUXB, RDAUXC, RDAUXD, RDSTATA, RDSTATB commands to verify a 0x9555 pattern in all the registers.
5. Issue CLRCELL, CLRAUX, and CLRSTAT commands.
6. Issue RDCVA, RDCVB, RDCVC, RDCVD, RDCVE, RDCVF, RDAUXA, RDAUXB, RDAUXC, RDAUXD, RDSTATA, RDSTATB commands to verify a 0xFFFF pattern in all the registers.
7. Issue a CVST option 2 command, normal mode.

8. Issue an AXST option 2 command, normal mode.
9. Issue a STATST option 2 command, normal mode.
10. Issue RDCVA, RDCVB, RDCVC, RDCVD, RDCVE, RDCVF, RDAUXA, RDAUXB, RDAUXC, RDAUXD, RDSTATA, RDSTATB commands to verify a 0x6AAA pattern in all the registers.
11. Issue CLRCELL, CLRAUX, and CLRSTAT commands.
12. Issue RDCVA, RDCVB, RDCVC, RDCVD, RDCVE, RDCVF, RDAUXA, RDAUXB, RDAUXC, RDAUXD, RDSTATA, RDSTATB commands to verify a 0xFFFF pattern in all the registers.

SM33. Verify that V+ and C18 are not shorted.

If the V+ and C18 pins are shorted together, the V+ supply current will flow through the parallel combination of the V+ filter resistor and the top C pin filter resistor. This may cause additional measurement error on the top cell due to the IR drop across these resistors. This fault can be detected by adding the circuitry shown in Figure 13. to the DRIVE pin. This circuit connects an extra 1mA load to the DRIVE pin when the GPIO is written low. The DRIVE pin current is supplied by the V+ pin, so this circuit allows the V+ current to be changed by the state of the GPIO. The 1000k resistor to VREG prevents the voltage on the GPIO from pulling up to the DRIVE voltage when the GPIO is off.

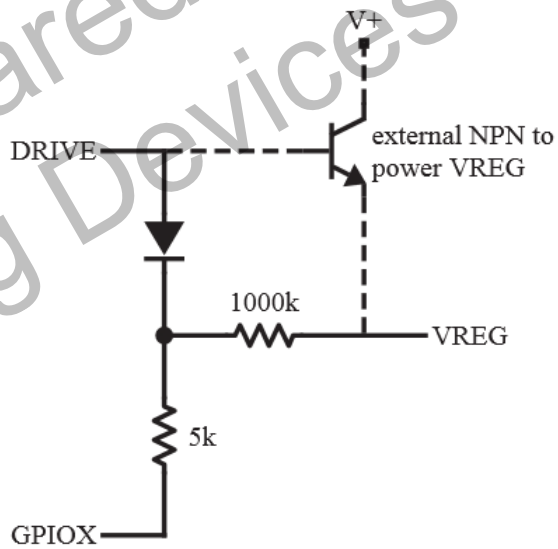

Figure 13. Circuit to Increase V+ Current for V+/C18 Short Detection

To check for a V+ to C18 short, issue an ADCV command on the top cell with and without the increased V+ current turned on and compare the results. If the results with the increased V+ current are more than 25mV lower than the normal results a short is detected.

SM34. Thermistor pull-up reference crosscheck.

If a buffered VREF2 is used to bias external thermistor circuitry in Figure 16, compare measurement of GPIOy pin against the internal VREF2 measurement described in SM2 to detect faults in the GPIOy pin, PCB trace, or the external buffer. If VGPIOy < 0.994 x VREF2 or if VGPIOy > 1.006 x VREF2, then a fault is detected and temperature measurement by external NTCs shall be considered inaccurate.

It should be noted that SM34 is not valid if SM2 indicates a fault.

6 Design Development Process

Analog Devices' quality management system for the development and manufacture of high performance integrated circuits is certified by an accredited registrar to be in accordance with ISO/TS 16949 and ISO 9001. Analog Devices' design Product Development Process (design PDP) is a series of five distinct phases that provide structure and review milestones for the development activities. The design PDP also describes methods in which the design tools are verified. Detailed below are the phases and key milestones of the process:

1. DEFINITION PHASE Identify and develop the new product concept
   - Define key features and specifications
   - Identify required design and development resources
   - Develop detailed schedule

2. DESIGN PHASE
   - Schematic design
   - ESD plan approval
   - Chip design review (schematics only)
   - Test inputs review
   - Product review meeting
   - Intellectual property (IP) review

3. MASK DESIGN PHASE
   - Mask design
   - Layout review

4. DEVELOPMENT PHASE
   - Bench evaluation
   - Correlation of ATE test measurements
   - Characterization
   - Qualification tests
   - Complete initial stocking quantities

5. RELEASE PHASE

- Released products listing launch meeting
- Prepare press release and marketing material
- With the adoption of the ISO 26262 functional safety standard, Analog Devices has included the following items in the design PDP for the LTC6813:
  - Established a functional safety team and safety manager
  - Incorporated safety critical items into the Analog Devices product tracking system (PTS) such that the PTS is the safety plan
  - Tailoring analysis of ISO 26262 to determine which deliverables are applicable to the LTC6813
  - Systems level safety usage assumptions
  - Failure modes effects and diagnostic analysis (FMEDA)

7 Evaluation and Verification Process

The evaluation of any Analog Devices device (hardware unit, SEooC) follows a comprehensive evaluation plan. The design PDP details how to develop an evaluation plan, design and process FMEAs, process capability studies and copies of our quality certifications which demonstrate an effective quality system.

The evaluation process is described in the design PDP. As appropriate, safety mechanisms are verified by placing the device in various test modes. The inclusion of test modes is incorporated in the design phase of the device. Documentation of findings and methods of evaluation are maintained during the process.

Evaluation review meetings are periodically scheduled to review any findings. An errata list and revision list are maintained throughout the evaluation process. A completed evaluation checklist and summary is a work product of the evaluation process.

For ISO26262 compliance LTC6813 summarizes testing of safety related functions in the LTC6813 Verification and Validation Report.

8 Supporting Processes

Analog Devices designs commercial off-the-shelf (COTS) high-performance linear integrated circuits. Within the scope of ISO 26262, these are hardware unit safety element out of context (SEooC). The safety-related characteristics of Analog Devices' circuits are defined in Analog Devices' design PDP and ensured in manufacture and test through our quality systems.

Safety requirement inputs for test hardware and test program development are outputs of the design PDP. All electrical testing requirements are determined in the design PDP and are an input into Test Engineering's test Product Development Process (test PDP). Test hardware development and qualification are accomplished per the test PDP.

Production verification measures and acceptance criteria are based on the outputs from the design PDP. All supporting process requirements are implemented and maintained as part of Analog Devices' ISO/TS 16949 certified quality system.

Analog Devices is ISO/TS 16949 certified in the design, manufacture, and test of high performance integrated circuits. Included in our Production Part Approval Process (PPAP) documentation are design records, control plans, design and process FMEAs, process capability studies and copies of our quality certifications which demonstrate an effective quality system.

9 Architecture Diagnostics / Integration Manual

This section provides a description of each functional block shown in Figure 1 and Figure 2, the Hardware Safety Requirements (HSRs) and Instructions on using the Safety Mechanisms (SM).

For each block there are HSRs needed to meet the ATSRs. Each HSR results in a diagnostic, or "safety mechanism". This section also describes how to use the diagnostics.

9.1 C0 to C7 MUX (FB2), C6 to C13 MUX (FB3), C12 to C18 MUX (FB4), and AUX MUX (FB11)

HSR1 - Sequential Channel Measurement: Each of the 3 ADC's (ADC1, ADC2, and ADC3) in the LTC6813 shall be able to measure up to 6 cell voltages (at (C(n) – C(n-1) pins, where n=1,2,3,4,5,6 for ADC1, n=7,8,9,10,11,12 for ADC2, and n=13,14,15,16,17,18 for ADC3) sequentially.

HSR2 - Mux Decoder Check: The LTC6813 shall implement a decoder checker on decoder logic of the ADC input channel multiplexers. Once executed, the decoder logic shall cycle through all of the channel selections and the diagnostic checker will verify that each channel is decoded correctly in the right sequence. If any fault is found during this process the LTC6813 shall set a fault status flag, MUXFAIL, in the STBR5 register in the Status Register Group B.

HSR3 - Mux Channel Impedance: The channels of the multiplexer shall be sufficiently low impedance to allow accurate ADC operation.

The MUX blocks consist of analog switches controlled by a decoder. The MUXes are used to connect specific C-pin inputs to each differential ADC modulator. The operation of these MUX blocks is verified by using the MUX decoder check, the open wire test (ADOW command), the sum of cells measurement (ADSTAT, ADSTATD or ADCVSC command) and the overlap check (ADOL command). The MUX DIAG command (SM1) is a diagnostic command that can verify the operation of the MUX decoder. The cell open wire test (SM4) is a self-test that tests if the analog switches are stuck off, or are high impedance. The sum of cells measurement (SM23) can be used to confirm that multiple switches are not asserted simultaneously. The overlap check (SM8) can be used to confirm that there are no faults affecting the outputs of the MUX.

The LTC6813 includes 9 general purpose inputs (GPIOs). The AUX MUX block is used to connect each of these auxiliary input signals to the ADC, for example to measure thermistors. The AUX MUX operation is verified as part of the DIAG command (SM1). AUX MUX impedance can be verified by measuring internal voltages (SM3 and SM23), by having redundant GPIO pins connected to thermistors (SM14) or by utilizing the open wire test on the GPIOs (SM21).

9.2 1st Reference (FB15) and 2nd Reference (FB16)

HSR4 - ADC Measurement Accuracy: The total measurement error (TME) on a single channel shall not be greater than ±4.2mV for cell or GPIO inputs up to 4.2V.

HSR5 - VREF2 Measurement: The LTC6813 shall allow the host controller to monitor a second internal voltage reference output by selecting a dedicated channel in the AUX MUX into an ADC. Total measurement error shall be no greater than 0.2% in normal mode.

The 1st reference block provides the reference voltage for the 3 ADCs and is the most critical portion of the data acquisition system. The only way to verify the operation of the first reference is to measure a second, independent reference. The 2nd reference block (SM2) is provided for this purpose.

9.3 ADC1, ADC2 and ADC3 Modulators (FB8-10)

The total measurement error (TME) on a single channel shall not be greater than ±4.2mV for CELL or GPIO inputs up to 4.2V. A minimum accuracy level of the cell measurements and GPIO measurements shall be verifiable through diagnostics. HSR4 and HSR5 also apply to the ADCs.

HSR6 - Cell Overlap Measurement: The LTC6813 shall allow the host controller to measure the voltages of cells in the middle of the battery stack with two ADCs at the same time. Cell 7 is measured with ADC1 and ADC2, while CELL13 is measured with ADC2 and ADC3. The measurement results shall be available for the host controller to compare.

Each delta-sigma ADC is composed of a 1-bit pulse density modulator followed by a digital filter as is shown in Figure 14. A pulse density modulated bit stream has a higher percentage of 1s for higher analog input voltages. The digital filter block converts this high frequency 1-bit stream into a single 16-bit word.

The ADC1, ADC2 and ADC3 blocks represent the 1-bit modulators and are tested separately from the digital filter portion of the ADCs. The analog portions of ADC1, ADC2 and ADC3 are verified by making subsequent CELL7 measurements (with ADC1 and ADC2) and CELL13 measurements (with ADC2 and ADC3). This is accomplished using the ADOL command (SM8).

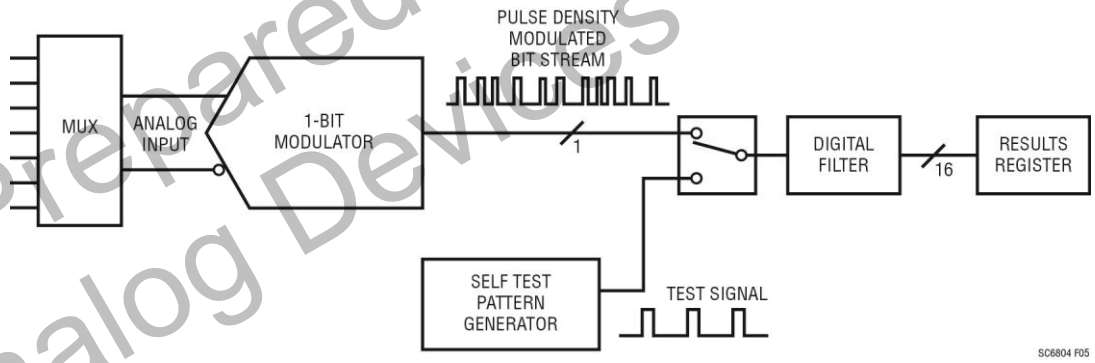

Figure 14. ADC Block Diagram

9.4 Digital Filters (FB19-21, FB41)

HSR7 - Redundant Digital Filter: The LTC6813 shall implement a redundant digital filter to detect faults in the primary digital filter of the ADC. Calculations from the two paths shall be compared, if they don't match, conversions results shall be outside the valid range, indicating a fault.

HSR8 - Diagnostic Test on Redundant Digital Filter: A diagnostic test shall be available for the host controller to test the redundant digital filter within multiple-point fault detection interval defined in the item level. The diagnostics shall inject a fault onto the output of the primary digital filter.

The proper operation of the digital filter in Figure 14 is verified using the digital redundancy feature (SM5 and SM13) of the LTC6813.

Since there is a single redundant digital filter, redundancy can only be applied to one ADC at a time. Which

ADC has redundancy for a given cell measurement is determined by the path select bits, PS[1:0]. The operation of PS[1:0] and the redundancy logic can be verified by performing an algorithm which includes setting the configuration bit FDRF (SM26). Asserting FDRF will cause all redundancy checks to fail and values greater than 0xFF00 will appear in the results registers.

9.5 Serial Communication (FB25-29)

HSR9 - CRC on SPI command: The LTC6813 shall detect error in incoming commands over SPI ports from the host controller. The host controller shall send a command followed by a 15-bit CRC. The LTC6813 shall calculate a CRC value for the received command and compare it against the received CRC from the host controller. The command shall be regarded as valid only if the two CRC values match.

HSR10 - Dual isoSPI Ports: The LTC6813 shall implement 2 isoSPI ports (A and B) that can be configurable either to master A/slave B or to master B/slave A, depending on direction of SPI communication when multiple devices are wired in a daisy chain configuration.

The serial communication blocks consist of the standard SPI port, the isoSPI drivers, isoSPI receivers and isoSPI bias circuit including the IBIAS generator. The functionality of these blocks is verified by the communication check (SM16), which includes verification of a packet error code (PEC) on every serial transmission. The PEC must be used to verify the serial communication data.

9.6 LDO1, LDO2 and Sum of Cells (FB13-14, FB35)

HSR11 - VREGD Measurement: The LTC6813 shall allow the host controller to monitor internal regulated supply (VREGD) output voltage by selecting a dedicated channel in the AUX MUX into an ADC. The measurement shall be between 2.7V and 3.6V.

HSR12 - VREG Measurement: The LTC6813 shall allow the host controller to monitor VREG regulated supply output voltage by selecting a dedicated channel in the AUX MUX into an ADC. The measurement shall be between 4.5V and 5.5V.

HSR13 - C18 to C0 Measurement Accuracy: The total measurement error (TME) of the Sum of Cells measurement shall not be greater than ±0.35% of the actual voltage.

The LDO1 consists of the circuitry that generates the internal VREGD. The VREGD supply is used by all of the internal digital logic and control circuitry including the digital filter. The VREGD operation can be verified by measurement with the ADSTATD command (SM3).

The LDO2 block consists of the circuitry that generates the DRIVE voltage. Using an external NPN, the DRIVE voltage (Pin 49 on the LTC6813) is used to create the voltage on the VREG input (pin 48 on the LTC6813). To confirm proper operation of the LDO2 block, a VREG measurement is required, which is also accomplished with the ADSTATD command (SM3).

The Sum of All Cells measurement is the voltage between C18 and C0 with a 30:1 attenuation. The 16-bit ADC value of Sum of Cells measurement (SC) is stored in Status Register Group A. Any potential difference between the C0 and V- pins results in an error in the SC measurement equal to this difference. From the SC value, the sum of all cell voltage measurements is given by: Sum of All Cells = SC • 30 • 100 µV

9.7 Logic and Memory, ADC Pattern Generator (FB22, FB30-31, FB34, FB40)

HSR14 - Cell Voltage Register Clear: The LTC6813 shall allow the host controller a dedicated clear command to reset memory registers that hold ADC measurement results on C pins.

HSR15 - Auxiliary Register Clear: The LTC6813 shall allow the host controller a dedicated clear command to reset memory registers that hold ADC measurement results on GPIO pins and VREF2.

HSR16 - Status Register Clear: The LTC6813 shall allow the host controller a dedicated clear command to reset memory registers that hold ADC measurement results on sum-of-cells, internal die temperature, and internal supplies.

HSR17 - Pattern Generator for Cell Voltage Registers: Register bits in the Cell Voltage Register groups shall be tested for faults. Pattern generator in the LTC6813 shall generate unique pattern values for the memory registers. The pattern values shall be inverted by changing the ST[1:0] bits. The host controller shall activate the pattern generator and compare read back values against an expected result to detect a fault.

HSR18 - Pattern Generator for Auxiliary Registers: Register bits in the Auxiliary Register groups shall be tested for faults. Pattern generator in the LTC6813 shall generate unique pattern values for the memory registers. The pattern values shall be inverted by changing the ST[1:0] bits. The host controller shall activate the pattern generator and compare read back values against an expected result to detect a fault.

HSR19 - Pattern Generator for Status Registers: Register bits in the Status Register groups shall be tested for faults. Pattern generator in the LTC6813 shall generate unique pattern values for the memory registers. The pattern values shall be inverted by changing the ST[1:0] bits. The host controller shall activate the pattern generator and compare read back values against an expected result to detect a fault.

The LOGIC and MEMORY blocks consist of the data registers and the state machine that controls the LTC6813. The state machine and memory operation is verified with the use of the ADC self-test commands (SM7, SM11) and the register clear commands (SM6, SM9). The cell, AUX and status self-tests must be used to verify that registers do not have any stuck bits. The clear commands can be used to verify that the data being read in the registers is new data.

HSR14-HSR19 also apply to the digital filters (FB19-21, FB41). As seen in Figure 14, the pattern is generated prior to the digital filter and will detect faults in the digital filter in addition to those in the memory registers.

9.8 Balance FETS (FB12)

The LTC6813 includes signals (pins S1 through S18) that can be used to balance cells with internal or external discharge. Cells can be discharged using the internal N-channel NMOS at the S pins, or the S pins can act as digital outputs to drive external MOSFETs. Figure 15 shows examples of cell balancing using the LTC6813.

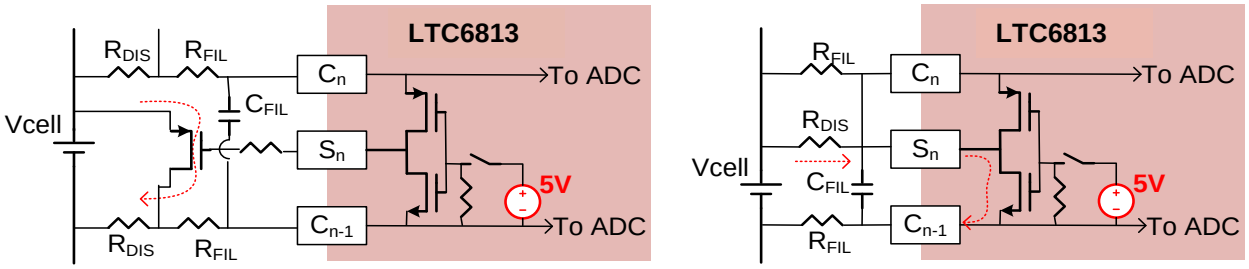

Figure 15. Cell Balancing Examples

The functionality of the balancing circuitry is related to ATSR-1 if any discharge is stuck on during cell measurements.

The functionality of the discharge circuitry can be verified by C pin measurements (SM27). The resistor between the battery and the source of the discharge MOSFET causes cell measurements to change. The amount of measurement change depends on the resistor values and MOSFET on resistance.

In both circuits of Figure 15 the voltage between Cn and Cn-1 will decrease when Sn is active (switch closed). Also, the voltage between Cn-1 and Cn-2 will increase a similar amount.

9.9 Open Wire Sources (FB36)

HSR20 - Cell Open-Wire Check: The LTC6813 shall allow the host controller to detect open wires between battery cells and the ADCs in the LTC6813. An open wire conversion command will connect cell inputs C(n) and C(n-1) to pull up (PUP = 1) or pull down (PUP = 0) current sources at the output of the multiplexer. The internal currents will stay connected while the conversion is in progress. The host controller compares the pull up (PUP = 1) and pull down (PUP = 0) measurement results, a difference less than -400mV indicates an open wire at C(n-1).

HSR21 - GPIO Open-Wire Check: The LTC6813 shall allow the host controller to detect open wires between thermistors and the ADCs in the LTC6813. Activate internal pull-down switch to bring the GPIO pin voltage down to V- and release the switch before measuring the voltage again. If the GPIO voltage does not rise above minimum voltage defined by system, then the GPIO pin is at open state.

The ADOW command is used to check for any open wires between the ADCs of the LTC6813 and the external cells. This command performs ADC conversions on the C pin inputs identically to the ADCV command, except two internal current sources sink or source current into the two C pins while they are being measured. The pull-up (PUP) bit of the ADOW command determines whether the current sources are sinking or sourcing 100µA.

Internal pull-down switch at each GPIO pin can be used to diagnose open wires between the GPIO pin of the LTC6813 and the external thermistor circuit as described in SM21.

9.10 Watchdog Timer (WDT) and Discharge Timer (FB38-39)

The LTC6813 includes a watchdog timer. If there is no activity on the communication ports for 2 seconds, the part will time out. Upon a timeout, the LTC6813 will go to a low power state and the configuration registers will be reset to their default values. Note that the discharge switches are not turned off if the watchdog timer expires and the discharge timer is being used. The discharge timer is designed to keep the

discharge switches turned on for a programmable duration. After the discharge timer expires there will be no cell discharge.

The watchdog timer is not related to ATSR-1 or ATSR-2, therefore, it does not appear in section 5.2, Assumptions of Use.

9.10.1 Timer Verification

The timer blocks can be verified by allowing them to expire and then reading the contents of the configuration registers.

The WDT will expire if no command is received within a 2 second period. When the watchdog timer expires the value of CFGAR0-3 (under voltage comparison value in memory) will be reset to 0x000. At this time the GPIO bits in CFGBR0 will also be reset to 0. When the watchdog timer expires, the values at CFGAR4 and CFGAR5 will also be reset to 0x0000 when the discharge timer is disabled. At this time the discharge bits in CFGBR0-1 will also be reset to 0.

If the discharge timer is enabled, then, after the timer expires, the discharge time out value (DCTO) in memory will be set to 0x0000.

The status of the discharge timer can be determined by reading Configuration Register Group A using the RDCFGA command. The DCTO value indicates the time left for the discharge timer to fire.

9.11 Temperature Measurements

HSR22 - Multiple GPIO Pins For Measurement: The LTC6813 shall allow the host controller to utilize multiple GPIO pins for temperature measurements.

Temperature measurements can be made with the GPIO pins and an external thermistor. Figure 16 shows the typical biasing circuit for a single negative temperature-coefficient (NTC) thermistor. The pull-up resistor, R_{PU} is selected to correspond to the NTC value, R_{NTC} such that V_{NTC} is around 0.5 V_{PU} at 25°C. The overall circuit response is approximately -1%/°C in the range of typical cell temperatures. If internally generated VREF2 is directly used for pull-up reference, V_{PU}, then there is no need to measure it at a GPIO pin because VREF2 can be measured via internal routing by ADAXD command. However, if system requires a single LTC6813 to measure multiple NTC sensors, then VREF2 can be isolated by an external unity-gain buffer that generates V_{PU}. In such a case system should monitor and compare V_{PU} to VREF2 measured by ADAXD command as described in SM34.

It is recommended that a 1µF capacitor is fitted to the GPIO pins for best overall TME performance across wide range of input voltage. Assuming 1kΩ for R_{FTR_x} and 10kΩ for R_{PU} and R_{NTC} at 25ºC, R_{FTR_y} can be around 10 kΩ such that it matches equivalent input resistance seen by GPIOx.

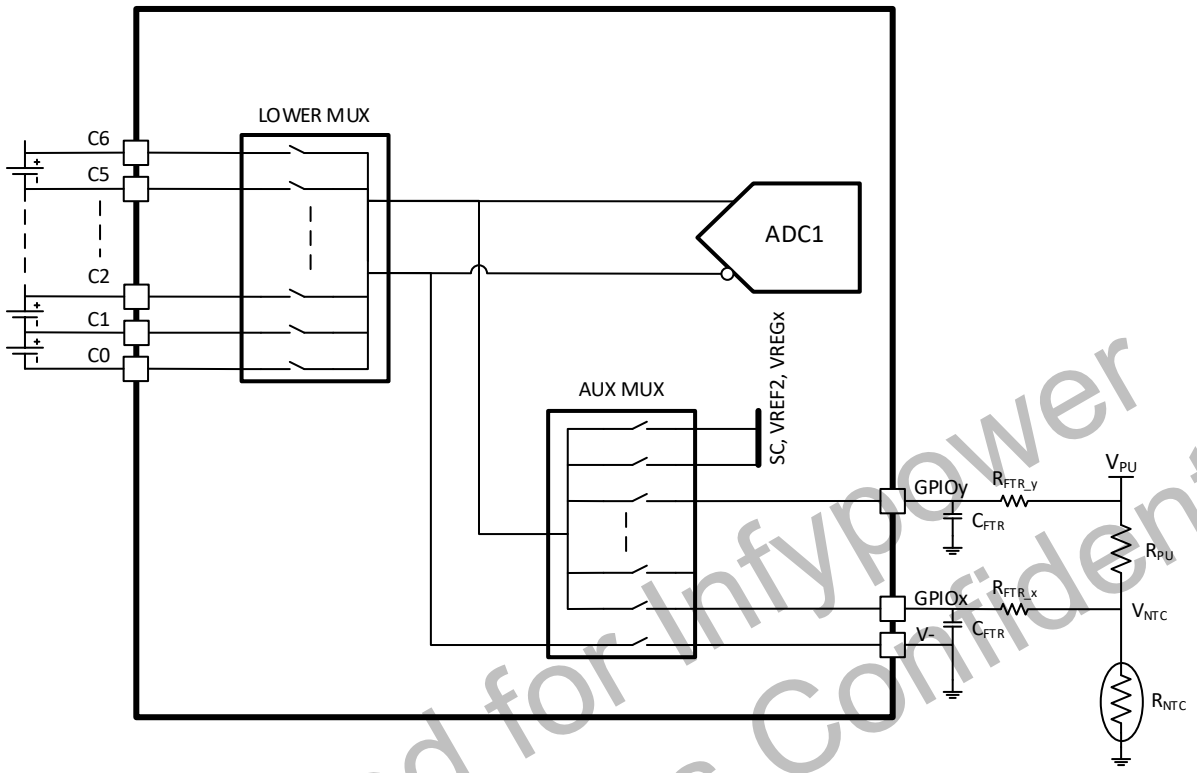

Figure 16. Typical application circuit for external NTC thermistor

HSR23 - Die Temperature Measurement: The LTC6813 shall allow the host controller to monitor the internal die temperature by selecting a dedicated channel in the AUX MUX into an ADC.

The internal temperature is also measured via the AUX MUX and ADC1. The ADSTATD command is used to measure the internal die temperature with digital redundancy, followed by the RDSTATA command to read the result. The die temperature block includes a thermal shutdown circuit. If the internal die temperature exceeds 150°C the cell discharging will be turned off by the thermal shutdown circuit. When the part is in thermal shutdown, the THSD bit in Status Register Group B will be set high.

The thermal shutdown circuit is always present; therefore, it is not included in section 5.2, Assumptions of Use.

9.12 Summary of Hardware Safety Requirements and Related Safety Mechanisms

ATSR / HSR / SM Relationship

Table 8. Relationship between Safety Requirements and Diagnostics

Assumed Technical Safety Requirements	Hardware Safety Requirements		Safety Mechanisms
ATSR-1: Accurate Cell Measurements	HSR1	Sequential Channel Measurement	SM1, SM27, SM29, SM33
	HSR2	Mux Decoder Check	SM1

Assumed Technical Safety Requirements	Hardware Safety Requirements		Safety Mechanisms
ATSR-2: Accurate Temperature Measurements	HSR3	Mux Channel Impedance	SM4, SM21
	HSR4	ADC single channel measurement accuracy	SM1, SM27, SM29, SM33
	HSR5	VREF2 Measurement	SM2
	HSR6	Cell Overlap Measurement	SM8
	HSR7	Redundant Digital Filter	SM5, SM13, SM18, SM20
	HSR8	Diagnostic Test on Redundant Digital Filter	SM5, SM13, SM26
	HSR11	VREGD Measurement.	SM3
	HSR12	VREG Measurement.	SM3
	HSR13	Sum of Cells Measurement	SM23
	HSR14	Cell Voltage Register Clear	SM6, SM7, SM16, SM32
	HSR15	Auxiliary Register Clear	SM2, SM9, SM11, SM16, SM32
	HSR16	Status register Clear	SM3, SM16, SM32
	HSR17	Cell Voltage Register Pattern Generator	SM7
	HSR18	Auxiliary Register Pattern Generator	SM11
	HSR19	Status Register Pattern Generator	SM32
	HSR20	Cell Open Wire Check	SM4, SM29
	HSR21	GPIO Open Wire Check	SM21, SM29
	HSR22	Multiple GPIO Pins For Measurement	SM1, SM14, SM30, SM34
	HSR23	Die Temperature Measurement	SM22
ATSR-3: Detect Communication Errors	HSR9	CRC on SPI Command	SM16, SM19
	HSR10	Dual isoSPI Ports	SM16

9.13 Considerations of Soft Errors

9.13.1 Definitions and Scope

JEDEC Standard No. 89A defines soft errors as nondestructive functional errors induced by energetic ion strikes. Soft errors include single-event upsets (SEU), multiple-bit upsets (MBU), single event functional interrupts (SEFI), single-event transient (SET), and single-event latchup (SEL).

- SEU – Change of state caused by transient signal induced by a single energetic strike. Typically, sequential logic such as latches and RAM are subject to SEU.
- SEFI – Causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device to restore operability. It is often associated with an upset in a control bit or register. SEFI is practically a subset of SEU since SEU in control bits and registers can cause SEFI.
- SET – A momentary voltage excursion (spike) at a node in an IC caused by a single energetic particle strike. It can cause fault in combination logic, clock and other common resources.
- SEL – An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality. SEL is not safety-critical until it results in a hard error due to loss of device functionality. Otherwise, it is most likely to cause higher quiescent current. State-of-art design practices and qualification test should be able to prevent/catch this.

In subsequent discussion on the LTC6813, focus will be on cosmic ray or alpha particle-induced SEU and SET.

9.13.2 Qualitative Analysis

The LTC6813 BMS ASIC from Analog Devices is a precision analog and mixed-signal IC that is distinctively different from other ICs in advanced CMOS technology in terms of devices in use, power supply level, and memory element. Table 9 provides summary of such differences in a high-level.

Table 9. Comparison of LTC6813 and other IC's in advanced CMOS technology

Attribute	LTC6813	Other ICs in Advanced CMOS Technology[1]	Note
Device Feature Size	Minimum 0.5um gate length	Less than 100nm gate length	A device in larger gate length is less susceptible to particle strike due to intrinsically larger parasitic junction capacitor
Power Supply	Minimum 3V	Usually less than 1.5V to reduce power dissipation and leakage	It takes higher charge deposed by a particle strike to flip the logic value of a device with larger supply
Operating Frequency	3.3MHz	> 10's MHz	Probability of error is proportional to operating frequency
Memory Size	< 200Byte	> 100's kByte	The larger the size of memory is the higher the error rate is
Memory Element	Flip-Flop for storing measurement results,	DRAM (1 transistor + 1 capacitor),	Flip-Flops are much more robust at the expense of silicon

	configuration, and device state information, and Fuse OTP for device trim and calibration data	SRAM (6 transistors), or FLASH	size

1) An example is ADSP-CM409F microcontroller.

The level of energy that can cause soft error in the LTC6813 is therefore much larger than in ICs in sub-100nm process technologies. Consequently, soft-error rate (SER) of the LTC6813 is lower by multiple orders of magnitude than that of those ICs, which typically have much larger on-chip memory.

If energized particles ever cause soft errors in the LTC6813 even at insignificant rate, most of them can be either mitigated by system-level measures or can be detected by system as shown in Table 10.

Table 10. Qualitative analysis of soft errors in the LTC6813

Soft Error	Mitigation or Detection
SEU in cell voltage registers	• The register contents are constantly updated at the end of ADC measurement. Only those SEUs that occur before the registers are read by host controller are of concern. • Any SEU causing unrealistic cell voltages can be rejected by host controller. • Other SEU can be mitigated by taking an average value from multiple measurements.
SEU in configuration registers	An SEU in configuration registers will exhibits itself as erroneous measurement or malfunction in measurement. It can be either rejected or detected by host controller by existing safety mechanisms (e.g., reading back registers).
SEU in NVM	There is no shadowing. In other words, contents in NVM directly read whenever ADC conversion is executed.
SET in common resource such as clock tree	• Can cause state machine to malfunction such ADC terminating early or a wrong command executed. Existing safety mechanisms such as SM6 followed by reading back CV registers can detect this. • Can cause malfunction in ADC filter and ADC controller. Fault in ADC filter can be detected by redundant filter (SM5). Fault in ADC controller will result in similar failure modes as in state machine, therefore they can be detected.

9.13.3 Summary

SER of the LTC6813 is negligible compared to other ICs in advanced CMOS technology, which inherently have much higher logic and memory density as well as lower power supply voltage. Improbable transient fault due to SEU and SET can mostly be detected or mitigated by existing safety mechanisms or measures at system level.

10 Dedicated Measures – AEC-Q100 Qualification and Automotive Flow

Analog Devices has qualified this product based on reliability stress tests defined by the Automotive Electronics Council (AEC). Analog Devices guarantees that this product meets or exceeds current AEC-Q100 requirements (qualification guidelines for integrated circuits) by conducting additional device and package level stress tests. These additional tests may include but are not limited to: power cycling, liquid- to-liquid thermal shock, instant solder shock, extended duration autoclave tests, and 100% oxide stress tests. These unique and rigorous tests validate the robustness of Analog Devices' products prior to production release.

Additional dedicated measures are available for lots identified for automotive flow. Our automotive flows were designed to eliminate test escapes and infant mortality failures. Automotive flows incorporate additional screening and inspections and/or tightened criteria in wafer fab, assembly, electrical test, and reliability monitor.

11 Quantitative Analysis Results

The random hardware fault analysis assumes that the LTC6813 is used within the scope of the stated assumptions. The system must utilize the diagnostic features of the LTC6813 to ensure that the reported measurements are not in error. An FMEDA was the quantitative analysis chosen.

11.1 Metric Calculations

Using the assumptions as outlined in section 5.2, the following metrics were calculated. The total FIT was calculated using IEC 62380.

FSR	Total Fault/FIT λ	Safety-Related Fault/FIT λ_{SR}	SPF, Residual Fault/FIT λ_{SPF}, λ_{RF}	Latent MPF/FIT $\lambda_{MPF,l}$	Detected MPF/FIT $\lambda_{MPF,det}$	SPFM/%	LFM/%	PMHF ($T_{Lifetime}$ = 15 yrs)
FSR1	53.56	53.48	0.69	0.20	43.02	98.71	99.61	0.69
FSR2	53.56	48.40	0.52	0.07	39.82	98.92	99.86	0.52

12 Functional Safety Considerations

In addition to this safety manual, an LTC6813 Level 3 PPAP document is also available to customers under an NDA. The Level 3 PPAP document includes AEC-Q100 qualification data, quality systems compliance in design, operations, and manufacturing of ICs.

Please contact your local Analog Devices sales office for further information on ISO 26262 documentation. http://www.analog.com/en/about-adi/contact-us.html

13 Appendix – Command codes and memory map for the LTC6813

Commands

Table 11 lists all the commands and its options for both LTC6813-1 and LTC6813-2.

Table 11. Command Codes

COMMAND DESCRIPTION	NAME	CC[10:0] - COMMAND CODE										
		10	9	8	7	6	5	4	3	2	1	0
Write Configuration Register Group A	WRCFGA	0	0	0	0	0	0	0	0	0	0	1
Write Configuration Register Group B	WRCFGB	0	0	0	0	0	1	0	0	1	0	0
Read Configuration Register Group A	RDCFGA	0	0	0	0	0	0	0	0	0	1	0
Read Configuration Register Group B	RDCFGB	0	0	0	0	0	1	0	0	1	1	0
Read Cell Voltage Register Group A	RDCVA	0	0	0	0	0	0	0	0	1	0	0
Read Cell Voltage Register Group B	RDCVB	0	0	0	0	0	0	0	0	1	1	0
Read Cell Voltage Register Group C	RDCVC	0	0	0	0	0	0	0	1	0	0	0
Read Cell Voltage Register Group D	RDCVD	0	0	0	0	0	0	0	1	0	1	0
Read Cell Voltage Register Group E	RDCVE	0	0	0	0	0	0	0	1	0	0	1
Read Cell Voltage Register Group F	RDCVF	0	0	0	0	0	0	0	1	0	1	1
Read Auxiliary Register Group A	RDAUXA	0	0	0	0	0	0	0	1	1	0	0
Read Auxiliary Register Group B	RDAUXB	0	0	0	0	0	0	0	1	1	1	0
Read Auxiliary Register Group C	RDAUXC	0	0	0	0	0	0	0	1	1	0	1
Read Auxiliary Register Group D	RDAUXD	0	0	0	0	0	0	0	1	1	1	1
Read Status Register Group A	RDSTATA	0	0	0	0	0	0	1	0	0	0	0
Read Status Register Group B	RDSTATB	0	0	0	0	0	0	1	0	0	1	0
Write S Control Register Group	WRSCTRL	0	0	0	0	0	0	1	0	1	0	0
Write PWM Register Group	WRPWM	0	0	0	0	0	1	0	0	0	0	0
Write PWM/S Control Register Group B	WRPSB	0	0	0	0	0	0	1	1	1	0	0
Read S Control Register Group	RDSCTRL	0	0	0	0	0	0	1	0	1	1	0
Read PWM Register Group	RDPWM	0	0	0	0	0	1	0	0	0	1	0
Read PWM/S Control Register Group B	RDPSB	0	0	0	0	0	0	1	1	1	1	0
Start S Control Pulsing and Poll Status	STSCTRL	0	0	0	0	0	0	1	1	0	0	1

COMMAND DESCRIPTION	NAME	CC[10:0] - COMMAND CODE										
		10	9	8	7	6	5	4	3	2	1	0
Clear S Control Register Group	CLRSCTRL	0	0	0	0	0	0	1	1	0	0	0
Start Cell Voltage ADC Conversion and Poll Status	ADCV	0	1	MD[1]	MD[0]	1	1	DCP	0	CH[2]	CH[1]	CH[0]
Start Open Wire ADC Conversion and Poll Status	ADOW	0	1	MD[1]	MD[0]	PUP	1	DCP	1	CH[2]	CH[1]	CH[0]
Start Self-Test Cell Voltage Conversion and Poll Status	CVST	0	1	MD[1]	MD[0]	ST[1]	ST[0]	0	0	1	1	1
Start Overlap Measurements of Cell 7 and Cell 13 Voltages	ADOL	0	1	MD[1]	MD[0]	0	0	DCP	0	0	0	1
Start GPIOs ADC Conversion and Poll Status	ADAX	1	0	MD[1]	MD[0]	1	1	0	0	CHG [2]	CHG [1]	CHG [0]
Start GPIOs ADC Conversion with Digital Redundancy and Poll Status	ADAXD	1	0	MD[1]	MD[0]	0	0	0	0	CHG [2]	CHG [1]	CHG [0]
Start GPIOs Open Wire ADC Conversion and Poll Status	AXOW	1	0	MD[1]	MD[0]	PUP	0	1	0	CHG [2]	CHG [1]	CHG [0]
Start Self-Test GPIOs Conversion and Poll Status	AXST	1	0	MD[1]	MD[0]	ST[1]	ST[0]	0	0	1	1	1
Start Status Group ADC Conversion and Poll Status	ADSTAT	1	0	MD[1]	MD[0]	1	1	0	1	CHST [2]	CHST [1]	CHST [0]
Start Status Group ADC Conversion with Digital Redundancy and Poll Status	ADSTATD	1	0	MD[1]	MD[0]	0	0	0	1	CHST [2]	CHST [1]	CHST [0]
Start Self-Test Status Group Conversion and Poll Status	STATST	1	0	MD[1]	MD[0]	ST[1]	ST[0]	0	1	1	1	1
Start Combined Cell Voltage and GPIO1, GPIO2 Conversion and Poll Status	ADCVAX	1	0	MD[1]	MD[0]	1	1	DCP	1	1	1	1
Start Combined Cell Voltage and SC Conversion and Poll Status	ADCVSC	1	0	MD[1]	MD[0]	1	1	DCP	0	1	1	1
Clear Cell Voltage Register Groups	CLRCELL	1	1	1	0	0	0	1	0	0	0	1
Clear Auxiliary Register Groups	CLRAUX	1	1	1	0	0	0	1	0	0	1	0
Clear Status Register Groups	CLRSTAT	1	1	1	0	0	0	1	0	0	1	1
Poll ADC Conversion Status	PLADC	1	1	1	0	0	0	1	0	1	0	0
Diagnose MUX and Poll Status	DIAGN	1	1	1	0	0	0	1	0	1	0	1
Write COMM Register Group	WRCOMM	1	1	1	0	0	1	0	0	0	0	1
Read COMM Register Group	RDCOMM	1	1	1	0	0	1	0	0	0	1	0
Start I2C/SPI Communication	STCOMM	1	1	1	0	0	1	0	0	0	1	1
Mute Discharge	MUTE	0	0	0	0	0	1	0	1	0	0	0
Unmute Discharge	UNMUTE	0	0	0	0	0	1	0	1	0	0	1

Table 12. Command Bit Descriptions

NAME	DESCRIPTION	VALUES								
MD[1:0]	ADC Mode	MD	ADCOPT(CFGAR0[0]) = 0				ADCOPT(CFGAR0[0]) = 1			
		00	422Hz Mode				1kHz Mode			
		01	27kHz Mode (Fast)				14kHz Mode			
		10	7kHz Mode (Normal)				3kHz Mode			
		11	26Hz Mode (Filtered)				2kHz Mode			
DCP	Discharge Permitted	DCP								
		0	Discharge Not Permitted							
		1	Discharge Permitted							
CH[2:0]	Cell Selection for ADC Conversion			**Total Conversion Time in the 8 ADC Modes**						
		CH		27kHz	14kHz	7kHz	3kHz	2kHz	1kHz	422Hz	26Hz
		000	All Cells	1.1ms	1.3ms	2.3ms	3.0ms	4.4ms	7.2ms	12.8ms	201ms
		001	Cells 1, 7, 13	203µs	232µs	407µs	523µs	756µs	1.2ms	2.2ms	34ms
		010	Cells 2, 8, 14								
		011	Cells 3, 9, 15								
		100	Cells 4, 10, 16								
		101	Cells 5, 11, 17								
		110	Cells 6, 12, 18								
PUP	Pull-Up/Pull-Down Current for Open Wire Conversions	PUP								
		0	Pull-Down Current							
		1	Pull-Up Current							
ST[1:0]	Self-Test Mode Selection			**Self-Test Conversion Result**						
		ST		27kHz	14kHz	7kHz	3kHz	2kHz	1kHz	422Hz	26Hz
		01	Self-Test 1	0x9565	0x9553	0x9555	0x9555	0x9555	0x9555	0x9555	0x9555
		10	Self-test 2	0x6A9A	0x6AAC	0x6AAA	0x6AAA	0x6AAA	0x6AAA	0x6AAA	0x6AAA
CHG[2:0]	GPIO Selection for ADC Conversion			**Total Conversion Time in the 8 ADC Modes**						
		CHG		27kHz	14kHz	7kHz	3kHz	2kHz	1kHz	422Hz	26Hz
		000	GPIO 1-5, 2nd Ref, GPIO 6-9	1.8ms	2.1ms	3.9ms	5.0ms	7.4ms	12.0ms	21.3ms	335ms
		001	GPIO 1 and 6	380µs	439µs	788µs	1.0ms	1.5ms	2.4ms	4.3ms	67.1ms
		010	GPIO 2 and 7								
		011	GPIO 3 and 8								
		100	GPIO 4 and 9								
		101	GPIO 5	200µs	229µs	403µs	520µs	753µs	1.2ms	2.1ms	34ms
		110	2nd Ref								
CHST[2:0]*	Status Group Selection			**Total Conversion Time in the 8 ADC Modes**						
		CHST		27kHz	14kHz	7kHz	3kHz	2kHz	1kHz	422Hz	26Hz
		000	SC, ITMP, VA, VD	742µs	858µs	1.6ms	2.0ms	3.0ms	4.8ms	8.5ms	134ms
		001	SC	200µs	229µs	403µs	520µs	753µs	1.2ms	2.1ms	34ms
		010	ITMP								
		011	VA								
		100	VD								

*Note: Valid options for CHST in ADSTAT command are 0-4. If CHST is set to 5/6 in ADSTAT command, the LTC6813 treats it like ADAX command with CHG =5/6.

Memory Map

Table 13. Configuration Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CFGAR0	RD/WR	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	REFON	DTEN	ADCOPT
CFGAR1	RD/WR	VUV[7]	VUV[6]	VUV[5]	VUV[4]	VUV[3]	VUV[2]	VUV[1]	VUV[0]
CFGAR2	RD/WR	VOV[3]	VOV[2]	VOV[1]	VOV[0]	VUV[11]	VUV[10]	VUV[9]	VUV[8]
CFGAR3	RD/WR	VOV[11]	VOV[10]	VOV[9]	VOV[8]	VOV[7]	VOV[6]	VOV[5]	VOV[4]
CFGAR4	RD/WR	DCC8	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1
CFGAR5	RD/WR	DCTO[3]	DCTO[2]	DCTO[1]	DCTO[0]	DCC12	DCC11	DCC10	DCC9

Table 14. Configuration Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CFGBR0	RD/WR	DCC16	DCC15	DCC14	DCC13	GPIO9	GPIO8	GPIO7	GPIO6
CFGBR1	RD/WR	MUTE	FDRF	PS[1]	PS[0]	DTMEN	DCC0	DCC18	DCC17
CFGBR2	RD/WR	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0
CFGBR3	RD/WR	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0
CFGBR4	RD/WR	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0
CFGBR5	RD/WR	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0

Table 15. Cell Voltage Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVAR0	RD	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
CVAR1	RD	C1V[15]	C1V[14]	C1V[13]	C1V[12]	C1V[11]	C1V[10]	C1V[9]	C1V[8]
CVAR2	RD	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
CVAR3	RD	C2V[15]	C2V[14]	C2V[13]	C2V[12]	C2V[11]	C2V[10]	C2V[9]	C2V[8]
CVAR4	RD	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
CVAR5	RD	C3V[15]	C3V[14]	C3V[13]	C3V[12]	C3V[11]	C3V[10]	C3V[9]	C3V[8]

Table 16. Cell Voltage Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVBR0	RD	C4V[7]	C4V[6]	C4V[5]	C4V[4]	C4V[3]	C4V[2]	C4V[1]	C4V[0]
CVBR1	RD	C4V[15]	C4V[14]	C4V[13]	C4V[12]	C4V[11]	C4V[10]	C4V[9]	C4V[8]
CVBR2	RD	C5V[7]	C5V[6]	C5V[5]	C5V[4]	C5V[3]	C5V[2]	C5V[1]	C5V[0]
CVBR3	RD	C5V[15]	C5V[14]	C5V[13]	C5V[12]	C5V[11]	C5V[10]	C5V[9]	C5V[8]
CVBR4	RD	C6V[7]	C6V[6]	C6V[5]	C6V[4]	C6V[3]	C6V[2]	C6V[1]	C6V[0]
CVBR5	RD	C6V[15]	C6V[14]	C6V[13]	C6V[12]	C6V[11]	C6V[10]	C6V[9]	C6V[8]

Table 17. Cell Voltage Register Group C

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVCR0	RD	C7V[7]	C7V[6]	C7V[5]	C7V[4]	C7V[3]	C7V[2]	C7V[1]	C7V[0]
CVCR1	RD	C7V[15]	C7V[14]	C7V[13]	C7V[12]	C7V[11]	C7V[10]	C7V[9]	C7V[8]
CVCR2*	RD	C8V[7]*	C8V[6]*	C8V[5]*	C8V[4]*	C8V[3]*	C8V[2]*	C8V[1]*	C8V[0]*
CVCR3*	RD	C8V[15]*	C8V[14]*	C8V[13]*	C8V[12]*	C8V[11]*	C8V[10]*	C8V[9]*	C8V[8]*
CVCR4	RD	C9V[7]	C9V[6]	C9V[5]	C9V[4]	C9V[3]	C9V[2]	C9V[1]	C9V[0]
CVCR5	RD	C9V[15]	C9V[14]	C9V[13]	C9V[12]	C9V[11]	C9V[10]	C9V[9]	C9V[8]

*After performing the ADOL command, CVCR2 and CVCR3 of Cell Voltage Register Group C will contain the result of measuring Cell 7 from ADC1.

Table 18. Cell Voltage Register Group D

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVDR0	RD	C10V[7]	C10V[6]	C10V[5]	C10V[4]	C10V[3]	C10V[2]	C10V[1]	C10V[0]
CVDR1	RD	C10V[15]	C10V[14]	C10V[13]	C10V[12]	C10V[11]	C10V[10]	C10V[9]	C10V[8]
CVDR2	RD	C11V[7]	C11V[6]	C11V[5]	C11V[4]	C11V[3]	C11V[2]	C11V[1]	C11V[0]
CVDR3	RD	C11V[15]	C11V[14]	C11V[13]	C11V[12]	C11V[11]	C11V[10]	C11V[9]	C11V[8]
CVDR4	RD	C12V[7]	C12V[6]	C12V[5]	C12V[4]	C12V[3]	C12V[2]	C12V[1]	C12V[0]
CVDR5	RD	C12V[15]	C12V[14]	C12V[13]	C12V[12]	C12V[11]	C12V[10]	C12V[9]	C12V[8]

Table 19. Cell Voltage Register Group E

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVER0	RD	C13V[7]	C13V[6]	C13V[5]	C13V[4]	C13V[3]	C13V[2]	C13V[1]	C13V[0]
CVER1	RD	C13V[15]	C13V[14]	C13V[13]	C13V[12]	C13V[11]	C13V[10]	C13V[9]	C13V[8]
CVER2*	RD	C14V[7]*	C14V[6]*	C14V[5]*	C14V[4]*	C14V[3]*	C14V[2]*	C14V[1]*	C14V[0]*
CVER3*	RD	C14V[15]*	C14V[14]*	C14V[13]*	C14V[12]*	C14V[11]*	C14V[10]*	C14V[9]*	C14V[8]*
CVER4	RD	C15V[7]	C15V[6]	C15V[5]	C15V[4]	C15V[3]	C15V[2]	C15V[1]	C15V[0]
CVER5	RD	C15V[15]	C15V[14]	C15V[13]	C15V[12]	C15V[11]	C15V[10]	C15V[9]	C15V[8]

*After performing the ADOL command, CVER2 and CVER3 of Cell Voltage Register Group E will contain the result of measuring Cell 13 from ADC2.

Table 20. Cell Voltage Register Group F

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVFR0	RD	C16V[7]	C16V[6]	C16V[5]	C16V[4]	C16V[3]	C16V[2]	C16V[1]	C16V[0]
CVFR1	RD	C16V[15]	C16V[14]	C16V[13]	C16V[12]	C16V[11]	C16V[10]	C16V[9]	C16V[8]
CVFR2	RD	C17V[7]	C17V[6]	C17V[5]	C17V[4]	C17V[3]	C17V[2]	C17V[1]	C17V[0]
CVFR3	RD	C17V[15]	C17V[14]	C17V[13]	C17V[12]	C17V[11]	C17V[10]	C17V[9]	C17V[8]
CVFR4	RD	C18V[7]	C18V[6]	C18V[5]	C18V[4]	C18V[3]	C18V[2]	C18V[1]	C18V[0]
CVFR5	RD	C18V[15]	C18V[14]	C18V[13]	C18V[12]	C18V[11]	C18V[10]	C18V[9]	C18V[8]

Table 21. Auxiliary Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVAR0	RD	G1V[7]	G1V[6]	G1V[5]	G1V[4]	G1V[3]	G1V[2]	G1V[1]	G1V[0]
AVAR1	RD	G1V[15]	G1V[14]	G1V[13]	G1V[12]	G1V[11]	G1V[10]	G1V[9]	G1V[8]
AVAR2	RD	G2V[7]	G2V[6]	G2V[5]	G2V[4]	G2V[3]	G2V[2]	G2V[1]	G2V[0]
AVAR3	RD	G2V[15]	G2V[14]	G2V[13]	G2V[12]	G2V[11]	G2V[10]	G2V[9]	G2V[8]
AVAR4	RD	G3V[7]	G3V[6]	G3V[5]	G3V[4]	G3V[3]	G3V[2]	G3V[1]	G3V[0]
AVAR5	RD	G3V[15]	G3V[14]	G3V[13]	G3V[12]	G3V[11]	G3V[10]	G3V[9]	G3V[8]

Table 22. Auxiliary Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVBR0	RD	G4V[7]	G4V[6]	G4V[5]	G4V[4]	G4V[3]	G4V[2]	G4V[1]	G4V[0]
AVBR1	RD	G4V[15]	G4V[14]	G4V[13]	G4V[12]	G4V[11]	G4V[10]	G4V[9]	G4V[8]
AVBR2	RD	G5V[7]	G5V[6]	G5V[5]	G5V[4]	G5V[3]	G5V[2]	G5V[1]	G5V[0]
AVBR3	RD	G5V[15]	G5V[14]	G5V[13]	G5V[12]	G5V[11]	G5V[10]	G5V[9]	G5V[8]
AVBR4	RD	REF[7]	REF[6]	REF[5]	REF[4]	REF[3]	REF[2]	REF[1]	REF[0]
AVBR5	RD	REF[15]	REF[14]	REF[13]	REF[12]	REF[11]	REF[10]	REF[9]	REF[8]

Table 23. Auxiliary Register Group C

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVCR0	RD	G6V[7]	G6V[6]	G6V[5]	G6V[4]	G6V[3]	G6V[2]	G6V[1]	G6V[0]
AVCR1	RD	G6V[15]	G6V[14]	G6V[13]	G6V[12]	G6V[11]	G6V[10]	G6V[9]	G6V[8]
AVCR2	RD	G7V[7]	G7V[6]	G7V[5]	G7V[4]	G7V[3]	G7V[2]	G7V[1]	G7V[0]
AVCR3	RD	G7V[15]	G7V[14]	G7V[13]	G7V[12]	G7V[11]	G7V[10]	G7V[9]	G7V[8]
AVCR4	RD	G8V[7]	G8V[6]	G8V[5]	G8V[4]	G8V[3]	G8V[2]	G8V[1]	G8V[0]
AVCR5	RD	G8V[15]	G8V[14]	G8V[13]	G8V[12]	G8V[11]	G8V[10]	G8V[9]	G8V[8]

Table 24. Auxiliary Register Group D

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVDR0	RD	G9V[7]	G9V[6]	G9V[5]	G9V[4]	G9V[3]	G9V[2]	G9V[1]	G9V[0]
AVDR1	RD	G9V[15]	G9V[14]	G9V[13]	G9V[12]	G9V[11]	G9V[10]	G9V[9]	G9V[8]
AVDR2	RD	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1
AVDR3	RD	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1
AVDR4	RD	C16OV	C16UV	C15OV	C15UV	C14OV	C14UV	C13OV	C13UV
AVDR5	RD	RSVD1	RSVD1	RSVD1	RSVD1	C18OV	C18UV	C17OV	C17UV

Table 25. Status Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STAR0	RD	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]
STAR1	RD	SC[15]	SC[14]	SC[13]	SC[12]	SC[11]	SC[10]	SC[9]	SC[8]
STAR2	RD	ITMP[7]	ITMP[6]	ITMP[5]	ITMP[4]	ITMP[3]	ITMP[2]	ITMP[1]	ITMP[0]
STAR3	RD	ITMP[15]	ITMP[14]	ITMP[13]	ITMP[12]	ITMP[11]	ITMP[10]	ITMP[9]	ITMP[8]
STAR4	RD	VA[7]	VA[6]	VA[5]	VA[4]	VA[3]	VA[2]	VA[1]	VA[0]
STAR5	RD	VA[15]	VA[14]	VA[13]	VA[12]	VA[11]	VA[10]	VA[9]	VA[8]

Table 26. Status Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STBR0	RD	VD[7]	VD[6]	VD[5]	VD[4]	VD[3]	VD[2]	VD[1]	VD[0]
STBR1	RD	VD[15]	VD[14]	VD[13]	VD[12]	VD[11]	VD[10]	VD[9]	VD[8]
STBR2	RD	C4OV	C4UV	C3OV	C3UV	C2OV	C2UV	C1OV	C1UV
STBR3	RD	C8OV	C8UV	C7OV	C7UV	C6OV	C6UV	C5OV	C5UV
STBR4	RD	C12OV	C12UV	C11OV	C11UV	C10OV	C10UV	C9OV	C9UV
STBR5	RD	REV[3]	REV[2]	REV[1]	REV[0]	RSVD	RSVD	MUXFAIL	THSD

Table 27. COMM Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMM0	RD/WR	ICOM0[3]	ICOM0[2]	ICOM0[1]	ICOM0[0]	D0[7]	D0[6]	D0[5]	D0[4]
COMM1	RD/WR	D0[3]	D0[2]	D0[1]	D0[0]	FCOM0[3]	FCOM0[2]	FCOM0[1]	FCOM0[0]
COMM2	RD/WR	ICOM1[3]	ICOM1[2]	ICOM1[1]	ICOM1[0]	D1[7]	D1[6]	D1[5]	D1[4]
COMM3	RD/WR	D1[3]	D1[2]	D1[1]	D1[0]	FCOM1[3]	FCOM1[2]	FCOM1[1]	FCOM1[0]
COMM4	RD/WR	ICOM2[3]	ICOM2[2]	ICOM2[1]	ICOM2[0]	D2[7]	D2[6]	D2[5]	D2[4]
COMM5	RD/WR	D2[3]	D2[2]	D2[1]	D2[0]	FCOM2[3]	FCOM2[2]	FCOM2[1]	FCOM2[0]

Table 28. S Control Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SCTRL0	RD/WR	SCTL2[3]	SCTL2[2]	SCTL2 [1]	SCTL2[0]	SCTL1[3]	SCTL1[2]	SCTL1[1]	SCTL1[0]
SCTRL1	RD/WR	SCTL4[3]	SCTL4[2]	SCTL4[1]	SCTL4[0]	SCTL3[3]	SCTL3[2]	SCTL3[1]	SCTL3[0]
SCTRL2	RD/WR	SCTL6[3]	SCTL6[2]	SCTL6[1]	SCTL6[0]	SCTL5[3]	SCTL5[2]	SCTL5[1]	SCTL5[0]
SCTRL3	RD/WR	SCTL8[3]	SCTL8[2]	SCTL8[1]	SCTL8[0]	SCTL7[3]	SCTL7[2]	SCTL7[1]	SCTL7[0]
SCTRL4	RD/WR	SCTL10[3]	SCTL10[2]	SCTL10[1]	SCTL10[0]	SCTL9[3]	SCTL9[2]	SCTL9[1]	SCTL9[0]
SCTRL5	RD/WR	SCTL12[3]	SCTL12[2]	SCTL12[1]	SCTL12[0]	SCTL11[3]	SCTL11[2]	SCTL11[1]	SCTL11[0]

Table 29. PWM Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWMR0	RD/WR	PWM2[3]	PWM2[2]	PWM2 [1]	PWM2[0]	PWM1[3]	PWM1[2]	PWM1[1]	PWM1[0]
PWMR1	RD/WR	PWM4[3]	PWM4[2]	PWM4[1]	PWM4[0]	PWM3[3]	PWM3[2]	PWM3[1]	PWM3[0]
PWMR2	RD/WR	PWM6[3]	PWM6[2]	PWM6[1]	PWM6[0]	PWM5[3]	PWM5[2]	PWM5[1]	PWM5[0]
PWMR3	RD/WR	PWM8[3]	PWM8[2]	PWM8[1]	PWM8[0]	PWM7[3]	PWM7[2]	PWM7[1]	PWM7[0]
PWMR4	RD/WR	PWM10[3]	PWM10[2]	PWM10[1]	PWM10[0]	PWM9[3]	PWM9[2]	PWM9[1]	PWM9[0]
PWMR5	RD/WR	PWM12[3]	PWM12[2]	PWM12[1]	PWM12[0]	PWM11[3]	PWM11[2]	PWM11[1]	PWM11[0]

Table 30. PWM/S Control Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PSR0	RD/WR	PWM14[3]	PWM14[2]	PWM14 [1]	PWM14[0]	PWM13[3]	PWM13[2]	PWM13[1]	PWM13[0]
PSR1	RD/WR	PWM16[3]	PWM16[2]	PWM16[1]	PWM16[0]	PWM15[3]	PWM15[2]	PWM15[1]	PWM15[0]
PSR2	RD/WR	PWM18[3]	PWM18[2]	PWM18[1]	PWM18[0]	PWM17[3]	PWM17[2]	PWM7[1]	PWM17[0]
PSR3	RD/WR	SCTL14[3]	SCTL14[2]	SCTL14[1]	SCTL14[0]	SCTL13[3]	SCTL13[2]	SCTL13[1]	SCTL13[0]
PSR4	RD/WR	SCTL16[3]	SCTL16[2]	SCTL16[1]	SCTL16[0]	SCTL15[3]	SCTL15[2]	SCTL15[1]	SCTL15[0]
PSR5	RD/WR	SCTL18[3]	SCTL18[2]	SCTL18[1]	SCTL18[0]	SCTL17[3]	SCTL17[2]	SCTL17[1]	SCTL17[0]

Table 31. Memory Bit Descriptions

NAME	DESCRIPTION	VALUES
GPIOx	GPIOx Pin Control	Write: 0 -> GPIOx Pin Pull-Down ON; 1-> GPIOx Pin Pull-Down OFF (Default) Read: 0 -> GPIOx Pin at Logic 0; 1 -> GPIOx Pin at Logic 1
REFON	Reference Powered Up	1 -> Reference Remains Powered Up Until Watchdog Timeout 0 -> Reference Shuts Down After Conversions (Default)
DTEN	Discharge Timer Enable (READ ONLY)	1 -> Enables the Discharge Timer for Discharge Switches 0 -> Disables Discharge Timer
ADCOPT	ADC Mode Option Bit	ADCOPT: 0 -> Selects Modes 27kHz, 7kHz, 422Hz or 26Hz with MD[1:0] Bits in ADC Conversion Cmds (Default) 1 -> Selects Modes 14kHz, 3kHz, 1kHz or 2kHz with MD[1:0] Bits in ADC Conversion Cmds
VUV	Undervoltage Comparison Voltage*	Comparison Voltage = (VUV + 1) • 16 • 100μV Default: VUV = 0x000
VOV	Overvoltage Comparison Voltage*	Comparison voltage = VOV • 16 • 100μV Default: VOV = 0x000
DCC[x]	Discharge Cell x	x = 1 to 18 1 -> Turn ON Shorting Switch for Cell x 0 -> Turn OFF Shorting Switch for Cell x (Default) x = 0 1 -> Turn ON GPIO9 Pull-Down 0 -> Turn OFF GPIO9 Pull-Down (Default)
DCTO	Discharge Time Out Value	DCTO (Write): 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F Time (Min): Disabled | 0.5 | 1 | 2 | 3 | 4 | 5 | 10 | 15 | 20 | 30 | 40 | 60 | 75 | 90 | 120 DCTO (Read): 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F Time Left (Min): Disabled or Timeout | 0-0.5 | 0.5-1 | 1-2 | 2-3 | 3-4 | 4-5 | 5-10 | 10-15 | 15-20 | 20-30 | 30-40 | 40-60 | 60-75 | 75-90 | 90-120
MUTE	Mute Status (READ ONLY)	1 -> Mute is Activated, and Discharging is Disabled 0 -> Mute is Deactivated
FDRF	Force Digital Redundancy Failure	1 -> Forces the Digital Redundancy Comparison for ADC Conversions to Fail 0 -> Enables the Normal Redundancy Comparison
PS[1:0]	Digital Redundancy Path Selection	11 -> Redundancy is Applied Only to ADC3 Digital Path 10 -> Redundancy is Applied Only to ADC2 Digital Path 01 -> Redundancy is Applied Only to ADC1 Digital Path 00 -> Redundancy is Applied Sequentially to ADC1, ADC2 and ADC3 Digital Paths During Cell Conversions and Applied to ADC1 During AUX and STATUS Conversions
DTMEN	Enable Discharge Timer Monitor	1 -> Enables the Discharge Timer Monitor Function if the DTEN Pin is Asserted 0 -> Disables the Discharge Timer Monitor Function. The Normal Discharge Timer Function Will Be Enabled If the DTEN Pin Is Asserted
CxV	Cell x Voltage*	x = 1 to 18 16-Bit ADC Measurement Value for Cell x Cell Voltage for Cell x = CxV • 100μV CxV is Reset to 0xFFFF on Power-Up and After Clear Command

NAME	DESCRIPTION	VALUES	
GxV	GPIO x Voltage*	x = 1 to 9	16-Bit ADC Measurement Value for GPIOx Voltage for GPIOx = GxV • 100μV GxV is Reset to 0xFFFF on Power-Up and After Clear Command
REF	2nd Reference Voltage*		16-Bit ADC Measurement Value for 2nd Reference Voltage for 2nd Reference = REF • 100μV **Normal Range is within 2.988V to 3.012V Considering Data Sheet Limits, Thermal Hysteresis and Long-Term Drift**
SC	Sum of Cells Measurement*		16-Bit ADC Measurement Value of the Sum of all Cell Voltages Sum of all Cells Voltage = SC • 100μV • 30
ITMP	Internal Die Temperature*		16-Bit ADC Measurement Value of Internal Die Temperature **Temperature Measurement Voltage = ITMP • 100μV/7.6mV/°C – 276°C**
VA	Analog Power Supply Voltage*		16-Bit ADC Measurement Value of Analog Power Supply Voltage Analog Power Supply Voltage = VA • 100μV **The Value of VA is Set by External Components and Should Be in the Range 4.5V to 5.5V for Normal Operation**
VD	Digital Power Supply Voltage*		16-Bit ADC Measurement Value of Digital Power Supply Voltage Digital Power Supply Voltage = VD • 100μV **Normal range is within 2.7V to 3.6V**
CxOV	Cell x Over-voltage Flag	x = 1 to 18	Cell Voltage Compared to VOV Comparison Voltage 0 -> Cell x Not Flagged for Overvoltage Condition; 1 -> Cell x Flagged
CxUV	Cell x Under-voltage Flag	x = 1 to 18	Cell Voltage Compared to VUV Comparison Voltage 0 -> Cell x Not Flagged for Undervoltage Condition; 1 -> Cell x Flagged
REV	Revision Code	Device Revision Code	
RSVD	Reserved Bits	Read: Read Back Value Can Be 1 or 0	
RSVD0	Reserved Bits	Read: Read Back Value is Always 0	
RSVD1	Reserved Bits	Read: Read Back Value is Always 1	
MUXFAIL	Multiplexer Self-Test Result	Read: 0 -> Multiplexer Passed Self-Test; 1 -> Multiplexer Failed Self-Test	
THSD	Thermal Shutdown Status	Read: 0 -> Thermal Shutdown Has Not Occurred; 1 -> Thermal Shutdown Has Occurred THSD Bit Cleared to 0 on Read of Status Register Group B	
SCTLx[x]	S Pin Control Bits	0000 – Drive S Pin High (De-Asserted) 0001 – Send 1 High Pulse on S Pin 0010 – Send 2 High Pulses on S Pin 0011 – Send 3 High Pulses on S Pin 0100 – Send 4 High Pulses on S Pin 0101 – Send 5 High Pulses on S Pin 0110 – Send 6 High Pulses on S Pin 0111 – Send 7 High Pulses on S Pin 1XXX – Drive S Pin Low (Asserted)	

NAME	DESCRIPTION	VALUES					
PWMx[x]	PWM Discharge Control	0000 – Selects 0% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired 0001 – Selects 6.7% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired 0010 – Selects 13.3% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired … 1110 – Selects 93.3% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired 1111 – Selects 1000% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired					
ICOMn	Initial Communication Control Bits	Write	I^2C	0110	0001	0000	0111
				START	STOP	BLANK	NO TRANSMIT
			SPI	1000	1010	1001	1111
				CSB Low	CSB Falling Edge	CSB High	NO TRANSMIT
		Read	I2C	0110	0001	0000	0111
				START from Master	STOP from Master	SDA Low Between Bytes	SDA High Between Bytes
			SPI	0111			
Dn	I^2C/SPI Communication Data Byte	Data Transmitted (Received) to (from) I^2C/SPI Slave Device					
FCOMn	Final Communication Control Bits	Write	I2C	0000	1000	1001	
				Master ACK	Master NACK	Master NACK + STOP	
			SPI	X000	1001		
				CSB Low	CSB High		
		Read	I2C	0000	0111	1111	0001	1001
				ACK from Master	ACK from Slave	NACK from Slave	ACK from Slave + STOP from Master	NACK from Slave + STOP from Master
			SPI	1111				

*Voltage equations use the decimal value of registers, 0 to 4095 for 12 bits and 0 to 65535 for 16 bits.