Lab 2: SPI Memory Report

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Input Conditioner:

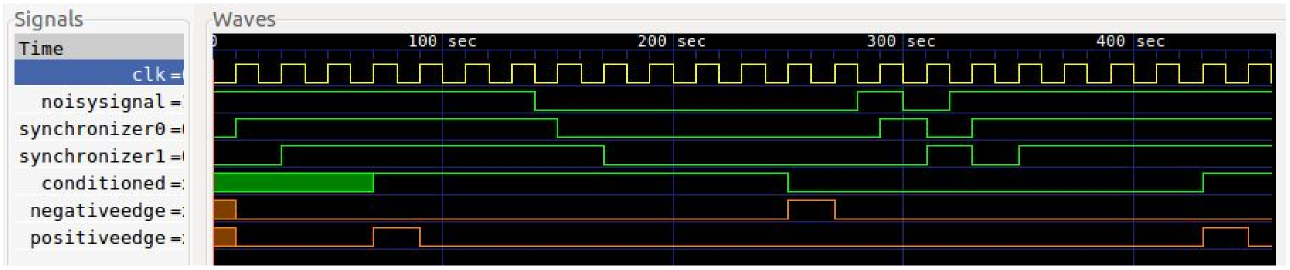

Figure 1: Waveform for the input conditioner.

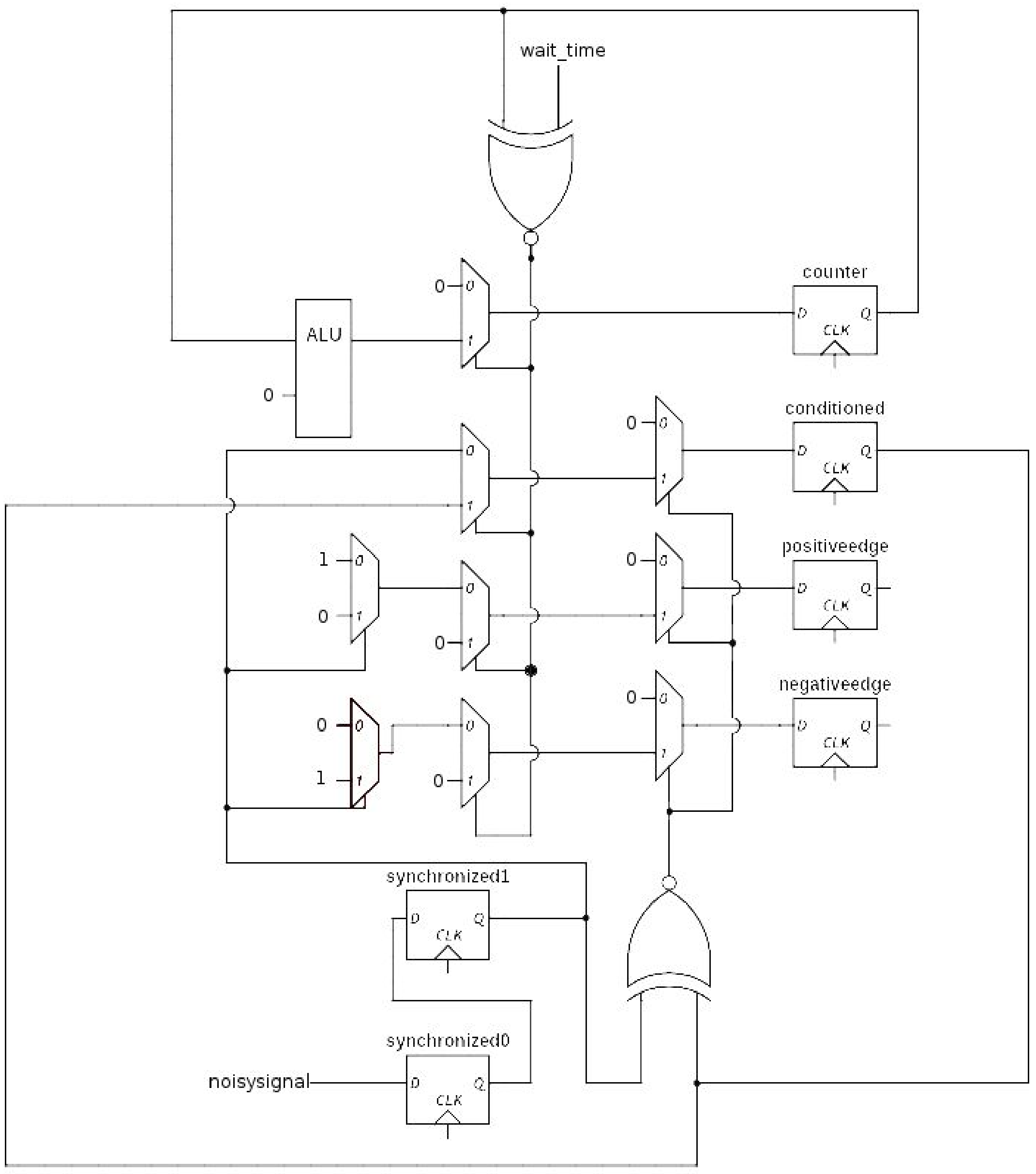

Figure 2: Input conditioner circuit diagram

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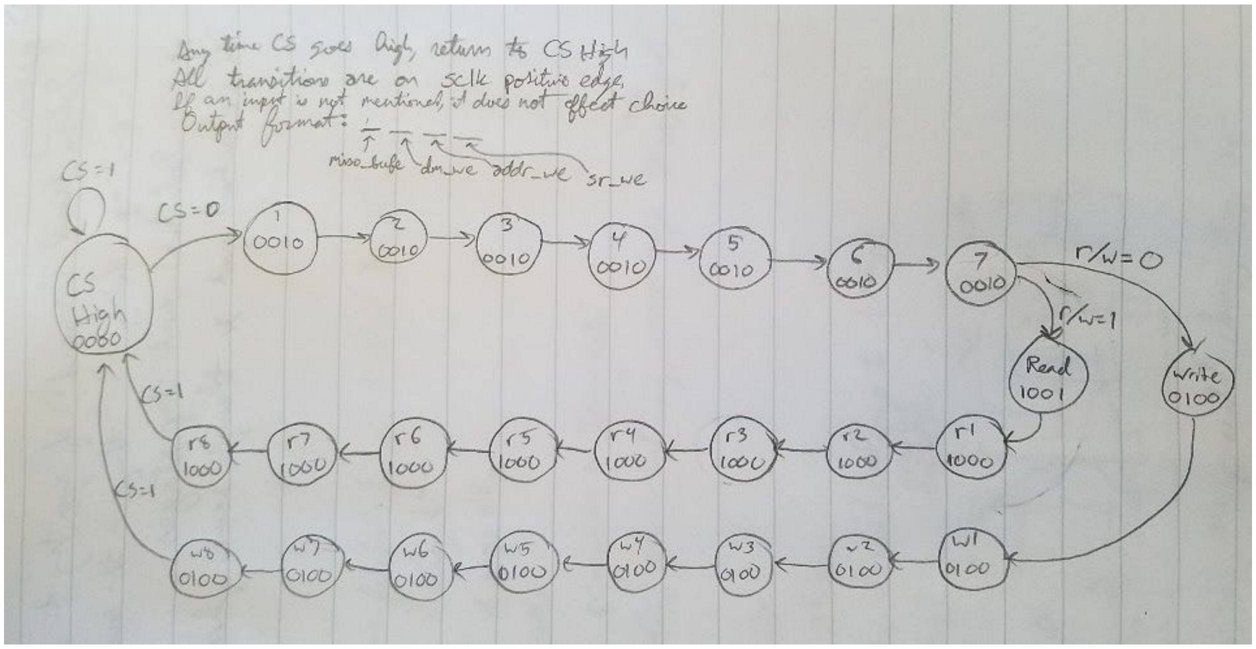
The maximum glitch length would be 2400 nanoseconds. If the wait time is 10, there are a total of 13 clock cycles before the change occurs. For 50MHz, each clock cycle is 20 nanoseconds, so a glitch of 2400 nanoseconds or less would not alter the output.

Our test strategy for the shift register was simply checking that parallel load and serial loading was working correctly. We tested both serial and parallel output for parallel loading and serial loading. We also stepped through 8 bits of shifting to make sure they would all be output correctly. We also checked that parallel load was given precedence over serial loading if both the flag and the peripheral clock edge occurred, in accordance to our design.

Full SPI:



Our finite state machine is shown above. It spends 7 steps in the address write, then branches to either reading or writing. In the single step when it gets the 'write' flag, it loads the shift register with data from the data memory, then turns that flag back off. Any time that CS goes high, everything returns to zero and it resets. ALl transitions happen on the positive edge of sclk. The order of output is: miso_bufe, dm_we, addr_we, sr_we.

The table is shown here. The bolded headers represent the finite state machine's inputs and the cells below them represent the output state after the input transitions.

CS High	**Address Write**	**Read Initialize**	**Read Normal**	**Write**

All 0	miso_bufe = 0
	dm_we = 0
	addr_we = 1
	sr_we = 0
		miso_bufe = 1
		dm_we = 0
		addr_we = 0
		sr_we = 1
			miso_bufe = 1
			dm_we = 0
			addr_we = 0
			sr_we = 0
				miso_bufe = 0
				dm_we = 1
				addr_we = 0
				sr_we = 0

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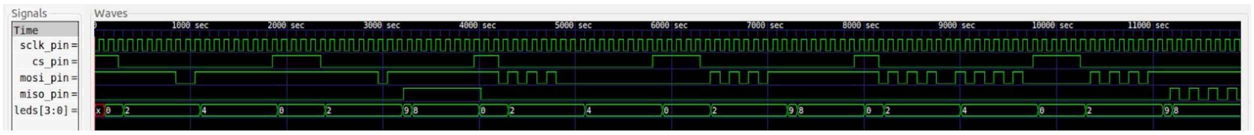
We used the schematic shown in the lab to wire our SPI, with the address for data writing using the most significant 7 digits from the address_latch.

Testing:
Our testing was abbreviated due to time. We ran three big test cases, where we made sure to write to the same address a couple of times and read both all of one value and alternating pieces of memory. This let us catch an issue with our sr_we flag, where it was getting overwritten with all ones or all zeros. We also did a good amount of personal examination of waveforms, as we found those easier to parse than timing in the test file. Alternating let us ensure that things happened when we expected them to, while the solid patterns of all zeros or all ones were easy to see with waveforms. The addresses were fairly arbitrary.



Above you can see three tests, where we would write to an address and then read from that address. The read values matched what we expected. The leds represent the outputs of the finite state machine, converted from binary. MOSI was left high when reading, as it no longer affected the memory.

Work Plan:

Our input conditioner took significantly less time than we allocated, mostly because the input conditioner was mostly implemented beforehand. The test bench for the input conditioner took a little longer because we didn't anticipate how difficult it would be to test something so dependent on exact timing. The shift register also took much less time than anticipated. The midpoint took around the allotted time, but we spent less time coding and more time compiling/synthesizing/programming the FPGA. However, making the finite state machine was not something we set aside time for in our work plan, and that ended up taking a while to understand. We also did not include the SPI module in our work plan, so that was a big oversight on our part. Since there was a diagram in place, it didn't take too long to figure out how to build it, but it did take us a long time to make tests for it, since there were so many moving and timing dependent parts. We spent a long time looking at the timing of the tests before we the tests were complete and correct.