12.7 A 1.2V 4.5mW 10b 100MS/s Pipeline ADC in a 65nm CMOS

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Applications using broadband digital wireless modulation require high-resolution low-power ADC over a bandwidth of few megahertz. For a WiFi or a WiMAX standard, an ADC of ~10b resolution in 5 to 20MHz bandwidth is needed. Its sampling frequency should be in a ratio of 5× the channel bandwidth to simplify the anti-aliasing filter. In order to integrate the ADC with the digital functions in an advanced CMOS technology, compliance with the thin-oxyde voltage supply is necessary.

A low-power 1.2V pipelined ADC is implemented in a 65nm CMOS process to achieve 10b resolution at 100MS/s based on the use of a dedicated thin-oxyde high-performance analog (HPA) MOS transistor.

The pipeline ADC, shown in Fig. 12.7.1(a), is composed of eight 1.5b pipelined stages followed by a 2b flash converter as the last stage. In order to optimize the power consumption, the capacitances and the bias current of each stage have been scaled down along the pipeline chain. Measurement results of this ADC revealed a SNDR of 59dB with a power dissipation of 4.5mW. The core occupies 0.07mm^2, and 0.1 mm^2 with the reference.

Figure 12.7.1(b) shows the architecture of the input pipeline stage. To obtain such performances at a low supply voltage (1.2V), this work was based on (i) the use of HPA TMOS for sampling the input signal, (ii) a specific capacitor layout for matching improvement, (iii) a one-stage opamp with adaptive biasing.

Conventional CMOS switches hardly meet the linearity and input-bandwidth requirements due to low gate-driving voltages with low supply voltages. Although bootstrapping circuits exist to improve the on-resistance variations of the sampling switch, conventional circuits based on deep-submicron CMOS may have long-term reliability problems due to bias voltages exceeding the power supply. Thanks to the low threshold voltage (V_t) of our HPA MOS transistor, no artifacts or double oxide transistor have to be used to achieve a very linear input sampling switch. Figure 12.7.2 shows the characteristic of the HPA MOS.

The sampling capacitor value is chosen carefully according to the thermal noise (kT/C) and the matching characteristics to meet the SNDR specifications. The capacitor matching directly impacts the ADC linearity. This requirement is achieved thanks to the interleaving of the sampling capacitor and the DAC capacitor at the layout level. Figure 12.7.3 shows the interleaved capacitor cell.

For high-speed and low-power applications, a single-stage opamp is a perfect candidate. However, its output swing is limited due to cascaded transistors over a reduced supply voltage (1.2V). Here again, the low V_t of the HPA MOS transistor combined with an adaptive biasing circuit allows the use of a single-stage telescopic amplifier (Fig. 12.7.4) that is well-suited to drive a capacitive load at high speed with a low power consumption.

This design achieves a $1V_{pp\text{-}diff}$ output swing with 75db of DC gain at 1.0V supply in simulation. This high output swing can be obtained thanks to an adaptive biasing that controls the input common mode according to temperature and process variations. The adaptive biasing contains a control feedback loop that adjusts the drain-source voltage (V_{ds}) of the opamp current source (TMOS M1 and M1B) and the active load (M8, M9) to about 100mV. The drain-source voltage of the differential input pair is determined by the regulated cascade transistors. A passive switched-capacitor common-mode feedback circuit is applied to keep the output common voltage at half of the supply.

In the 1.5b pipeline architecture, there is one redundant quantization level in each stage that together with the digital correction permits ±Vref/4 (125mV in this design) error in the comparator decision levels. Consequently, the comparator can be a fairly simple dynamic circuit. The implementation consists of a latch stage using the same capacitor for both the input sampling and DAC signal. During the reset phase, the capacitor is pre-charged to the reference voltage. In the acquisition phase, the latch input experiences a voltage that is the difference between the input and the reference voltage. The comparator architecture is shown in Fig. 12.7.1(c).

Figure 12.7.5(a) shows the nonlinearity of the ADC. The DNL is <±0.1LSB, and the INL is <±0.2LSB, demonstrating well-matched capacitors and enough opamp DC gain.

Figure 12.7.5(b) shows measured THD, SNDR, SFDR and ENOB as a function of conversion rate at an input frequency of 5MHz. Thanks to adaptive biasing, the amplifier biasing current can be multiplied by 2 up to 8mA to obtain 9.1b at 170 MS/s.

The THD, SNDR, SFDR and ENOB as a function of the input frequency at 100MS/s are shown in Fig. 12.7.5(c). The HPA input switches are linear enough to achieve 9b for f_{in}=200MHz.

The ENOB as a function of the supply voltage is shown in Fig. 12.7.5(d). The signal frequency is 5MHz and the conversion rate is 100MS/s. The adaptive biasing allows to achieve 9.3b at 0.9V.

As a reference, the comparison with reporting 10b ADCs is shown in Fig. 12.7.6(a). Using the typical FOM definition for ADCs,

$$FOM = \frac{Power}{2^{ENOB} * Fs}$$

The circuit is implemented in 65nm CMOS technology. The performances of the ADC are summarized in Fig. 12.7.6(b). The total power consumption of the ADC is 4.5mW for a 100MHz sinusoidal input signal at 100MS/s. The measured DNL and INL are ±0.1 LSB and ±0.2 LSB, respectively, for 1.0 $V_{pp\text{-}diff}$ signal. The core area of the ADC is 0.07mm^2, as shown in Fig. 12.7.7.

References:

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[2] R. Wang, K. Martin, D. Johns, and G. Burra, "A 3.3mW 12MS/s 10b Pipelined ADC in 90nm Digital CMOS," *ISSCC Dig. Tech. Papers*, pp 278-279, Feb. 2005.

[3] M. Yoshioka, M. Kudo, K. Gotoh, and Y. Watanabe, "A 10b 125MS/s 40mW Pipelined ADC in 0.18µm CMOS," *ISSCC Dig. Tech. Papers*, pp 282-283, Feb. 2005.

[4] G. Geelen, E. Paulus, D. Simanjuntak, et al., "A 90nm CMOS 1.2 V 10b Power and Speed Programmable Pipelined ADC with 0.5pJ/conversion-step," *ISSCC Dig. Tech. Papers*, pp 214-215, Feb. 2006.

[5] K. Honda, M. Furuta, S. Kawahito "A Low-Power Low-Voltage 10-bit 100-MS/s Pipeline A/D Converter Using Capacitance Coupling Techniques," *IEEE J. Solid-state circuit*, vol. 42, no. 4, pp. 757-765, Apr. 2007.

 978-1-4244-2011-7/08/$25.00

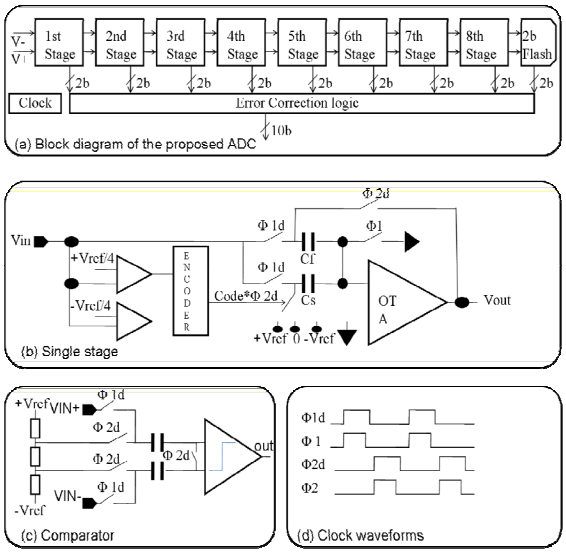

Figure 12.7.1: Pipeline architecture with 1.5-bit per stage.

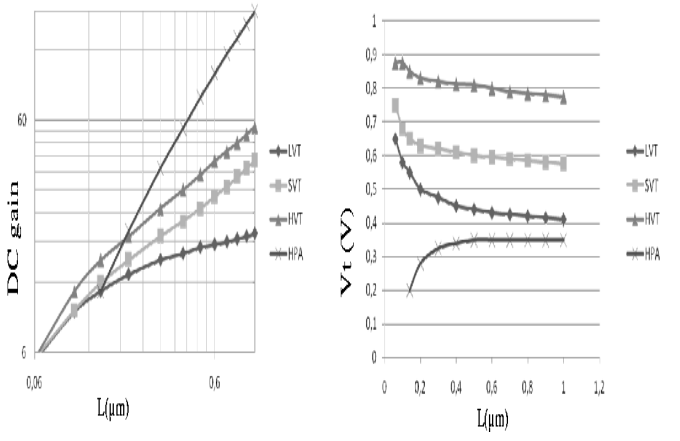

Figure 12.7.2: Characteristic of HPA TMOS.

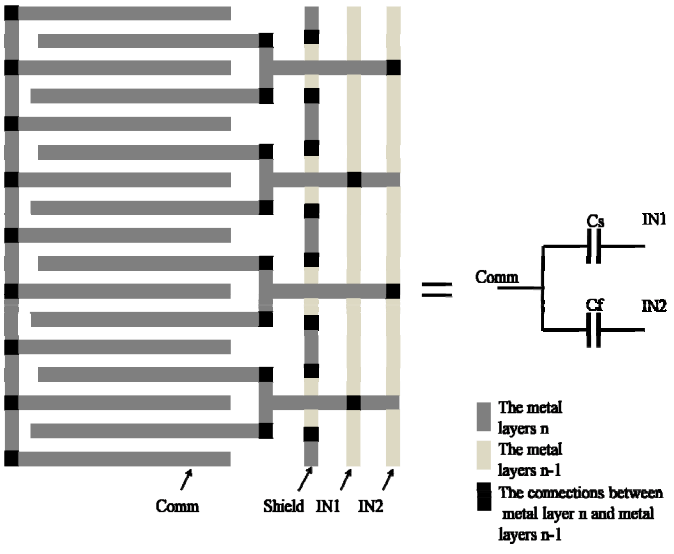

Figure 12.7.3: The interleaved capacitor.

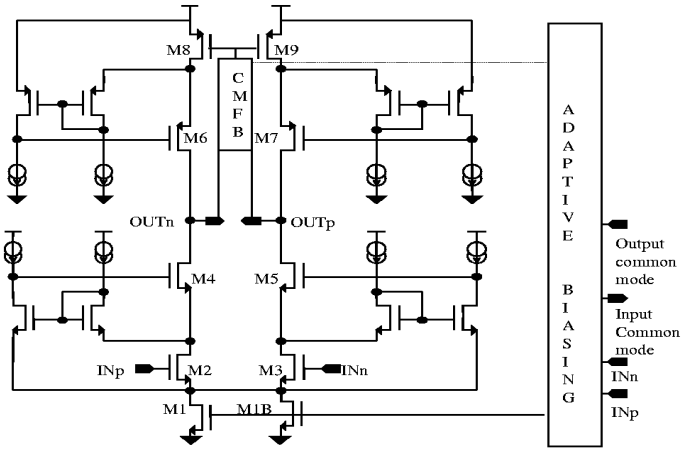

Figure 12.7.4: One-stage telescopic amplifier.

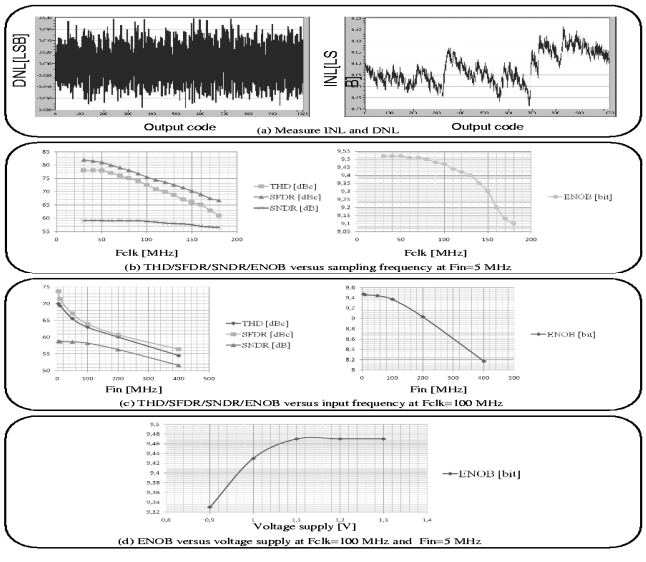

Figure 12.7.5: ADC measured performance

Tech (nm)	VDD (V)	Fs (MHz)	Power (mW)	SNDR (dB)	FOM (pj/step)	Ref.
180	1.8	125	40	53.7	0.79	M.Yoskioa [3]
130	1.2	120	90	57.1	1.25	B.Hemes [1]
90	1.2	12	3.3	52.6	0.76	R.Wang [2]
90	1.2	100	35	56.9	0.6	G.Geelen [4]
90	1.0	100	33	55.3	0.69	K.Honda [5]
65	1.2	100	4.5	59	0.062	This work

(a) Comparison to the state of the art

Resolution	10 bit
Sampling speed	100MS/s
Input range	1.0Vpp
Power Consumption	4.5mW
SNDR	59dB
Active area	0.07mm^2
Technology	65nm

(b) Performance summary

Figure 12.7.6: Performance summary and comparisons.

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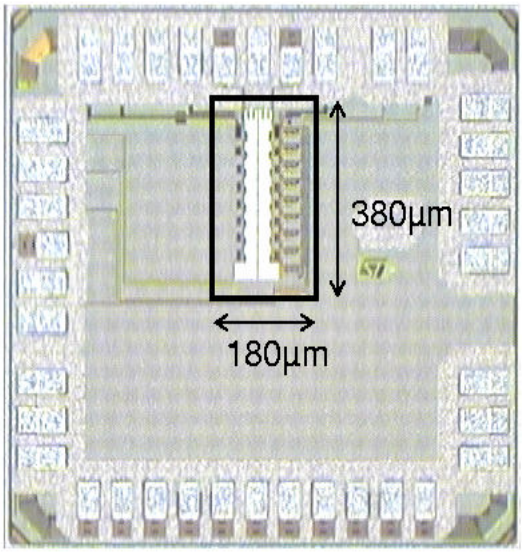

Figure 12.7.7: Die micrograph.

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