A 1.0V 40mW 10b 100MS/s Pipeline ADC in 90nm CMOS

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ABSTRACT

A 1.0V 10b 100MS/s pipeline ADC consuming 40mW fabricated in a 90nm CMOS process is described. Design consideration for the thermal noise of operational amplifiers effectively saves the power consumption of the ADC with conventional architecture at 1.0V supply. Measured peak SNDR of the ADC is 56.5dB. It occupies 0.52mm^2 with on-chip decoupling capacitors and 0.31mm^2 without the capacitors, both of which includes the buffer for reference voltages.

I. INTRODUCTION

Highly power efficient data converters are significant for every electrical equipments especially for battery powered ones. Furthermore, since performance of the converters have been required to be higher and higher while keeping or reducing the power, power efficiency of the converters should be improved greatly.

Power efficiency of ADCs have been drastically improved recently. In the recent papers describing the ADCs which have 10b resolution and sample at a rate of 100MHz, for example, [1] proposed the ADC with conventional architecture whereas [2] and [3] proposed the ADCs with modified front-end circuits. The latter ones succeed in reducing the power consumption at the cost of enlarging the input signal swing of the ADCs. Since the input driving circuit for the ADCs consumes more power to drive the enlarged signal swing than that for the other conventional ADCs in general, it should be noted that the circuit does not always contribute reduction of power consumption of an overall system including the ADCs.

In order to achieve high power efficiency, advanced CMOS devices are attractive for analog designers because the devices have high capability in its performance. However, using the devices does not always guarantee low power consumption in general because the devices require the low supply voltages such as 1.0V.

This paper describes a 10b 100MS/s pipelined ADC with conventional architecture fabricated in a 90nm CMOS process. The ADC operates at a supply voltage of 1.0V and consumes only 40mW. The paper also reveals that careful design consideration especially for the thermal noise of operational amplifiers can effectively save the power consumption of the ADC even with conventional architecture and even under the condition of the low supply voltages such as 1.0V.

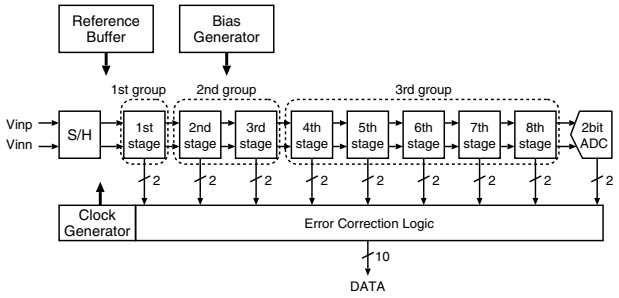

Fig. 1. Block digram of the ADC

II. ADC ARCHITECTURE

Pipeline architecture is selected for the ADC because of its area and power saving capability. Fig. 1 shows the block diagram of the ADC. Main part of the ADC consists of a S/H stage and eight 1.5b pipeline stages followed by a 2b flash converter. All of the pipeline stages are identical in architecture, while these are different in transistor width, current and sampling capacitance, which are described later.

The other blocks of the ADC are peripheral analog blocks and digital blocks. The analog blocks include a buffer for reference voltages and a bias current generator. The digital blocks consist of four phase clock generator, error correction logic and data registers.

The supply voltage for the ADC is 1.0V. Both the input and the internal differential signal swings are the same voltage (1.0Vpp).

III. CIRCUIT IMPLEMENTATION

A. S/H stage

Fig. 2 shows the architecture of the S/H stage. Flip-around architecture is selected due to the noise and power advantages [4].

As shown in the figure, three types of analog switches are employed in the stage. Bootstrapped switches [5] are employed as input sampling switches in the stage for reducing distortion which depends on input frequencies. The bootstrapped switch is composed of both the core transistors (i.e. the devices for a nominal supply voltage of 1.2V) and I/O transistors (i.e. the devices for a nominal supply voltage of 2.5V). NMOS switches are selected as two switches connected to sampling reference Vrs because NMOS has an advantage over PMOS in the on resistance. Taking account of the characteristics

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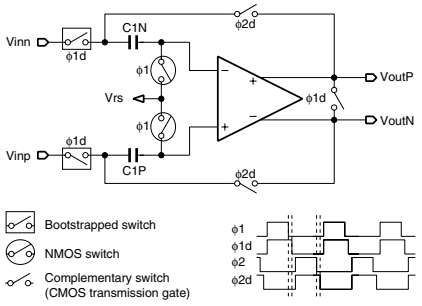

Fig. 2. S/H stage, switch symbols and four phase clocks

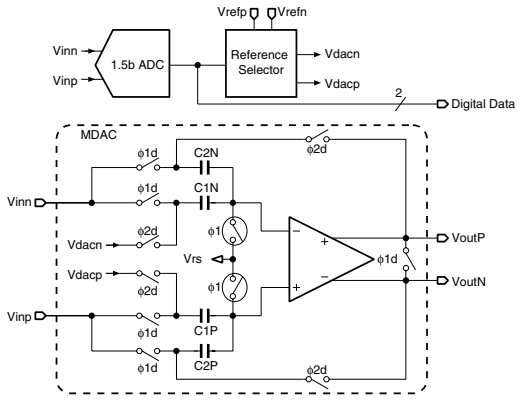

Fig. 3. Pipeline stage

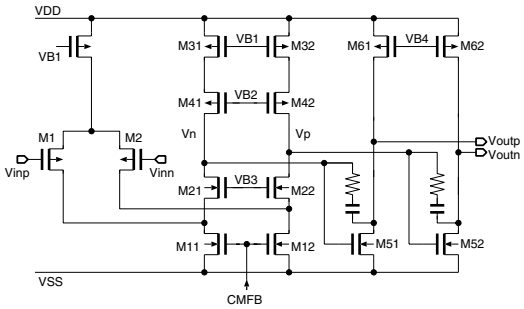

Fig. 4. Operational amplifier

of the NMOS switches, Vrs is set around a quarter of the supply voltage (i.e. 0.25V). The other switches are CMOS transmission gates.

B. Pipeline Stages

Fig. 3 shows the architecture of a pipeline stage, which consists of a 1.5b ADC, a selector for reference voltages and a multiplying DAC (MDAC). No bootstrapped switch is used in the stage because the input frequencies of the stage are limited to the Nyquist frequency. As shown in the figure, a NMOS switch or a CMOS transmission gate are selected for each switch in the similar manner of the S/H stage. The voltage of the sampling reference Vrs for the stages is also the same voltage as that for the S/H stage. Taking account of the matching characteristics and the kT/C noise, the value of four sampling capacitors C1N, C1P, C2N and C2P is designed to meet specifications on SNDR.

C. Operational Amplifier

1) Topology: Every operational amplifier (OPA) in the S/H and the pipeline stages has the same topology and consists of the core transistors. The OPA in the first pipeline stage is required to be the highest performance. The OPAs in the other pipeline stages can be scaled down because the performance of the OPAs can be relaxed compared with that of the OPA in the first pipeline stage.

Since the OPA outputs an differential signal voltage of 1.0Vpp at a supply voltage of 1.0V, two-stage architecture with Miller compensation, shown in Fig. 4, is selected for the OPA. A PMOS differential pair is used in the stage because the input common mode voltage is Vrs (i.e. around a quarter of a supply voltage).

The two-stage OPA and a single-stage OPA have different features. One of the important difference is thermal noise: the thermal noise power of a single-stage OPA depends on the load capacitance [6] whereas the thermal noise power of the two-stage OPA depends on the compensation capacitance. Detailed design considerations are discussed in the following.

2) Input Stage Design and Thermal Noise: The input stage of the OPA affects the gain-bandwidth product and the slew rate of the OPA to a large extent. The gain-bandwidth product and the slew rate affect the settling accuracy of the S/H and the MDACs. The compensation capacitance in the OPA can control the gain-bandwidth product and the slew rate. Increase in the capacitance decreases the gain-bandwidth product and the slew rate without degradation of the phase margin of the OPA. On the other hand, in the scaling which scales the channel width of each MOS transistor together with its drain current (i.e. the total current of the stage) and the compensation capacitance at the same rate, the gain-bandwidth product and the slew rate are maintained. Therefore, we can consider that the settling accuracy is controlled with the compensation capacitance and does not depend on the total current of the stage.

The input stage also determines the power spectral density (PSD) of the thermal noise of the OPA. In contrast to the gain-bandwidth product and the slew rate, the noise PSD is controlled with the scaling. The noise PSD referred to the differential input S_v is expressed as [7]

$$S_v = 8kT\frac{2}{3}\frac{1}{g_{m1}}\left(1+\frac{g_{m11}+g_{m31}}{g_{m1}}\right) \quad (1)$$

where g_{m1}, g_{m11} and g_{m31} are the transconductance of M1, M11 and M31 respectively. The transconductance of a MOSFET is proportional to its drain current under the condition of the scaling. Therefore, the noise PSD can be inversely proportional to the total current of the input stage.

An issue on the thermal noise is that the noise increases with a decrease in supply voltage. For example, drain-to-source voltage of the MOSFETs M11 and M13 in Fig. 4 should be

properly decreased with a decrease in supply voltage. In order to keep the drain current of the MOSFETs unchanged, the gate width of the MOSFETs are required to be enlarged. As a result, the transconductance g_{m11} and g_{m31} increases. As shown in (1), increase in the transconductance g_{m11} and g_{m31} increases the noise PSD of the OPA S_v. Therefore, we should carefully consider the thermal noise of the OPA especially in the case of the OPA operating at the low supply voltages such as 1.0V.

3) Output Stage Design: The output stage of the OPA determines the load capacitance drivability, which can be controlled with the scaling of the stage. The stage also affects the gain-bandwidth product of the OPA to some extent, which is only a constant shift of the gain-bandwidth product in the case of the scaling. Thus a main design issue of the stage is the load capacitance drivability. Since the load capacitance is dominated by the sampling capacitance of the current and the following pipeline stages, the design of the stage almost depends on the design of the sampling capacitance.

D. Stage Scaling

Scaling down the sampling capacitors and the amplifier in each S/H and the pipeline stage along with the stages is a typical design technique to reduce power consumption. This technique is also applied to the design of the ADC. Setting three groups in the ADC as shown in fig. 1, a scaling factor which is the ratio of the scaling between two adjacent groups is designed.

Since the current of the input stage of the OPA can be designed for the noise PSD as we discussed above, the current consumption of the ADC is deeply affected by consideration of the noise. Thus the relation between the sum of the current of the input stages in the OPAs and the total noise power which originates from the OPA should be considered to design the scaling factors.

Since the noise PSD is inversely proportional to the total current of the input stage, the total noise power referred to the input of the ADC P_{Ntotal} is calculated by

$$P_{Ntotal} = \sum_{n=0}^{8} \frac{S_{vn} f_{NBWn}}{A_n^2} = \sum_{n=0}^{8} \frac{f_{NBWn}}{I_n A_n^2} I_1 S_{v1} \qquad (2)$$

where S_{vn} is the input referred noise PSD of the n-th stage, f_{NBWn} is the equivalent noise bandwidth of the OPA in the n-th stage, A_n is a gain from the input of the ADC to the input of the n-th stage and I_n is the current consumption of the input stage of the OPA in the n-th stage. The S/H stage is represented as a "0th" stage in the above equation.

Assuming that the P_{Ntotal} is a certain value, the relation between the scaling factor and the normalized power consumption of the input stages (i.e. the power consumption includes only the power of the input stages in the OPAs) can be calculated using (2). Fig. 5 shows the result of the calculation in the case that the settling errors of the second and the third group of the pipeline stages is designed to be two and four times as large as that of the first group of the stages respectively.

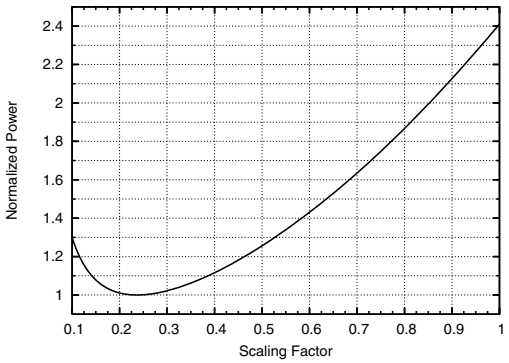

Fig. 5. Normalized power of the input stages vs. scaling factor

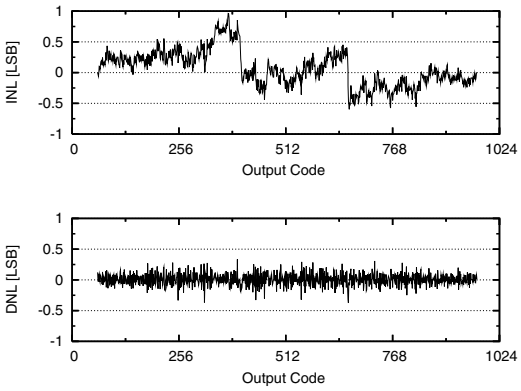

Fig. 6. Measured INL and DNL

E. Reference Buffer

The thermal noise of the buffer for the reference voltages should also be designed to be sufficiently small because the noise of the buffer also contributes the performance of the ADC. Both wide bandwidth with low noise PSD and narrow bandwidth with relatively high noise PSD are possible solutions. The former solution has a disadvantage in current consumption while the latter solution has a disadvantage in suppression of switching noise on the reference lines. Since the switching noise can be suppressed by decoupling capacitors, the latter solution is selected for low power consumption.

IV. Measurements

The ADC is fabricated in a 90nm CMOS process. All the data are measured at a supply voltage of 1.0V and a sampling rate of 100MHz. Power consumption of the ADC is 40mW including all the power of the blocks shown in Fig. 1 (i.e. including the power of the buffer for the reference voltages and the digital blocks.). Fig. 6 shows the measured INL and DNL plots at a input signal frequency of 1MHz. The INL is between 0.96LSB and -0.60LSB, and the DNL is between 0.34LSB and -0.38LSB. Fig. 7 shows the measured SNDR. The peak SNDR is 56.5dB with a input signal frequency of 1MHz. Fig. 8 shows the measured output spectrum with a input signal frequency of 10MHz.

Fig. 9 shows a die micrograph. The ADC occupies

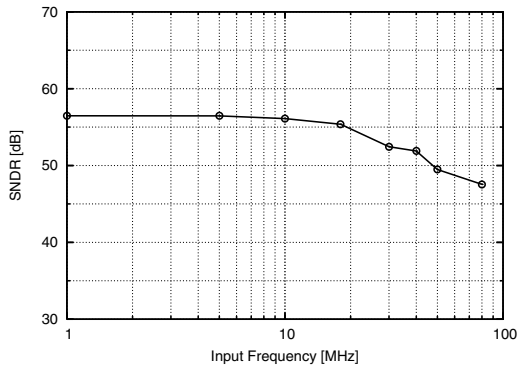

Fig. 7. Measured SNDR vs. input frequencies

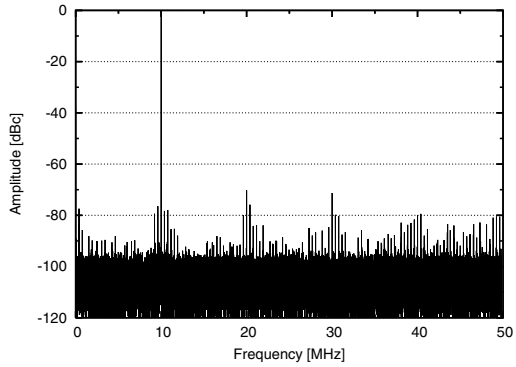

Fig. 8. Measured output spectrum (input frequency=10MHz)

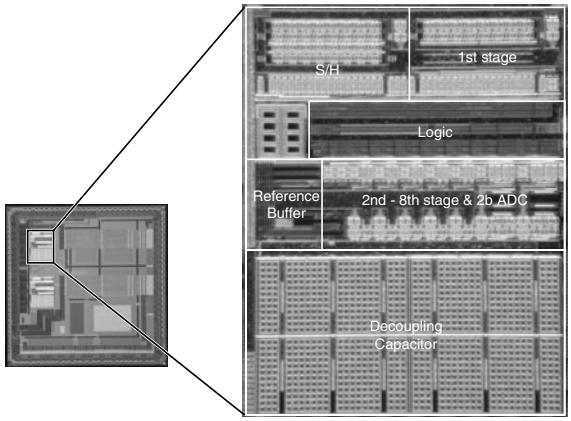

Fig. 9. Die micrograph

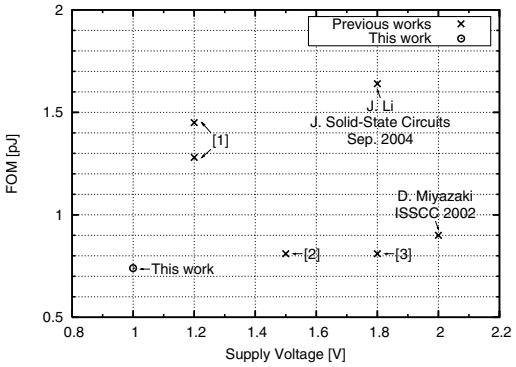

Fig. 10. FOM comparison between previous works and this work

0.52mm^2, including all the blocks shown in Fig. 1 and the decoupling capacitors which is added because the inductance of the package is not sufficiently small (e.g. the inductance is around 5nH). In the case that low inductance packaging technology is available, the ADC occupies 0.31 mm^2 because the on-chip decoupling capacitors can be removed,

Fig. 10 shows figures of merit (FOM) [6] of this work and the previous works which has 10b resolution, sampling rates over 10MHz and supply voltages below 2V. The FOM is defined as

$$\text{FOM} = \frac{P}{2^{\text{ENOB}} \cdot f_s} \tag{3}$$

where P is the power consumption and f_s is the sampling frequency. Since small FOM means high power efficiency, the figure shows that our ADC has the highest power efficiency.

V. Conclusion

A 10b 100MS/s pipeline ADC operating at a supply voltage of 1.0V is described. The ADC is fabricated in a 90nm CMOS process. Measured peak SNDR is 56.5dB and consuming only 40mW. These results shows that the design consideration for the thermal noise of the operational amplifiers can effectively save the power consumption of the ADC even with the conventional architecture and even under the condition of the low supply voltages such as 1.0V. Power consumption will be reduced more with switched amplifier techniques.

Acknowledgment

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