Design of a 1.5-Bit Stage for a 10-Bit Pipeline ADC using 45nm technology

Muhammad Aldacher, *Student Member, IEEE*
Electrical Engineering Department
San Jose State University
One Washington Square, San Jose, CA 95192
muhammad.aldacher@sjsu.edu

Enrique Hernandez, *Student Member, IEEE*
Electrical Engineering Department
San Jose State University
One Washington Square, San Jose, CA 95192
enrique.hernandezsanchez@sjsu.edu

***Abstract*— A 1.8V 1.5-bit stage for a 10-bit pipeline ADC designed using a 45nm CMOS process is proposed. The design utilizes a novel comparator architecture, a sub-ADC digital logic circuit, CMOS transmission gates, bootstrap switches, and a gain-boosted fully differential telescopic opamp for a switched-capacitor MDAC. Taking a 64-point FFT on the output of 1 stage in 2x-gain mode under typical conditions and an input-signal full-scale of 0.8V, the maximum ENOB achieved at 50 MHz sampling frequency is 9.756 bits, with an SNR of 60.495 dB & a total power consumption of 2.0286 mW. The figure-of-merit achieved, based on Walden's calculation, is 0.936 pJ/conv.**

***Index Terms*— Bootstrap switch, Comparator, Gain-boosted, Telescopic Opamp, Pipeline ADC.**

I. Introduction

PIPELINE analog-to-digital converters (ADCs) is considered one of the very popular ADCs architectures used in various applications today, like in communication, instrumentation, and imaging systems. This is because pipeline ADCs offer a good compromise between resolution, speed, and power dissipation. Unlike flash ADCs, pipeline ADCs use less number of comparators, resulting in less power dissipation for high number of bits (N). In addition to that, they are also usually more suitable than the successive-approximation (SAR) ADCs at higher sampling frequencies. This is due to the fact that a pipeline ADC works on several bits in a parallel manner [1-2]. On the other hand, some of the disadvantages of this architecture are in its latency and the complexity of designing the opamp circuit used in each of its stages.

In section II, the architecture of the 1.5 bit/stage pipeline ADC is explained. Section III discusses the Sub-ADC block that includes comparators and a Sub-ADC logic circuit. In section IV, the switches used in the system are presented. The opamp design for the MDAC block is explained in section V, and the final results are presented in section VI, followed by the conclusion in section VII.

II. 1.5 bit/stage Pipelined ADC

In a pipelined ADC, the input signal is sampled at the 1st stage during Φ1 clock phase and compared at the Sub flash ADC against 3 different regions within the full-scale range (V_{FS}), producing 2 digital bits. During Φ2, the sampled input value is multiplied by 2, then depending on the decision made by the sub-ADC, either $-V_{FS}$, $+V_{FS}$, or 0 is added to the multiplied value before passing it to the following stage. This is done using the multiplying DAC (MDAC), as shown in Fig. 1. The number of stages of a 10 bit 1.5bit/stage pipelined ADC is 9, the 1st 8 being 1.5bit/stage and the last one being a normal 2-bit flash ADC. The digital outputs of all the stages then go into a digital correction circuit that produces the final digital output of the whole system, as seen in Fig. 2 [3-5].

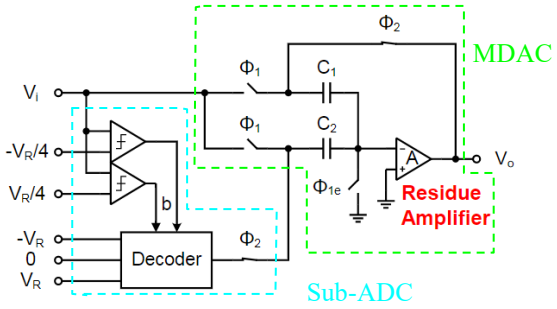


Fig. 1. 1.5bit pipelined stage.

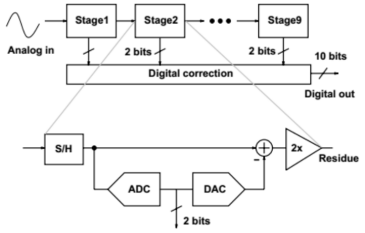


Fig. 2. Pipelined ADC Architecture.

III. Sub-ADC

A. Comparator

The sub-ADC block uses 2 differential clocked comparators. Each comparator receives the input signal, the references, and the common-mode voltage. Using the CMOS switches and the capacitors, Cinp and Cinn, a signal of $V_{CM} - (V_{IN} - V_{REF})$ is applied at the inputs of the Preamp during the amplification phase [6].

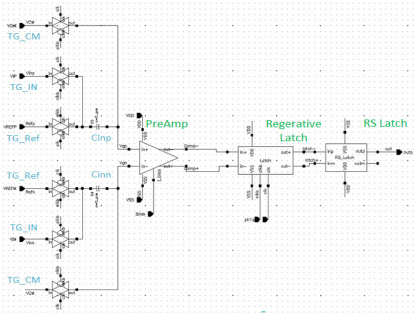
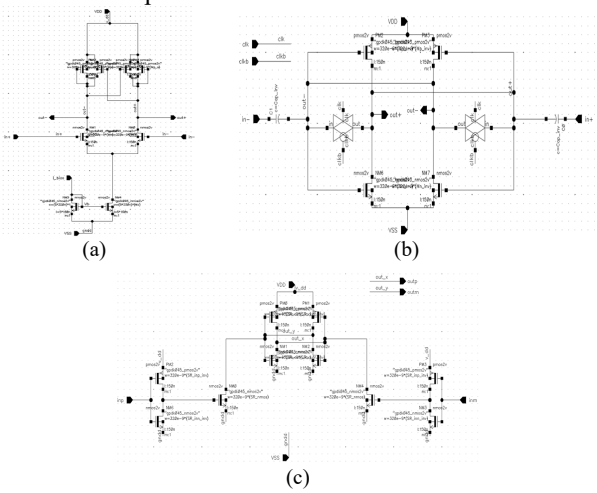


Fig. 3. Clocked Comparator

The preamp, shown in Fig. 4(a), detects the difference between the differential input signals and amplifies it. Using the regenerative latch (Fig. 4(b)), that difference is amplified to the rails. To keep the output values fixed during the sampling phase of the comparator, an RS-latch circuit is employed after the regenerative latch. Since only 2 comparators are used per stage, the comparator doesn't need to resolve extremely low differential input levels, thus can be designed with lower power. From the overdrive test, the minimum input that can be resolved is 14mV.



(a) (b) (c)

Fig. 4. Sub blocks of the Comparator
(a) Preamp (b) Regenerative Latch (c) RS Latch

B. Sub-ADC Logic

The sub-ADC logic receives the comparators' outputs and produces 2 sets of outputs. B1 and B0 are the digital bits that are sent to the digital correction circuit, while S1, S2, and S3 are the control signals that are applied to certain switches to provide the $-V_{FS}$, $+V_{FS}$, or 0 to the MDAC circuit. Table I shows the truth table used to build the logic circuit in Fig. 5.

TABLE I. SUB-ADC LOGIC CIRCUIT TRUTH TABLE

Inputs		Outputs			Stage Output
C2	C1	B2	B1	Controls	
1	1	1	0	S1 = 1	Vout = 2Vin – Vfs
0	1	0	1	S2 = 1	Vout = 2Vin
0	0	0	0	S3 = 1	Vout = 2Vin + Vfs

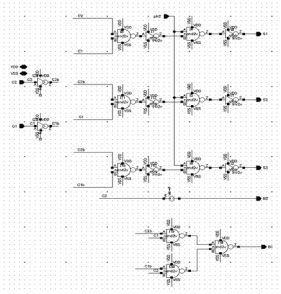


Fig. 5. Sub-ADC Logic Circuit

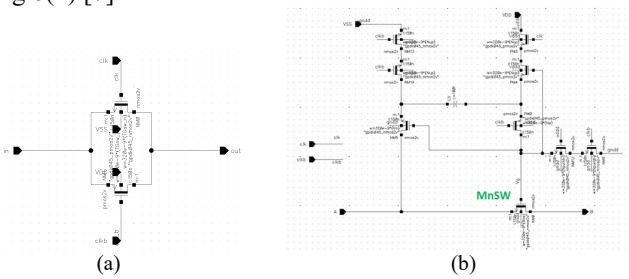
IV. SWITCHES

A. CMOS Transmission Gate

The advantage of using CMOS transmission gates (TGs) is that it passes well a high or a low value input, unlike in the case of using PMOS-only or NMOS-only switches. The TGs are used to pass fixed voltages like the reference voltages controlled by S1, S2, & S3, and the common-mode voltages for the Opamp.

B. Bootstrapped Switch

TGs are not suitable to pass high-swing signals since the R_{ON} of the transistors depend on the input signal that introduces non-linearities. For this reason, a bootstrapped switch is used for passing the input signal to the MDAC block and to connect the feedback capacitor to MDAC output. The bootstrapped switch uses a capacitor to fix the V_{GS} of the main switch transistor, MnSW, as shown Fig.6(b) [7].



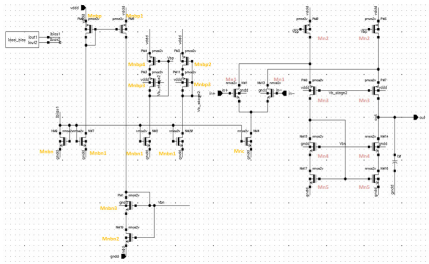
(a) (b)

Fig. 6. Switches used in the design (a) CMOS TG (b) Bootstrapped Switch

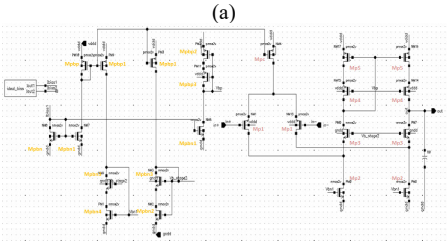
V. OPAMP DESIGN

A. Single-Ended Folded-Cascode Opamps

Single-ended opamps are used within the main gain-boosted telescopic opamp topology. These opamps are connected to the transistor's gate in the cascode stage of the main Opamp in a negative feedback manner, enhancing the total gain. It is required that the unity-gain frequency of the gain-boosting opamps be larger than the -3dB frequency of the original opamp and lower than the 1st non-dominant pole of the original opamp [8]. Depending on the input level to the gain-boosting opamps, the type of the input stage is chosen. For high-level inputs, the input stage is NMOS, and for low-level inputs, the input stage is PMOS. The single-ended opamps with NMOS-input and PMOS-input stages are shown in Fig. 7(a) & 7(b), respectively.



(a)



(b)

Fig. 7. Single-Ended Opamps (a) NMOS-input stage (b) PMOS-input stage

B. Gain-Boosted Telescopic Opamp

The open-loop gain and the unity-gain frequency of the main opamp used for the MDAC block is designed based on the gain and settling errors requirements, given by equations (1) and (2), respectively.

$$Gain\ Error = \frac{1}{A.\beta} < \frac{1}{4}\ LSB \quad (1)$$

$$Settling\ Error = e^{-t/\tau} < \frac{1}{2}\ LSB \quad (2)$$

High-swing cascode biasing is used in the single-ended and the boosted opamps to decrease the V_{DS} of the output stage transistors, increasing the headroom. NMOS-input opamps are used for the upper cascode transistors, with the negative terminals connected to the enhanced transistors' sources and the positive terminals to the desired value for those sources. The same goes for the lower cascode transistors but while using PMOS-input opamps. A switched-capacitor common-mode feedback circuit is a negative feedback, used to keep the output's common mode level close to the desired value during the MDAC's amplification phase.

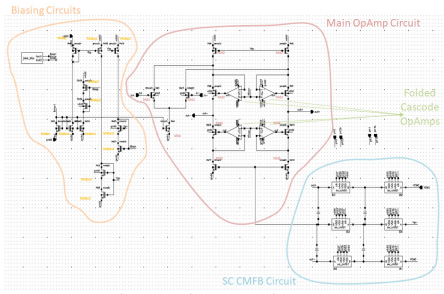


Fig. 8. Gain-Boosted Opamp

C. AC Responses

To find the AC responses for the opamps, the testbench shown in Fig. 9 is used for the single-ended opamps and that in Fig. 10 for the gain-boosted opamp. The AC responses are shown in Fig. 11 & 12, and a summary of the AC parameters are shown in Table II.

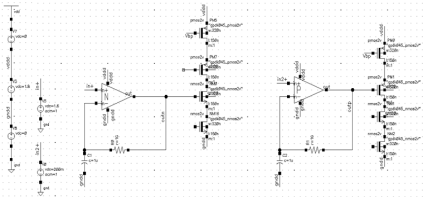


Fig. 9. Testbench for AC Response of Single-Ended Opamps

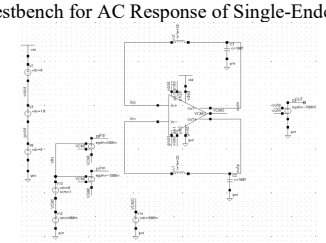
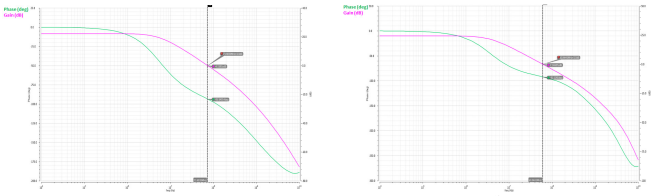


Fig. 10. Testbench for AC Response of Gain-Boosted Opamp



(a) (b)

Fig. 11. AC Responses (a) For NMOS-input Opamp (b) For PMOS-input Opamp

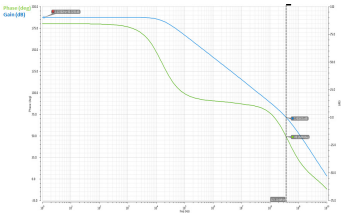


Fig. 12. AC Responses for the Gain-Boosted Opamp

TABLE II. SUMMARY OF OPAMPS' AC RESPONSE PARAMETERS

Parameters	NMOS Opamp	PMOS Opamp	Gain-Boosted Opamp
DC Gain	22.2 dB	25.3 dB	90.9 dB
Unity-Gain frequency	73.9 MHz	60.8 MHz	372.2 MHz
Phase Margin	86.45°	87.87°	49.2°

VI. RESULTS

A. Transient Simulations & FFT

Using the testbench for a 1.5-bit stage in Fig. 13, the functionality of the system is tested for a sampling frequency f_S = 50 MHz and an input signal of f = (7/64) * f_S and amplitude = 0.4V, in normal mode and in 2x gain mode, as presented in Fig. 14 & 15, respectively.

From the 64-point FFT spectrum of the output signal in 2x gain mode, shown in Fig. 16, the SNR is found to be 60.495 dB and the ENOB to be 9.756 bits under typical conditions (TT, V_{DD}=1.8V, 27°). When running the tests while decreasing the input signal amplitude, the SNR and the ENOB decrease as shown in Table III, since the signal level decreases with respect to the noise level.

TABLE III. ENOB & SNR VS INPUT SIGNAL AMPLITUDE

Input Amplitude	ENOB	SNR
Vin_amp = 0.4V	9.756 bits	60.495 dB
Vin_amp = 0.2V	8.943 bits	55.602 dB
Vin_amp = 0.1V	8.425 bits	52.484 dB

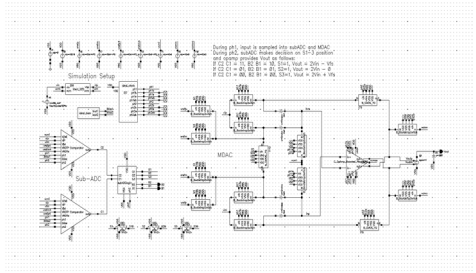


Fig. 13. Testbench for a 1.5-bit stage for a pipelined ADC

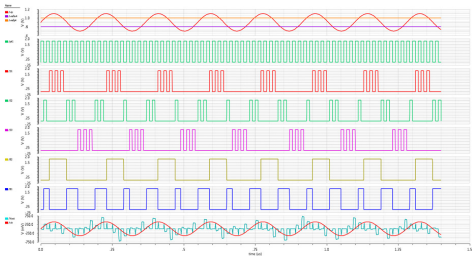


Fig. 14. Transient waveforms in Normal Mode

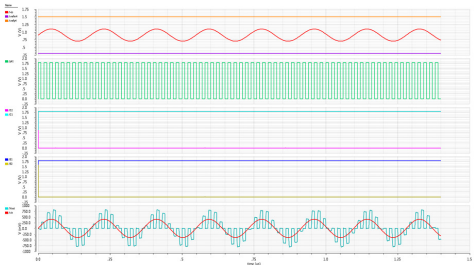


Fig. 15. Transient waveforms in 2x-Gain Mode

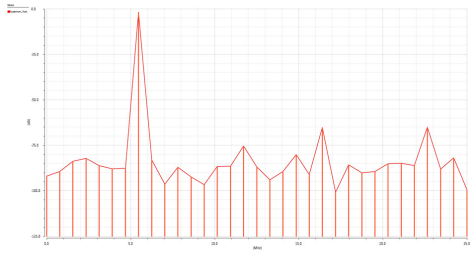


Fig. 16. 64-point FFT spectrum of the 2x-Gain Mode output

B. Corner Simulations

The previous simulations over PVT variations are performed and the results are tabulated in Table IV. The best case is found to be in the typical case (TT, V_{DD}=1.8V, 27°), and the worst cases is found in 2 cases: FF, V_{DD}=1.8V, 27° and SS, V_{DD}=1.7V, 70°. The reason is because biasing circuits are designed for the cascode transistors to have very low V_{DS}, so many of the transistors would have a V_{GS} close to the value of V_{th}. In case of SS corner, V_{th} increases, and the opposite happens in FF. So, during the FF and SS corners, some of the cascode transistors start to leave the saturation region.

TABLE IV. ENOB & SNR ACROSS PVT CORNERS

	TT, 1.8V_{DD}, 27°	TT, 1.8V_{DD}		TT, 27°		1.8V_{DD}, 27°		SS, 1.7V_{DD}, 70°
		0°	70°	1.7V_{DD}	1.9V_{DD}	FF	SS	
ENOB (bits)	9.76	8.57	8.49	9.38	9.31	7.09	8.50	7.09
SNR (dB)	60.5	53.3	52.9	58.2	57.8	44.5	53.0	44.4

C. Power Consumption

Table V shows the power consumption of 1 1.5bit stage. Assuming the total power of a 10-bit pipelined ADC would be 10 times the total power of 1 stage, and the ENOB to be 1 bit lower than that of the 1 stage, the figure-of-merit (FOM) is calculated from equation (3) to be **0.936** pJ/conv.

$$FOM = \frac{10\,x\,P}{2^{ENOB} x\, f_S} \qquad (3)$$

TABLE V. POWER CONSUMPTION

Circuit	Power dissipated
Comparators	2 x 431.100 uW
Sub-ADC Logic	3.586 uW
Switches	78.854 uW
Opamp	1083.96 uW
Total	**2.0286 mW**

VII. CONCLUSION

A 1.5-bit stage for a 10-bit pipelined ADC, with a sampling frequency of 50 MHz and designed using CMOS 45nm technology at 1.8V, is presented. The design utilizes clocked comparators with a resolution of 14mV, along with static CMOS gates to build the Sub-ADC clock. CMOS transmission gates and bootstrapped switches are used for better transmission of the different signals. The opamp used for the MDAC is a gain-boosted opamp, with a DC gain of 90.9 dB and unity-gain frequency of 372.2 MHz. Measured ENOB is 9.756 bits while consuming 2.029mW, resulting in an FOM of 0.936 pJ/conv.

Many improvements can still be applied to the design, like reducing power consumption in the comparators by applying tail switches in the latch. Also sacrificing some of the headroom in the opamps could result in better performance at corner conditions. Stage scaling can also be applied in the 10-bit system to improve the overall FOM.

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