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# EE288 Data Conversions/Analog Mixed-Signal ICs

## Spring 2018

### Lecture 22: OPAMP for ADC

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ENG-259

# Agenda

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- OPAMP Types
  - Telescopic
  - Folded-cascode
  - Gain-Boosting
  - Two-stage
  - Fully-differential
- Simulating OPAMP
  - DC, AC, stb, Transient

# OPAMP Gain Requirement for N-bit ADC

OPAMP is always used in closed loop configuration.

OPAMP Closed-loop Response:

$$V_{\text{out}} = G \times V_{\text{in}} \left( \frac{1}{1 + \frac{1}{A \times \beta}} \right) \left( 1 - e^{-\frac{t}{\tau}} \right)$$

Assume Gain Error should be less than ¼ LSB

$$\frac{1}{\beta A} < \frac{1}{2} \text{ LSB} \rightarrow \frac{1}{\beta A} < \frac{1}{2} \frac{V_{FS}}{2^N}$$

$$A > \frac{2 \cdot 2^N}{\beta \cdot V_{FS}}$$

Resolution	Full Scale	Beta	Gain (dB)	Gain (dB)
N	V <sub>FS</sub> (Volt)	β	$2 \cdot 2^N / (\beta \cdot V_{FS})$	20log(x)
10	0.8	1	5120	74
10	0.8	0.5	10240	80
11	0.8	1	10240	80
11	0.8	0.5	20480	86
12	0.8	1	20480	86
12	0.8	0.5	40960	92
13	0.8	1	40960	92
13	0.8	0.5	81920	98
14	0.8	1	81920	98
14	0.8	0.5	163840	104

# OPAMP Bandwidth Requirement for N-bit ADC

Assume Settling Error should be less than 1/2 LSB

$$e^{-t/\tau} < \frac{1}{2} \text{ LSB} \rightarrow e^{-t/\tau} < \frac{1}{2} \frac{V_{FS}}{2^N} \rightarrow \frac{t}{\tau} > (N + 1)\ln(2) - \ln(V_{FS})$$

$$t = \frac{T_s}{2} = \frac{1}{2f_s}$$

$$\tau = \frac{1}{\omega_{-3dB}} = \frac{1}{2\pi f_{-3dB}} = \frac{1}{2\pi \beta f_u}$$

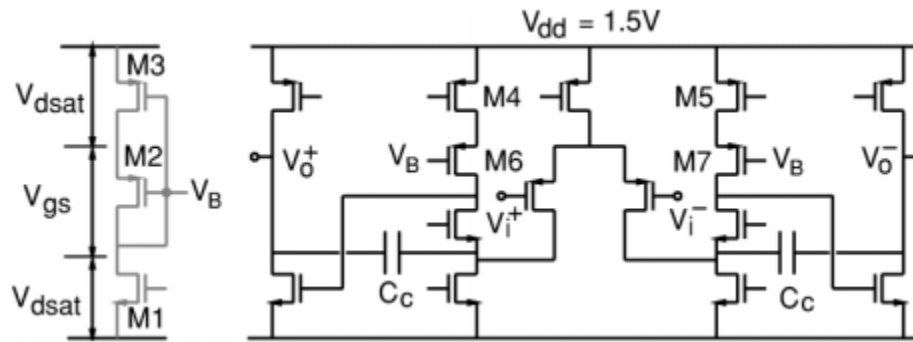
$$\frac{t}{\tau} = \frac{1}{2f_s} 2\pi \beta f_u > (N + 1)\ln(2) - \ln(V_{FS})$$

$$f_u > \frac{f_s}{\pi\beta} [(N + 1)\ln(2) - \ln(V_{FS})]$$

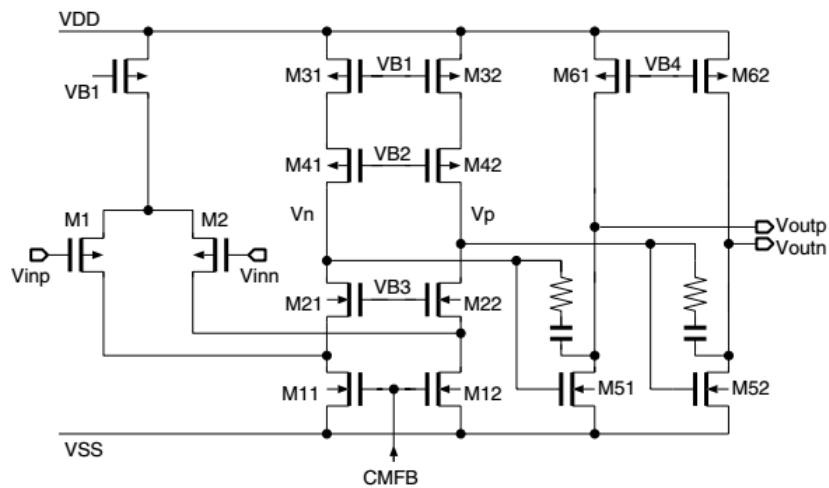
$$\ln(2) = 0.693$$

Resolution	Full Scale	Beta	Sampling Rate	UGB
N	V <sub>FS</sub> (Volt)	β	fs	fu
10	0.8	1	5.00E+07	1.25E+08
10	0.8	0.5	5.00E+07	2.50E+08
11	0.8	1	5.00E+07	1.36E+08
<b>11</b>	<b>0.8</b>	<b>0.5</b>	<b>5.00E+07</b>	<b>2.72E+08</b>
12	0.8	1	5.00E+07	1.47E+08
12	0.8	0.5	5.00E+07	2.94E+08
13	0.8	1	5.00E+07	1.58E+08
13	0.8	0.5	5.00E+07	3.16E+08
14	0.8	1	5.00E+07	1.69E+08
14	0.8	0.5	5.00E+07	3.38E+08

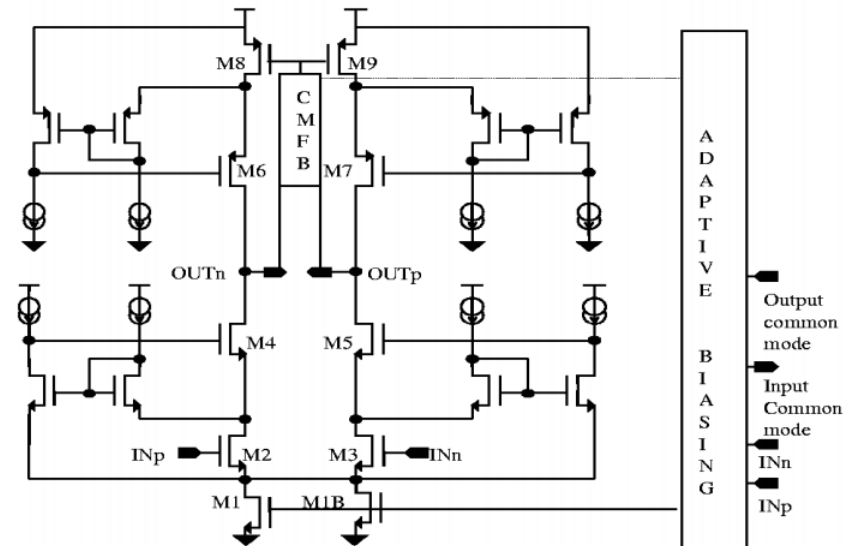
# Example OPAMP Circuits



[Ref. 1]



[Ref. 2]



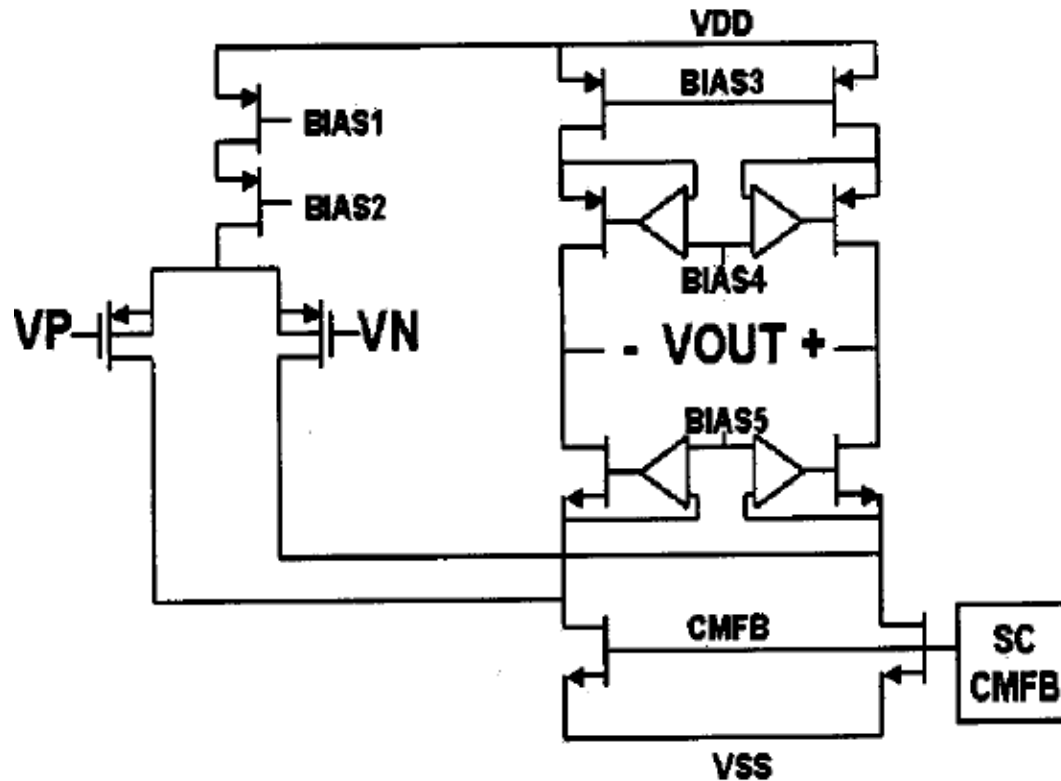
[Ref. 3]

# Example OPAMP in 14-bit Pipelined ADC

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001

A 3-V 340-mW 14-b 75-Msample/s CMOS ADC With 85-dB SFDR  
at Nyquist Input

Wenhua (Will) Yang, *Member, IEEE*, Dan Kelly, *Member, IEEE*, Iuri Mehr, *Member, IEEE*,  
Mark T. Sayuk, *Member, IEEE*, and Larry Singer, *Member, IEEE*



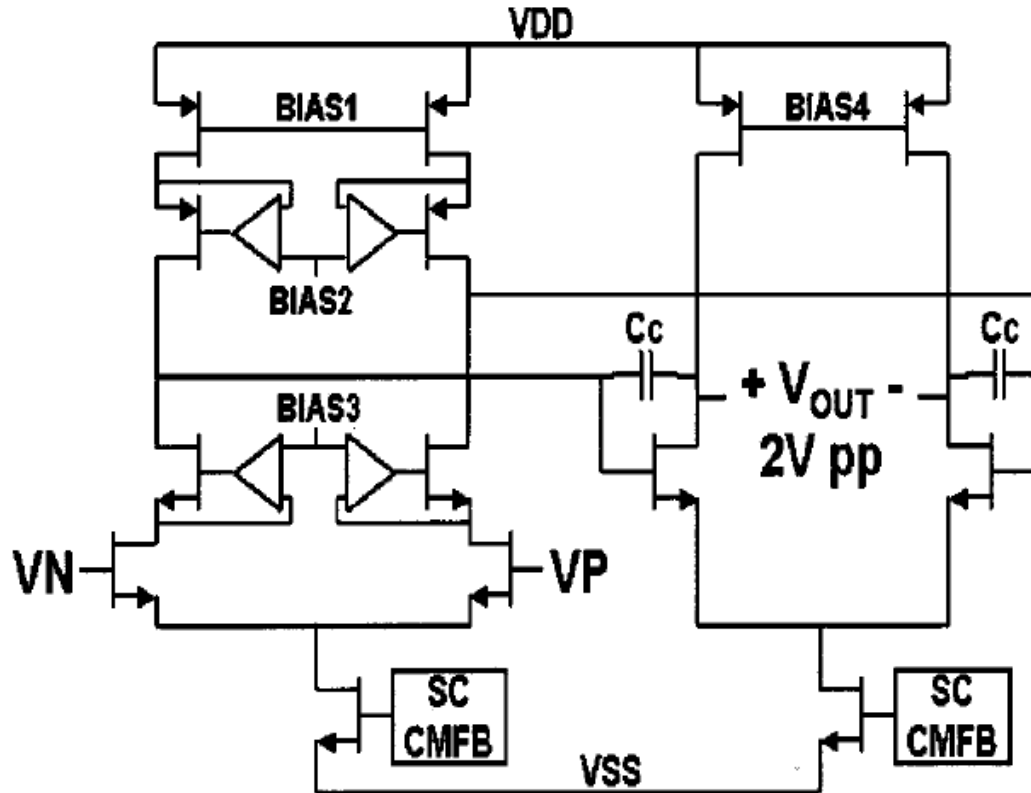
Amplifier in Flip-around THA

# Example OPAMP in 14-bit Pipelined ADC

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001

A 3-V 340-mW 14-b 75-Msample/s CMOS ADC With 85-dB SFDR  
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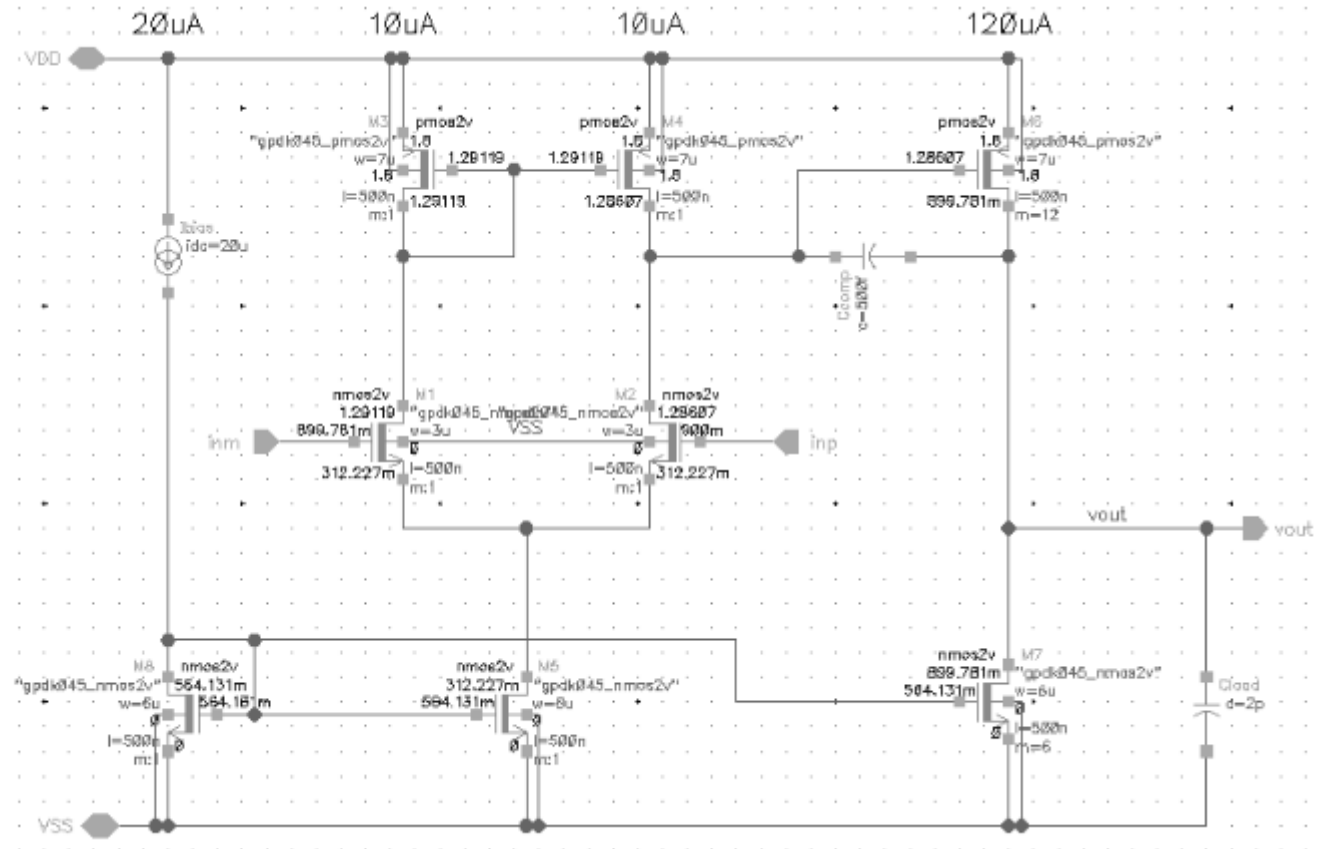


Amplifier in Stage 1

# 2-Stage OPAMP with NMOS Diff pair

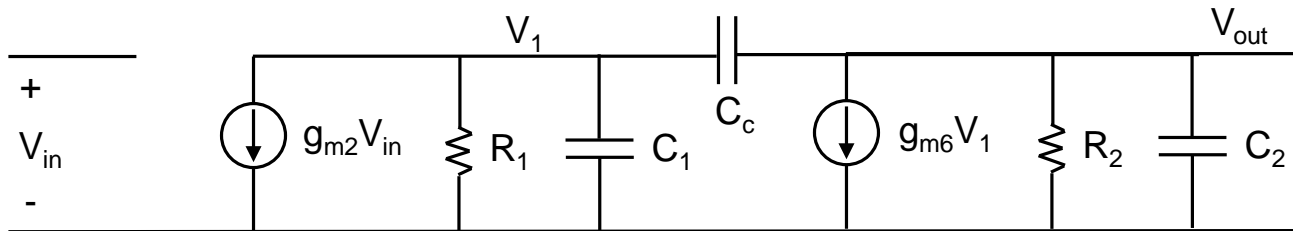
Technology:  
0.18um CMOS  
VDD=1.8V  
Lmin = 180nm  
Use  $L \geq 500\text{nm}$   
Ibias = 20uA

Spec:  
DC gain = 60dB  
GBW = 30MHz  
PM = 60°  
SR = 20V/us  
Clod = 2pF  
Power < 300uW





# Small-Signal Model of the OPAMP



By applying KCL, we can get the following approximate expression for 2 LHP poles and 1 RHP zero in the transfer function.

$$p1 = -1/(R_1 g_{m6} R_2 C_c)$$

$$p2 = -g_{m6}/(C_1 + C_2)$$

$$z = g_{m6}/C_c$$

$$Av = Av1 Av2 = -g_{m2} R_1 g_{m6} R_2$$

$$GBW = UGB = Av \times p1 = g_{m2}/C_c$$

For 60 deg PM,  $p2 > 2.2 \text{ GBW}$ , and for 45 deg PM,  $p2 > 1.2 \text{ GBW}$

$$\text{For } z = 10 \text{ GBW, } g_{m6} = 10 g_{m2} \quad C_c > 0.22 C_2$$

# Simulation Steps

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## 1. DC Simulation

- Construct the OPAMP schematic
- Run a DC simulation
- Check the operating point information by choosing Results→Print  
→DC Operating Points
- Make sure that all transistors are in Saturation (region=2)

## 2. AC Simulation

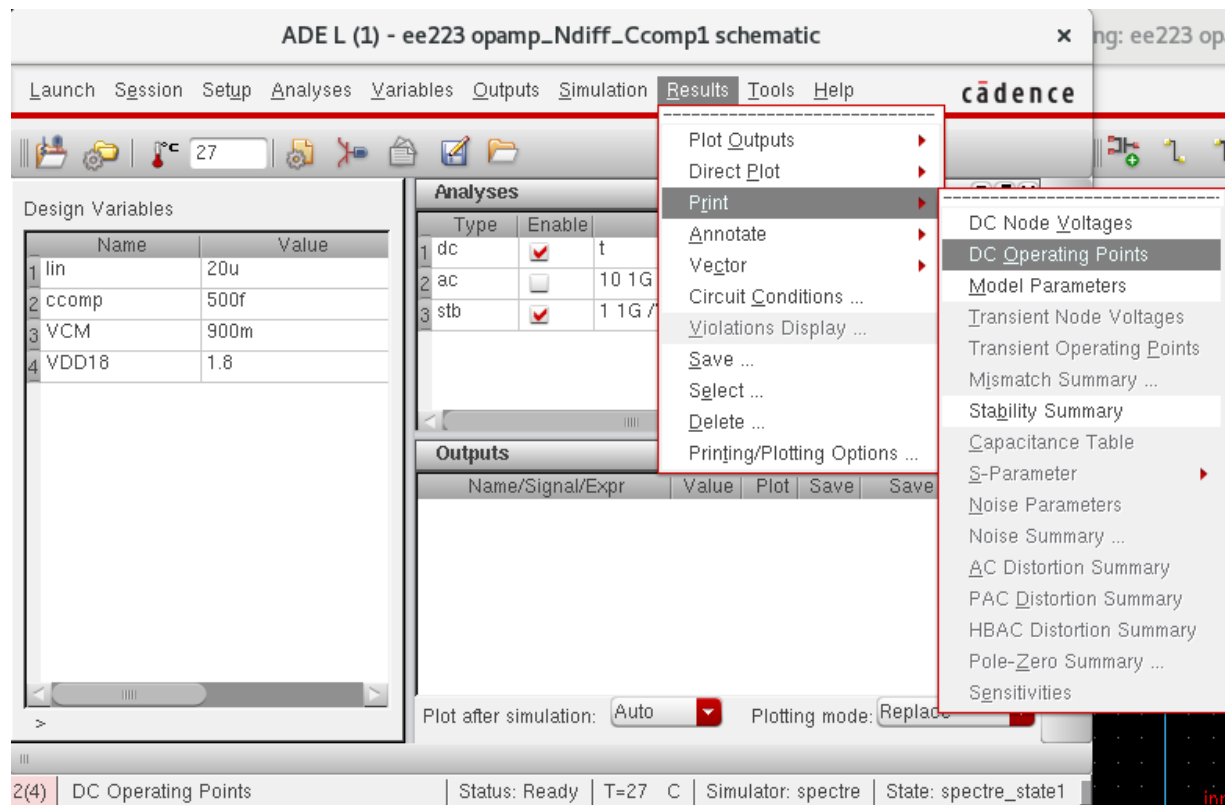
- Try RC Feedback approach to get the AC response
- Run stb analysis to check the stability

## 3. Transient Simulation

- Apply 10mV step pulse to check the small-signal transient response
- Apply 500mV step pulse to check the large-signal transient response

# DC Operating Points

To get the DC operating point information after you run the dc simulation, Choose Results→Print →DC Operating Points and then click on the transistor in the schematic.



# DC Gain Calculation from Operating Points

$$\text{DC Gain} = A_{v1} \times A_{v2}$$

$$A_{v1} = g_{m2} \times (r_{o2} // r_{o4}) = g_{m2} / (g_{ds2} + g_{ds4})$$

$$A_{v2} = g_{m6} \times (r_{o6} // r_{o7}) = g_{m6} / (g_{ds6} + g_{ds7})$$

From simulated DC operating point information of the circuit in slide 2,

$$g_{m2} = 125.9\mu \quad g_{ds2} = 1.84\mu \quad g_{ds4} = 3.53\mu$$

$$g_{m6} = 2.344\text{m} \quad g_{ds6} = 41.6\mu \quad g_{ds7} = 32.16\mu$$

$$A_{v1} = 125.8 / (1.84 + 3.53) = 23.4 = 27.4 \text{ dB}$$

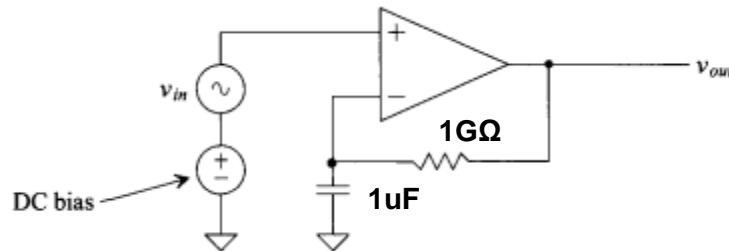
$$A_{v2} = 2344 / (41.6 + 32.16) = 31.8 = 30 \text{ dB}$$

$$A_v = 27.4 \text{ dB} + 30 \text{ dB} = \mathbf{57.4 \text{ dB} \leftarrow \text{Close to simulated gain}}$$

# OPAMP AC simulation Setup

## Two Simulation Approaches

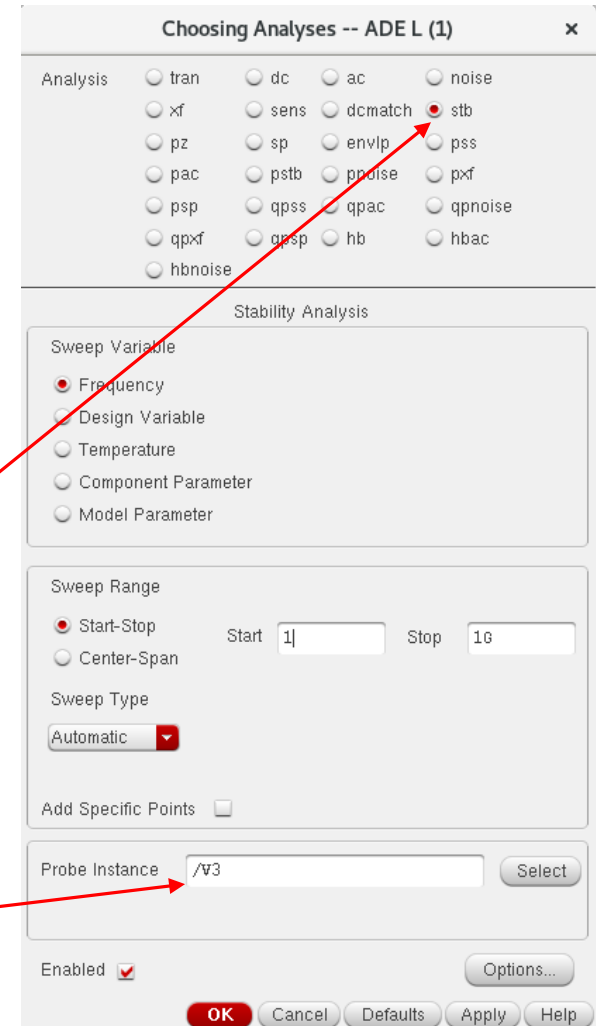
### 1. RC Feedback



### 2. Stability analysis

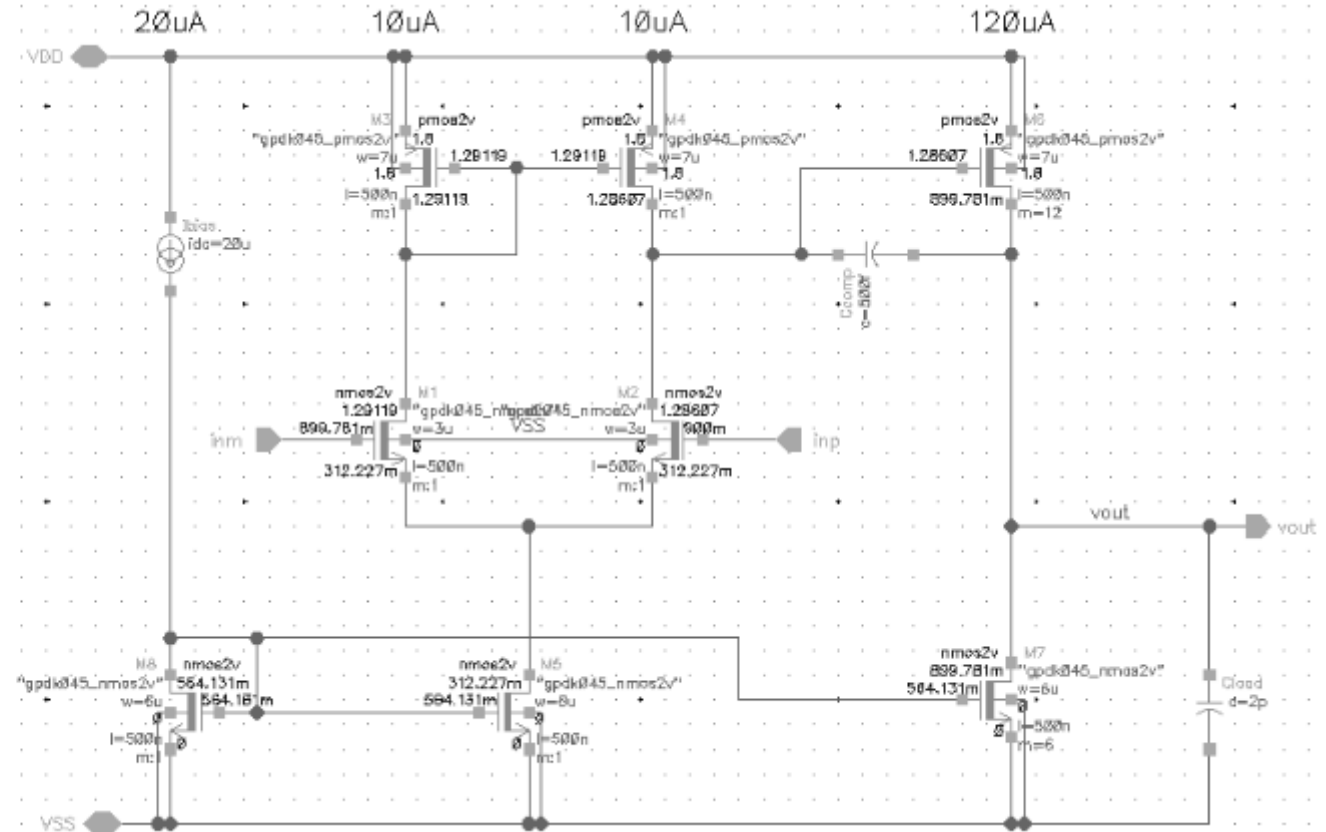
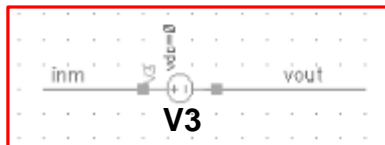
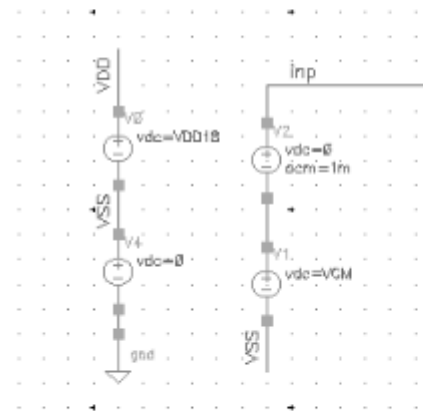
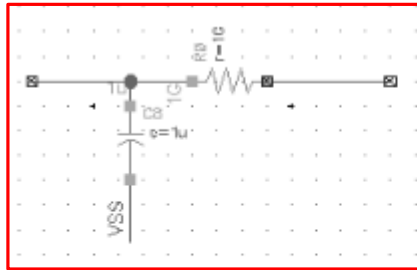
Choose “stb” in Cadence Analysis

DC voltage source for probing. See previous page.



# AC Simulation Test Bench

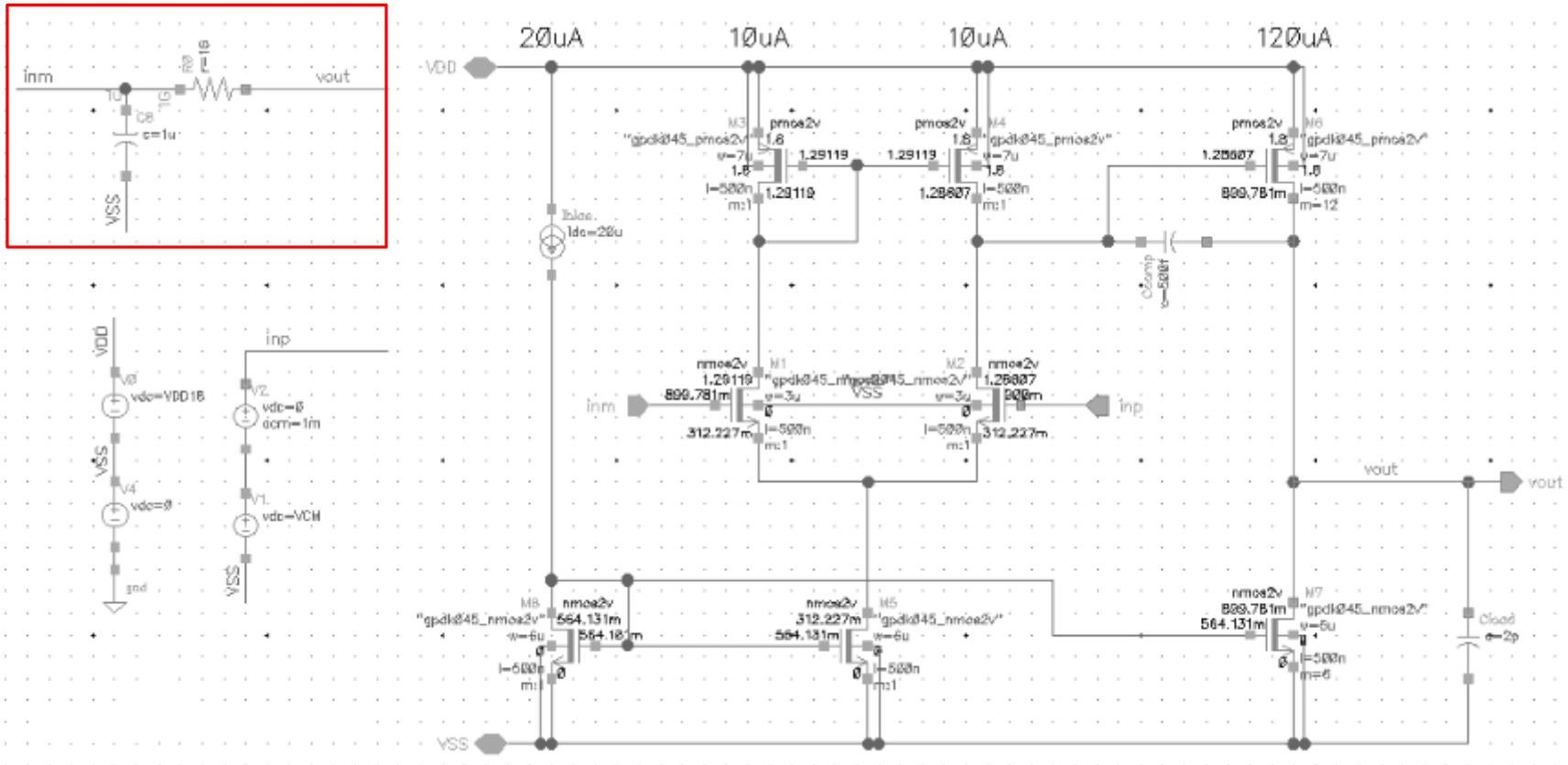
## RC-Feedback approach



For stb analysis

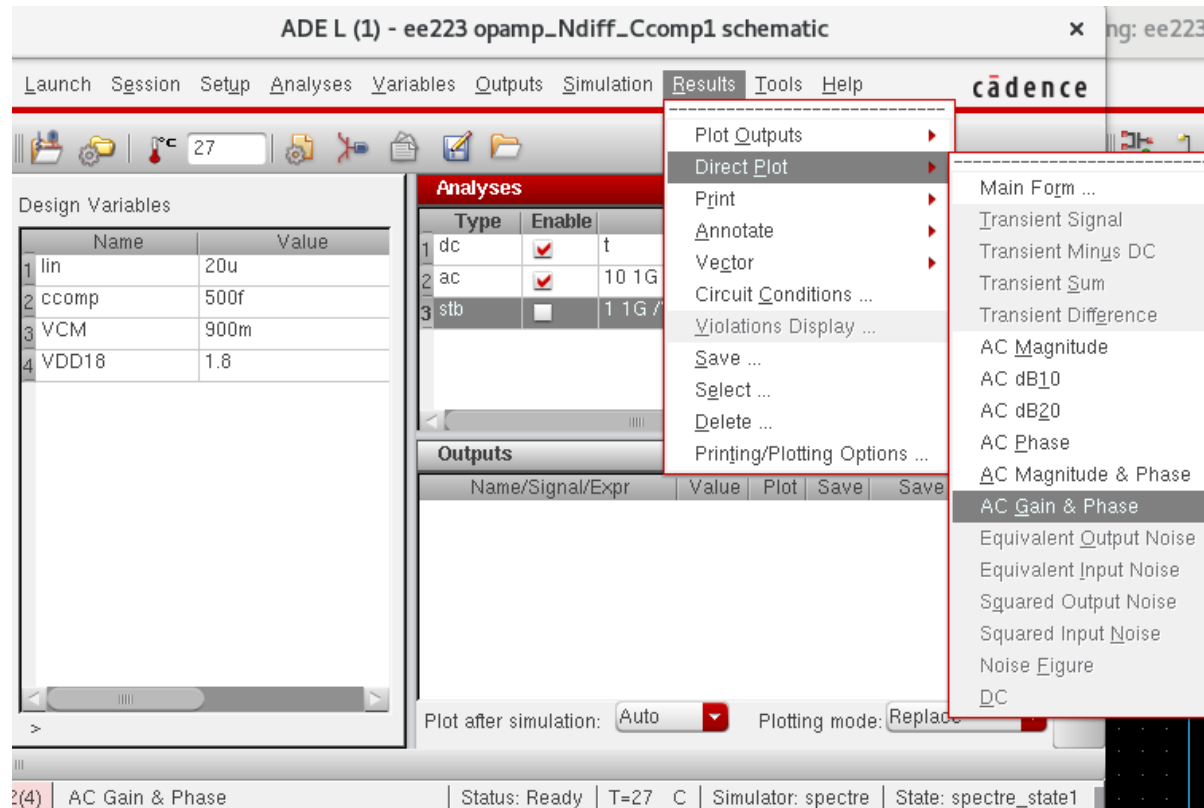
# AC Simulation Test Bench using RC-feedback

## RC-feedback approach



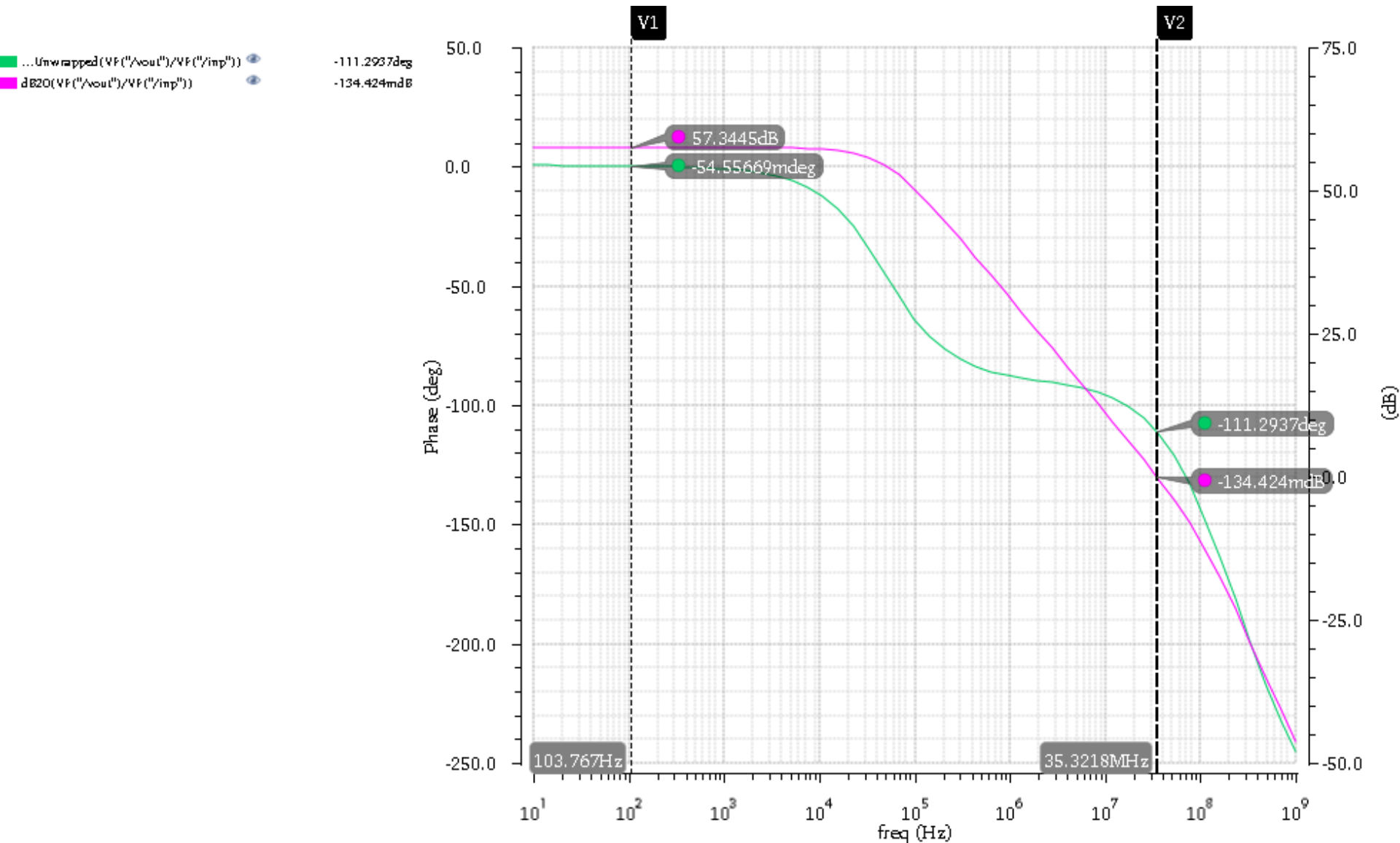
# Plotting the AC simulation Results

After running the AC simulation, choose Results→Direct Plot→AC Gain & Phase and then click on the output node (vout) and the input node (inp) to get the ac plot shown in next page.





# AC Simulation Result using RC Feedback



## For stb analysis



# AC simulation using stb analysis

After running the stb analysis, choose Results→Direct Plot→Main Form and then click on Plot to get the ac plot shown in slide 14

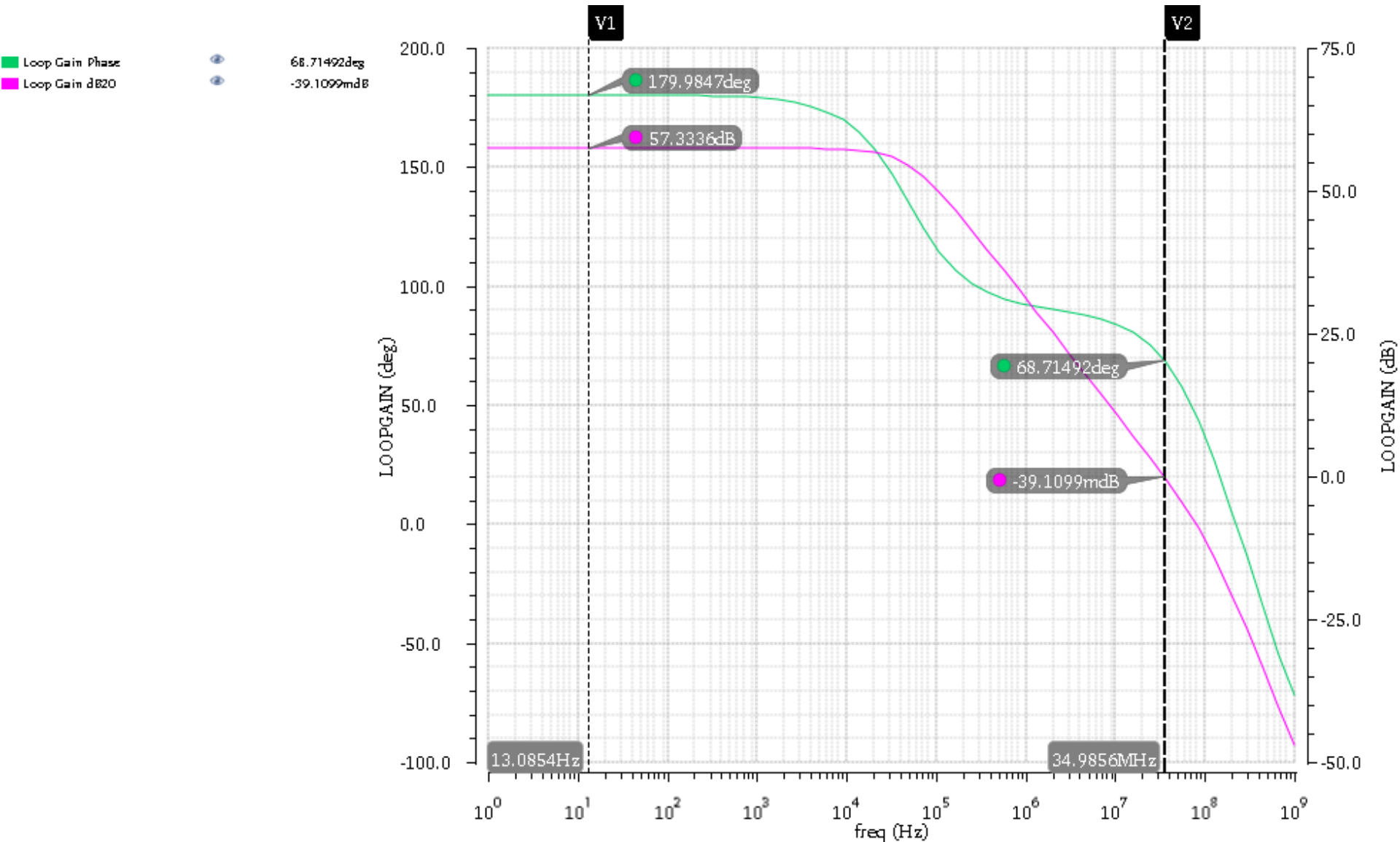
The screenshot shows the Cadence ADE L (1) - ee223 opamp\_Ndiff\_Ccomp1 schematic interface. The Results menu is open, showing the path: Results → Direct Plot → Main Form ... The Direct Plot Form dialog is also open, showing the following settings:

- Plotting Mode: Append
- Analysis: ☒ stb
- Function: ☒ Loop Gain, ☐ Stability Summary, ☐ Phase Margin, ☐ Gain Margin, ☐ PM Frequency, ☐ GM Frequency
- Modifier: ☐ Magnitude, ☐ Phase, ☒ Magnitude and Phase
- Magnitude Modifier: ☐ None, ☐ dB10, ☒ dB20
- Buttons: Add To Outputs, Plot, OK, Cancel, Help

The Design Variables table is also visible:

Name	Value
1 lin	20u
2 ccomp	500f
3 VCM	900m
4 VDD18	1.8

# AC Simulation Result using stb analysis



# Stability Summary from stb analysis

After running the stb analysis, choose Results→Direct Plot→Main Form and then click on Stability Summary

The screenshot shows the Cadence ADE L (1) - ee223 opamp\_Ndiff\_Ccomp1 schematic interface. The **Results** menu is open, showing the path **Direct Plot** → **Main Form ...**. The **Direct Plot Form** dialog is also shown, with the **Plotting Mode** set to **Append** and the **Analysis** set to **stb**. The **Function** section shows **Stability Summary** selected. The **Phase Margin** is 68.9146 (Deg) @ freq = 34.6175M (Hz) and the **Gain Margin** is 22.3828 (dB) @ freq = 220.21M (Hz).

**Design Variables**

Name	Value
1 lin	20u
2 ccomp	500f
3 VCM	900m
4 VDD18	1.8

**Analyses**

Type	Enable	t
1 dc	<input checked="" type="checkbox"/>	t
2 ac	<input type="checkbox"/>	10 1G
3 stb	<input checked="" type="checkbox"/>	1 1G /

**Outputs**

Name/Signal/Expr	Value	Plot	Save	Save
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**Direct Plot Form**

Plotting Mode: Append

**Analysis**

☒ stb

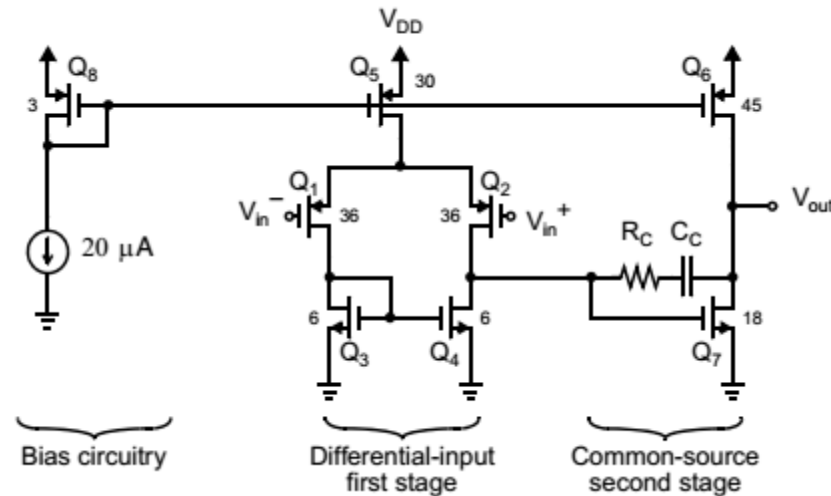
**Function**

☐ Loop Gain ☒ Stability Summary  
☐ Phase Margin ☐ Gain Margin  
☐ PM Frequency ☐ GM Frequency

Phase Margin = 68.9146 (Deg) @ freq = 34.6175M (Hz)  
Gain Margin = 22.3828 (dB) @ freq = 220.21M (Hz)

OK Cancel Help

# Two-Stage OPAMP with RC Compensation



$$A(s) = \frac{A_0(1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}$$

$$\omega_z = \frac{-1}{C_c(\frac{1}{g_{m7}} - R_c)}$$

# Choice of $R_c$

$$A(s) = \frac{A_0(1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}$$

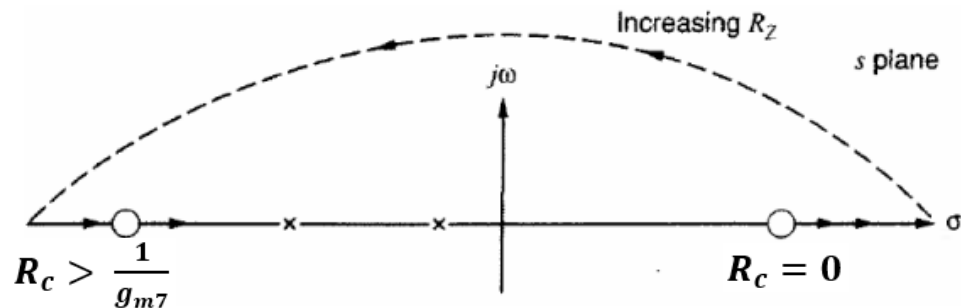
$$\omega_z = \frac{-1}{C_c(\frac{1}{g_{m7}} - R_c)}$$

- $R_c = 0 \rightarrow \omega_z = \frac{-1}{C_c(\frac{1}{g_{m7}})} = \frac{-g_{m7}}{C_c} \rightarrow \text{RHP Zero ! Stability Issue}$

- $R_c = \frac{1}{g_{m7}} \rightarrow \omega_z = \infty$

- $R_c > \frac{1}{g_{m7}}$

$$\rightarrow \omega_z = \omega_{p2}$$



$$\frac{-1}{C_c(\frac{1}{g_{m7}} - R_c)} = \frac{g_{m7}}{C_1 + C_2}$$

$$\rightarrow R_c = \frac{1}{g_{m7}} \left( 1 + \frac{C_1 + C_2}{C_c} \right)$$

- $R_c \gg \frac{1}{g_{m7}}$

$$\omega_z \approx \frac{1}{R_c C_c} = \alpha \omega_u = \alpha \frac{g_{m1}}{C_c}$$

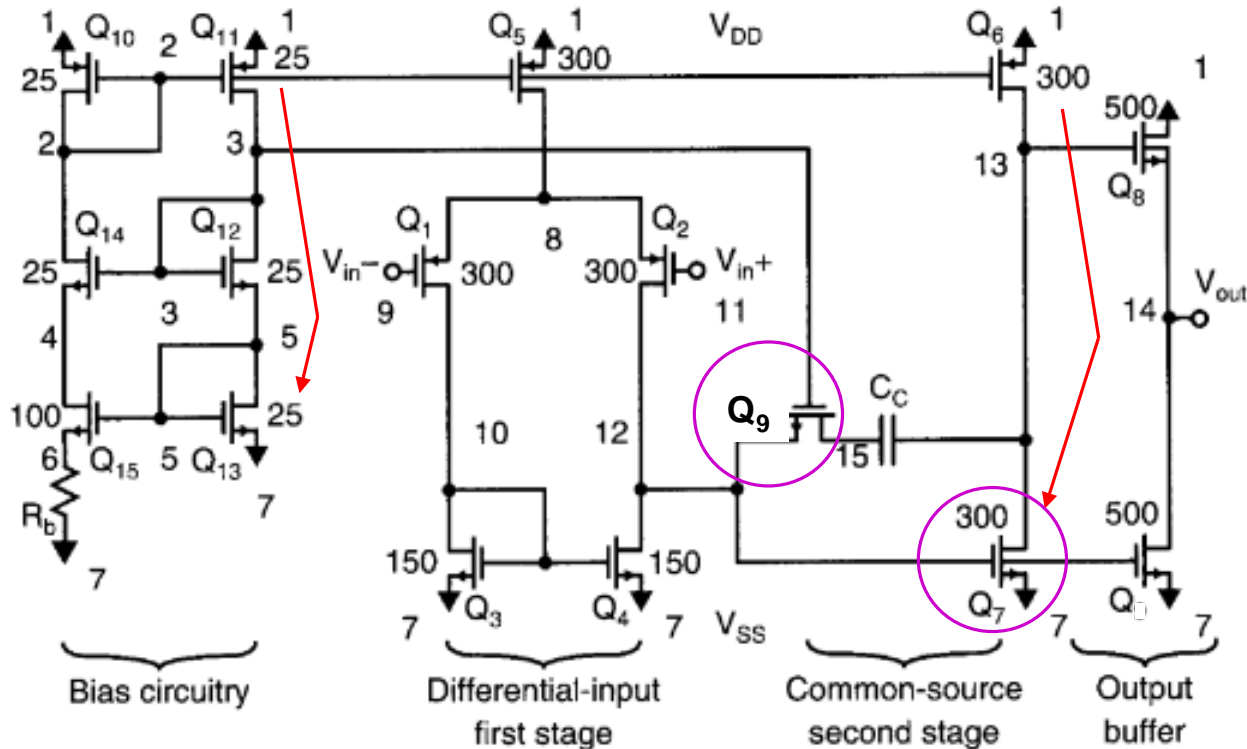
$$\rightarrow$$

$$R_c = \frac{1}{\alpha g_{m1}}$$

$\alpha = 1.7$  from Caruson, Johns, Martin

Equation 1

# Two-stage RC compensation

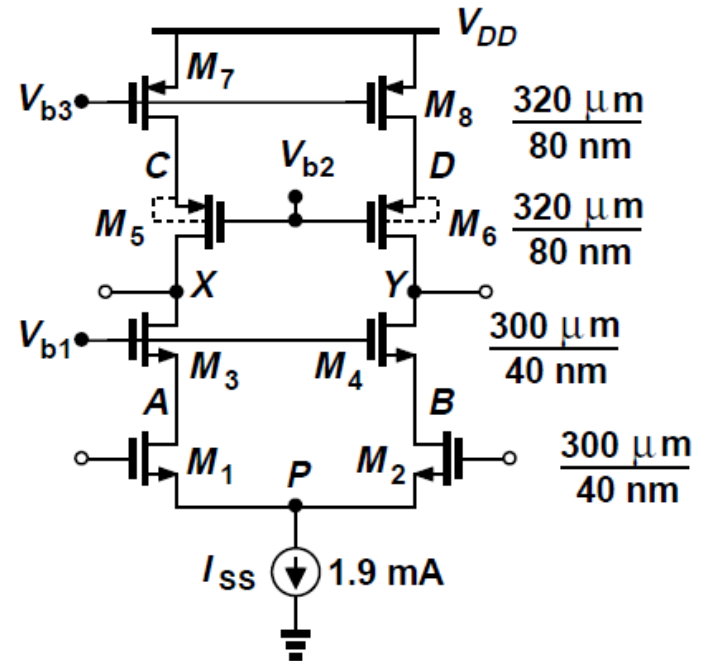
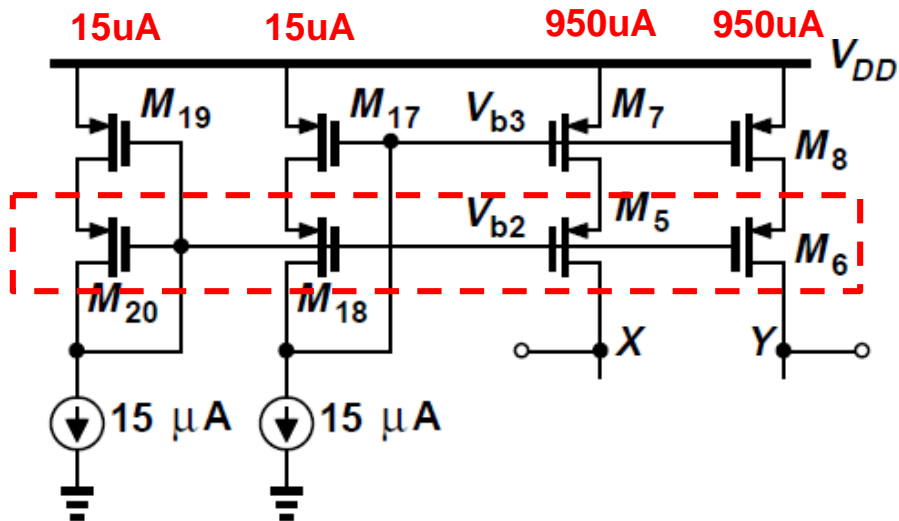


1.  $\frac{(W/L)_6}{(W/L)_7} = \frac{(W/L)_{11}}{(W/L)_{13}}$
2.  $\frac{(W/L)_{12}}{(W/L)_{13}} = \frac{(W/L)_{13}}{(W/L)_{13}}$
3.  $\frac{(W/L)_9}{(W/L)_7} = 0.2 \frac{(W/L)_7}{(W/L)_7}$

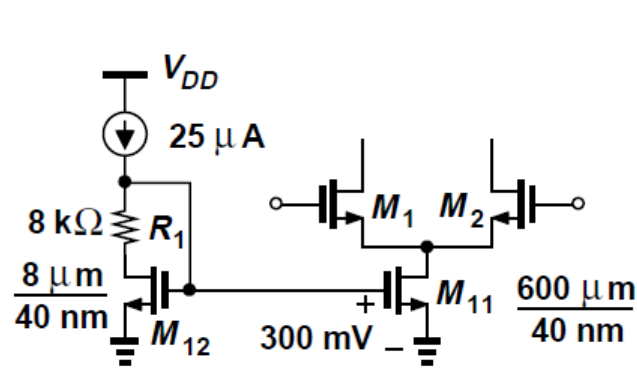


# Bias Circuit

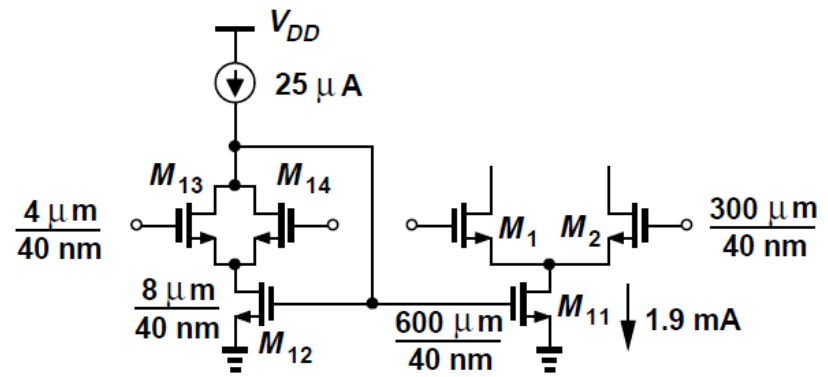
Key for cascode biasing : Maintain current density



# Bias for Tail Current Source

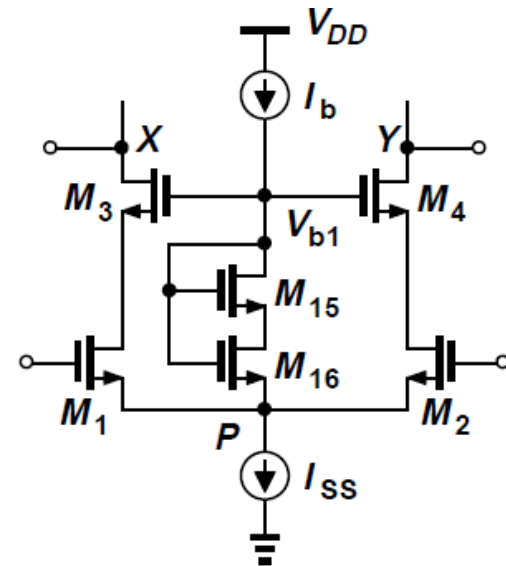
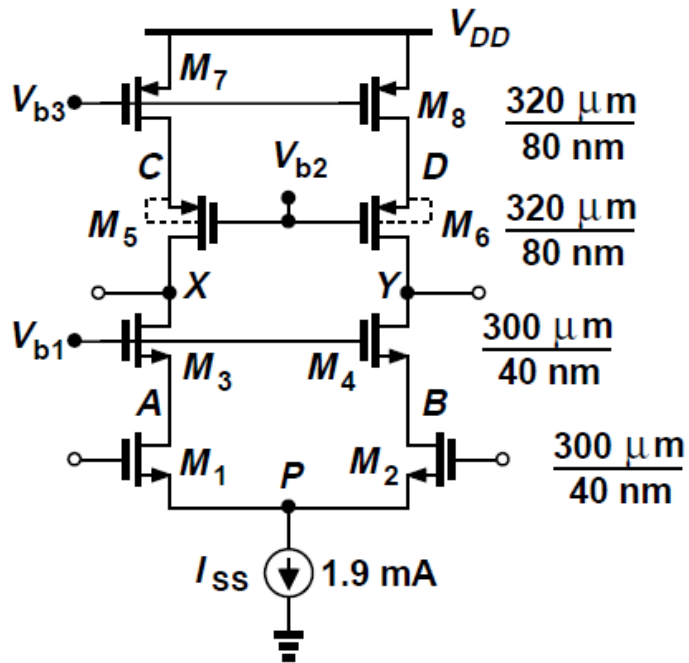


(a)

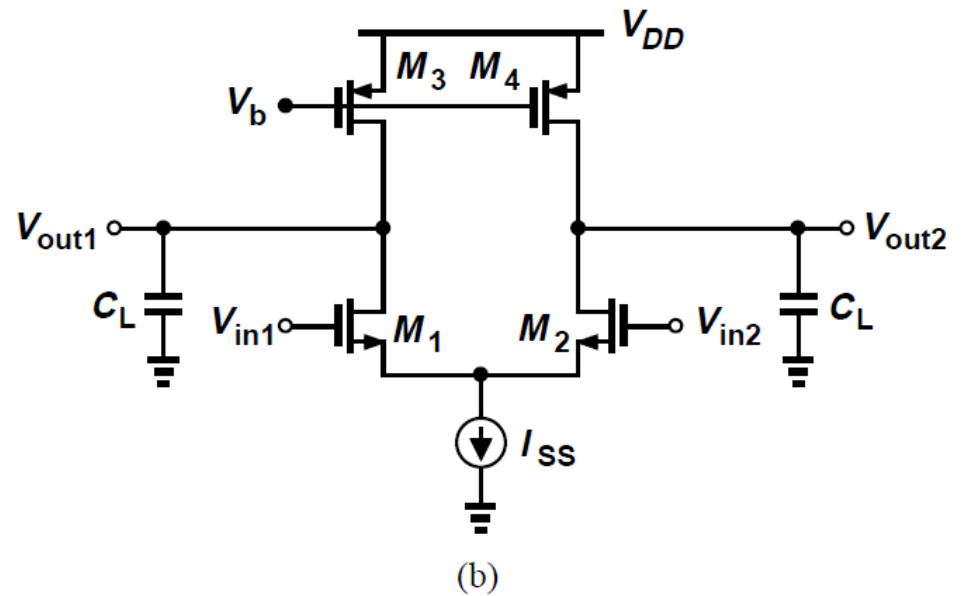
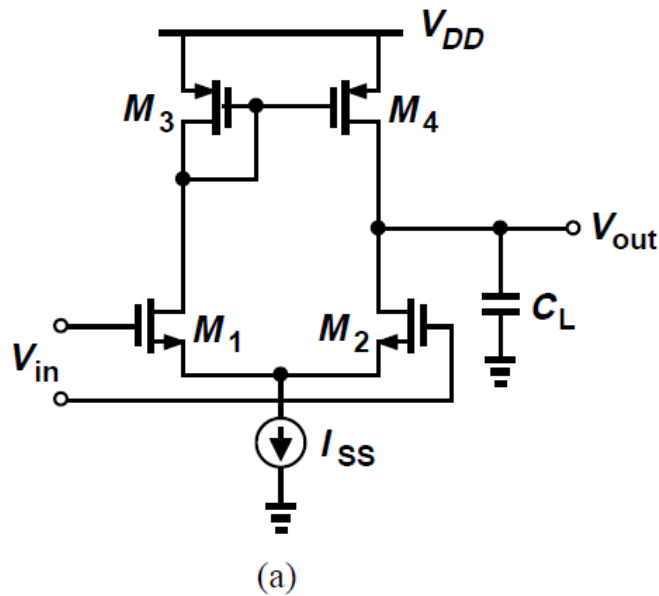


(b)

# Bias for Vb1



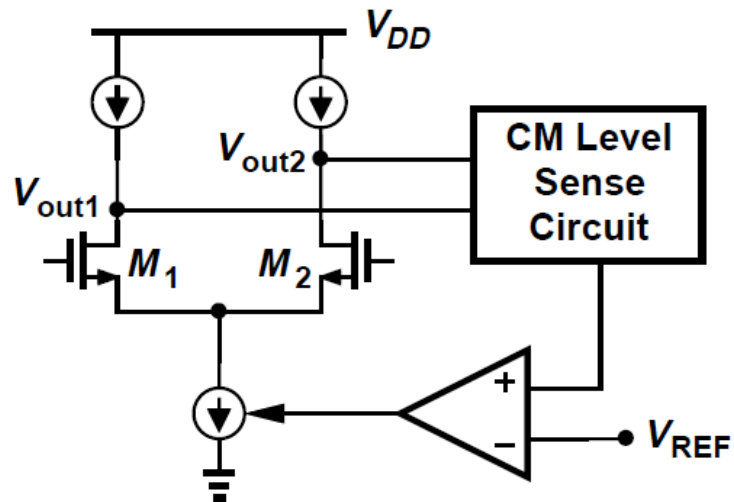
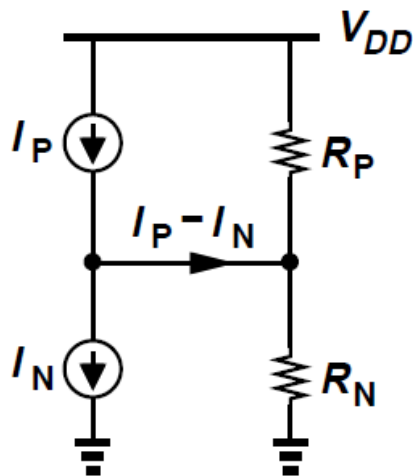
# Single-Ended vs. Fully-Differential OPAMP



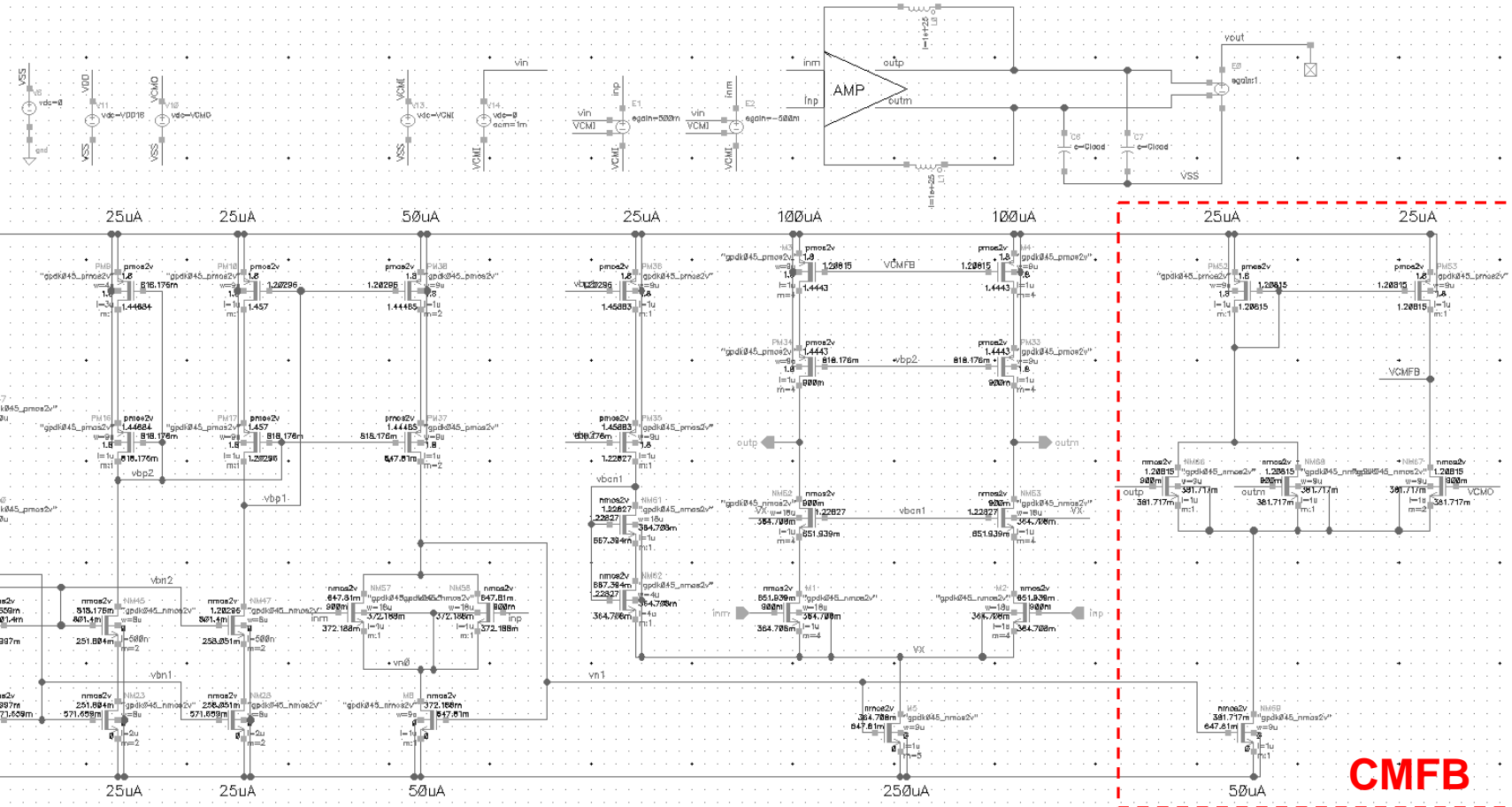
# CMFB for Fully-Differential OPAMP

Random mismatches between the top and bottom current sources cause the CM level to fall or rise considerably

→ We need CMFB to set the voltage to the desired DC level

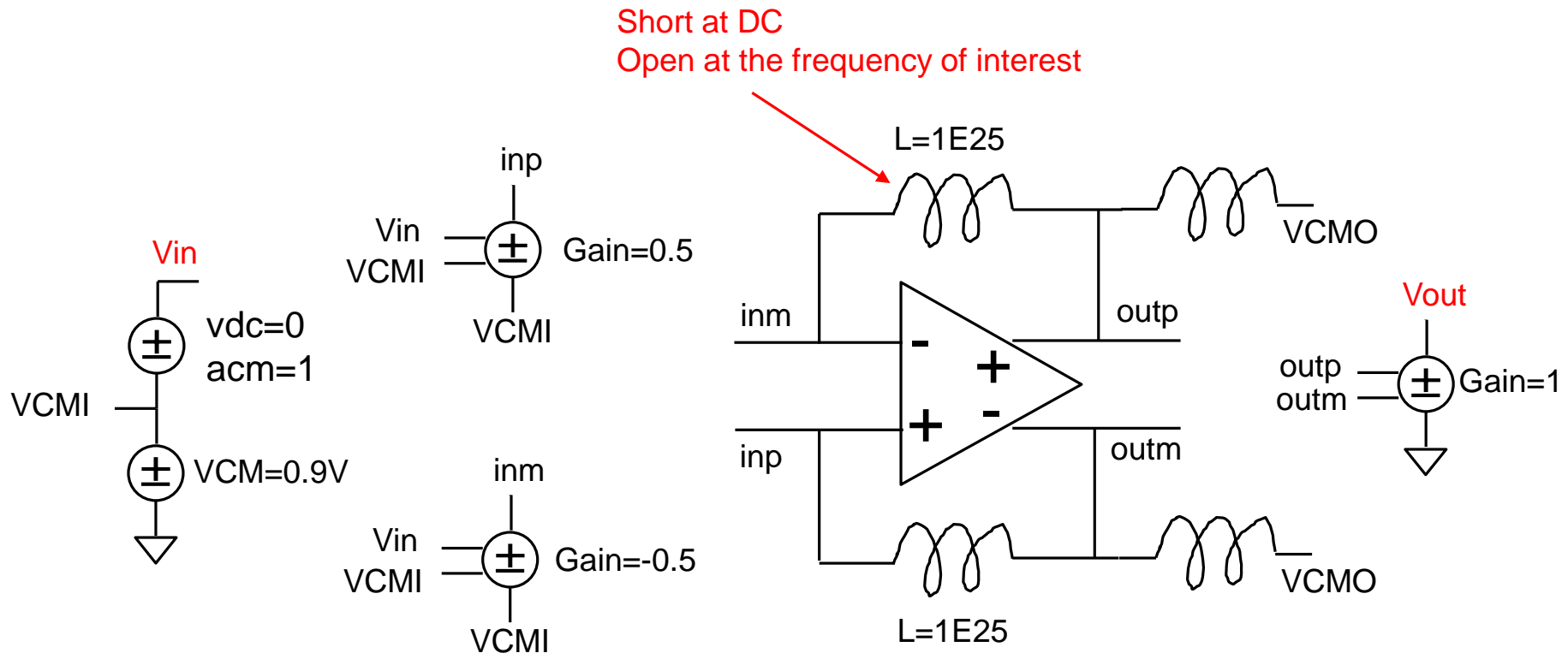


# Fully Differential Telescopic OTA with CMFB Example 1



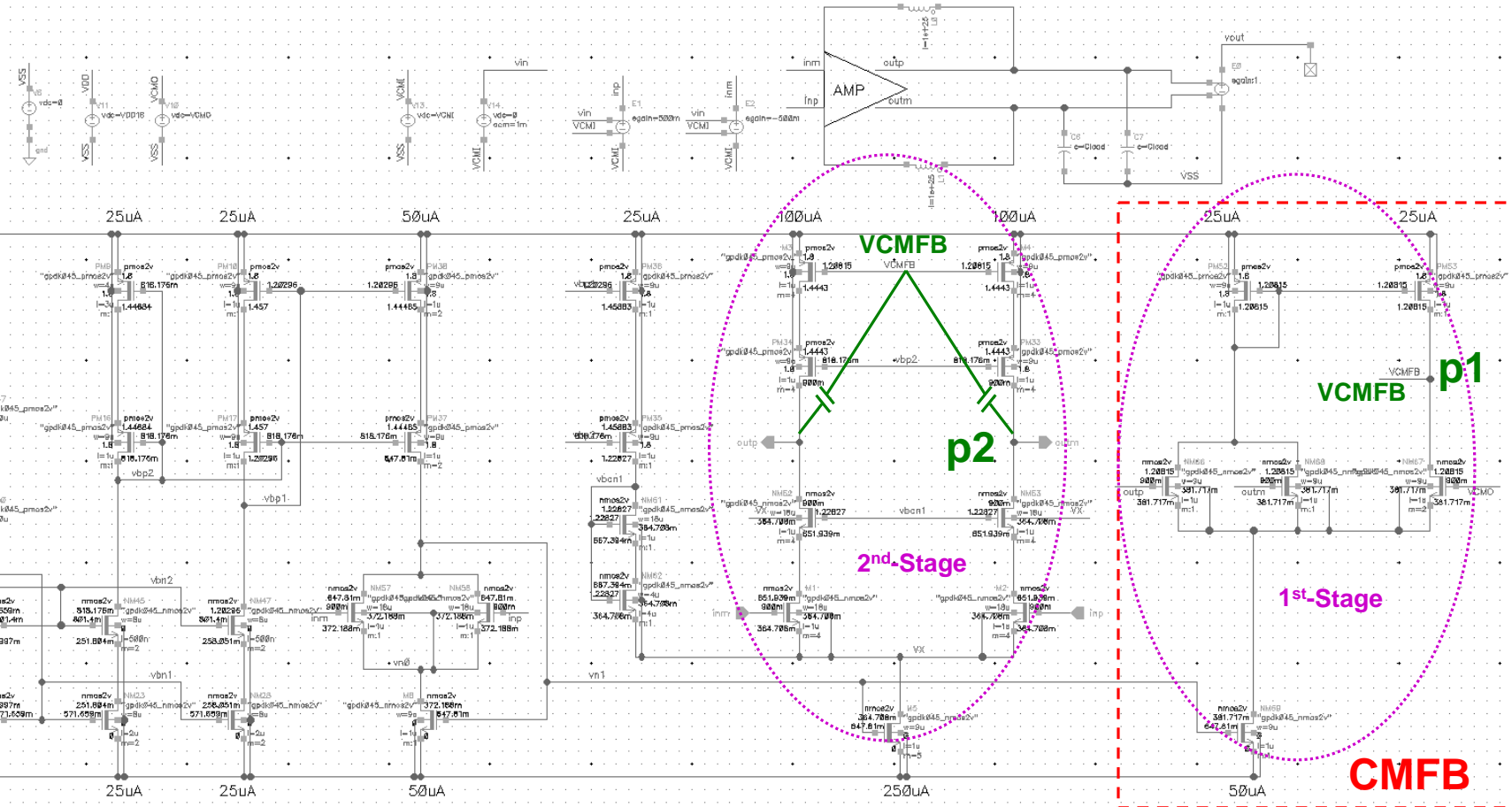
# Test Bench for Fully Differential OPAMP

Test bench to simulate the open loop response of the fully-differential opamp  
→ Use Inductor with large value



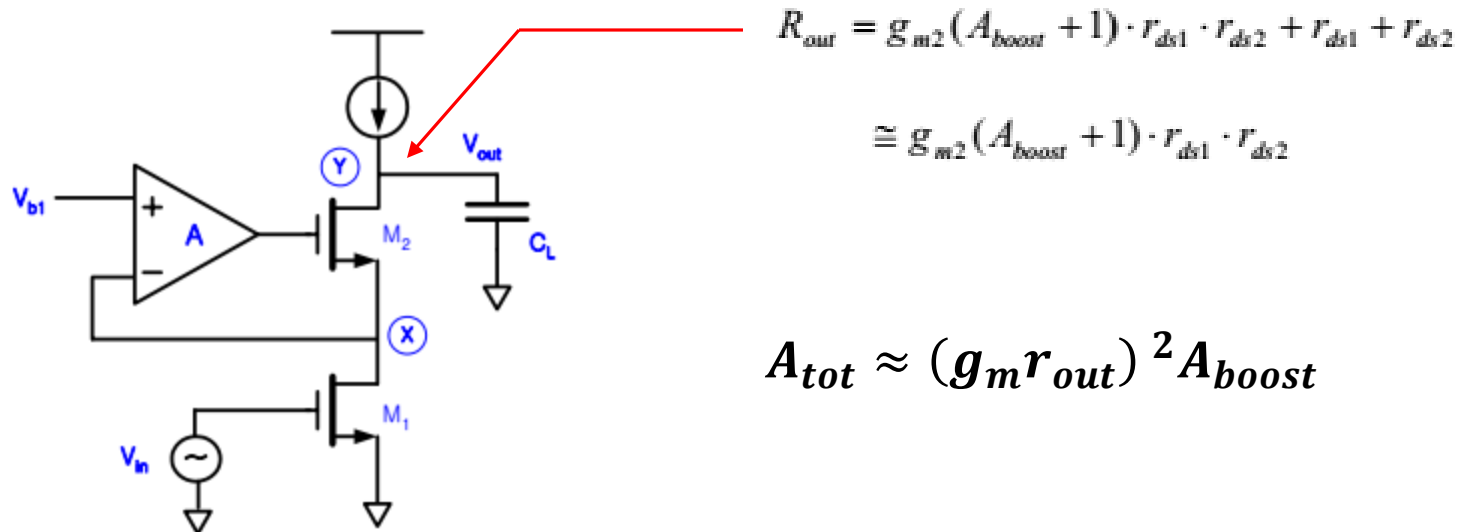
You may not need the inductor in the test bench  
if you have a continuous-time CMFB.

# Common-Mode Loop → Two-Stage



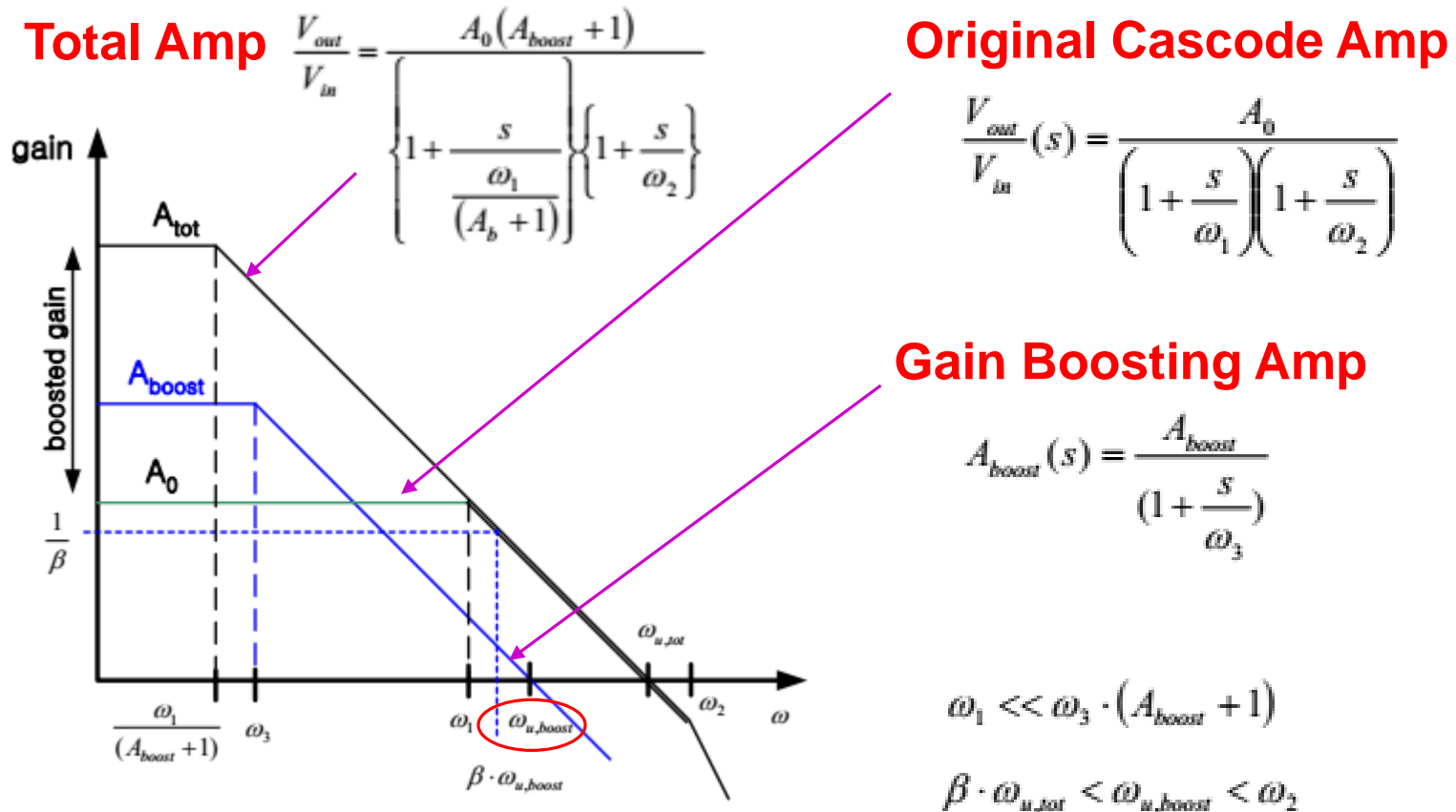


# Gain-Boosting Cascode Amplifier



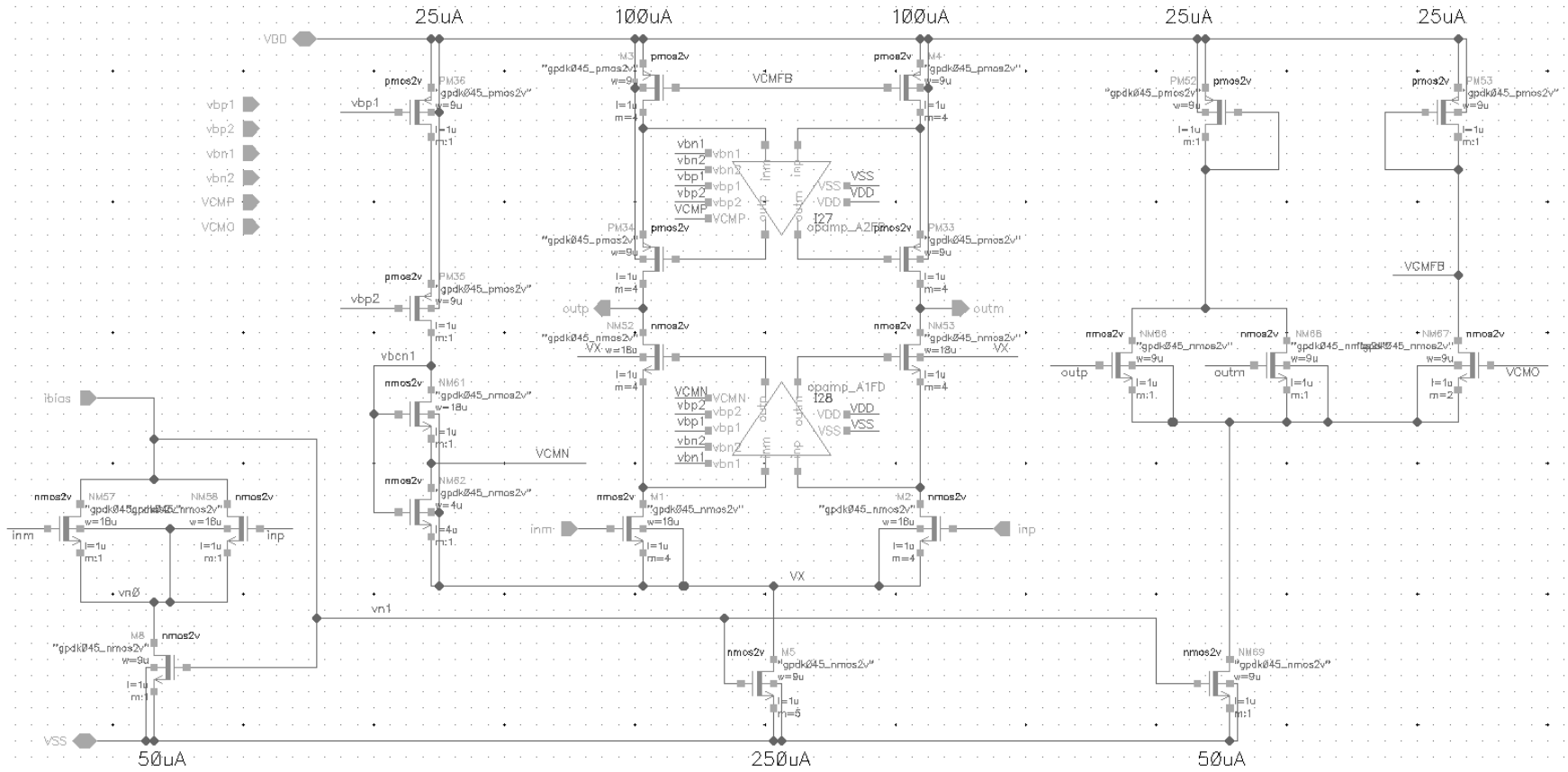
Chang-Hyuk Cho, PhD Thesis, Georgia Institute of Technology, 2005  
 “A Power Optimized Pipelined ADC Design in Deep Submicron CMOS Technology”

# Gain-Boosting Cascode Amplifier

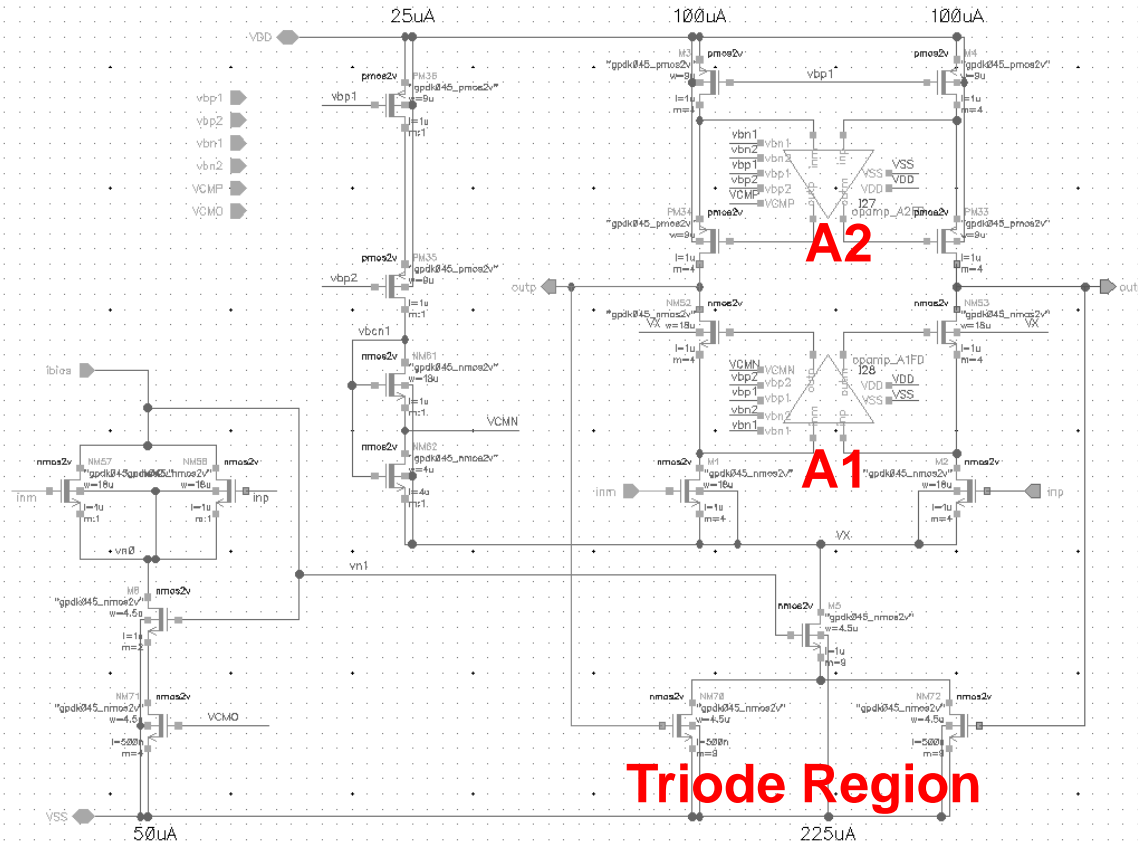


**Unity Gain frequency of the gain boosting amp should be  
Larger than -3dB frequency of the original amp and  
Lower than first non-dominant pole of the original amp**

# CMFB Example 2

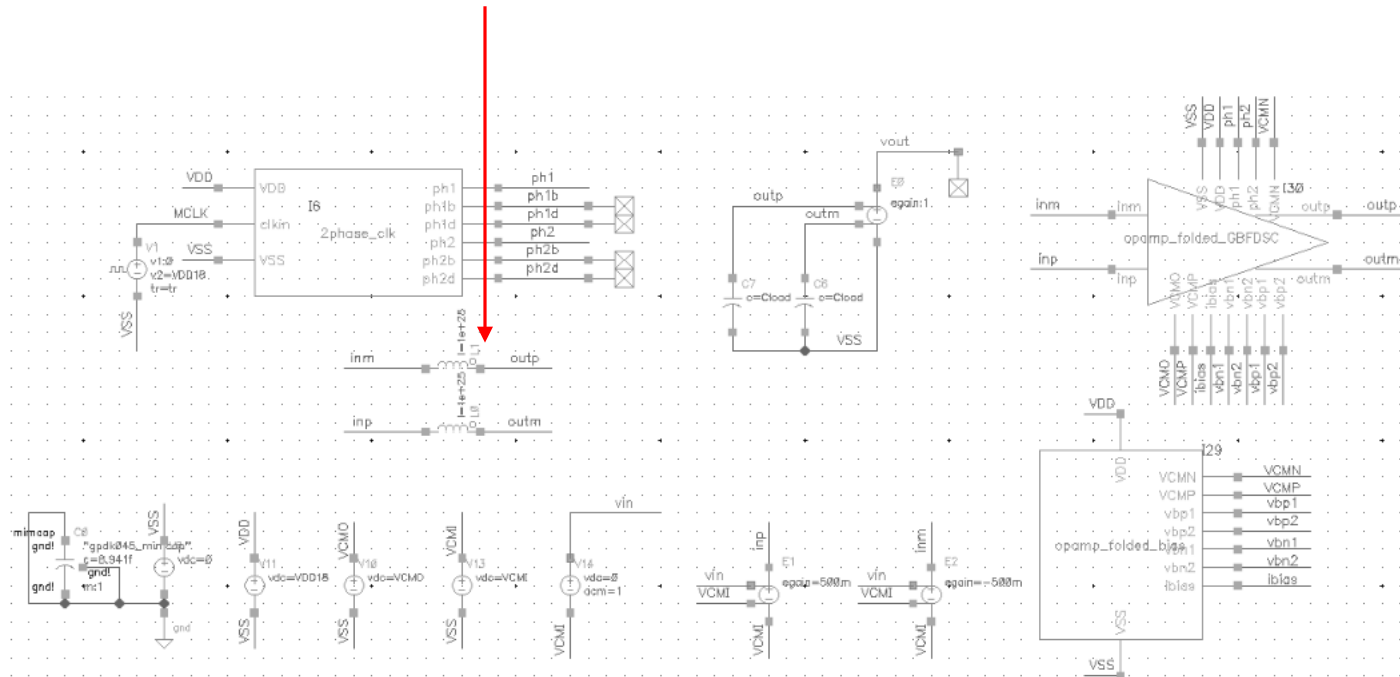


# CMFB Example 3



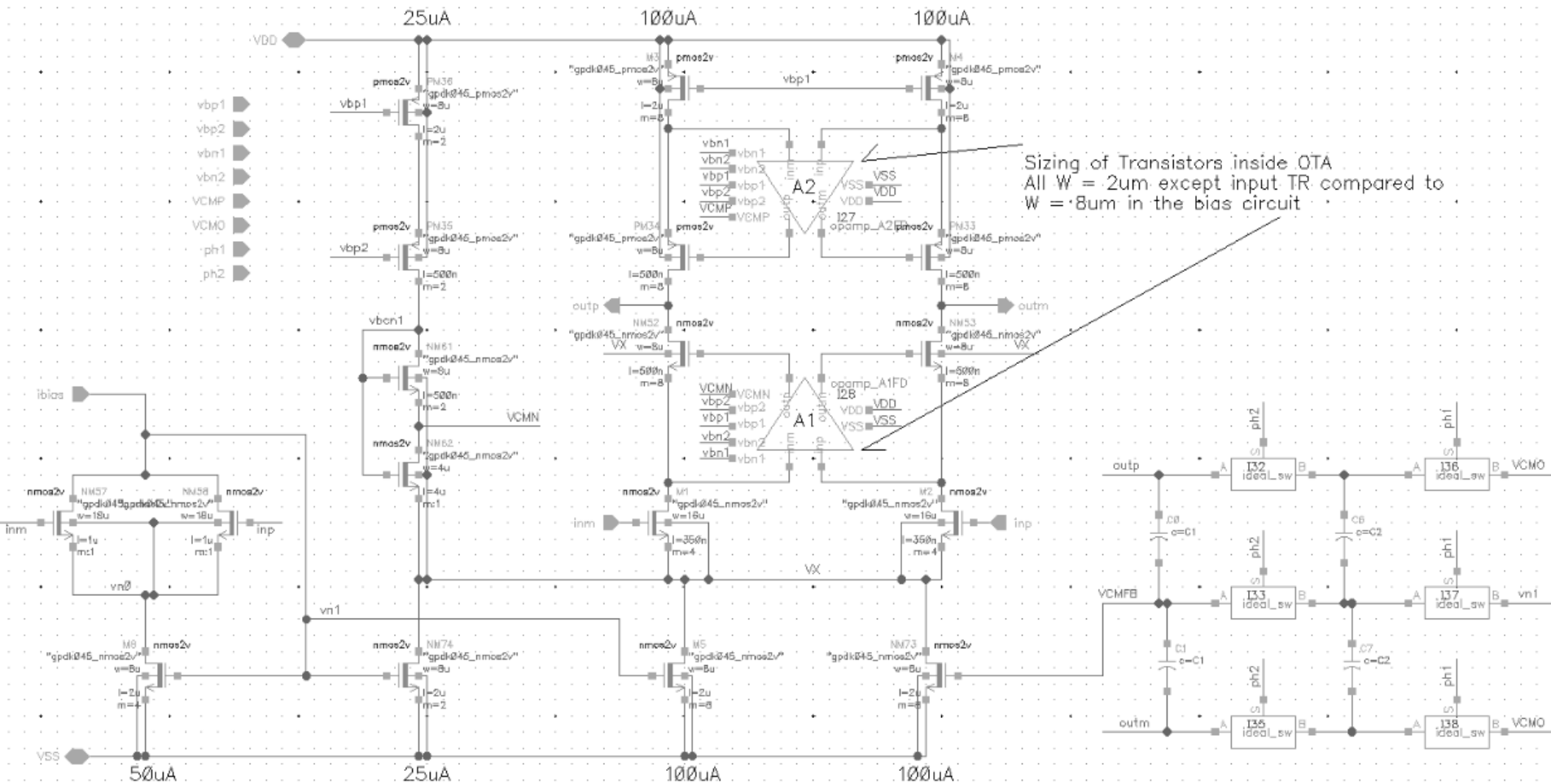
# Test Bench for Fully-Differential AMP ac simulation

Inductors to set the DC bias point in unity gain feedback.





# Gain-Boosted Telescopic OPAMP with SC CMFB



# Gain-Boosted Folded-Cascode AMP with SC CMFB

