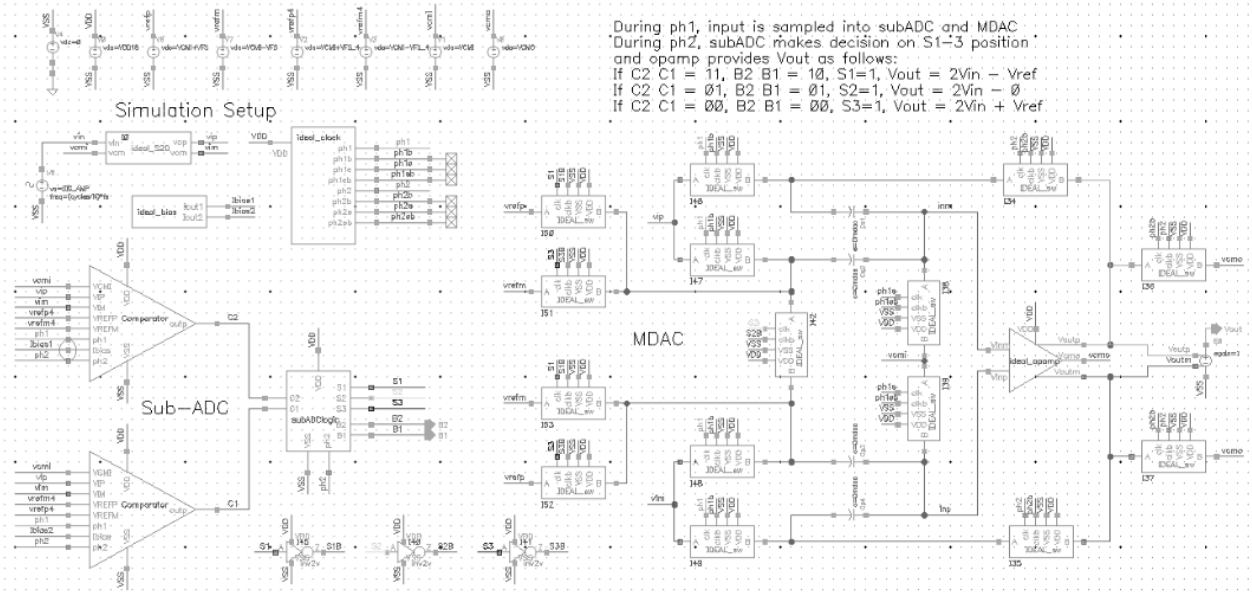
EE288 Homework #6 (**5 points**) Apr 23, 2018

Due: May 7, 2018 6:00PM. Homework will not be received after due.
Homework submission file should be in pdf format and file name should be EE288HW6_yourname.

In this homework, you will build a fully differential 1.5-bit pipeline stage. There are two goals for this homework problem. First goal is to create a functional 1.5-bit stage design using ideal references, ideal clocks and an ideal MDAC. You can use the comparators in HW4, but you have to create subADC logic. Use the simulation setup in the schematic cell "EE288HW6" in ee288lib as your baseline design.



Second goal is to choose proper switches in MDAC implementation. The baseline schematic includes ideal switches ("IDEAL_sw" cell) for MDAC operation. Your goal is to achieve the best possible 2x gain linearity after replacing the ideal switches with CMOS switches and boosted switches you designed in HW3. To make it easy for replacing switches in MDAC, CMOS_sw and Boost_sw symbols have been included in ee288lib. You will have to build the corresponding schematics for CMOS_sw and Boost_sw.

For the comparator circuits in sub-ADC, the timing of the clocked comparator should be carefully chosen so that you can sample the input signal to both the comparators and the MDAC during ph1 and make the gain of 2 amplification during ph2 as described in the schematic.

Assume the following design constraint and the parameter values for you design.
VDD = 1.8V
vrefp = 1.4V and vrefm = 0.4V
Input signal range 0.4V ~ 1.4V
VCMI = VCMO = 0.9V
VFS = VSIG_AMP = 0.5V
VFS_4 = 125mV for normal operation mode, VFS_4 = 600mV for MDAC in 2X gain mode
Sampling clock pulse, fs = 100 MHz
Input signal frequency at fin = (cycles/N) * fs where cycles = 7 and N = 64 for 64-point FFT

All capacitor values used in comparators, MDAC, and loading cap should be 100fF. Refer to various parameter values for the ideal opamp as shown in below ADE-L Design Variables.

Design Variables

	Name	Value
1	Cout	100f
2	VFS_4	600m
3	VFS	500m
4	SIG_AMP	500m
5	delay	0
6	freq_mclk	100M
7	cycles	7
8	fs	100M
9	N	64
10	IBIAS	500m
11	VCMI	900m
12	VCMO	900m
13	Ccomparator	100f
14	Cload	100f
15	Cmdac	100f
16	t_edge	10p
17	non_ov	100p
18	t_early	100p
19	BW	1G
20	Cin	10f
21	Rout	1K
22	Vos	0
23	Adm2	1K
24	Acm	0
25	Adm1	1K
26	VDD	1.8
27	Ron	10
28	tr	10p
29	VDD18	1.8

Analyses

	Type	Enable	Arguments
1	tran	☑	0 699n conservative
2	dc	☑	t

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	inp		☐	☐	allv
2	inm		☐	☐	allv
3	V0/MINUS		☐	☑	yes
4	ph1		☑	☐	allv
5	ph2		☑	☐	allv
6	vip		☑	☐	allv
7	vim		☑	☐	allv
8	Voutp		☑	☐	allv
9	Voutm		☑	☐	allv
10	C2		☐	☐	allv
11	C1		☐	☐	allv
12	B2		☐	☐	allv
13	B1		☐	☐	allv
14	S1		☑	☐	allv
15	S2		☑	☐	allv
16	S3		☑	☐	allv
17	vrefm		☐	☐	allv
18	vrefp		☐	☐	allv
19	vrefm4		☐	☐	allv
20	vrefp4		☐	☐	allv
21	Vout		☑	☐	allv
22	I1/Ibias		☑	☑	yes

To test the functionality of the MDAC and the stage operation,

1. Set VFS_4 = 125mV initially for normal mode of MDAC operation. Measure the amplitude of transient input signal just before ph1 goes low and then measure the MDAC output signal during ph2 when the signal is settled. Prove that result agrees with the value if the circuit operates correctly.
2. Set VFS_4 = 600mV so that the MDAC works as 2x gain mode all the time. Then, set SIG_AMP=500mV and run a transient simulation for 699ns in Cadence Spectre and plot the transient waveforms for input and MDAC output signals along with clocks and other relevant signals in white background. Then plot a frequency spectrum of the MDAC output using Cadence Spectrum measurement. The sample duration should be 59ns to 669ns for 64-point FFT.
3. Repeat the 2x gain mode simulations with SIG_AMP=250mV and 125mV and provide the explanation for the results for 3 different input signal levels.

Summary of what you need to submit electronically:

1. Schematics of your design – use white background in monochrome. (No color schematic)
2. Pipeline stage transient simulation results showing all relevant signal waveforms for normal mode
3. Pipeline stage simulation results showing all relevant signal waveforms for 2X gain mode
4. FFT plots for the output when the MDAC is in 2X gain mode for 3 different signal levels
5. Summary of what you have learned on this homework problem

Extra Credit (**2 points**)

Create a functional Verilog-A code set for 1.5bit stage operation. Use the schematic cell "ideal_1p5stage" in ee288lib as a baseline for the circuit structure for Verilog implementation. To receive the credit points, simulation results should prove that the Verilog codes are working.