# EE288 Data Conversions/Analog Mixed-Signal ICs
# Spring 2018

## Revised Project Description

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# Remaining Schedule

| | |
|---|---|
| 4/25 Wed | Lecture on ADC OPAMP 2 |
| 4/30 Mon | Lecture on Oversampled ADC 1 |
| 5/2 Wed | Lecture on Oversampled ADC 2 |
| 5/7 Mon | HW6 Due and Review |
| 5/9 Wed | Project Presentation 1 |
| 5/14 Mon | Project Presentation 2 |
| 5/21 Mon | Project Report Due |

# Revised Project Spec

| | |
|---|---|
| Process Technology | 45nm CMOS with 0.18um I/O devices |
| Process Corners | TT, FF, SS |
| Supply Voltage | VDD = 1.8V ± 5% |
| Temperature Range | 0 ~ 70 ºC |
| Sampling Rate, fs | 50 MS/s |
| Input Full Scale, VFS | 1.6 Vppd |
| Input Frequency | (7/64)*fs MHz |
| Power consumption | As small as possible |
| 2x gain mode Linearity | 10-bit ENOB at Typical, 7-bit at worst corner |

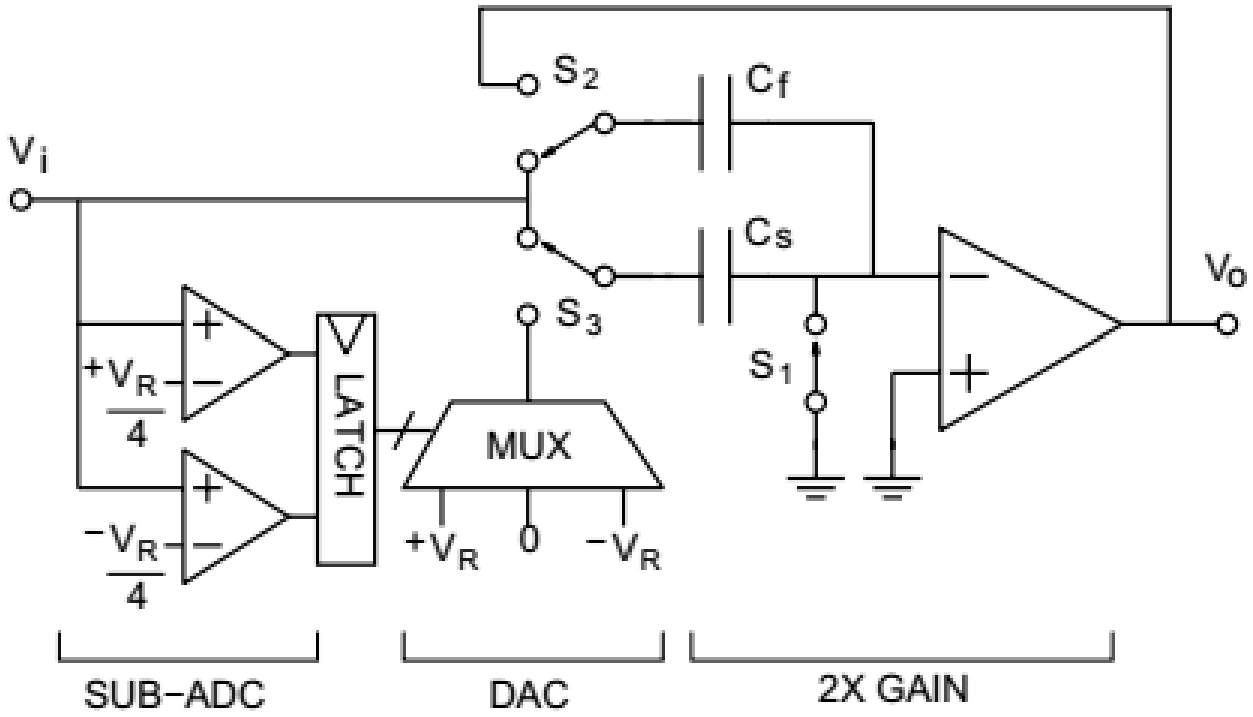
# Project Point Breakdown

| | | | |
|---|---|---|---|
| Total point | | | 40 |
| | | | |
| Condition 1 | Fully-Differential 1.5-bit | Stage Design | 10 |
| | | Typical corner (TT, 1.8V, 27C) | |
| | | Vin = 0.8Vpp (Full scale signal) | |
| | | fin = (cycles/N) * fs where cycles=7 and N=64 | |
| | | Fs = 50 MSPS | |
| | | Real switches & Real opamp | |
| | | ideal_clock, ideal_bias, and ideal voltages | |
| | | Target: 10-bit ENOB at 2x gain mode with Vin=0.8Vpp | |
| | | Report the results for Vin=0.4Vpp and 0.2Vpp as well | |
| | | | |
| Condition 2 | Condition 1 plus | Worst case ENOB > 7-bit for 2x gain mode, Vin=0.8Vpp | 10 |
| | | TT, 1.8V, 0C, 27C, 70C | |
| | | TT, 27C, 1.7V, 1.8V, 1.9V | |
| | | 27C, 1.8V, TT, FF, SS | |
| | | SS, 1.7V, 70C | |
| | | | |
| Presentation (5 min) on May 9 or 14 | | | 10 |
| | | | |
| Project report in 4-page IEEE conference | | paper submission format (Due May 21) | 10 |
| | | | |
| Extra point | | Functional Verilog-A codes for 10-bit ADC | 5 |

# Scoring Rule

- If your ENOB for TT corner is lower than 10-bit, you will get one point deduction for each ENOB you missed.
- If your ENOB for worst corner is lower than 7-bit, you will get one point deduction for each ENOB you missed.
- This rule will be applied to both the Presentation and the Report
  - For example, you have missed the target by 2-bit on Presentation day, but you missed the target by 1-bit on the final report, you will get a deduction of total 3-points.

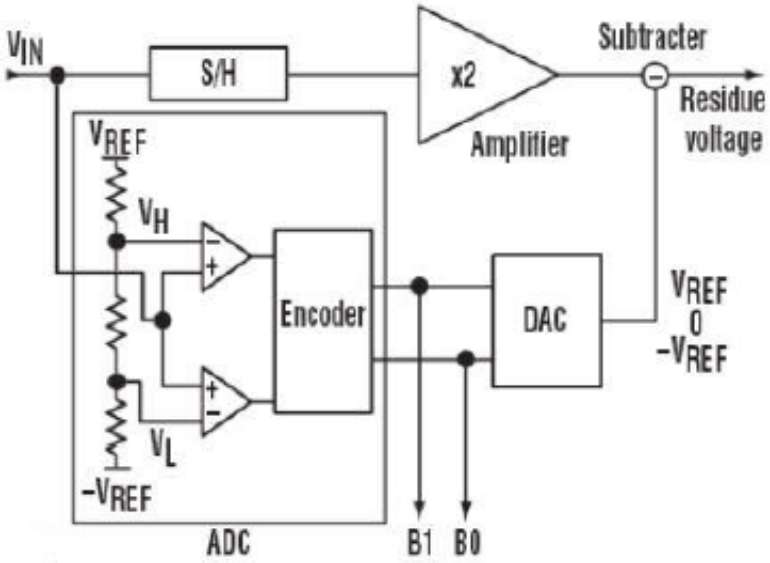
# 1.5-Bit Stage Architecture

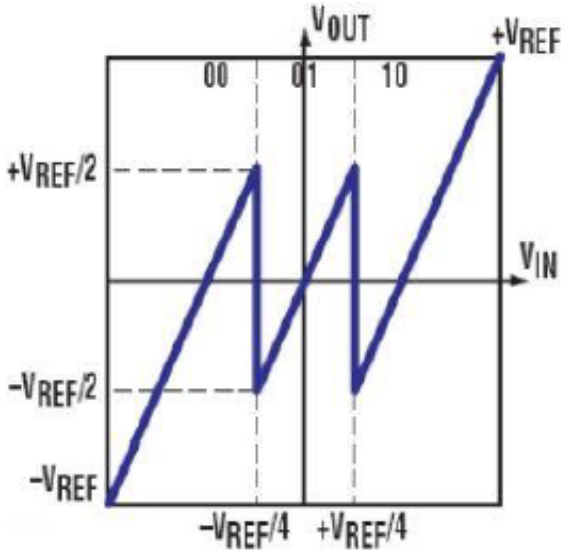



Reference Paper:

A. M. Abo and P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 599–606, May 1999

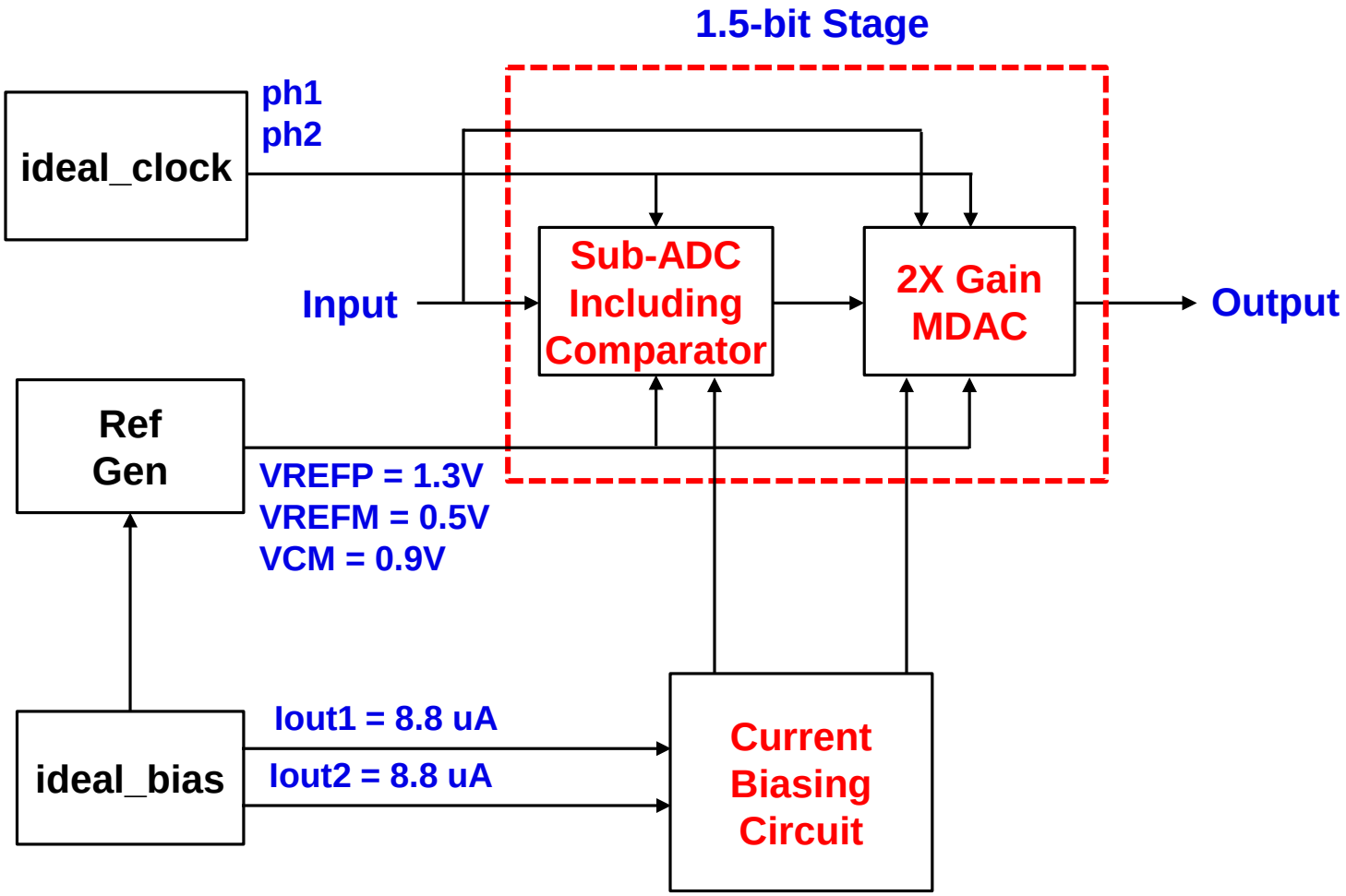
# 1.5-Bit Stage Architecture




| $V_{IN}$ | Range | B1 | B0 | DAC O/P | Residue |
|---|---|---|---|---|---|
| $V_{IN} > V_H$ | H | 1 | 0 | $+V_{REF}$ | $2V_{IN} - V_{REF}$ |
| $V_L < V_{IN} < V_H$ | M | 0 | 1 | 0 | $2V_{IN}$ |
| $V_H < V_L$ | L | 0 | 0 | $-V_{REF}$ | $2V_{IN} + V_{REF}$ |

# Key Blocks To Design in the Project



# OPAMP Requirement

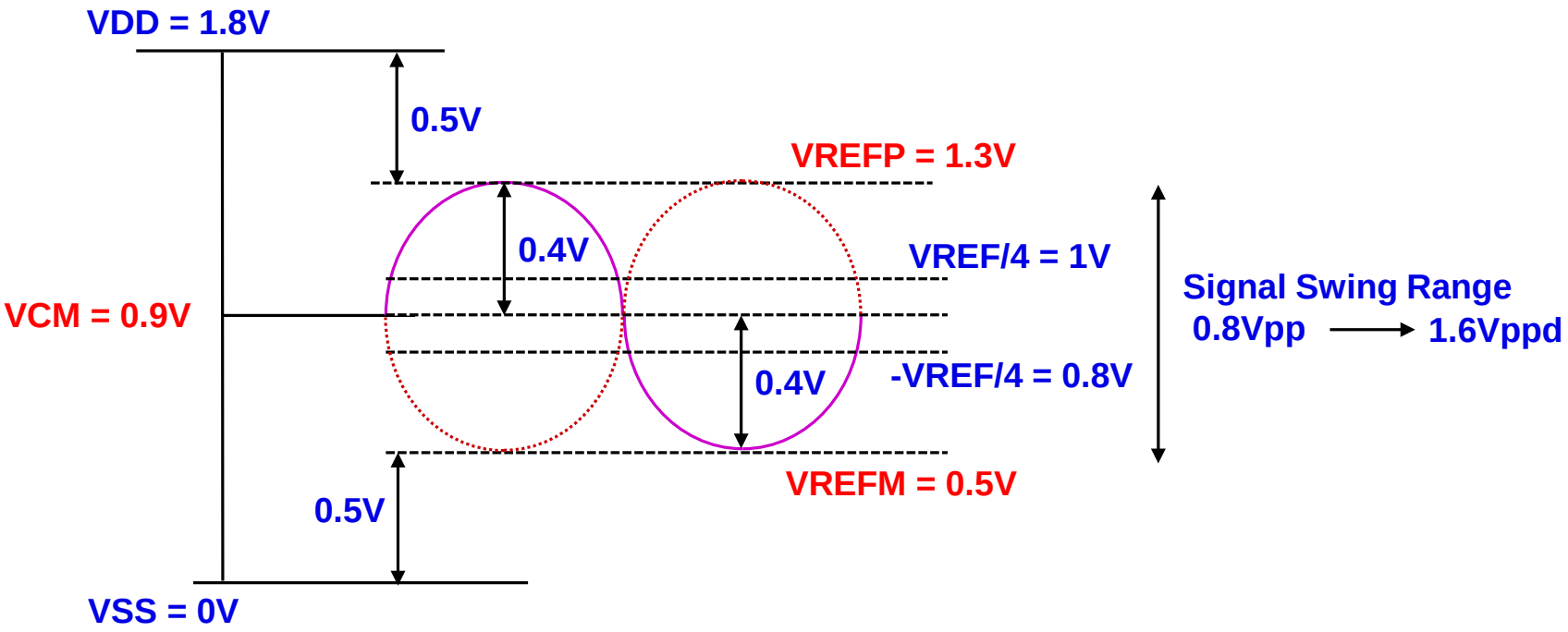
| Resolution | Full Scale | Beta | Gain (dB) | Gain (dB) |
|---|---|---|---|---|
| N | $V_{FS}$ (Volt) | β | $2 \cdot 2^{N} / (\beta \cdot V_{FS})$ | 20log(x) |
| 10 | 0.8 | 1 | 5120 | 74 |
| 10 | 0.8 | 0.5 | 10240 | 80 |
| 11 | 0.8 | 1 | 10240 | 80 |
| 11 | 0.8 | 0.5 | 20480 | 86 |
| 12 | 0.8 | 1 | 20480 | 86 |
| 12 | 0.8 | 0.5 | 40960 | 92 |

| Resolution | Full Scale | Beta | Sampling Rate | UGB |
|---|---|---|---|---|
| N | $V_{FS}$ (Volt) | β | fs | fu |
| 10 | 0.8 | 1 | 5.00E+07 | 1.25E+08 |
| 10 | 0.8 | 0.5 | 5.00E+07 | 2.50E+08 |
| 11 | 0.8 | 1 | 5.00E+07 | 1.36E+08 |
| 11 | 0.8 | 0.5 | 5.00E+07 | 2.72E+08 |
| 12 | 0.8 | 1 | 5.00E+07 | 1.47E+08 |
| 12 | 0.8 | 0.5 | 5.00E+07 | 2.94E+08 |

# Implementation Detail

- Start with your HW6 design as a baseline
- Use Ideal capacitor cell “cap” from analogLib
- Use “ideal_bias” cell in ee288lib for master current sources
- Use “ideal_clock” cell in ee288lib for 2-phase non-overlapping clocks
- Use Ideal DC voltage source for all voltage references such as VREFP, VREFM, and VCM
- Assume 100fF loading capacitance for your opamp
- You will need a switched-capacitor CMFB for your opamp

# Differential Signal Swing



# Items to prepare for project presentation

- Summary of your design
- Schematics
- Simulation Test Bench
- Simulation Results
  - OPAMP ac response
  - Comparator overdrive response
  - 1.5-bit Stage operation
  - 2x gain mode FFT plots for all 10 cases
  - Simulated average total power for the whole block (P)
  - TT case FoM calculation assuming the total ADC power = 10 x P

# Presentation Logistics

- Total score for Project Presentation is 10 points
- You are required to send the presentation file to me by 5PM May 9
- If you miss this deadline, you will get 2-point deduction
- Your presentation time should be no more than 5 min
- If your presentation is over 7 min, you will get 2-point deduction for using longer time and be forced to stop at that point
- Presentation order will be decided on the presentation day by lottery
- 40% for Neatness and clearness of the presentation materials to check if the slides are done professionally or not
- 40% for block functionality to check if the individual block design is functional or not
- 20% on if you answered the questions correctly or not in the Q&A session following your presentation

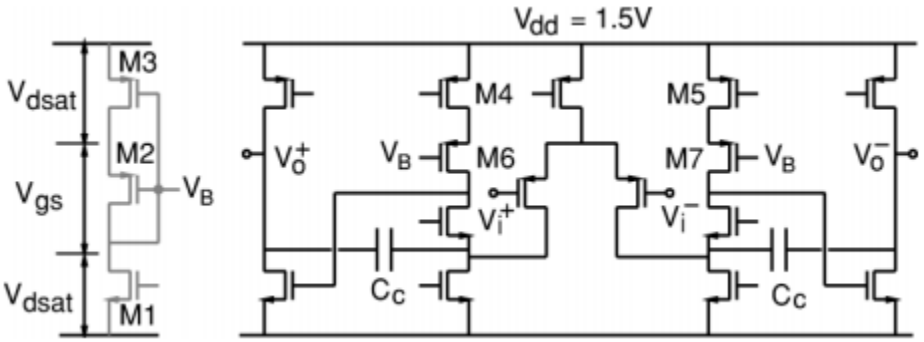
# Project Report Guideline

- Use the IEEE template file uploaded in project folder in Canvas
- Total report length should be 4-pages
- Report should include the following sections
  - Abstract
  - Introduction
  - Main sections
  - Conclusion
  - References

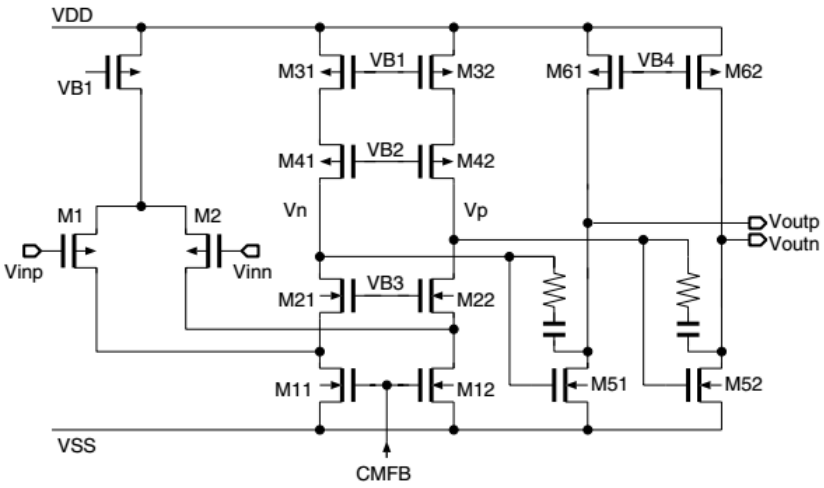
# Project Report Score Breakdown

- Total score for Project Report is 10 point
- Project report due is May 21, Monday midnight – If you miss the due date, each additional day will be 5 point deduction
- 40% for Neatness and clearness to check if the report is done professionally and if the report follows IEEE format
- 40% for block functionality to check if the individual block design is functional or not
- 20% for full stage design functionality - If you are working with another student, both of you will get the same score for the report

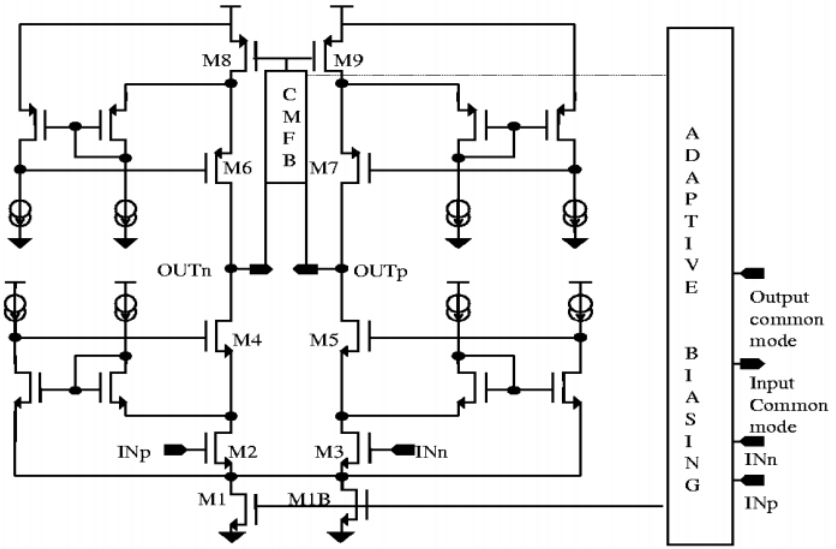
# Example OPAMP Circuits




[Ref. 1]

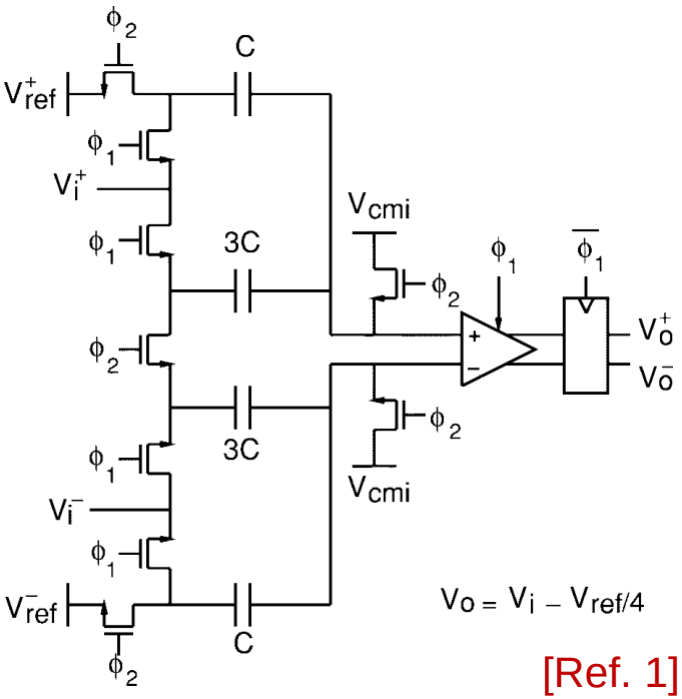


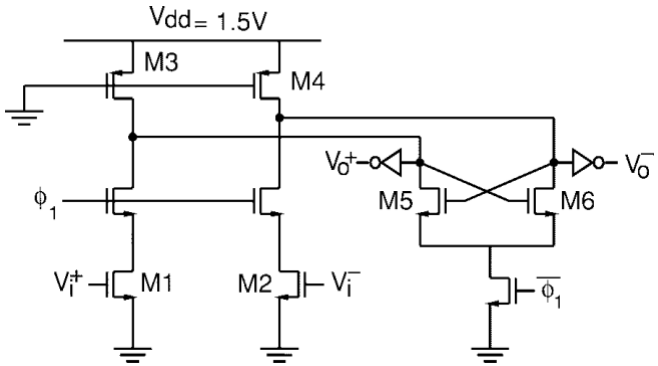

[Ref. 2]




[Ref. 3]

# Comparators

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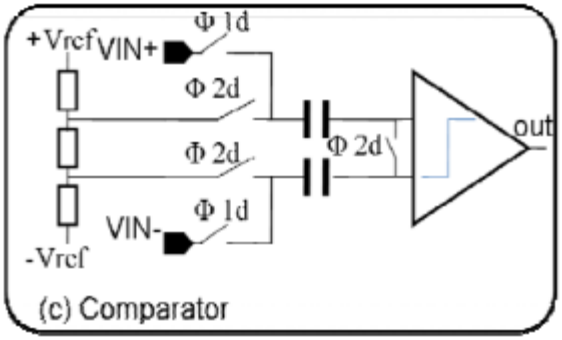


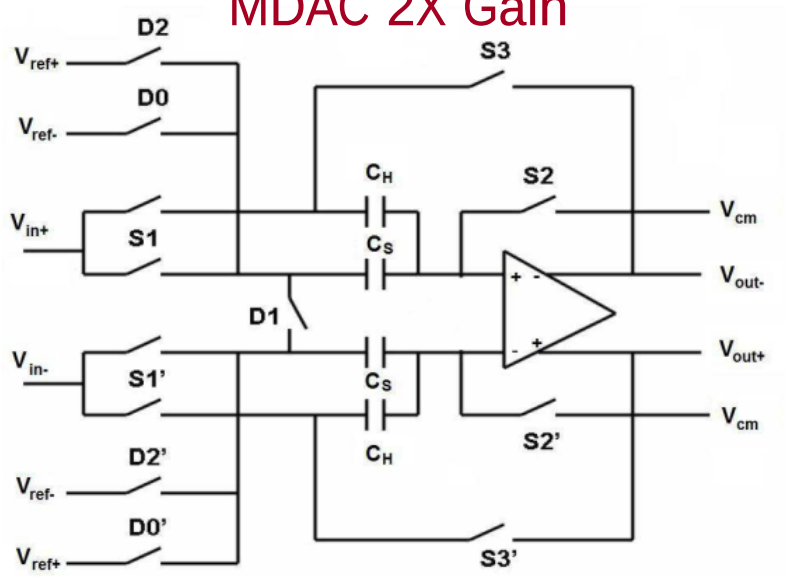

[Ref. 3]

# MDAC

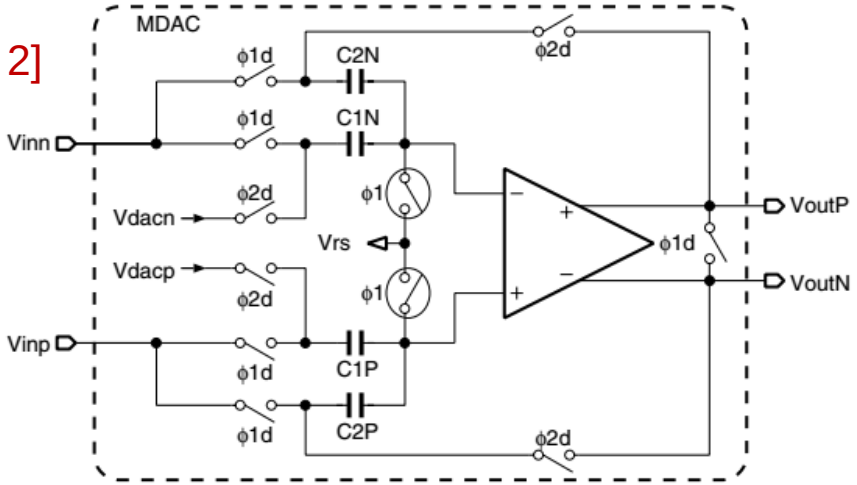
| $B_1$ | $B_0$ | $D_0$ | $D_1$ | $D_2$ |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | X | X | X |

Sub-ADC to DAC Bit Logic

MDAC 2X Gain




[Ref. 2]



# References


1. A. M. Abo and P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 599–606, May 1999

2. H. Ishii, K. Tanabe, and T. Iida, “A 1.0V 40mW 10b 100MS/s Pipeline ADC in 90nm CMOS,” *IEEE Custom Integrated Circuits Conference*, pp. 10.5.1–10.5.4, 2005

3. M. Boulemnakher, “A 1.2V 4.5mW 10b 100MS/s Pipeline ADC in 65nm CMOS,” ISSCC, pp. 250-251, 2008

4. M. E. Bayoumy, *MS Thesis, University of Texas, Austin*, A Study of 10-bit, 100Msps Pipeline ADC and the Implementation of 1.5-bit Stage, 2013

5. Overview of Pipelined ADC Chapter 13 from the book by M. Figueiredo et al., Reference-Free CMOS Pipeline Analog-to-Digital Converters, 2013