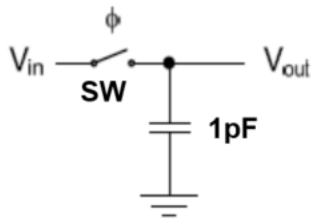
EE288 Homework #3 (5 points) Feb 26, 2018

Due: Mar 12, 2018 6:00PM
Homework will not be received after due.
The Homework submission file should be in pdf format and the file name convention should be EE288HW3_yourname.

In this homework, you will design a clock bootstrapped circuit to improve the nonlinearity of the switch used in Track & Hold circuit. You goal is to design a switch to achieve more than 10-bit accuracy. So, the SNR of the output signal should be larger than 60dB. Below is a simple Track and Hold circuit using a switch, SW, controlled by a clock ϕ and a capacitor to sample the signal for further processing in ADC.



To characterize the performance difference for various switch types, we will analyze the frequency spectrum of the output voltage using FFT in Cadence as well as in MATLAB. To do this, use the following information for transient simulations:

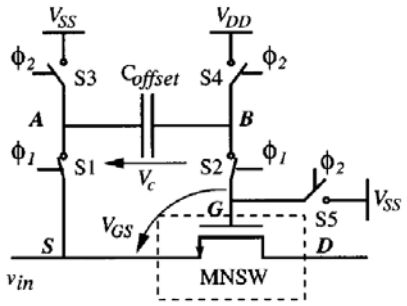
VDD = 1.8V
Sampling clock ϕ, fs = 100 MHz with 1.8V square wave. Use ph1 of the ideal_clock in ee288lib.
Input sine wave signal range 0.4V ~ 1.4V
Input signal frequency at fin = (cycles/N) * fs where cycles=7 and N=64 for 64-point FFT.

Then, run transient simulations for the following 3 different switch types.

1. Build a sample & hold circuit shown above using an ideal switch cell "ideal_swn" where the on-resistance of the switch is 1Ω. Run a transient simulation for 649ns and plot frequency spectrum of Vin and Vout using Cadence Spectrum measurement as well as MATLAB FFT. Report if the FFT plots for two methods agree or not.

2. Replace the ideal_swn with a CMOS transmission gate using nmos2v and pmos2v. Repeat the simulations described in step 1, and report the results.

3. Now replace the switch with a bootstrapped circuit similar to shown below using nmos2v and pmos2v, and repeat the step 1 and report the results. Use an ideal 2-phase non-overlapping clock "ideal_clock" in ee288lib library.



4. Finally, repeat the step 1-3 with half the input signal amplitude, i.e., signal range of 0.65V ~ 1.15V.

For the ideal clock, use the following parameter values in your simulation.

	Name	Value
1	Ron	1
2	delay	0
3	VDD	1.8
4	t_edge	50p
5	freq_mclk	100M
6	t_early	200p
7	non_ov	200p

For the bootstrapped circuit needed in step 3, read Section II and IV.A of the following reference paper to understand the circuit operation. You can find this paper in reference folder in Canvas.

M. Dessouky and A. Kaiser, "Very low-voltage digital-audio -sigma delta modulator with 88-dB dynamic range using local switch boot-strapping." IEEE J. Solid-State Circuits, vol. 36, pp. 349– 355, 2001.

Summary of what you need to submit electronically:

1. Schematics of your design – use white background in monochrome (No color for schematic)
2. Transient simulation results showing all relevant signal waveforms
3. FFT spectrum plots for different switch types
4. Summary table showing the ENOB, SNR, SFDR for all cases
5. Summary of what you learned on this homework problem