EE228 – HW3 Report
Track & Hold Circuits

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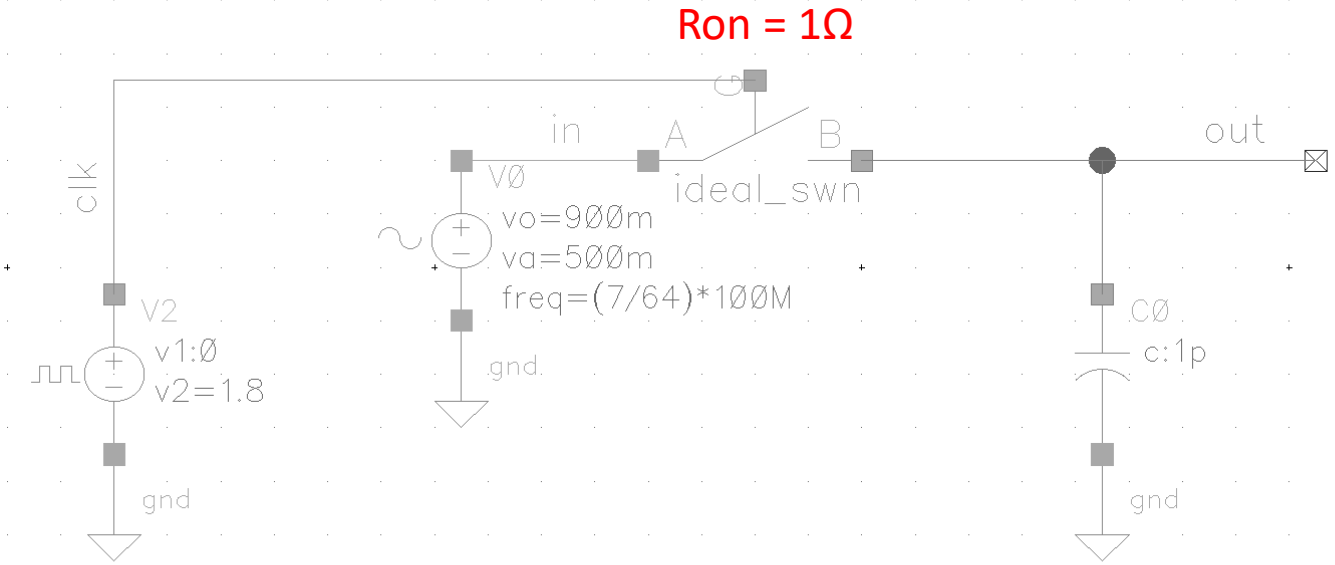
Overview

1. S/H using Ideal switch
2. S/H using NMOS or PMOS
3. S/H using CMOS Transmission Gate (TG)
4. Bootstrapped Circuits
   a) Using Ideal Switches
   b) Using transistors [2 topologies]
5. Summary

(1)
S/H Using Ideal Switch

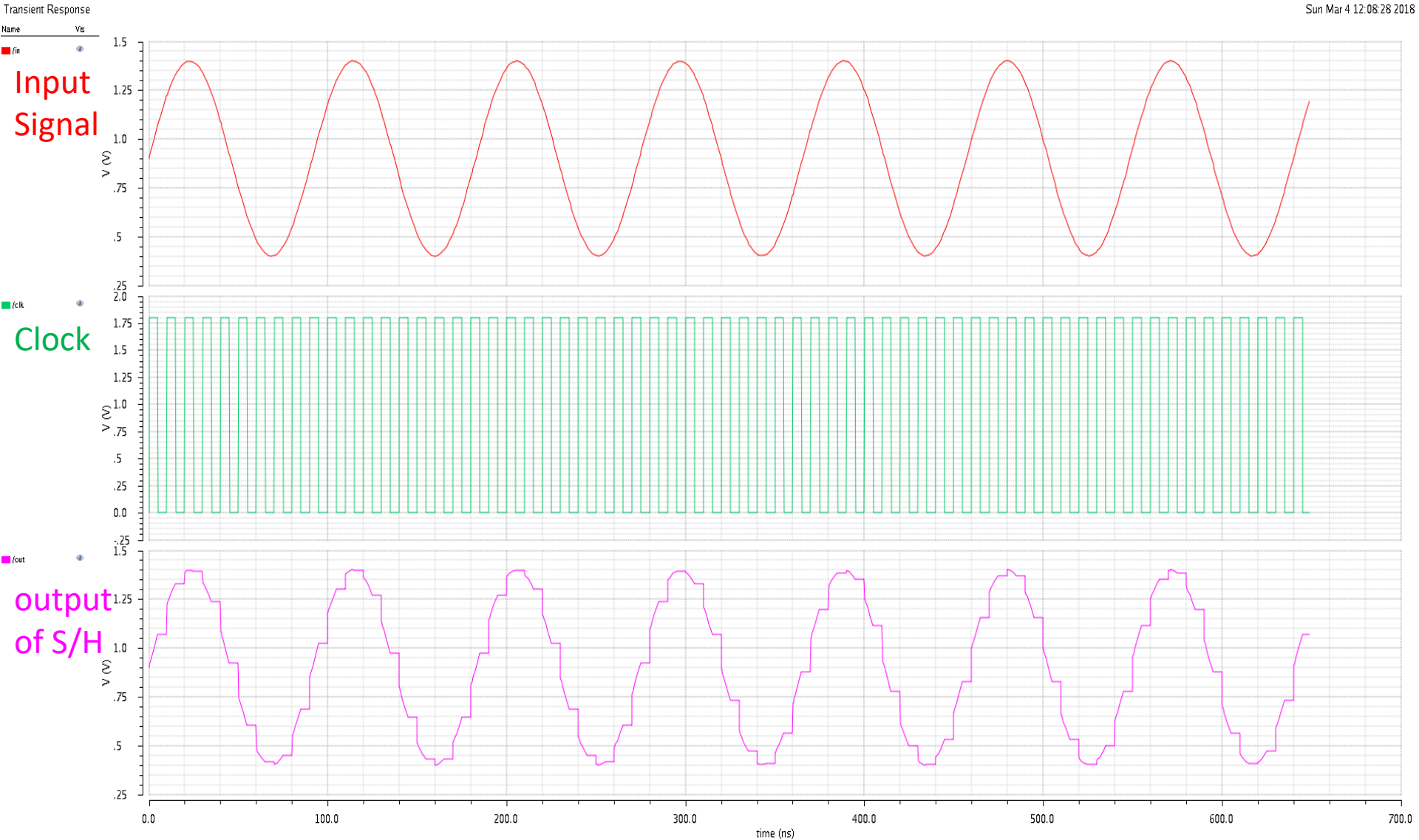
Circuit



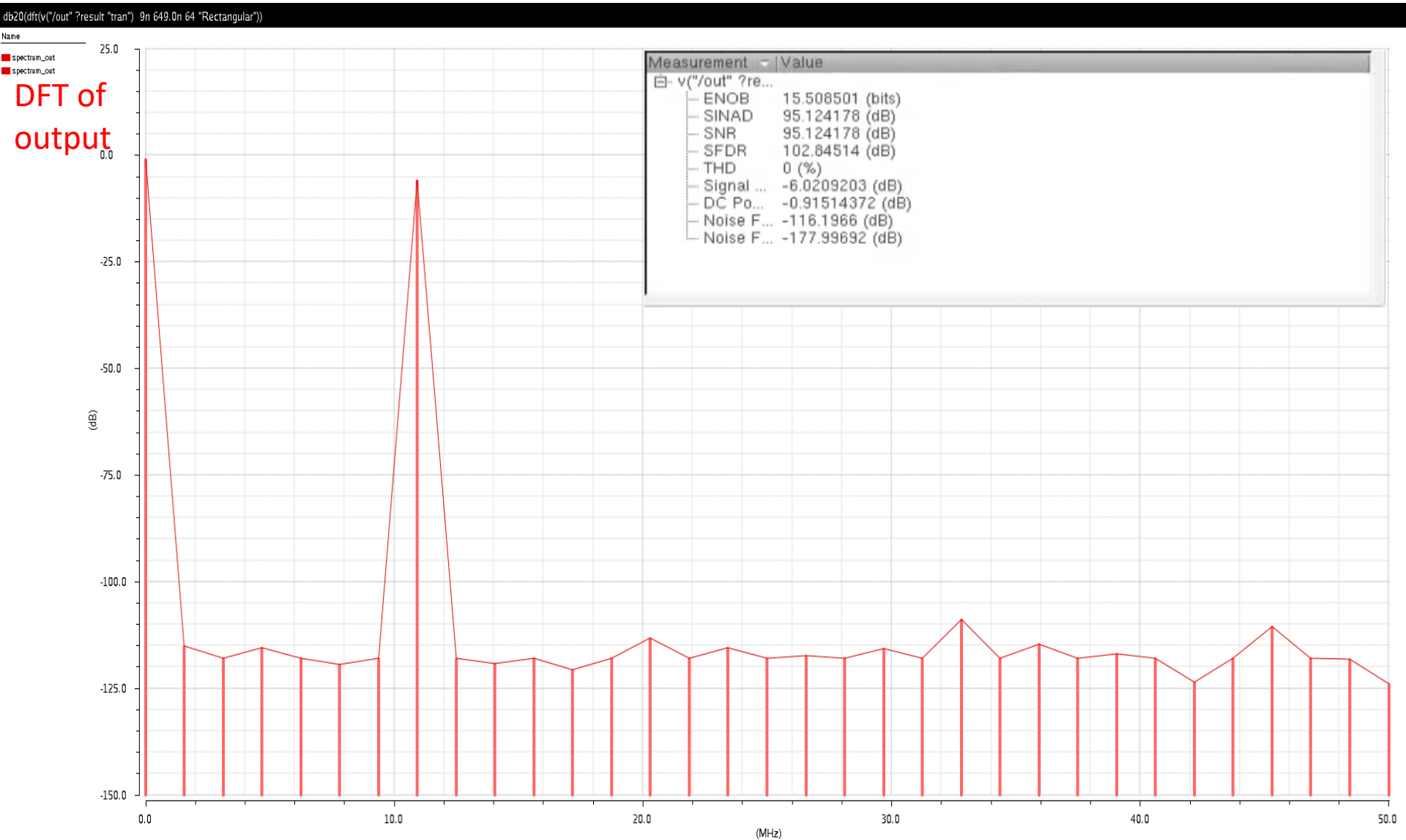
- Increasing the Ron of the switch, increases τ = RC …

This decreases ENOB, SINAD, SNR, & SFDR.

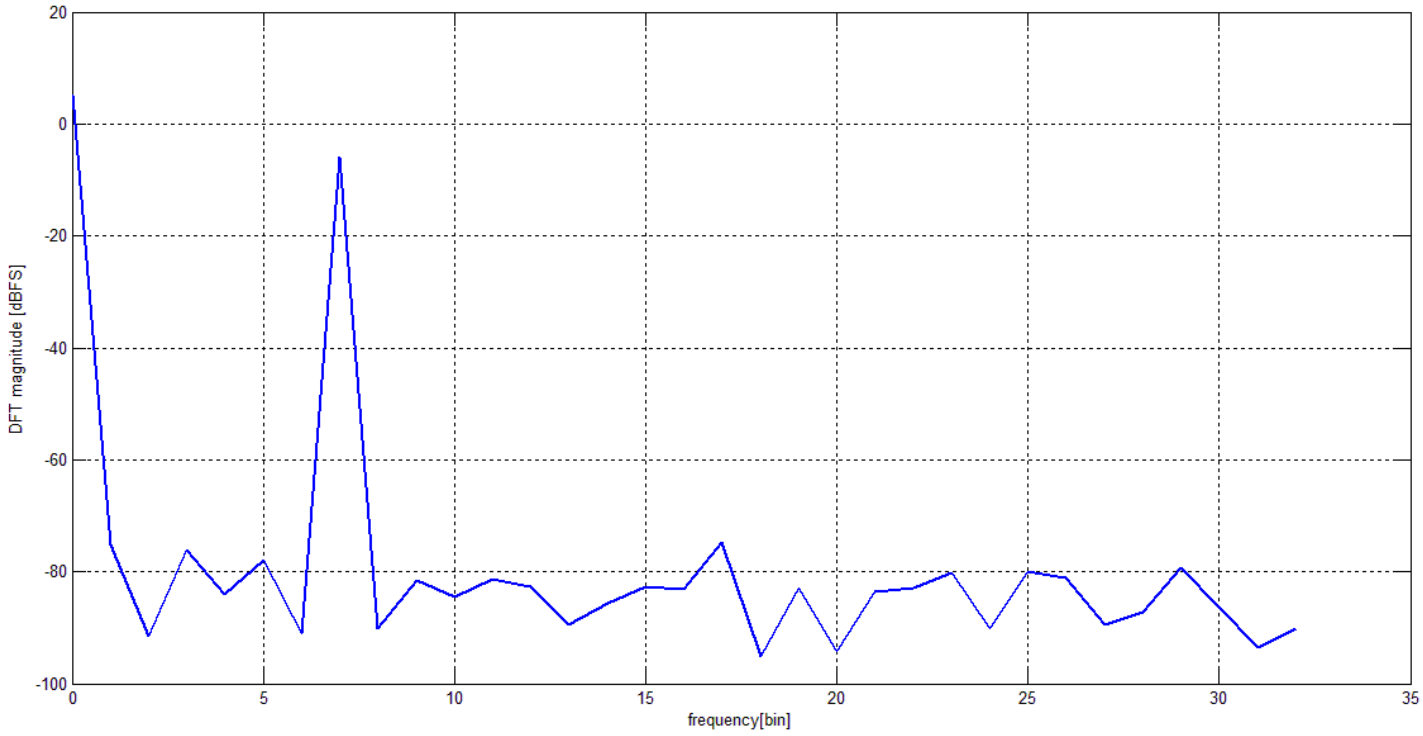
Waveforms


Transient Response
Sun Mar 4 12:08:28 2018
Name
Va
/in
Input Signal
/clk
Clock
/out
output of S/H
V (V)
time (ns)
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0

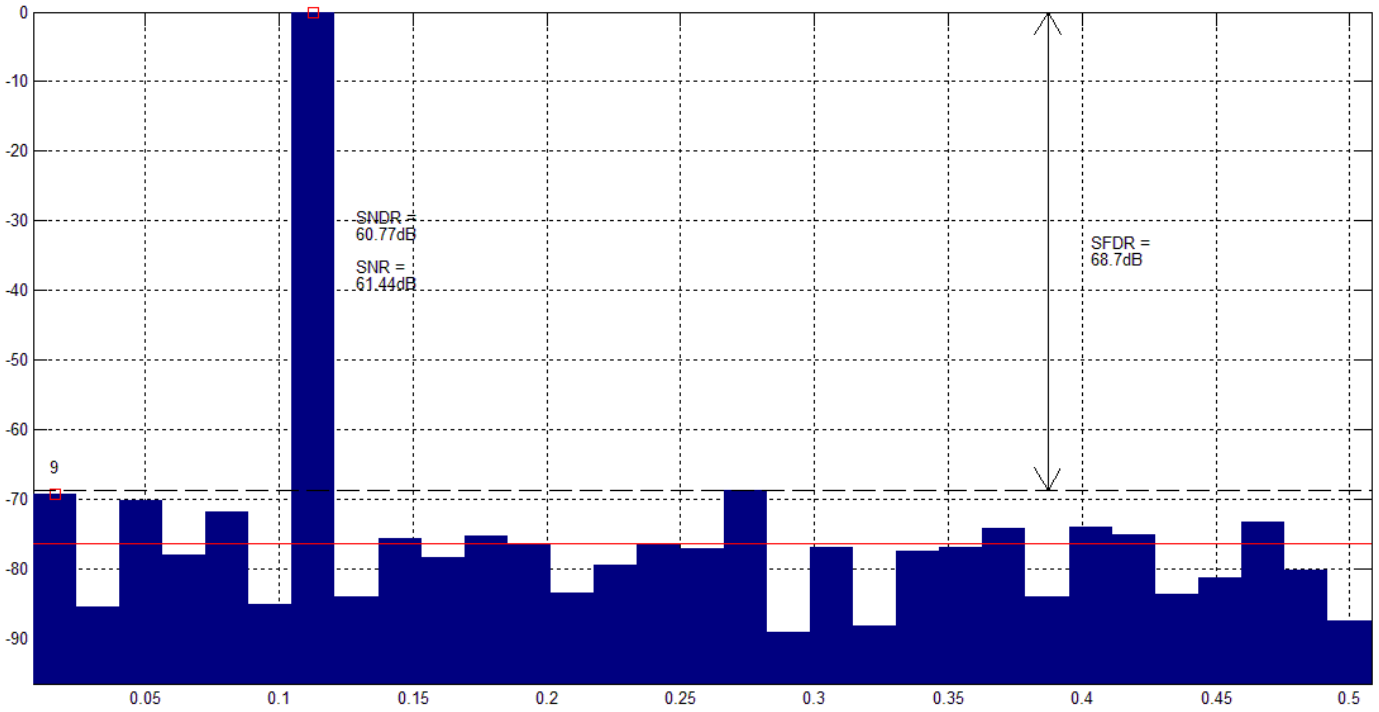
DFT


db20(dft(v("/out" ?result "tran") 9n 649.0n 64 "Rectangular"))
Name
spectrum_out
spectrum_out
DFT of output
Measurement
Value
v("/out" ?re...
ENOB 15.508501 (bits)
SINAD 95.124178 (dB)
SNR 95.124178 (dB)
SFDR 102.84514 (dB)
THD 0 (%)
Signal ... -6.0209203 (dB)
DC Po... -0.91514372 (dB)
Noise F... -116.1966 (dB)
Noise F... -177.99692 (dB)
25.0
0.0
-25.0
-50.0
-75.0
-100.0
-125.0
-150.0
(dB)
0.0
10.0
20.0
30.0
40.0
50.0
(MHz)

DFT (MATLAB)

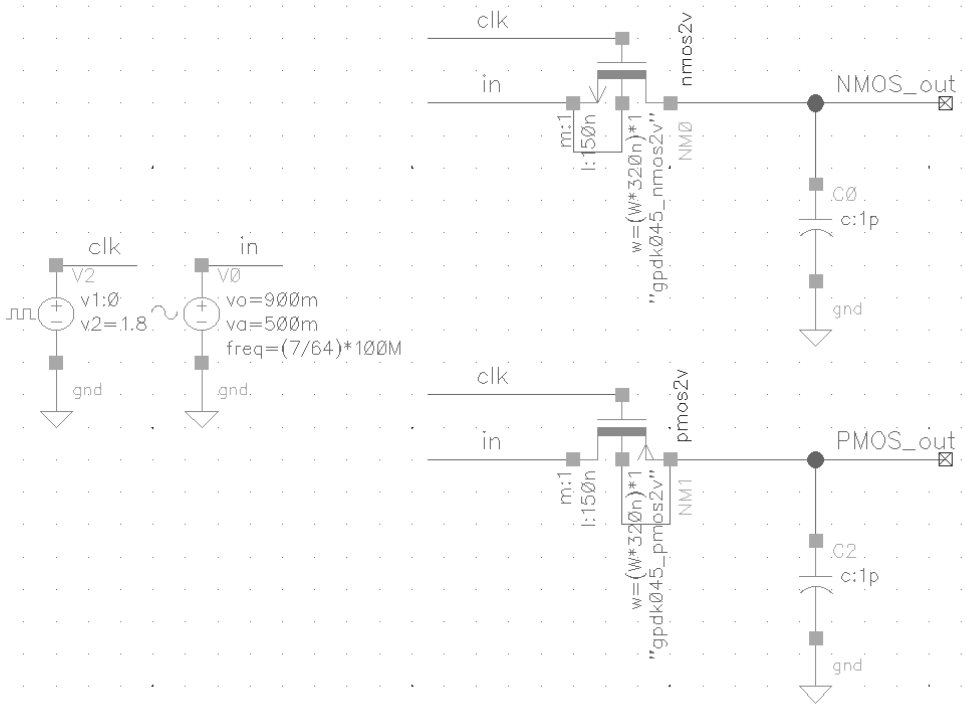

20
0
-20
-40
-60
-80
-100
DFT magnitude [dBFS]
0
5
10
15
20
25
30
35
frequency[bin]

Using PrettyFFT function



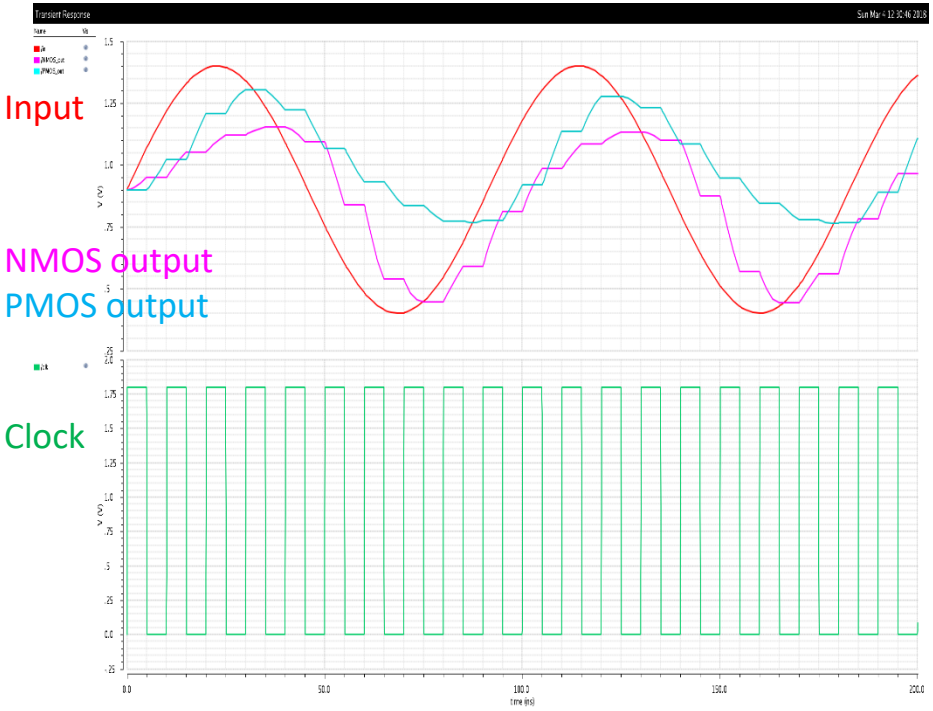
(2)
S/H Using NMOS or PMOS

Circuit

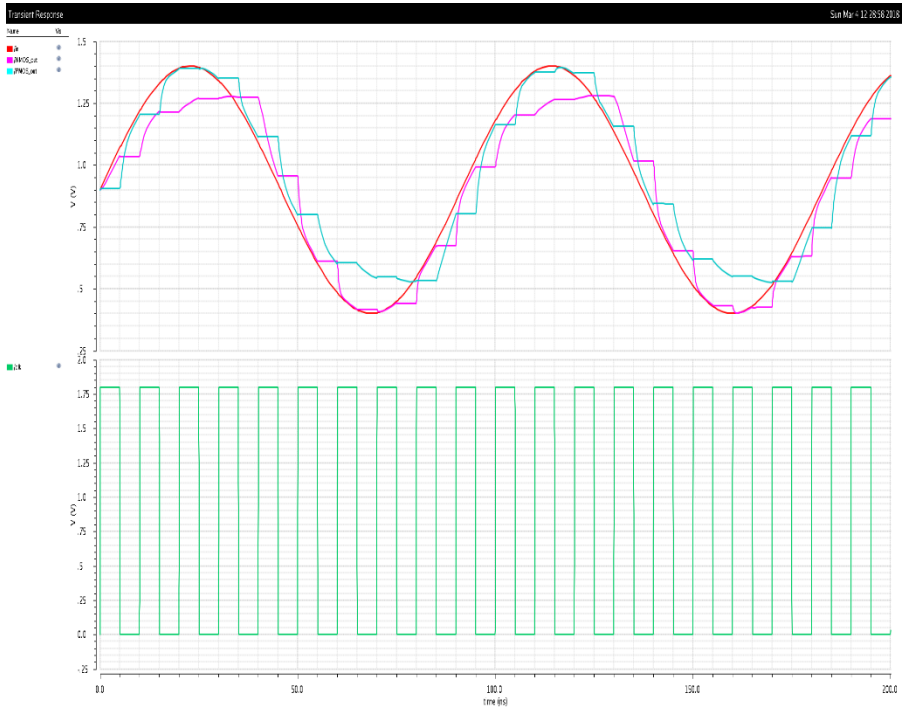

clk
in
nmos2v
NMOS_out
m:1
l:150n
w=(W*320n)*1
"gpdk045_nmos2v"
NM0
C0
c:1p
gnd
clk
in
pmos2v
PMOS_out
m:1
l:150n
w=(W*320n)*1
"gpdk045_pmos2v"
NM1
C2
c:1p
gnd
clk
V2
v1:0
v2=1.8
gnd
in
V0
vo=900m
va=500m
freq=(7/64)*100M
gnd

Waveforms

$Lower\ \left(\frac{W}{L}\right)_{n,p}$



$Higher\ \left(\frac{W}{L}\right)_{n,p}$

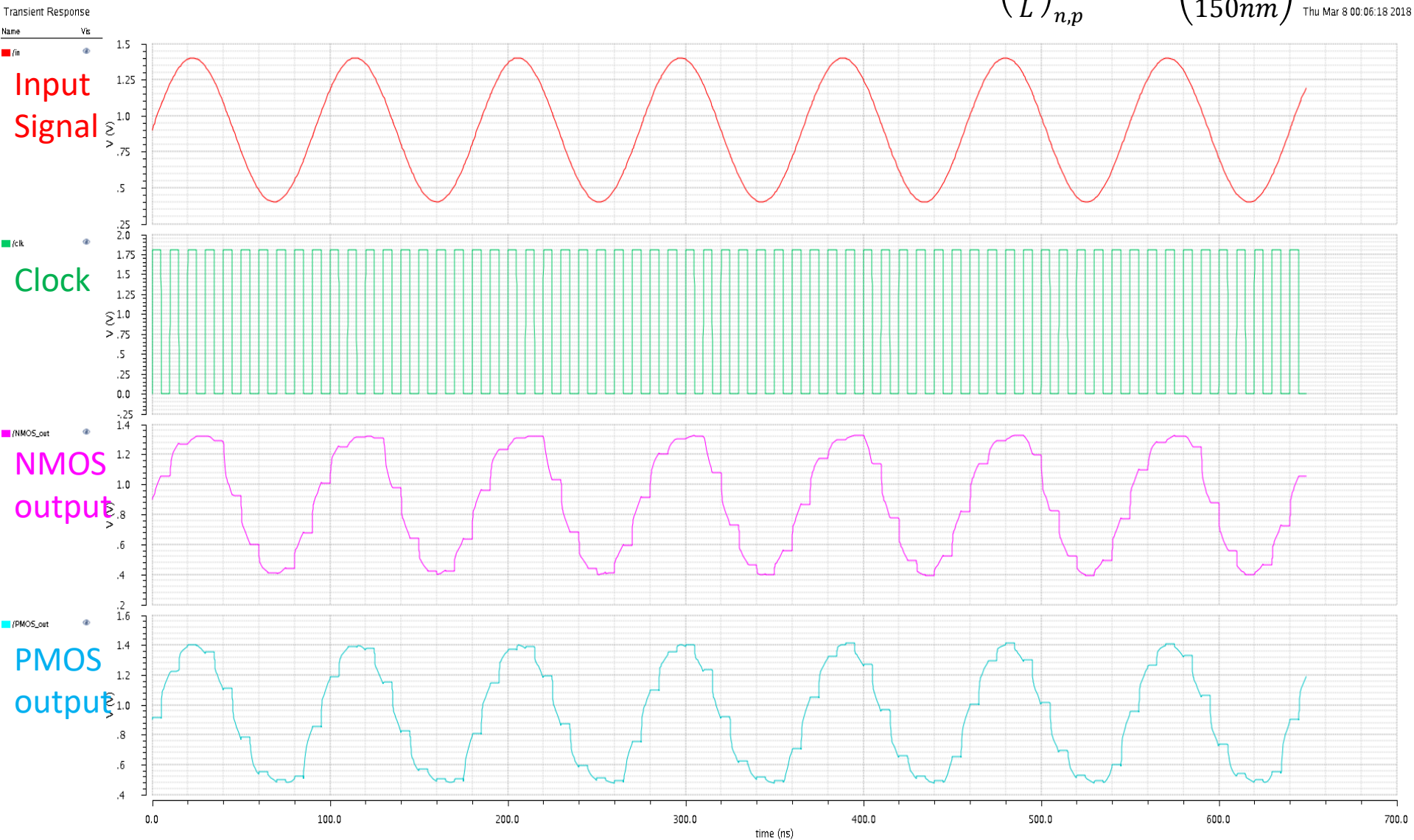


- NMOS is better for passing smaller Vin, while PMOS is better for passing larger Vin.
- Increasing (W/L), decreases Ron of the transistor, improving the S/H circuit performance.

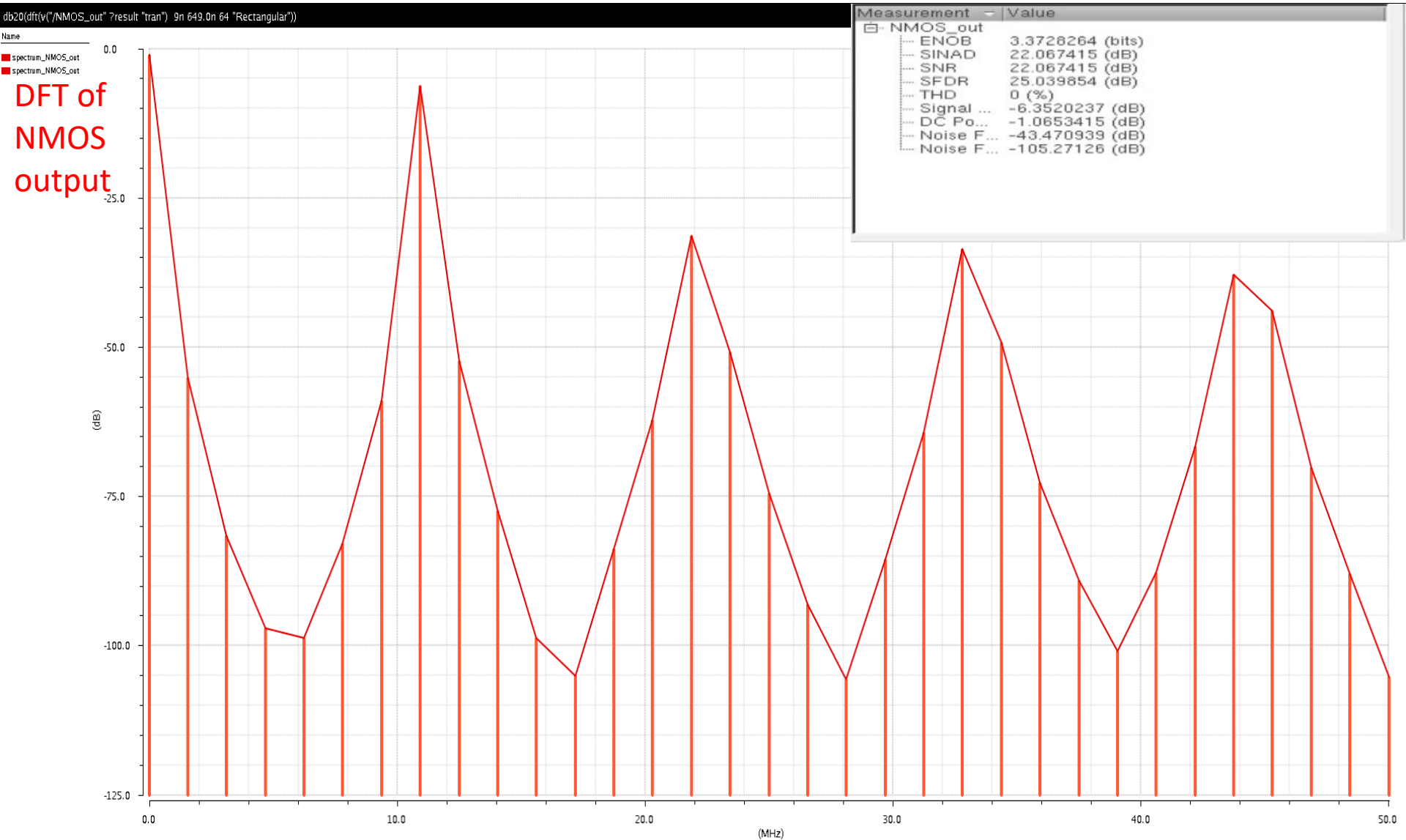
Waveforms

Maximum Allowed size for this technology

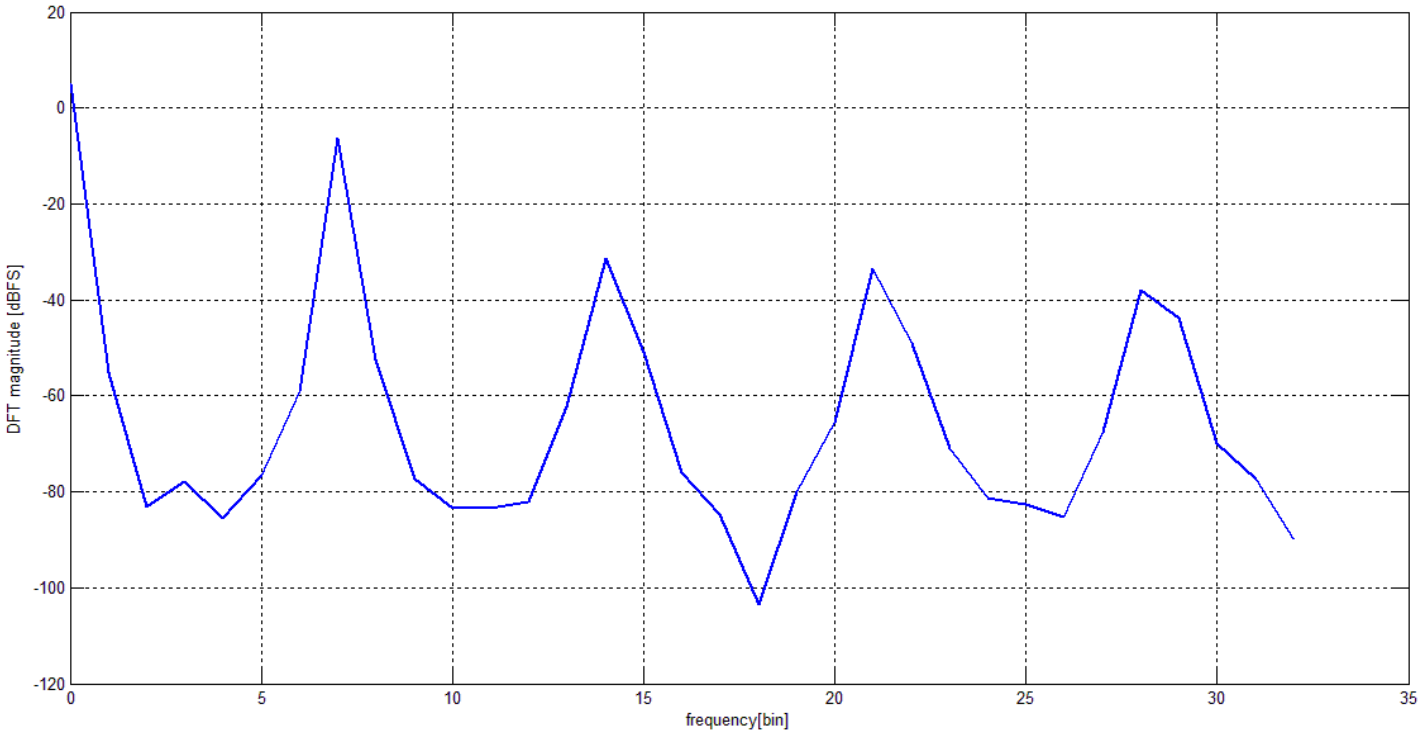
$$At\ \left(\frac{W}{L}\right)_{n,p} = 34\ x\left(\frac{320nm}{150nm}\right)$$



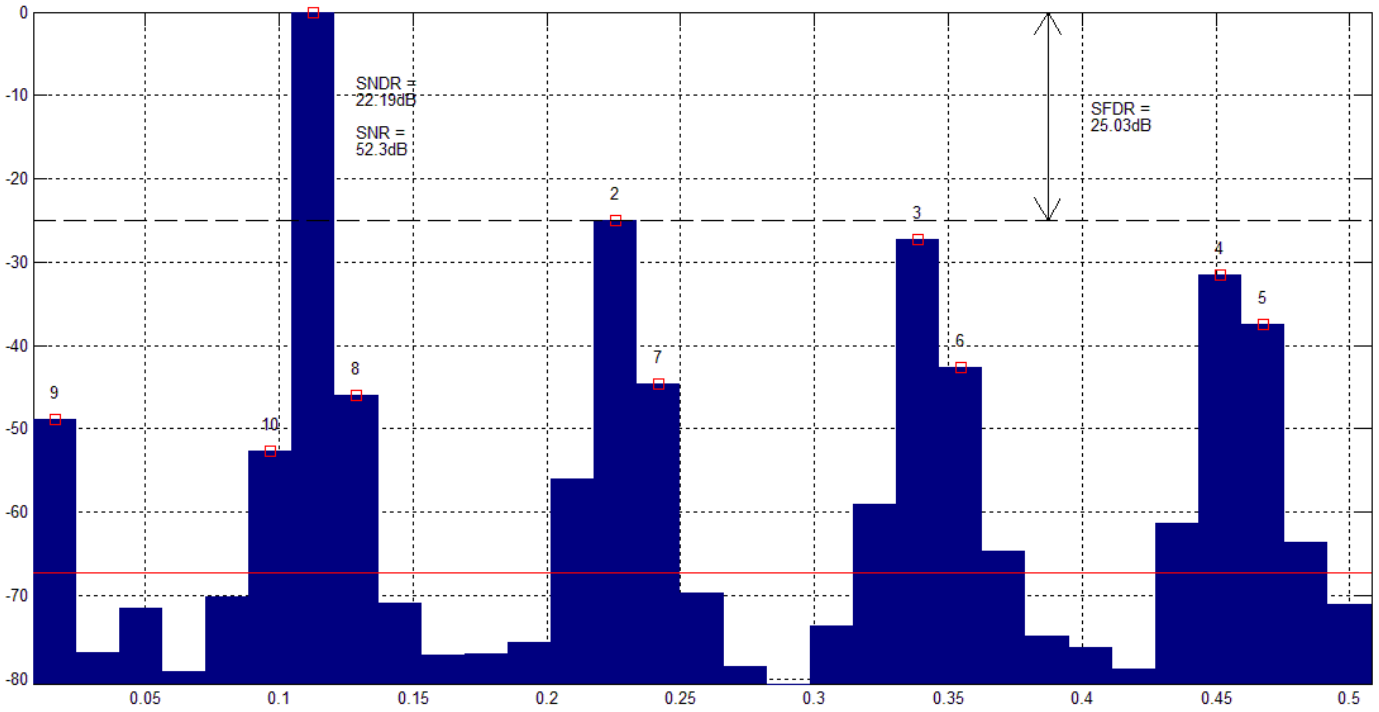
DFT of NMOS output



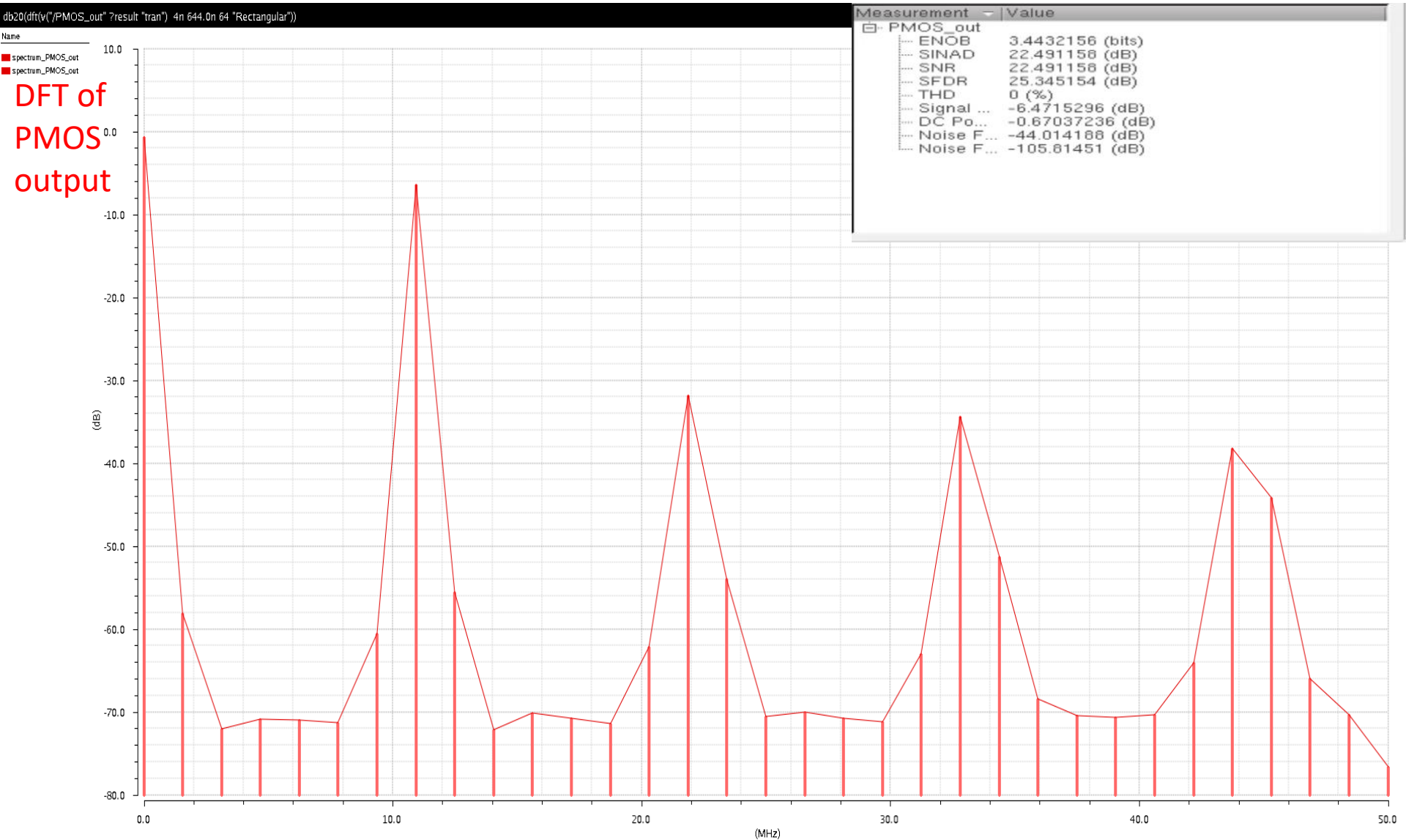
DFT of NMOS output (MATLAB)



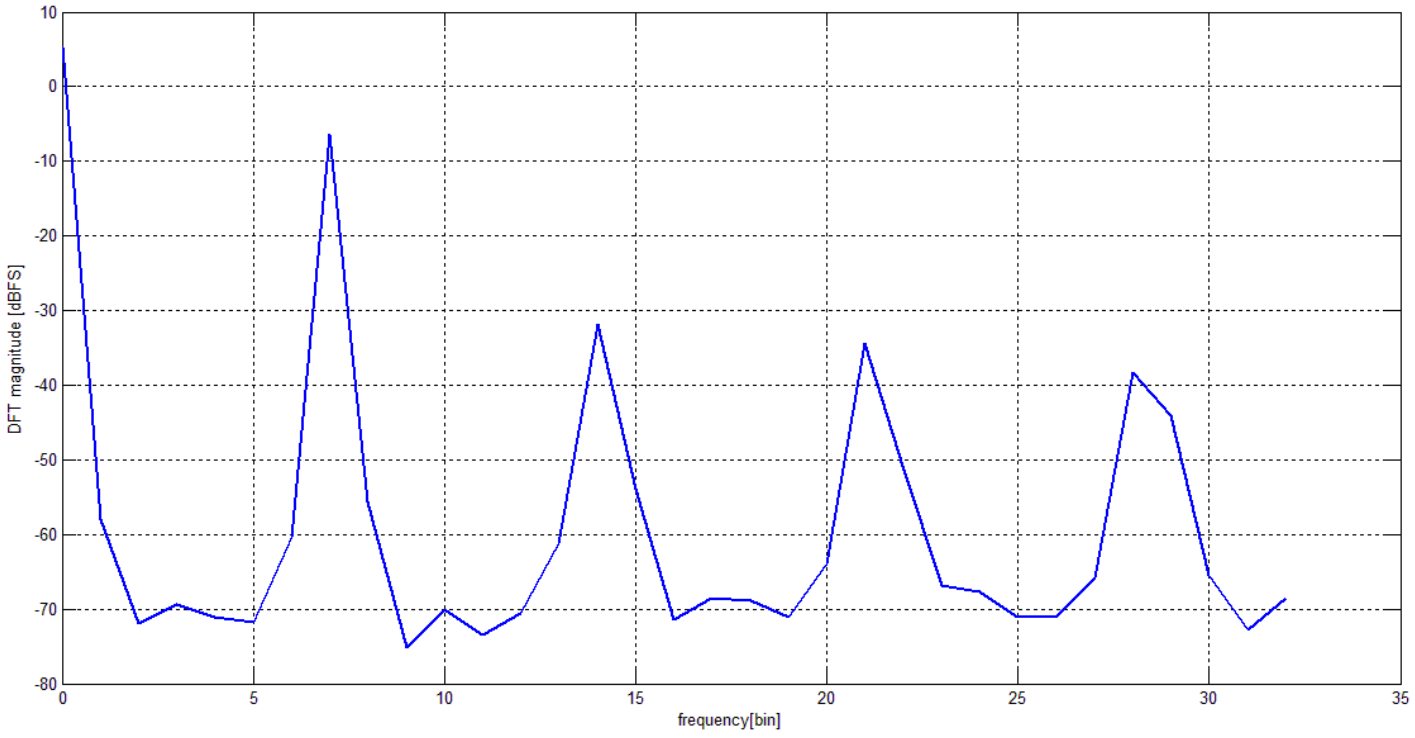
Using PrettyFFT function



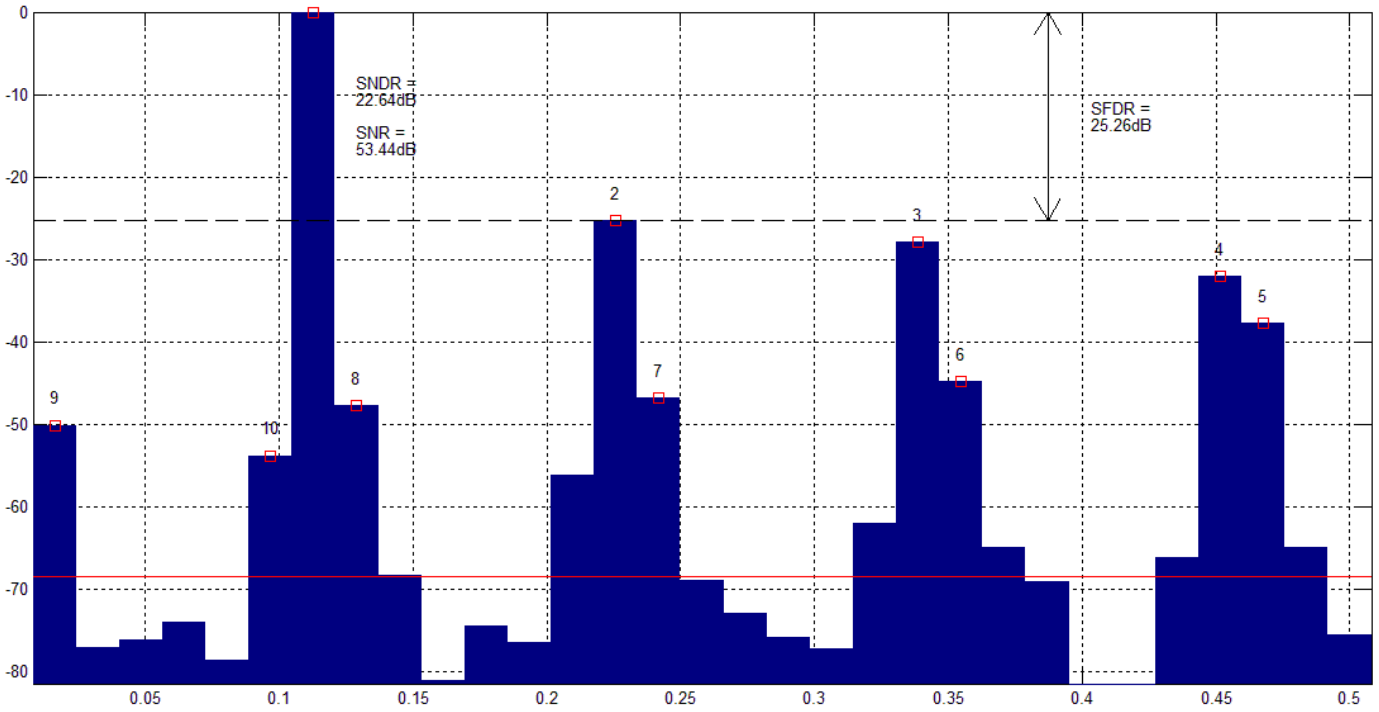
DFT of PMOS output



DFT of PMOS output (MATLAB)

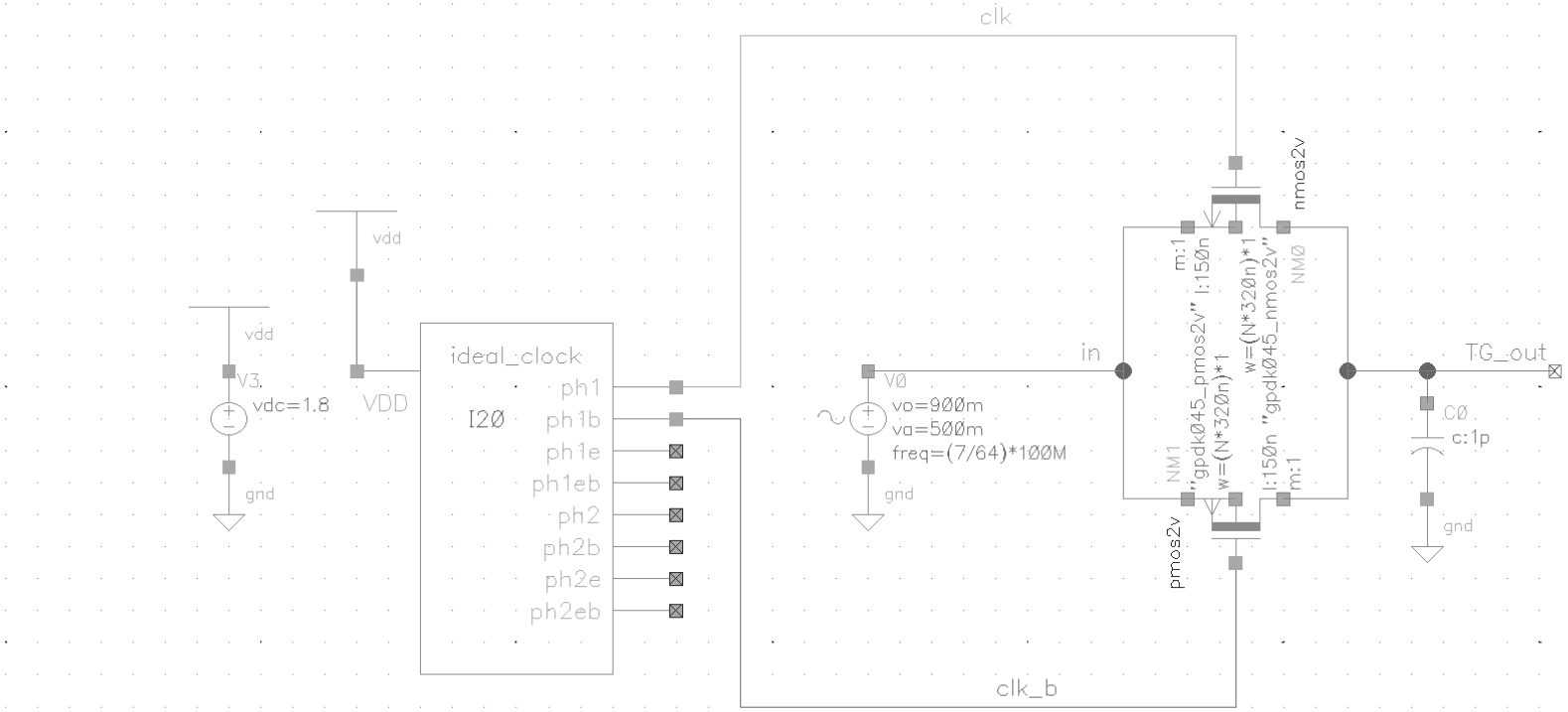


Using PrettyFFT function



(3)
S/H Using CMOS Transmission Gate

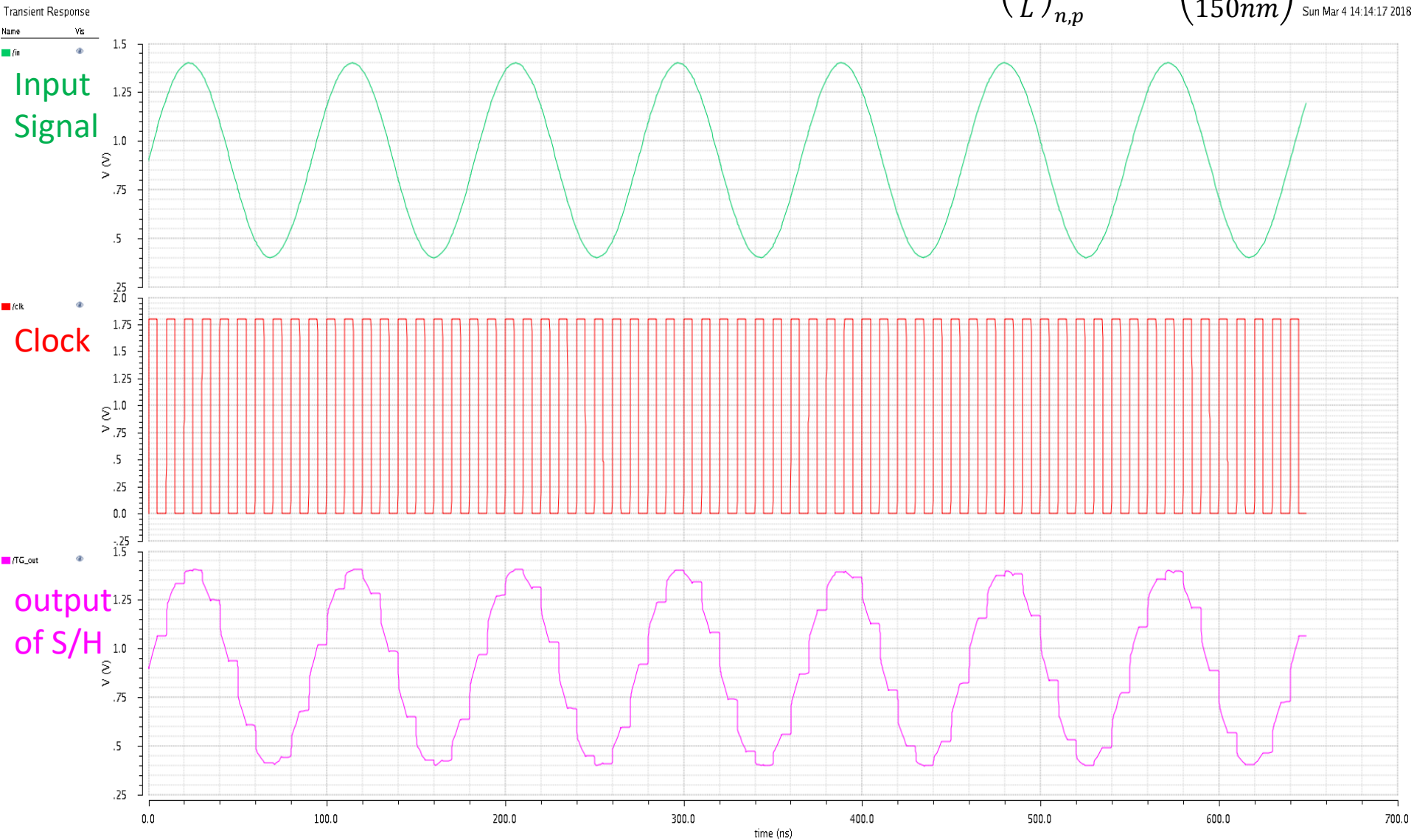
Circuit


clk
vdd
vdd
V3
vdc=1.8
gnd
VDD
ideal_clock
I2Ø
ph1
ph1b
ph1e
ph1eb
ph2
ph2b
ph2e
ph2eb
in
VØ
vo=9ØØm
va=5ØØm
freq=(7/64)*1ØØM
gnd
nmos2v
m:1
l:150n
"gpdk045_pmos2v"
w=(N*320n)*1
NM1
NMØ
w=(N*320n)*1
l:150n "gpdk045_nmos2v"
m:1
pmos2v
TG_out
CØ
c:1p
gnd
clk_b

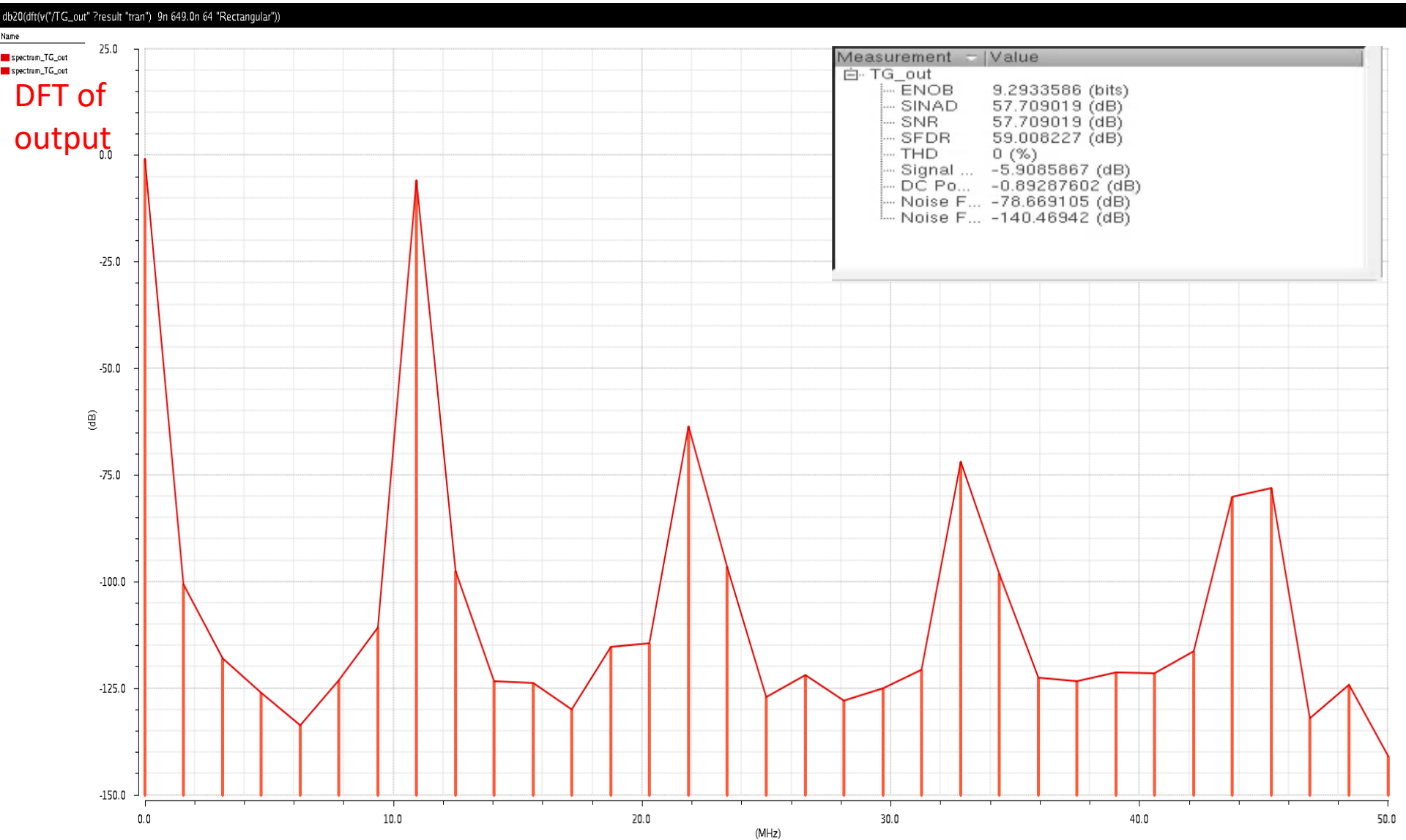
Waveforms

Max size for best ENOB & performance

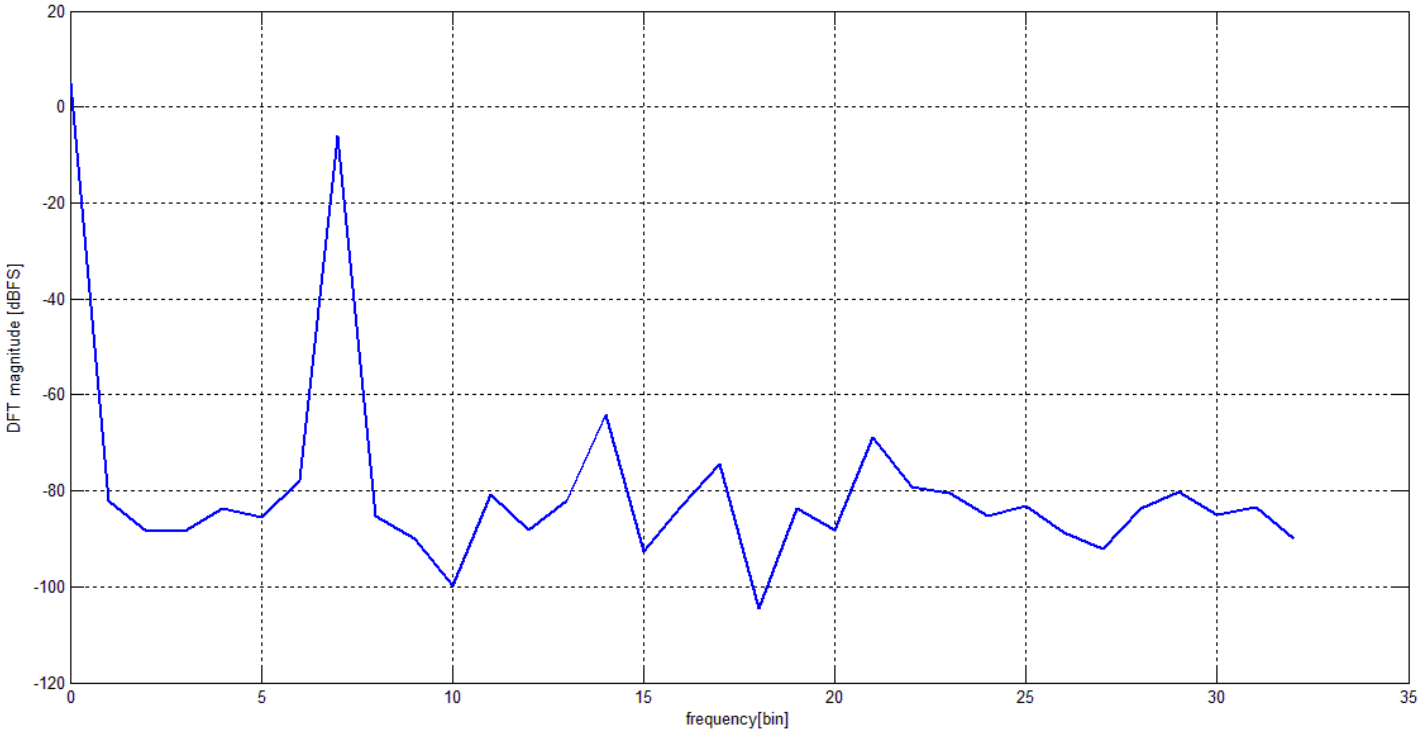
$$At \left(\frac{W}{L}\right)_{n,p} = 34\ x \left(\frac{320nm}{150nm}\right)$$



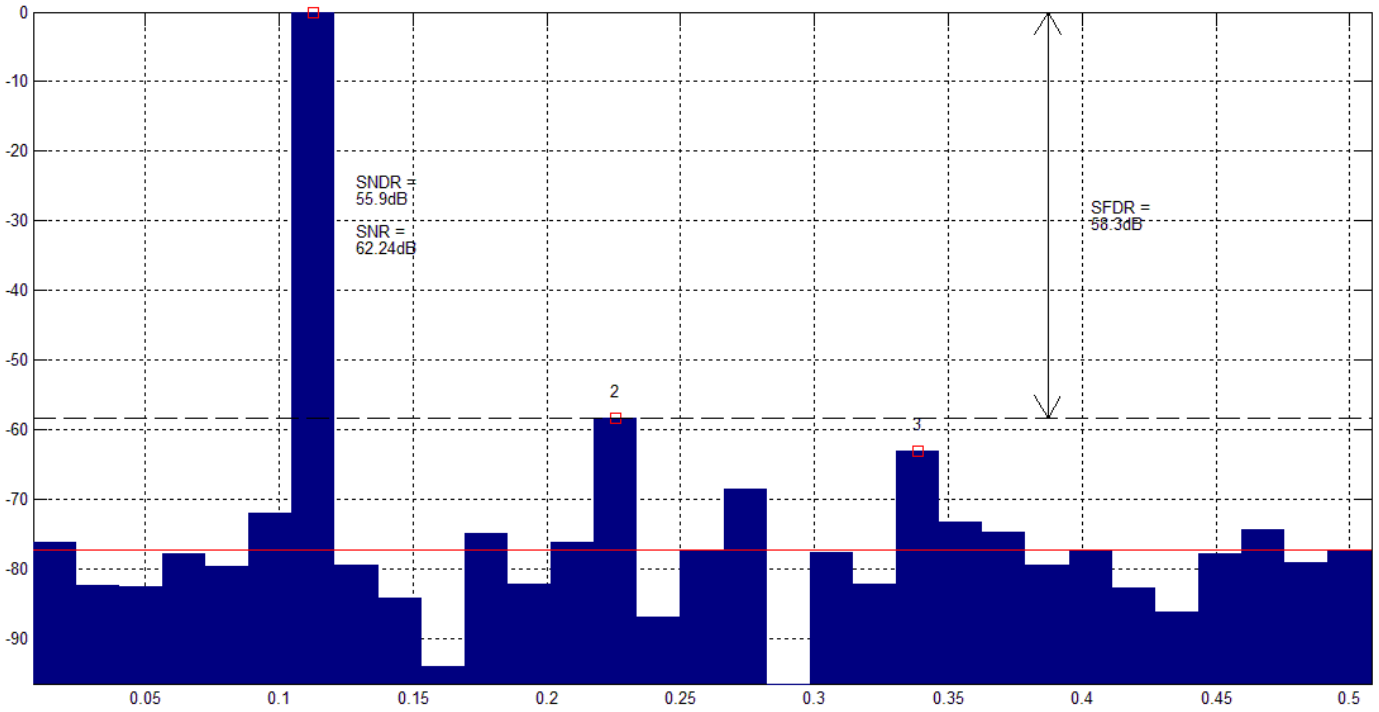
DFT of TG output



DFT of TG output (MATLAB)



Using PrettyFFT function

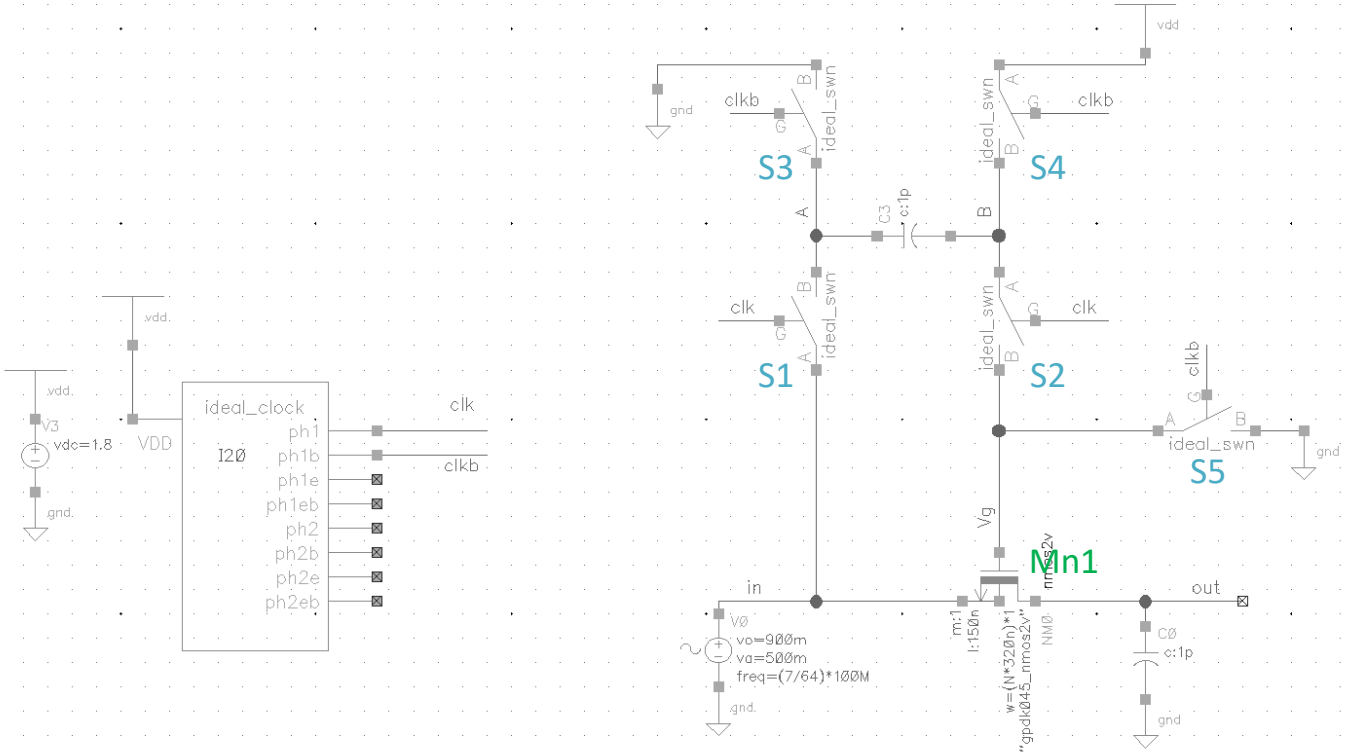


DFT of TG output

- Notes:
  - The TG gives better performance than NMOS only or PMOS only, at the same (W/L).
  - Increasing (W/L)n,p , decreases Ron of the TG, improving the S/H circuit performance.
  - With the maximum size for both transistors in the TG (best performance), the Maximum ENOB achieved = 9.29 bits (<10 bits).
  - Tradeoff:
    ➔ Increasing (W/L)n,p , decreases Ron but increases parasitic capacitors.

(4)
S/H Using Bootstrapped Circuit
a) With Ideal switches

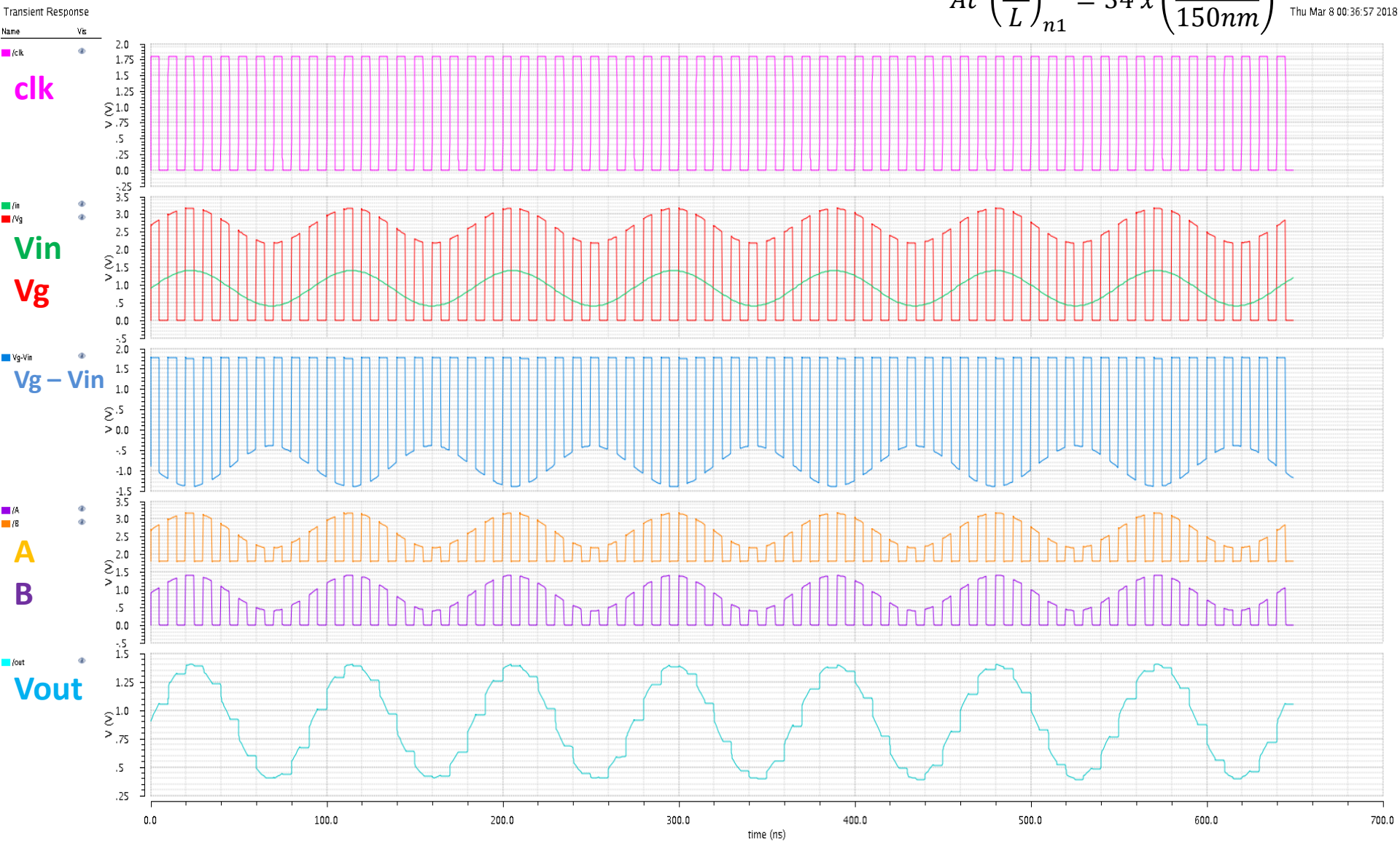
Circuit


vdd
V3
vdc=1.8
gnd
VDD
I2Ø
ideal_clock
ph1
ph1b
ph1e
ph1eb
ph2
ph2b
ph2e
ph2eb
clk
clkb
gnd
clkb
ideal_swn
S3
S4
C3
c:1p
clk
S1
S2
S5
Vg
Mn1
in
out
VØ
vo=9ØØm
va=5ØØm
freq=(7/64)*1ØØM
m:1
l:15Øn
w=(N*32Ø)*1
"gpdk045_nmos2v"
CØ
c:1p

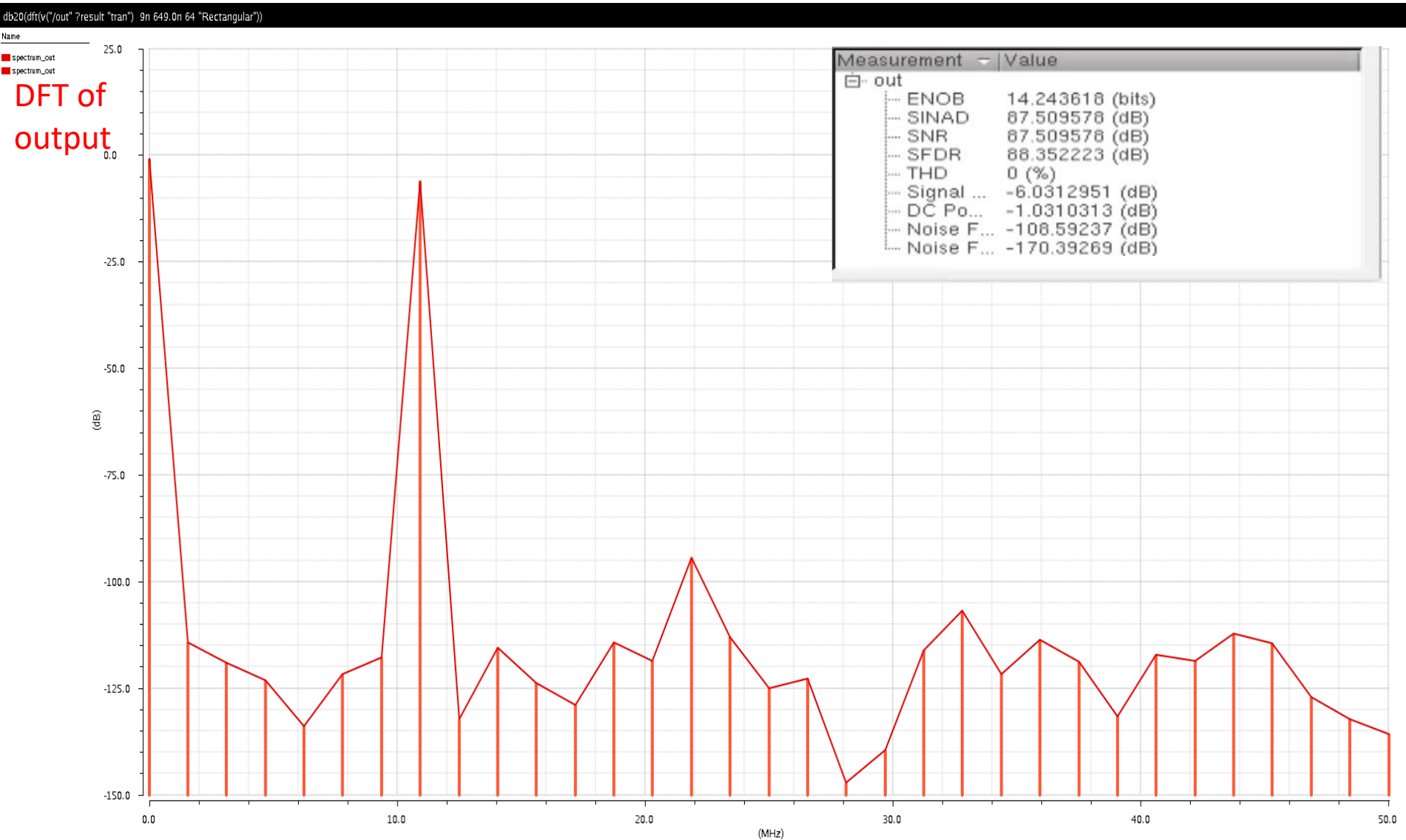
Waveforms

Max size for best ENOB & performance

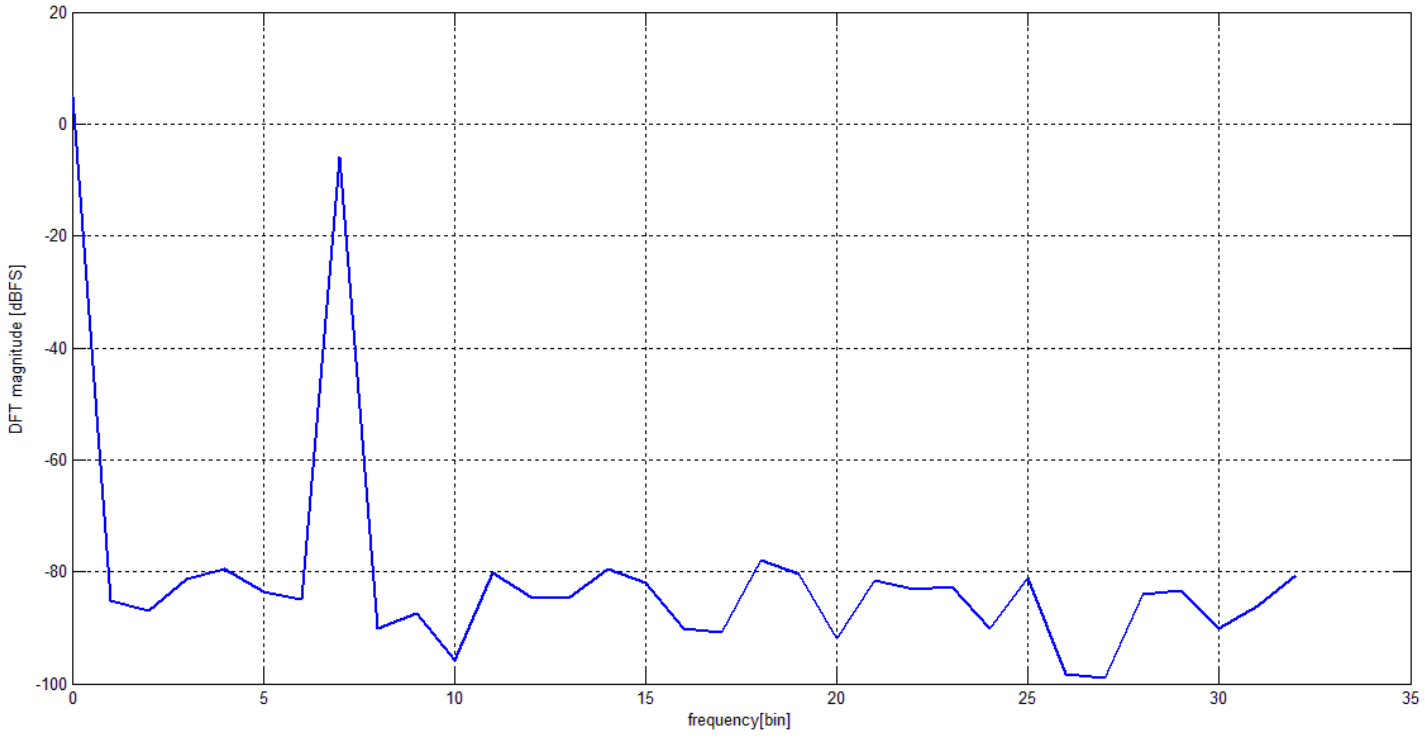
$$At\ \left(\frac{W}{L}\right)_{n1} = 34\ x\left(\frac{320nm}{150nm}\right)$$



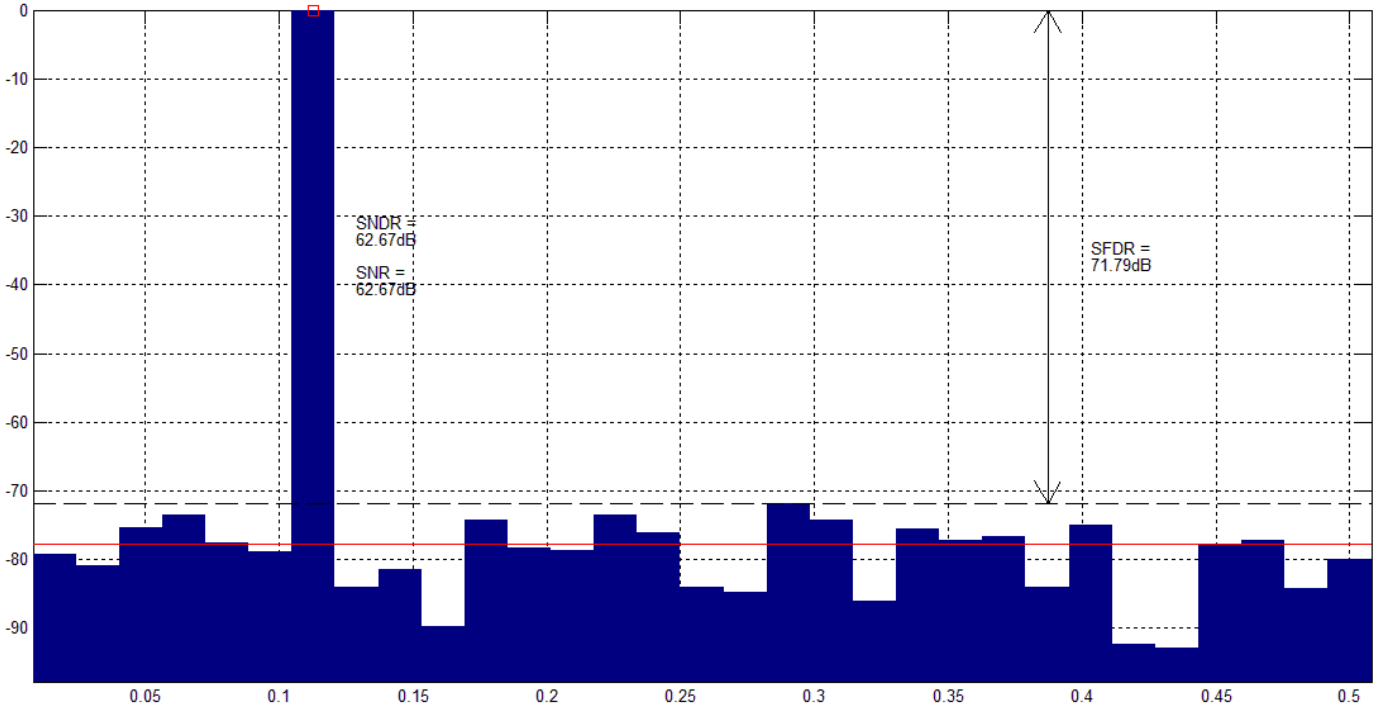
DFT of output



DFT of output (MATLAB)

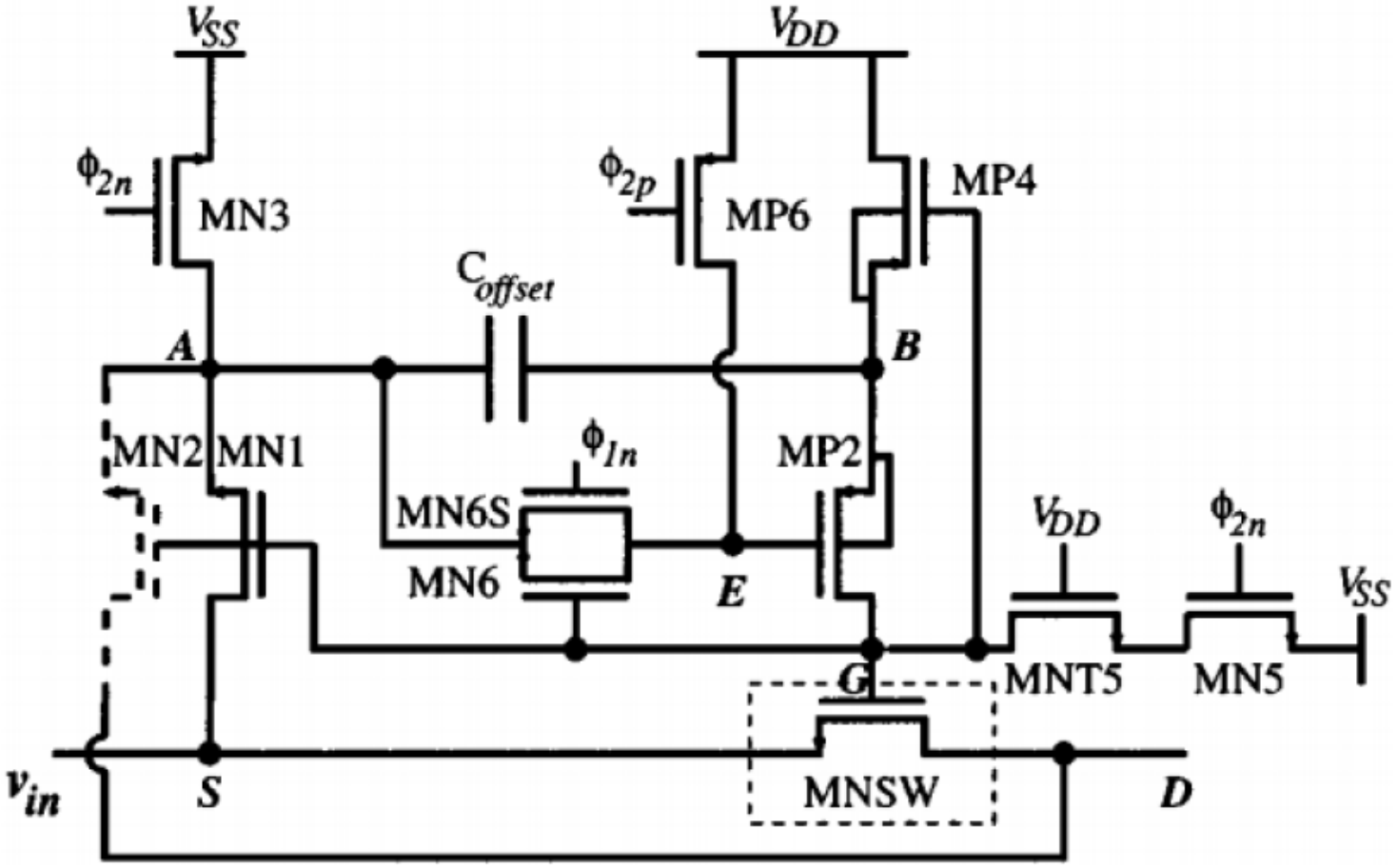


Using PrettyFFT function



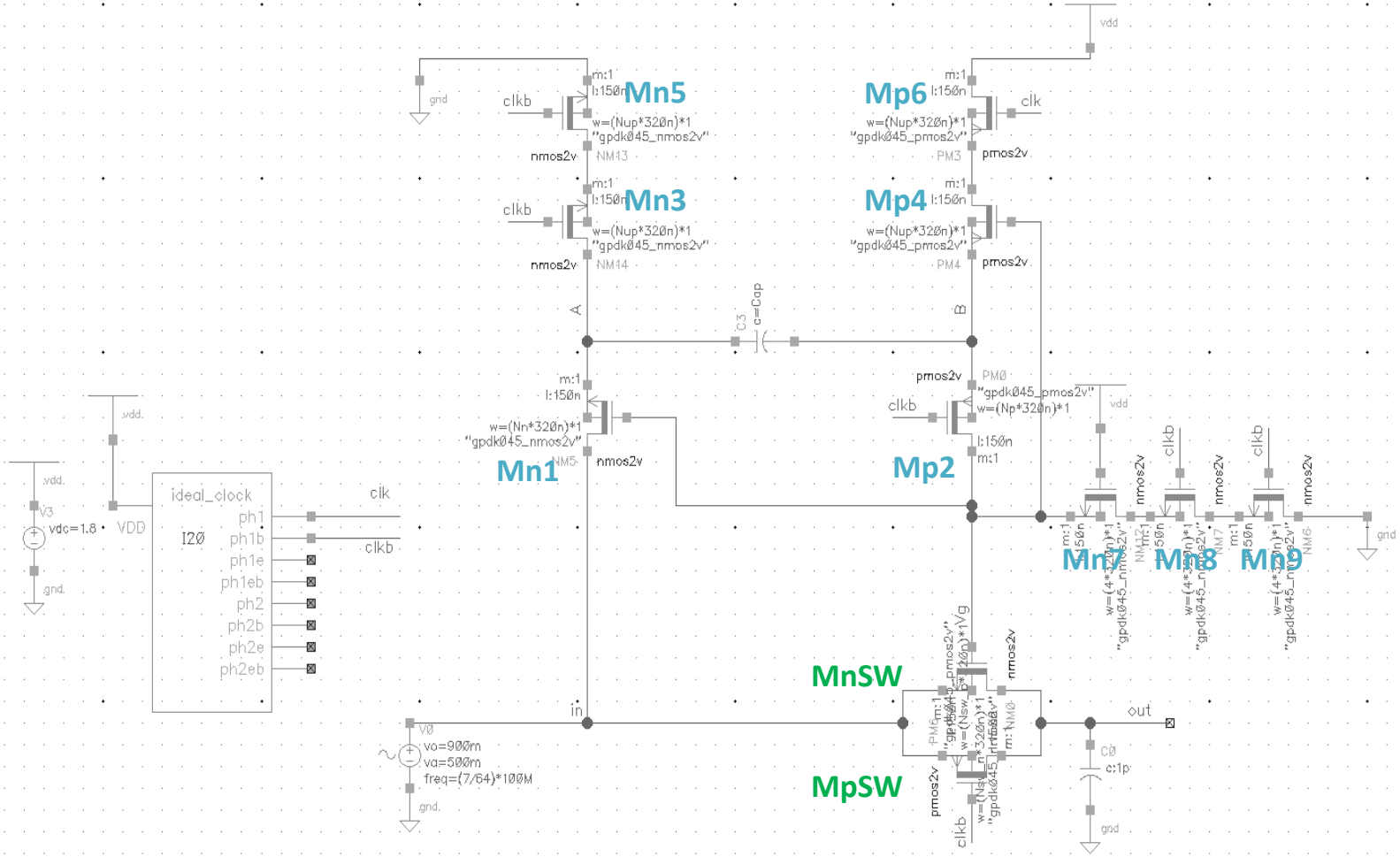
(4)
S/H Using Bootstrapped Circuit
b) Topology 1

Original Circuit



Mohamed Dessouky and Andreas Kaiser, "Very Low-Voltage Digital-Audio ΔΣModulator with 88-dB Dynamic Range Using Local Switch Bootstrapping", *IEEE J. Solid-State Circuits*, vol. 36, pp. 349–355, Mar. 2001

Implemented Circuit



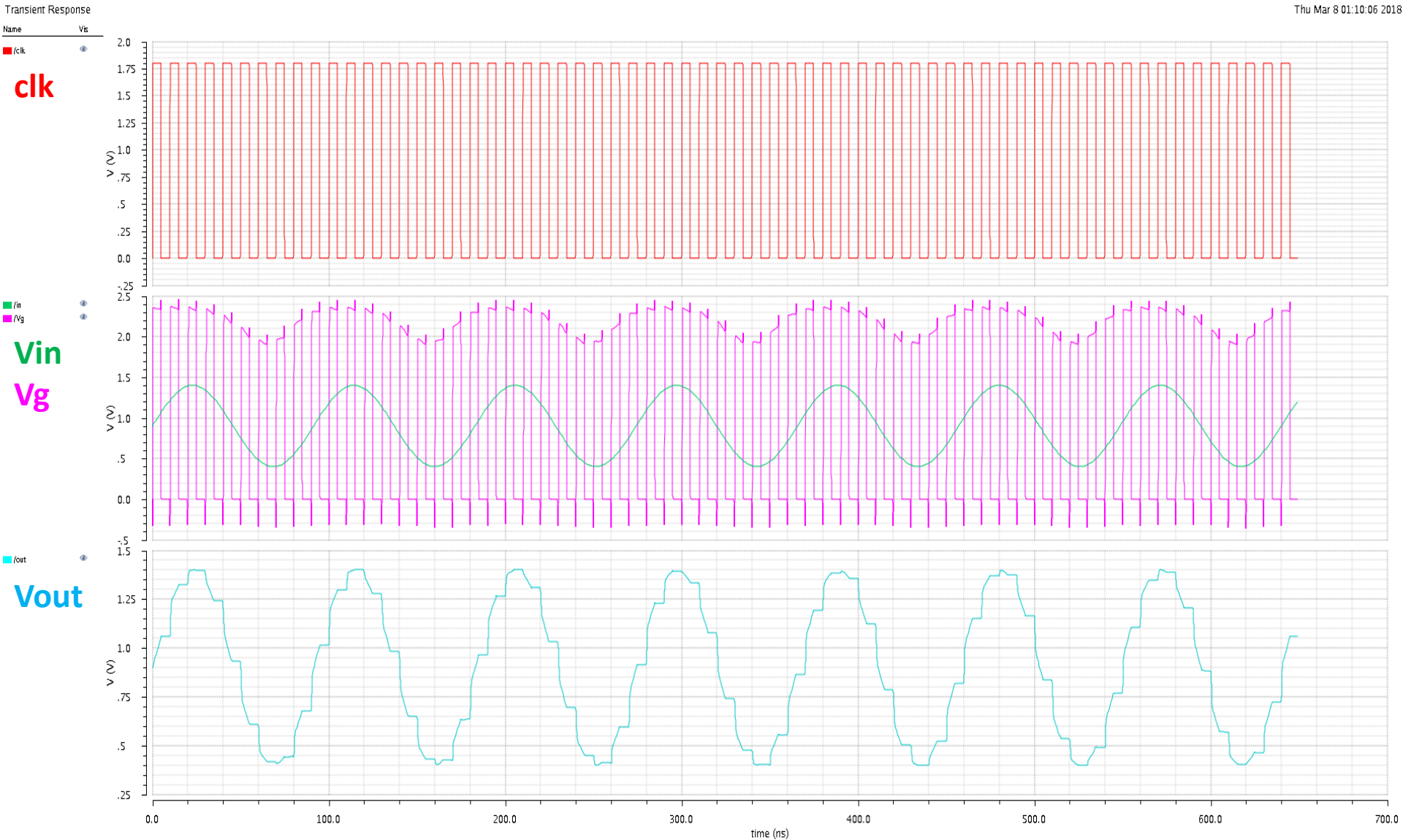
Sizing & Modifications

1. **Mn3,Mp4** are added to decrease charge sharing, by separating nodes A & B of the offset Cap from the parasitic Cap of Mn5,Mp6 that are directly connected to the rails (when Mn5,Mp6 are off).
2. **Mn1,Mp6** have their gates connected to Vg node, since this node goes from gnd in clkb phase, to the highest potential in the circuit in clk phase. Thus causing Mn1,Mp6 to turn on & off much better.
3. **Mn8** is added to decrease charge sharing, by separating gate node Vg of MnSW from the parasitic Cap of Mn9 that is directly connected to gnd when Mn9 is off.
4. **MpSW** is added to assist MnSW when Vin is high & to decrease the equivalent resistance of the switch (the ENOB of the system increases from ~9.7 bits to ~ 10.6 bits).

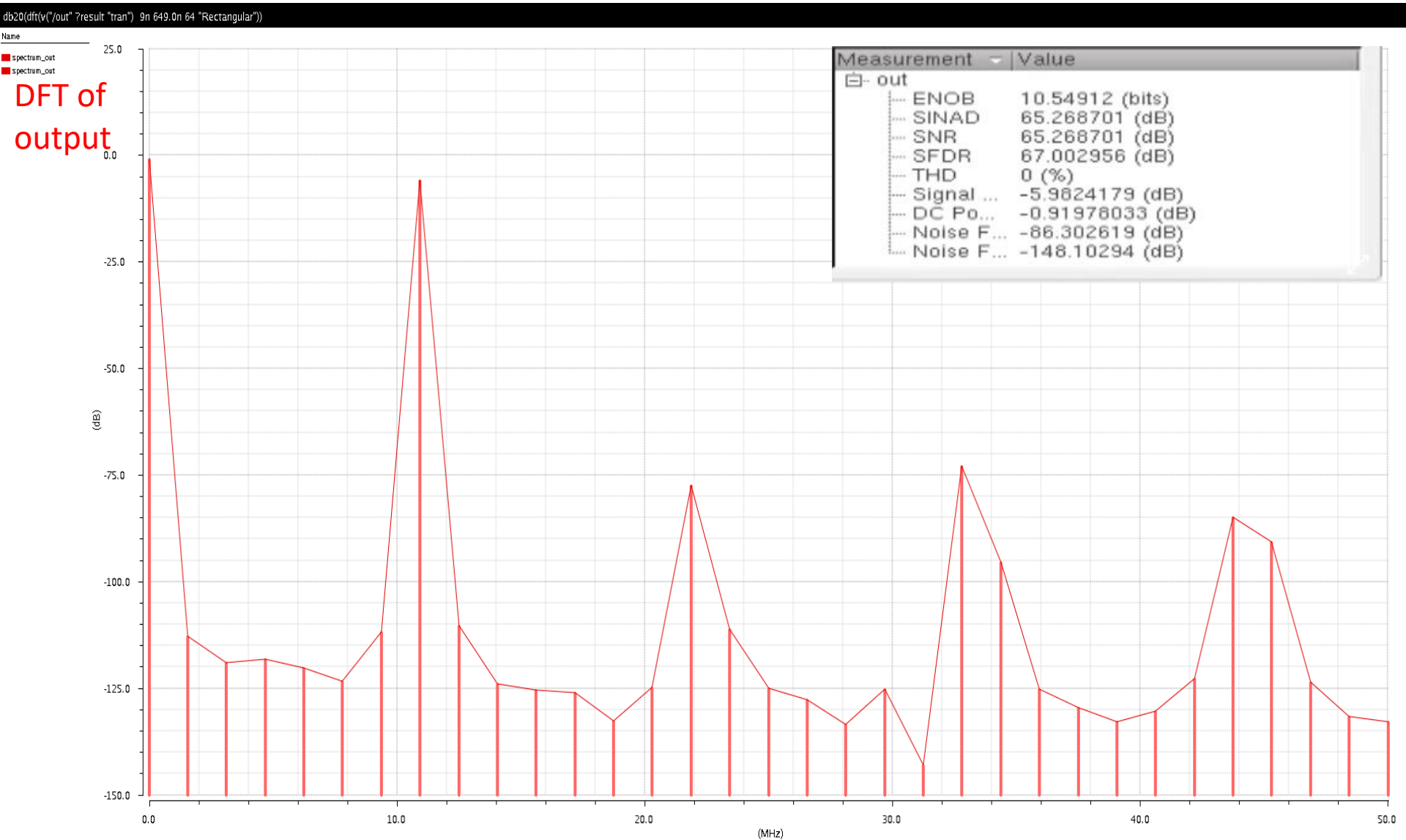
➔ Sizing:

Device	Size
MnSW	**15** * (320n/150n)
MpSW	**14** * (320n/150n)
Mn1	**4** * (320n/150n)
Mp2	**1** * (320n/150n)
Mn3,Mn5,Mp4,Mp6	**1** * (320n/150n)
Mn7,Mn8,Mn9	**4** * (320n/150n)
Offset Cap, Load Cap	**1pF**

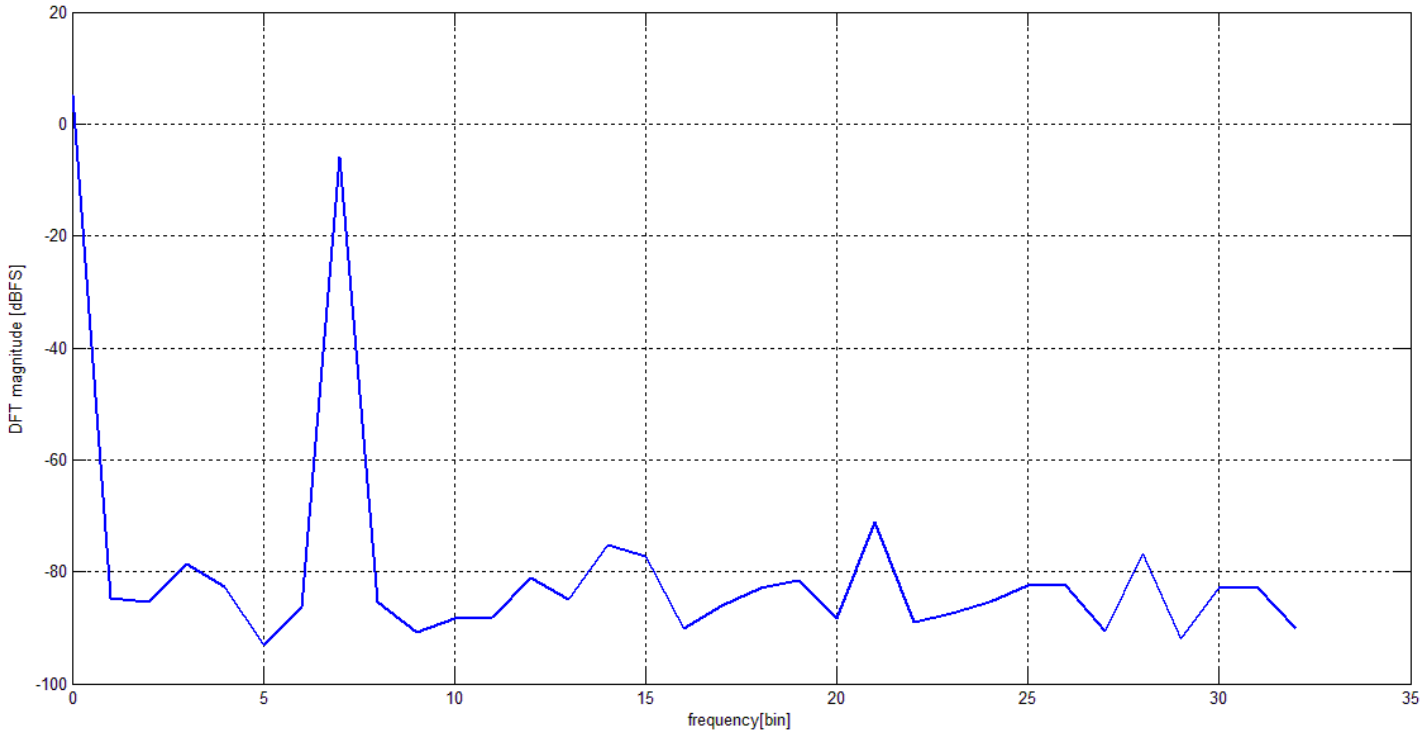
Waveforms


Transient Response
Thu Mar 8 01:10:06 2018
Name
Vis
/clk
clk
/in
/Vg
Vin
Vg
/out
Vout
V (V)
time (ns)
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0

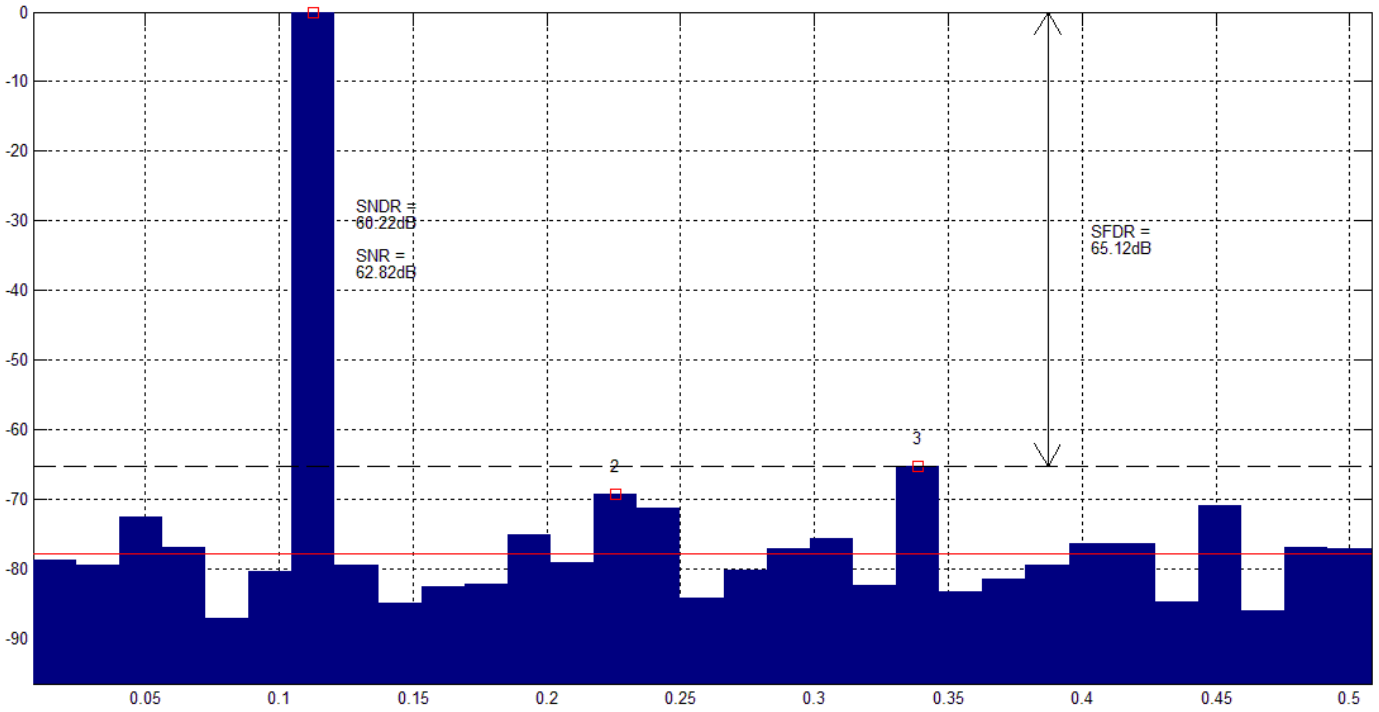
DFT of output



DFT of output (MATLAB)

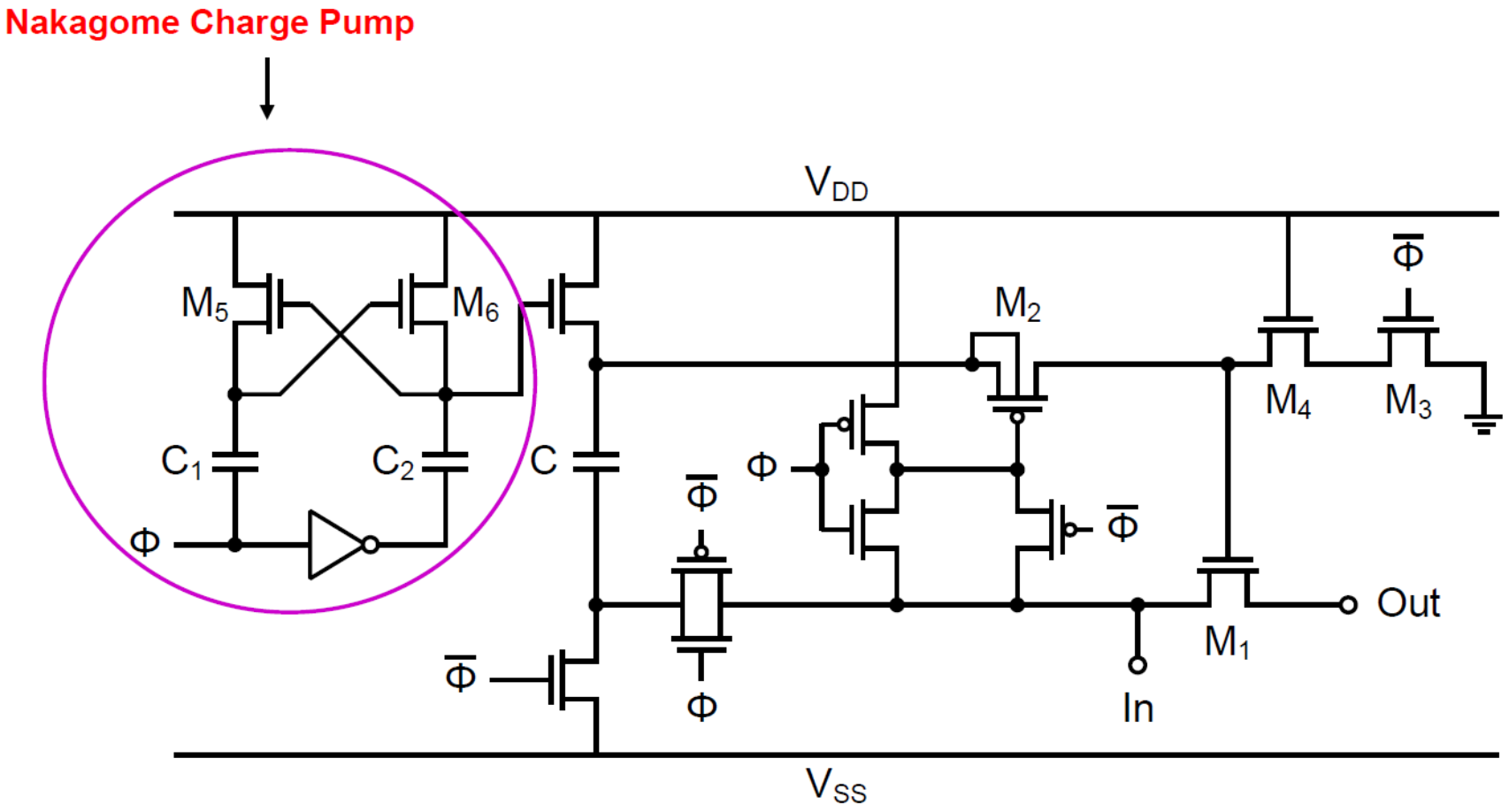


Using PrettyFFT function



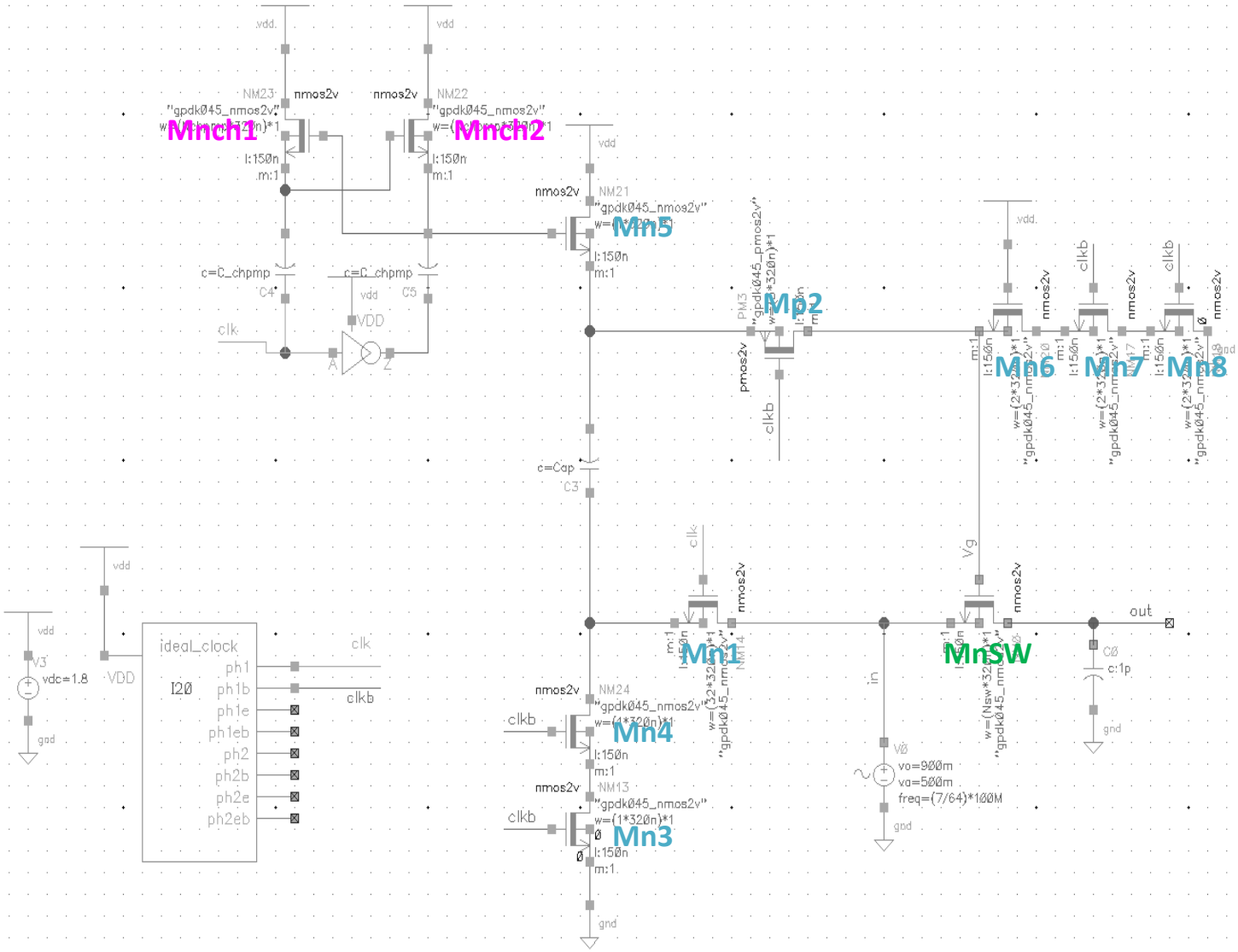
(4)
S/H Using Bootstrapped Circuit
c) Topology 2

Original Circuit



A. M. Abo and P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline ADC”, IEEE Journal of Solid-State Circuits, vol. 34, issue 5, pp. 599-606, 1999.

Implemented Circuit



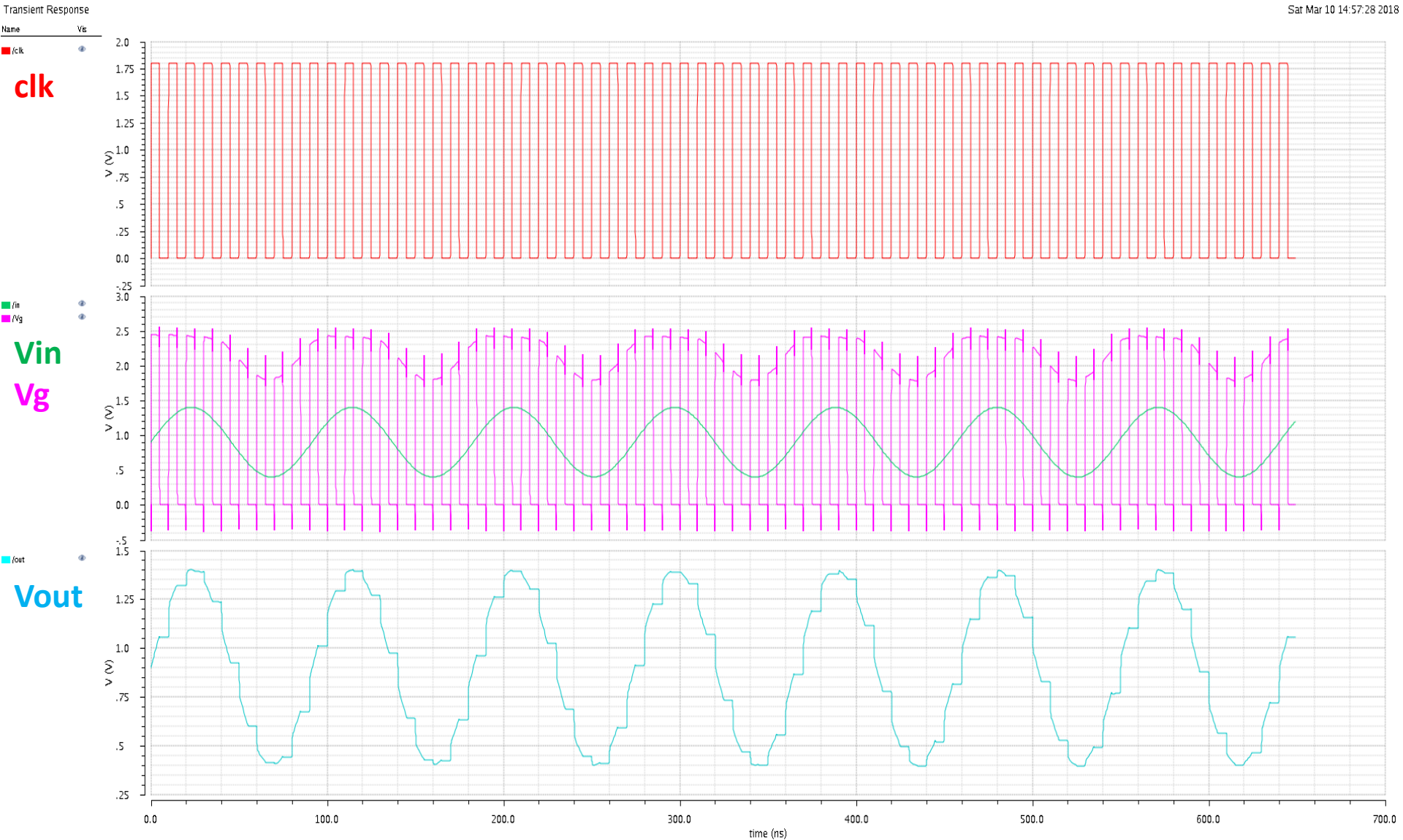
Sizing & Modifications

1. **A Charge Pump** is connected to the gate of Mn5 to keep Vgs of Mn5 to be much greater than Vth, & have a switch that can pass a strong VDD signal.
2. **Mn4** is added to decrease charge sharing, by separating the offset Cap from the parasitic Cap of Mn3 that is directly connected to gnd when Mn3 is off.
3. **Mn7** is added to decrease charge sharing, by separating gate node Vg of MnSW from the parasitic Cap of Mn8 that is directly connected to gnd when Mn8 is off.

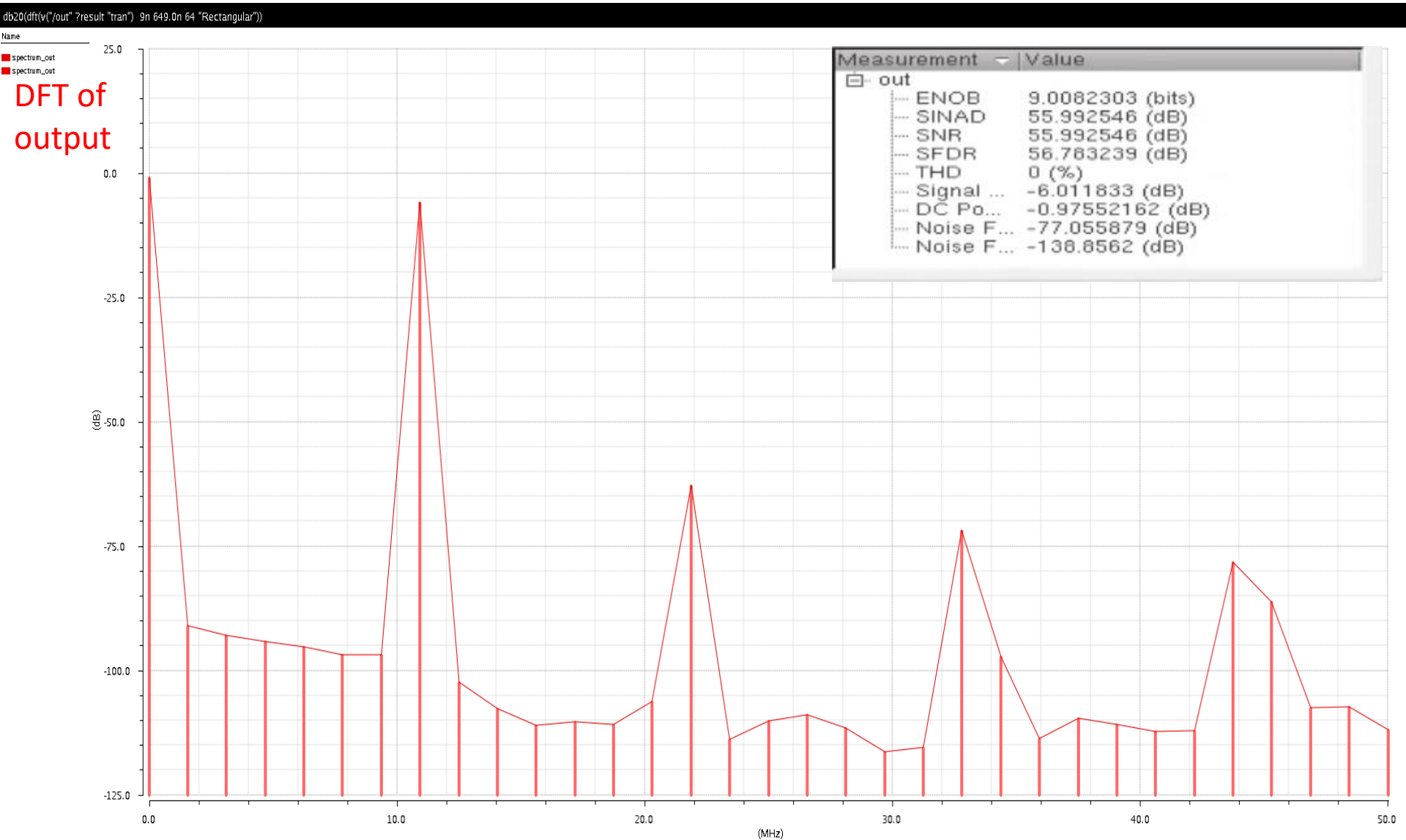
➔ Sizing:

Device	Size
MnSW	**30** * (320n/150n)
Mnch1,Mnch2	**10** * (320n/150n)
Mn1	**32** * (320n/150n)
Mp2	**3** * (320n/150n)
Mn3,Mn4,Mn5	**1** * (320n/150n)
Mn6,Mn7,Mn8	**2** * (320n/150n)
Ch Pump Caps, Load Cap	**1pF**
Offset Cap	**4pF**

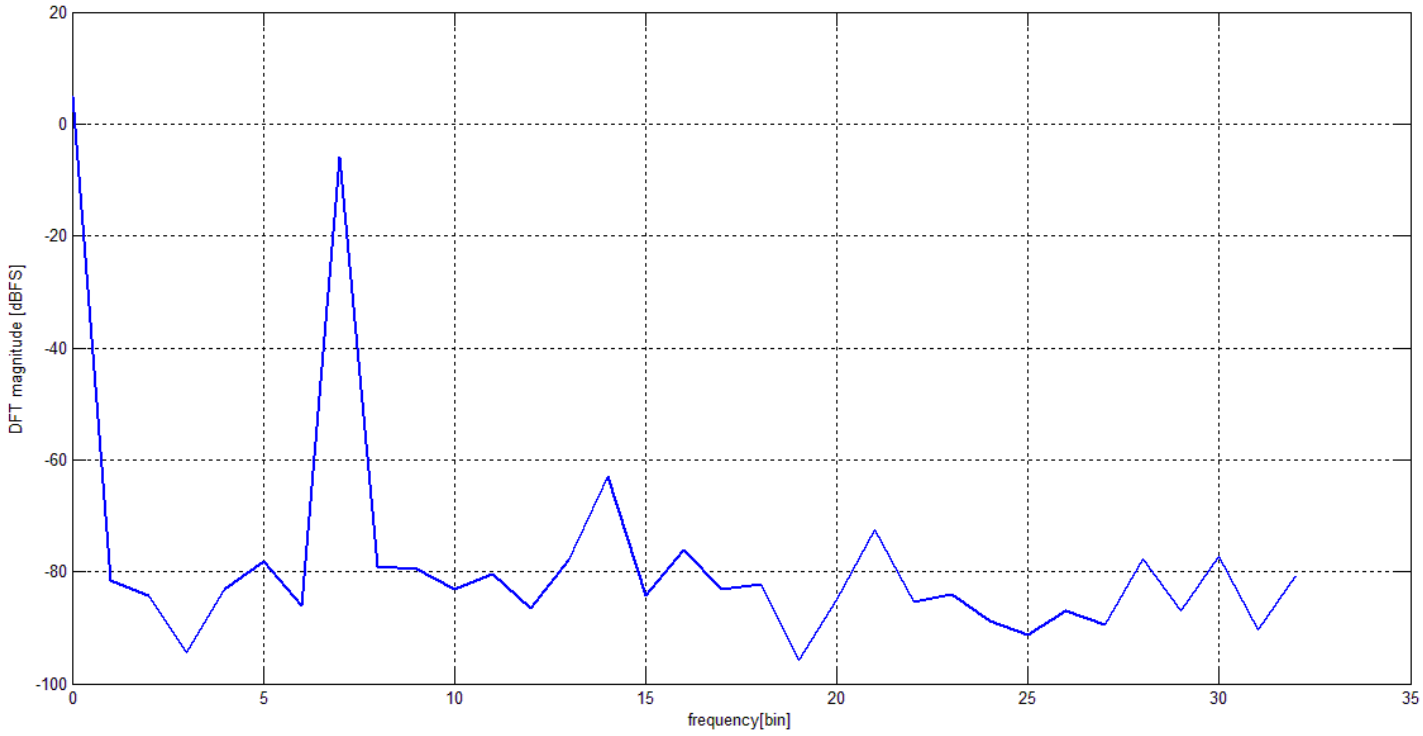
Waveforms


Transient Response
Sat Mar 10 14:57:28 2018
Name
Vis
/clk
clk
/in
/Vg
Vin
Vg
/out
Vout
V (V)
time (ns)
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0

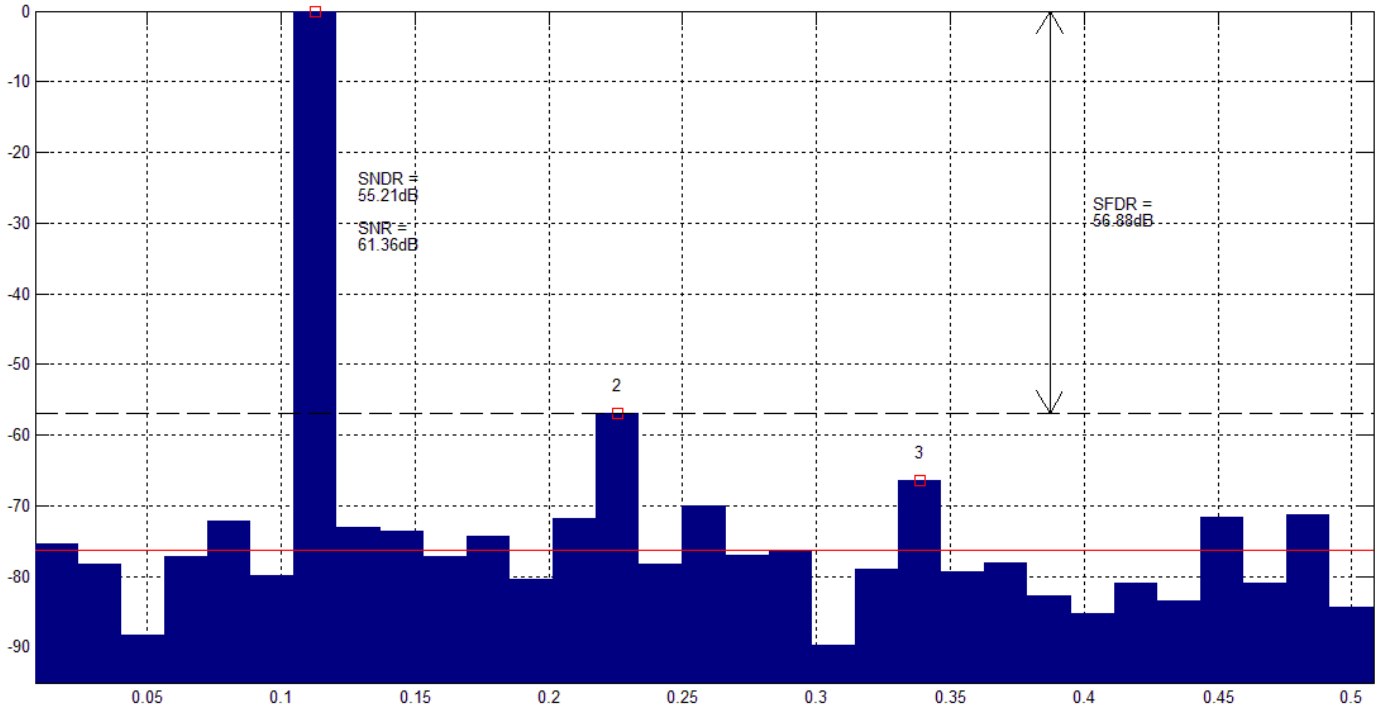
DFT of output



DFT of output (MATLAB)



Using PrettyFFT function



SUMMARY

- For Full-Scale input = 1V, from 0.4V to 1.4V:

	Ideal	NMOS Only	PMOS Only	Transmission Gate	Bootstrap (with ideal switches)	Bootstrap (topology 1)	Bootstrap (topology 2)
ENOB	15.51 bits	3.37 bits	3.44 bits	9.29 bits	14.24 bits	**10.55 bits**	9.01 bits
SNR	95.12 dB	22.07 dB	22.49 dB	57.71 dB	87.51 dB	**65.27 dB**	55.99 dB
SFDR	102.85 dB	25.04 dB	25.35 dB	59.01 dB	88.35 dB	**67.00 dB**	56.78 dB

* These are the best performances I was able to achieve for each case, after careful sizing of all the devices.

SUMMARY

- For Full-Scale input = 0.5V, from 0.65V to 1.15V:

	Ideal	NMOS Only	PMOS Only	Transmission Gate	Bootstrap (with ideal switches)	Bootstrap (topology 1)	Bootstrap (topology 2)
ENOB	15.01 bits	6.62 bits	6.59 bits	8.20 bits	13.90 bits	**12.29 bits**	10.10 bits
SNR	92.13 dB	41.63 dB	41.29 dB	51.14 dB	85.43 dB	**75.76 dB**	62.56 dB
SFDR	96.36 dB	42.64 dB	42.91 dB	51.51 dB	88.84 dB	**77.95 dB**	63.27 dB

* These results are achieved by only changing the input full-scale. The same sizes as before are used.

SUMMARY

Observations:

- The Bootstrapped techniques are shown to increase the ENOB, SNR, & SFDR, improving the performance.
- There is a tradeoff while sizing (W/L) of the transistors; Increasing (W/L), decreases the Ron of the transistors, but increases at the same the parasitic capacitances of the transistors.

- The Matlab results show a greater noise floor level than that on Cadence in the cases where ideal switches were used.
  But the Matlab results are very close to that of Cadence in the NMOS/PMOS circuits & the Bootstrapped circuits.

- Decreasing the full-scale input, improves the circuit performance for all the cases, except the ideal circuits & the transmission gate circuit.