$W = F \times 10 \times 320nm$

$L = 10 \times 150nm$

NMOS

$V_{th} \simeq 0.413\ V$

$\beta_{eff} = \mu_n C_{ox} \left(\frac{W}{L}\right) \simeq 899.515\mu$

$K_n = 421.65 \frac{\mu A}{V^2}$

PMOS

$V_{th} \simeq 0.381\ V$

$\beta_{eff} = \mu_p C_{ox} \left(\frac{W}{L}\right) \simeq 306.97\mu$

$k_n = 143.66 \frac{\mu A}{V^2}$

$I_o = 10\mu A$

$ICMR+ = 1.5\ V$

$ICMR- = 0.3\ V$

$V_{Bias} = 0.9\ V$

$A_V \geq 100$

$BW \geq 1GHz$

3dB

cuz you will have a Latch

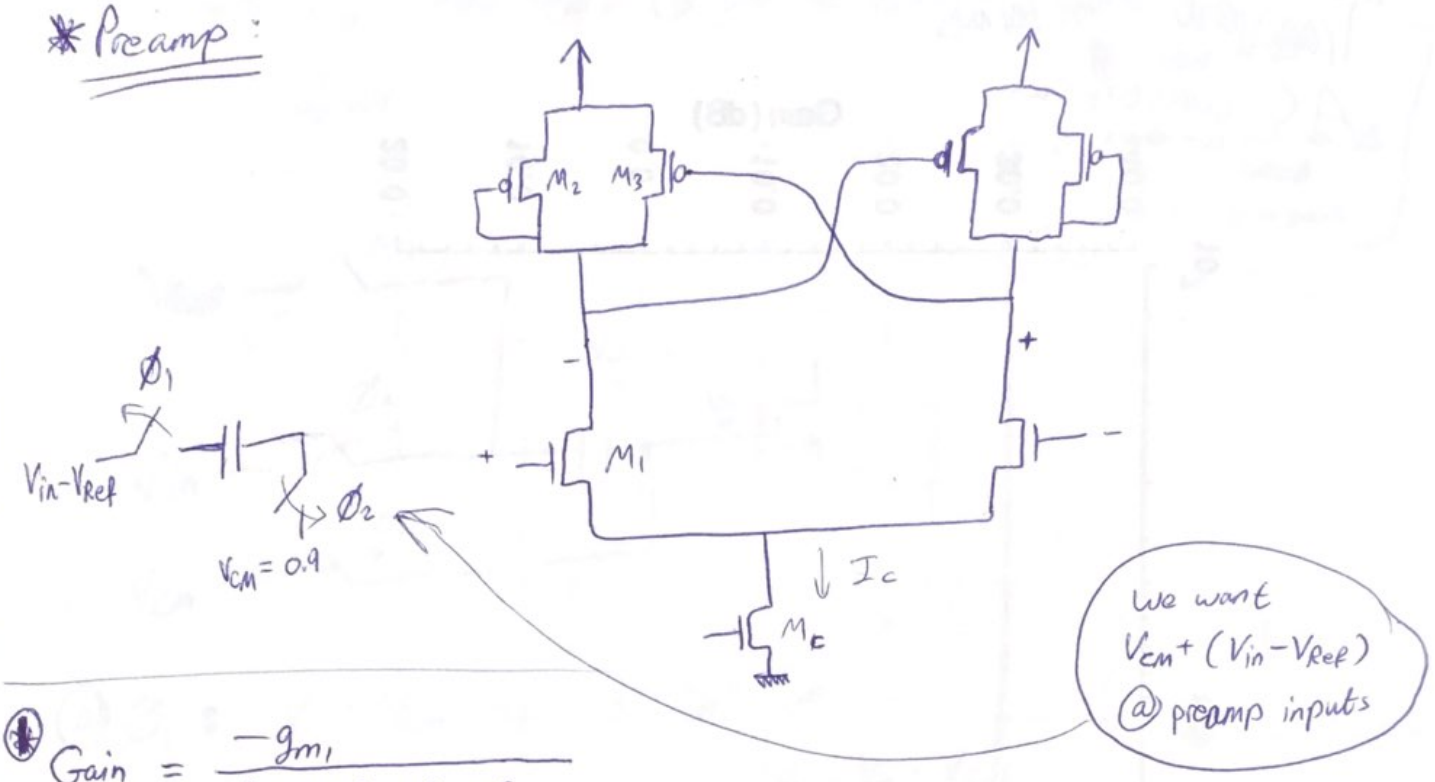
*For Preamp stage, Forget about gain (you're good with small gain)

↳ Speed (BW)

↳ Bias (CM)

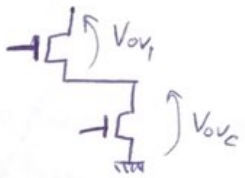
↳ must be able to give a differential output at $V_{CM} \simeq 0.4V$ & $1.4V$ (i/p rang) with $A_{mp_{min}} \simeq LSB$

* Preamp:



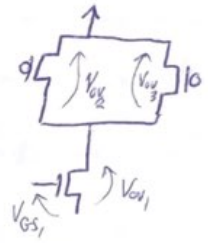
(1) $$\text{Gain} = \frac{-g_{m_1}}{g_{o_1}+g_{o_2}+g_{o_3}+g_{m_2}-g_{m_3}}$$

(2) $ICMR \geq V_{ov_C} + V_{ov_1} + V_{th_1}$



(3) $ICMR+ \leq V_{ov_{2 \text{ or } 3}} + V_{ov_1} - V_{GS_1}$

$V_{ov_{2 \text{ or } 3}} - V_{th_1}$



(4) $V_{ov_C} + V_{ov_1} < V_{out} < V_{ov_{2 \text{ or } 3}}$

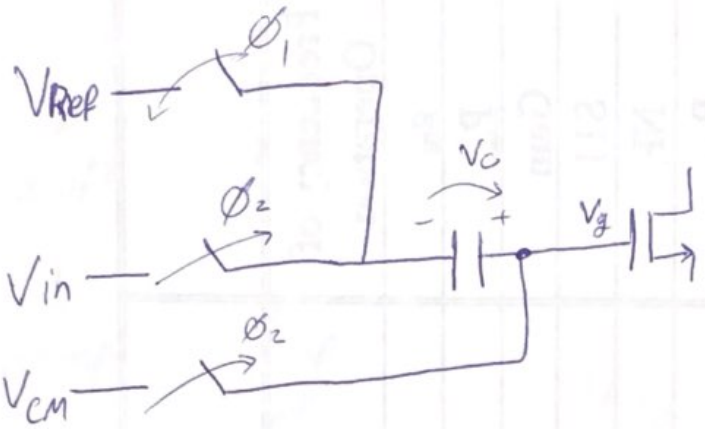
(5) $\text{Gain BW} = \frac{g_{m_1}}{C_L}$ → $\left(\frac{W}{L}\right)_1$, I_C

We want $V_{CM} + (V_{Ref} - V_{in})$ @ preamp inputs

↓ my bias

$V_{in} - V_{Ref} = \Delta$

$\Delta \xrightarrow[\text{preamp}]{\text{(-ve gain)}} -\Delta \xrightarrow[\text{latch}]{\text{(-ve gain)}} \Delta$



@ ϕ_1 : $V_C = V_{CM} - V_{in}$, $V_g = V_{CM}$

@ ϕ_2 : $V_C = V_{CM} - V_{in}$, $V_g = V_{CM} - V_{in} + V_{Ref}$

} So, design the circuit based on V_{CM} as the bias

* So, Now I am not including my V_{Ref} in the Biasing. ⤴
* I will also add a Cap. between the preamp & the latch to remove the output level DC but I want the output DC to be close to ~$V_{DD}/2$.

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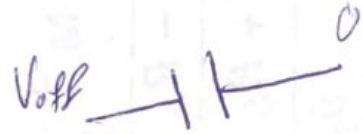
* Note: To increase the speed of preamp, you need to increase BW.
  ↳ In my circuit, inc. $(\frac{W}{L})$ of current tail to inc. "I".

latch is off → preamp ON

latch gives o/p → preamp OFF

$V_{inp} \rightarrow$ Comp $\rightarrow$



$0.9 + V_{in}$

$V_{off} + V_{in}$