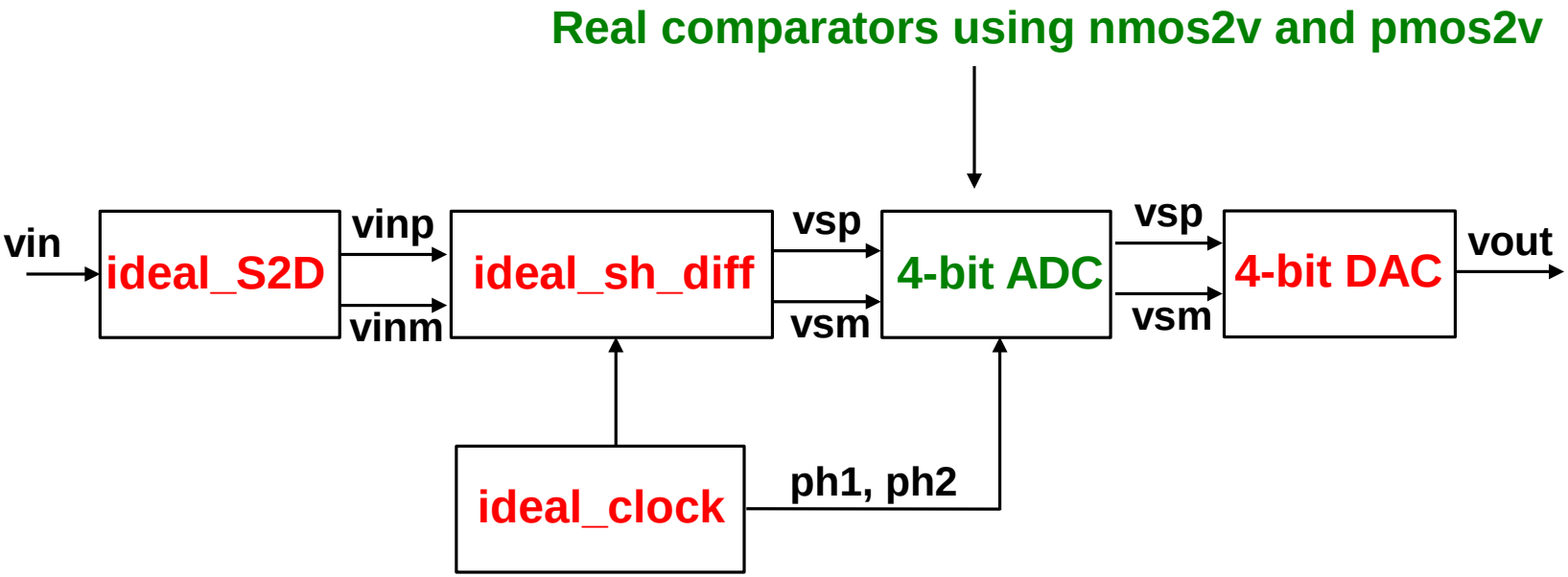
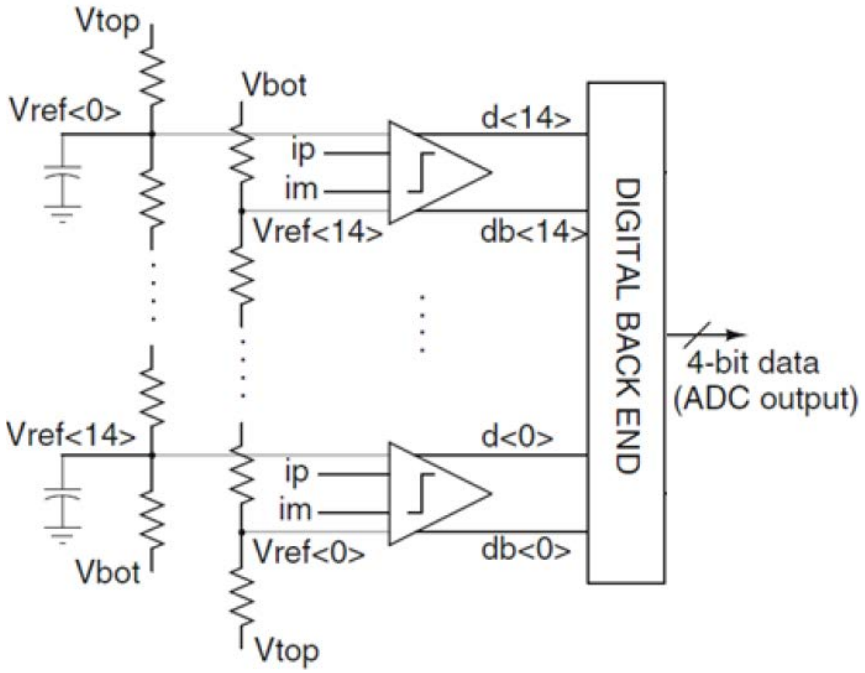
EE288 HW#4 : 4-bit Flash ADC

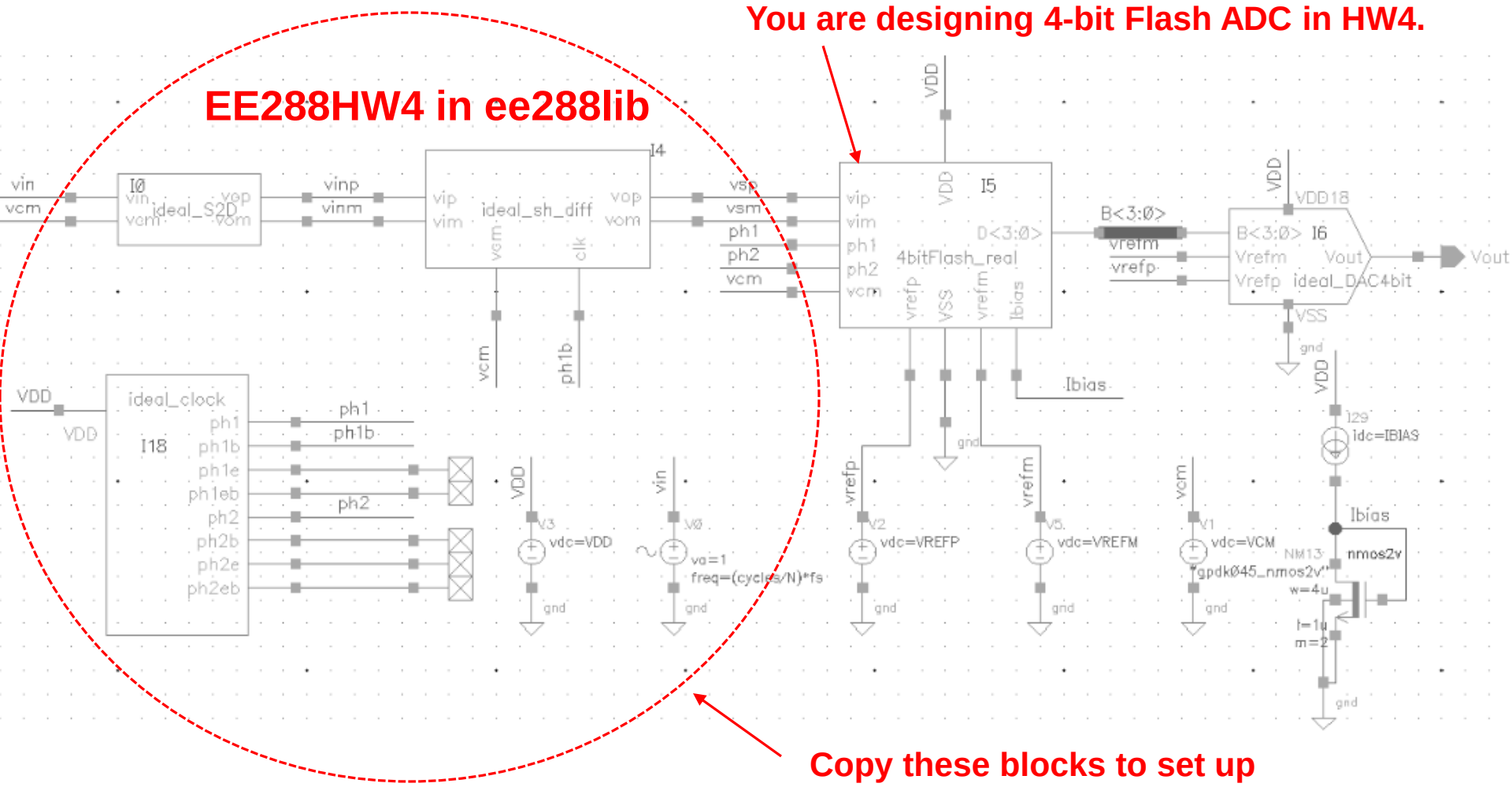


HW#4 : 4-bit Flash ADC



- Your goal is to minimize the ADC Figure of Merit given by
  FoM = Power / (fs*2^{ENOB}).
- Use ideal_swn, ideal_swp, ideal_clock, ideal_S2D, ideal_sh_diff from ee288lib

HW4 Simulation Test Bench – See EE288HW4 in ee288lib

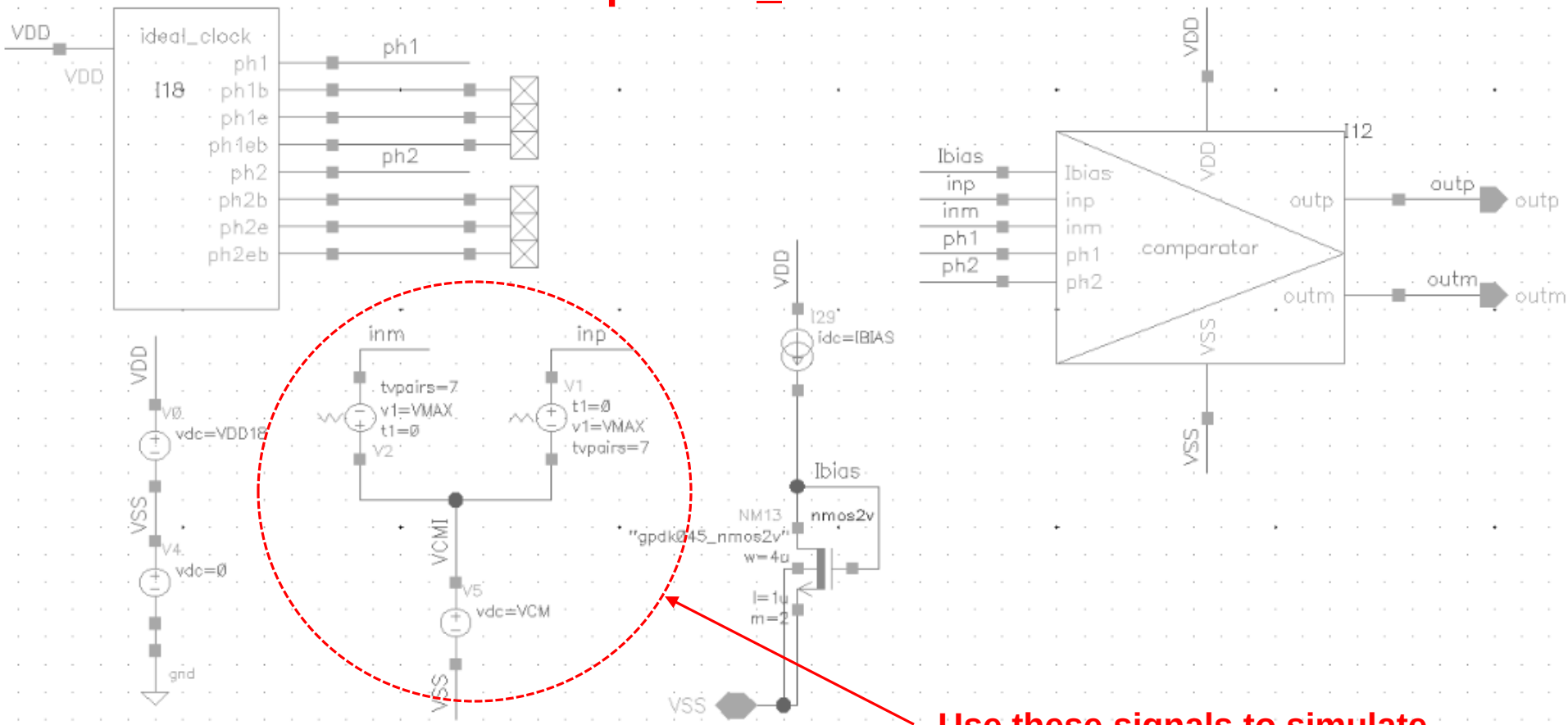


Comparator Test

- Key block in Flash ADC is Comparator.
- There are several options for comparator architectures.
- You will need a preamp + latch structure.
- The following slides show some options for preamps and latches.
- The output of the latch will be followed by a RS latch.
- Comparator overdrive test should show the output sequence 1011.
- See Comparator overdrive test bench in “comparator_tb” in ee288lib

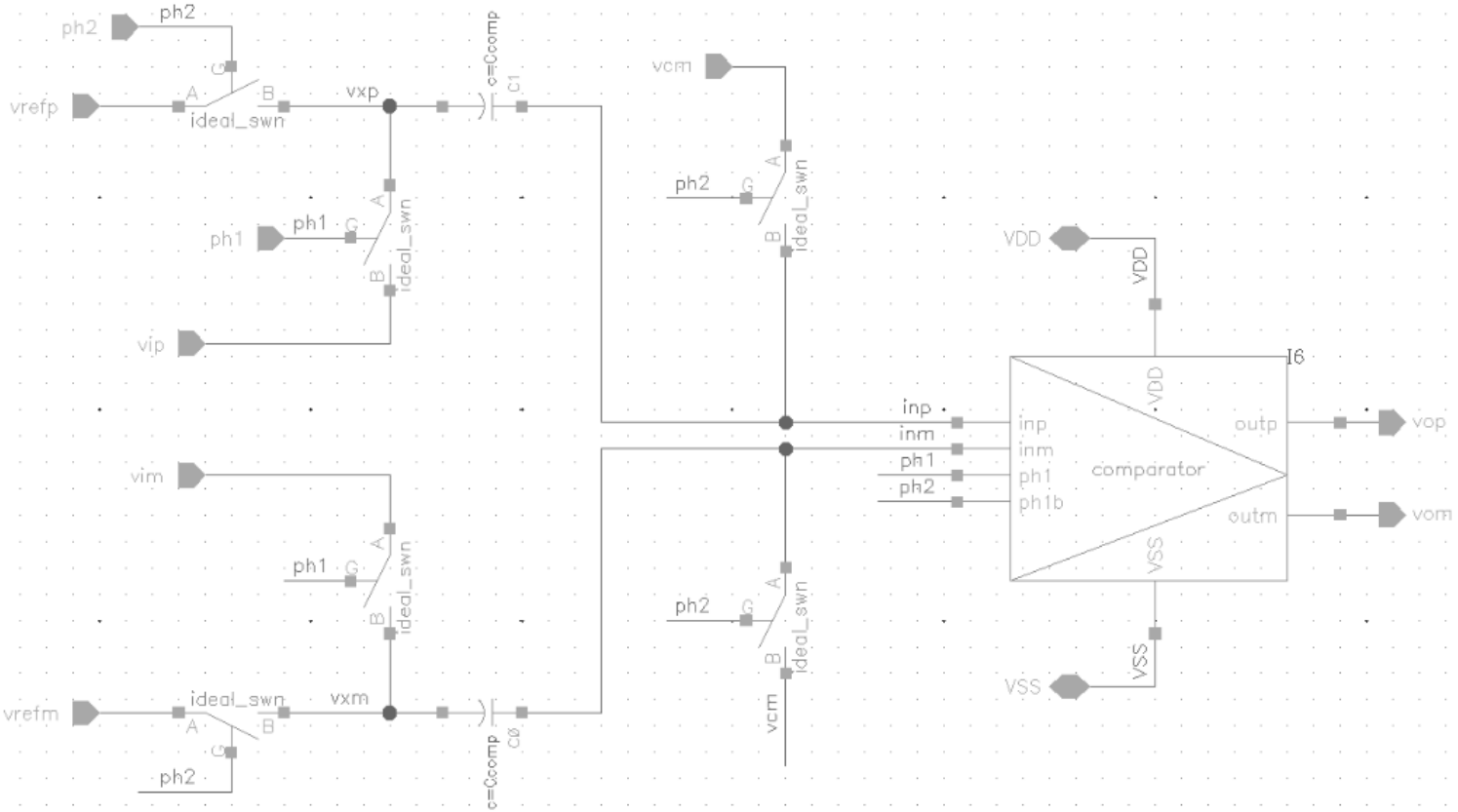
Comparator Overdrive Test Bench

comparator_tb in ee288lib

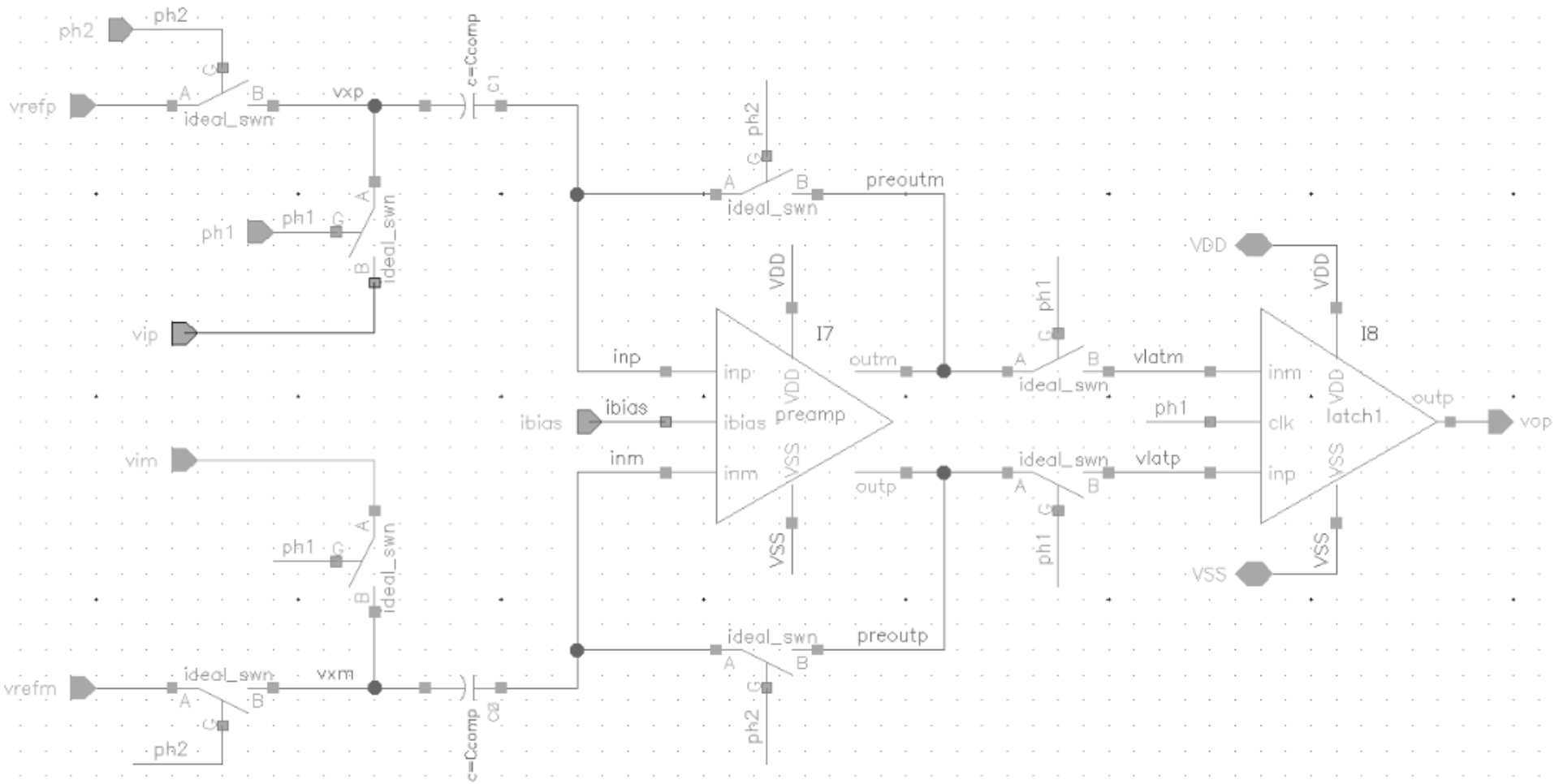


Use these signals to simulate The comparator overdrive test. VMAX=0.4, VMIN=10mV

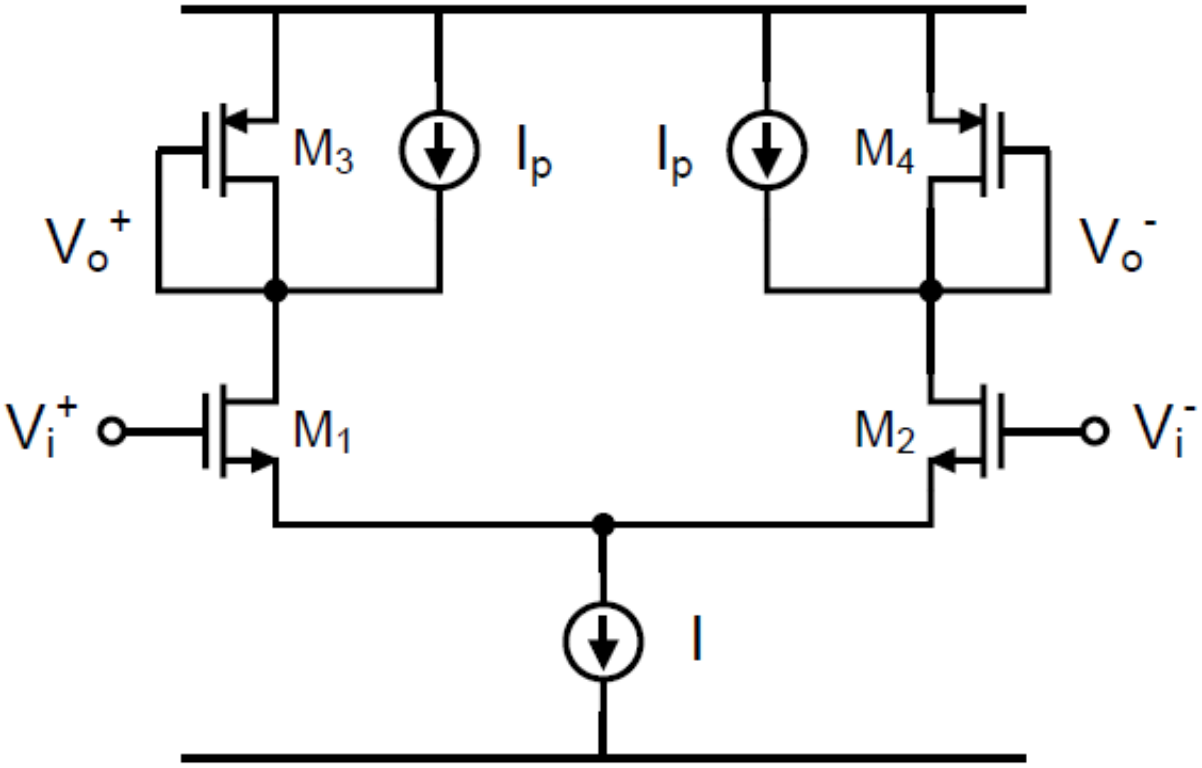
Comparator Architecture Option 1



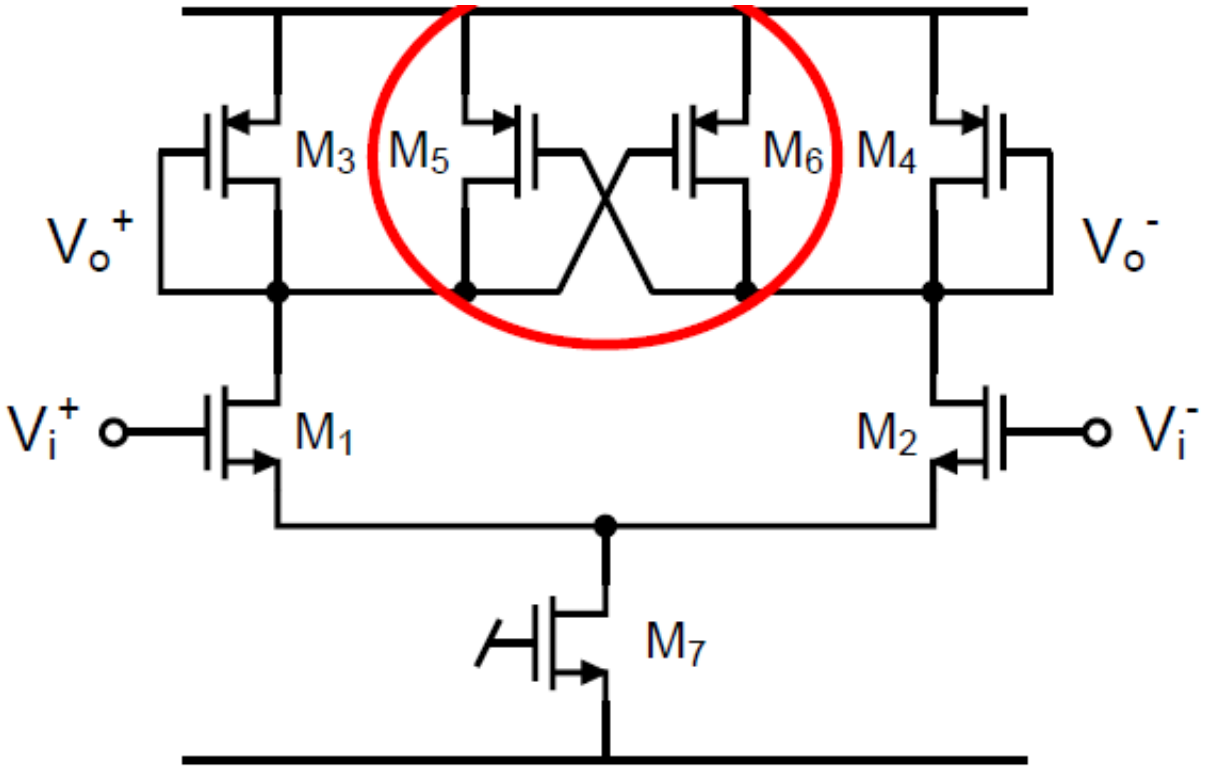
Comparator Architecture Option 2



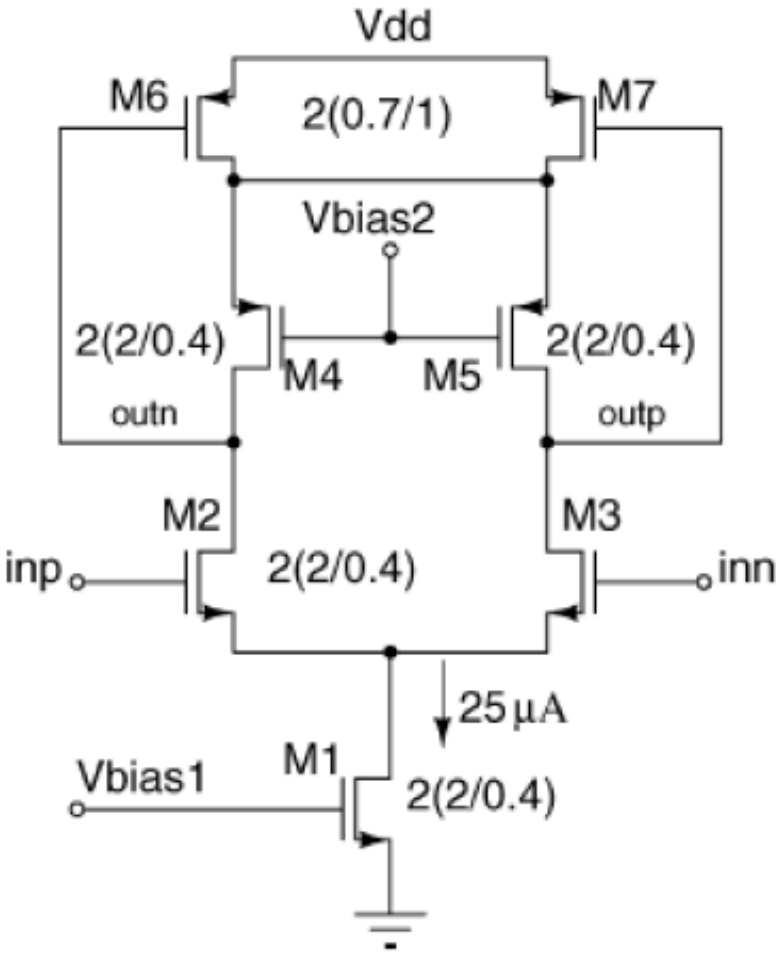
Differential Amplifier Example 1



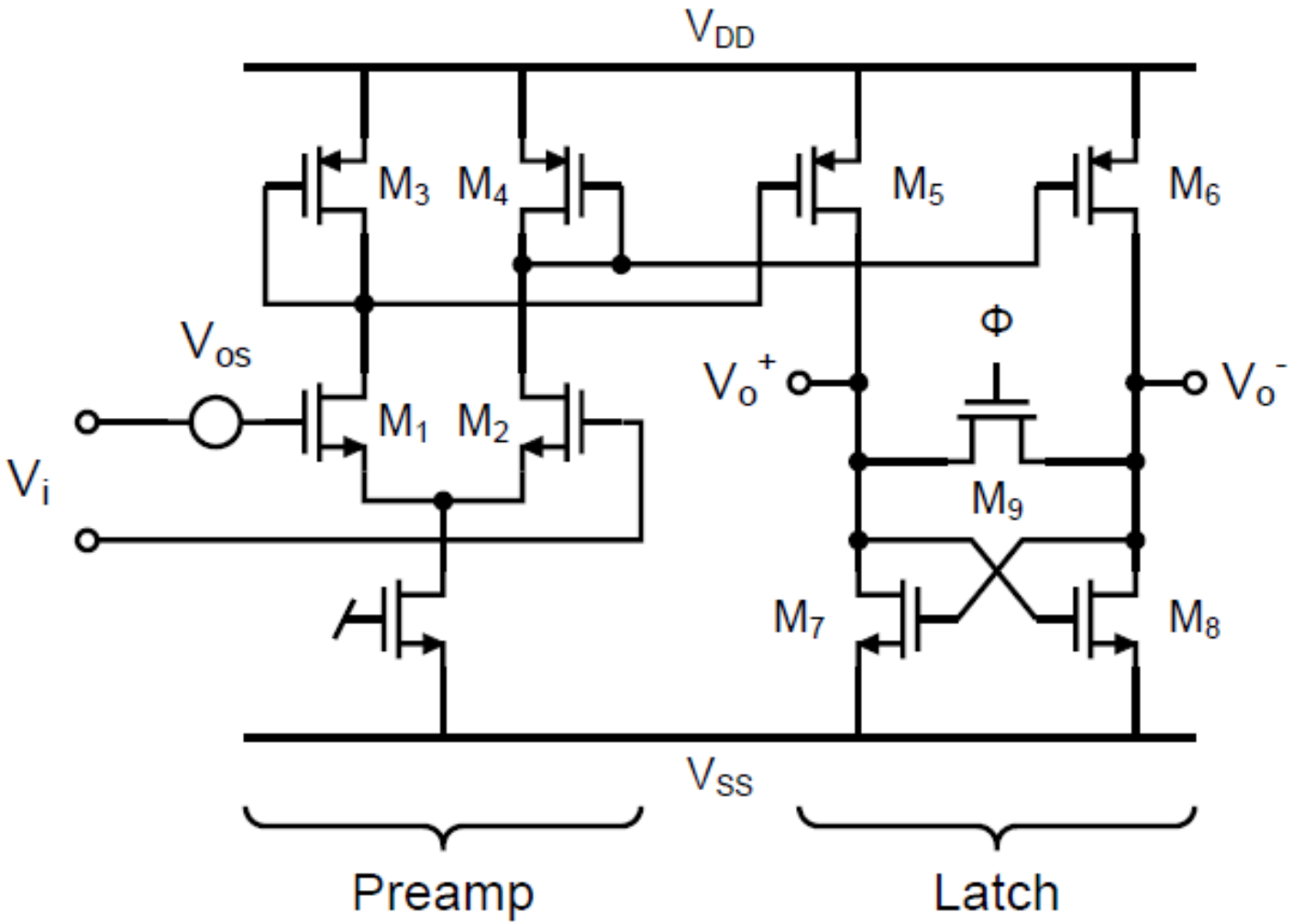
Differential Amplifier Example 2



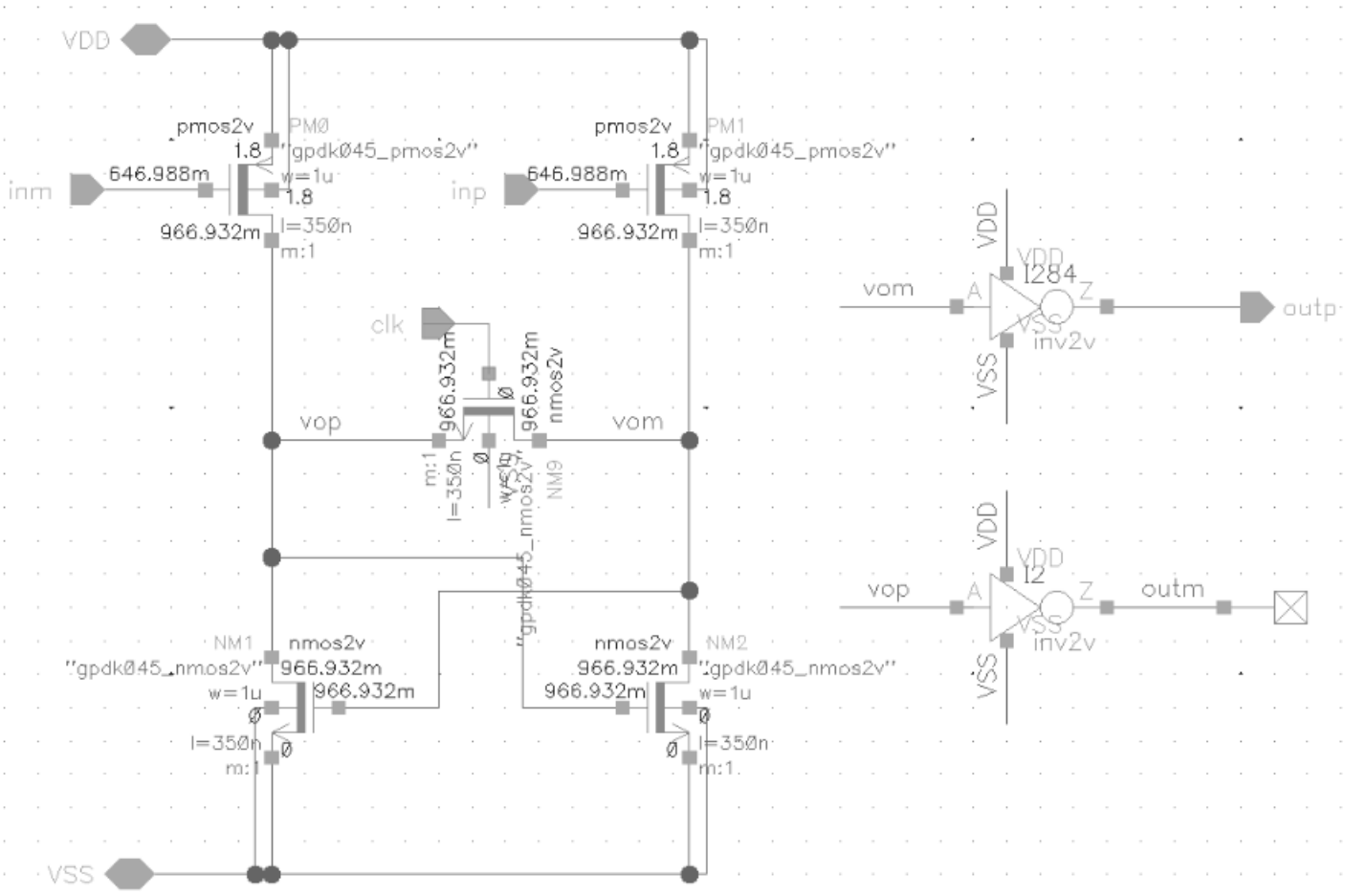
Differential Amplifier Example 3



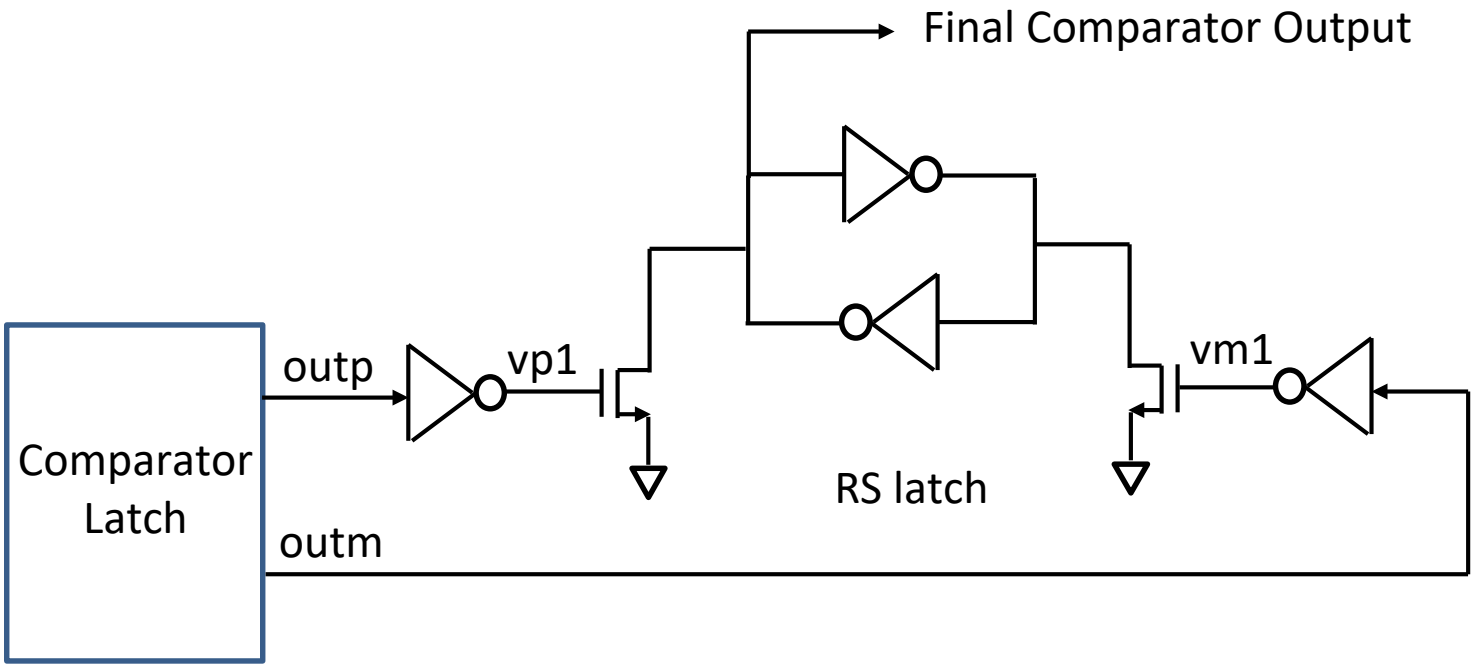
Latched Comparator Example 1



Latch Example 2

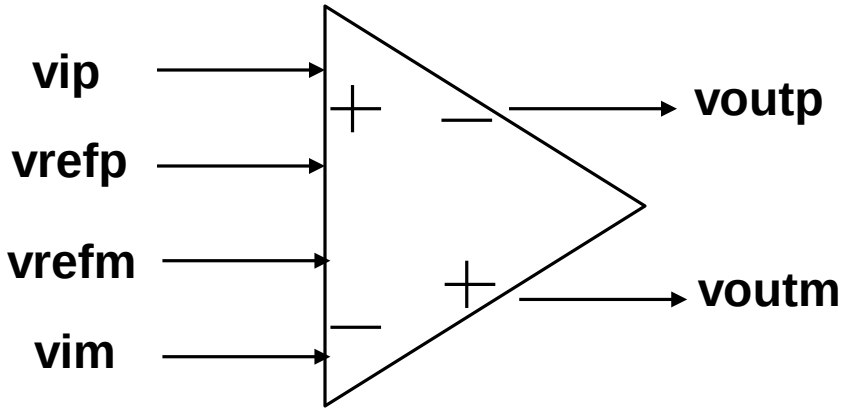


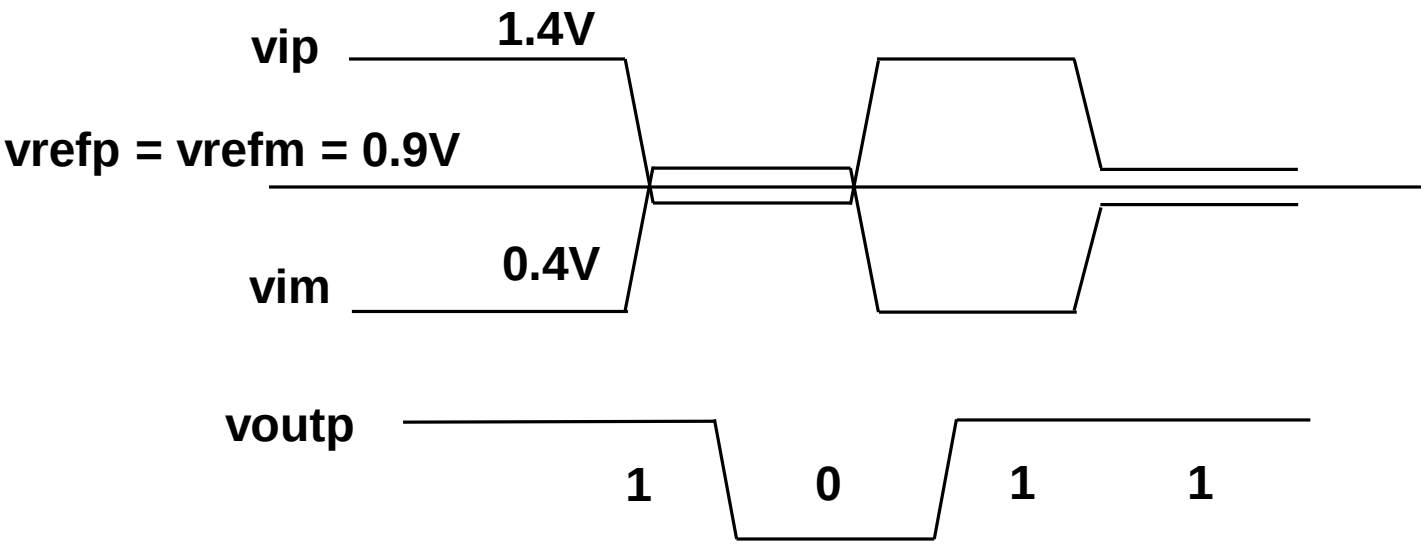
RS latch



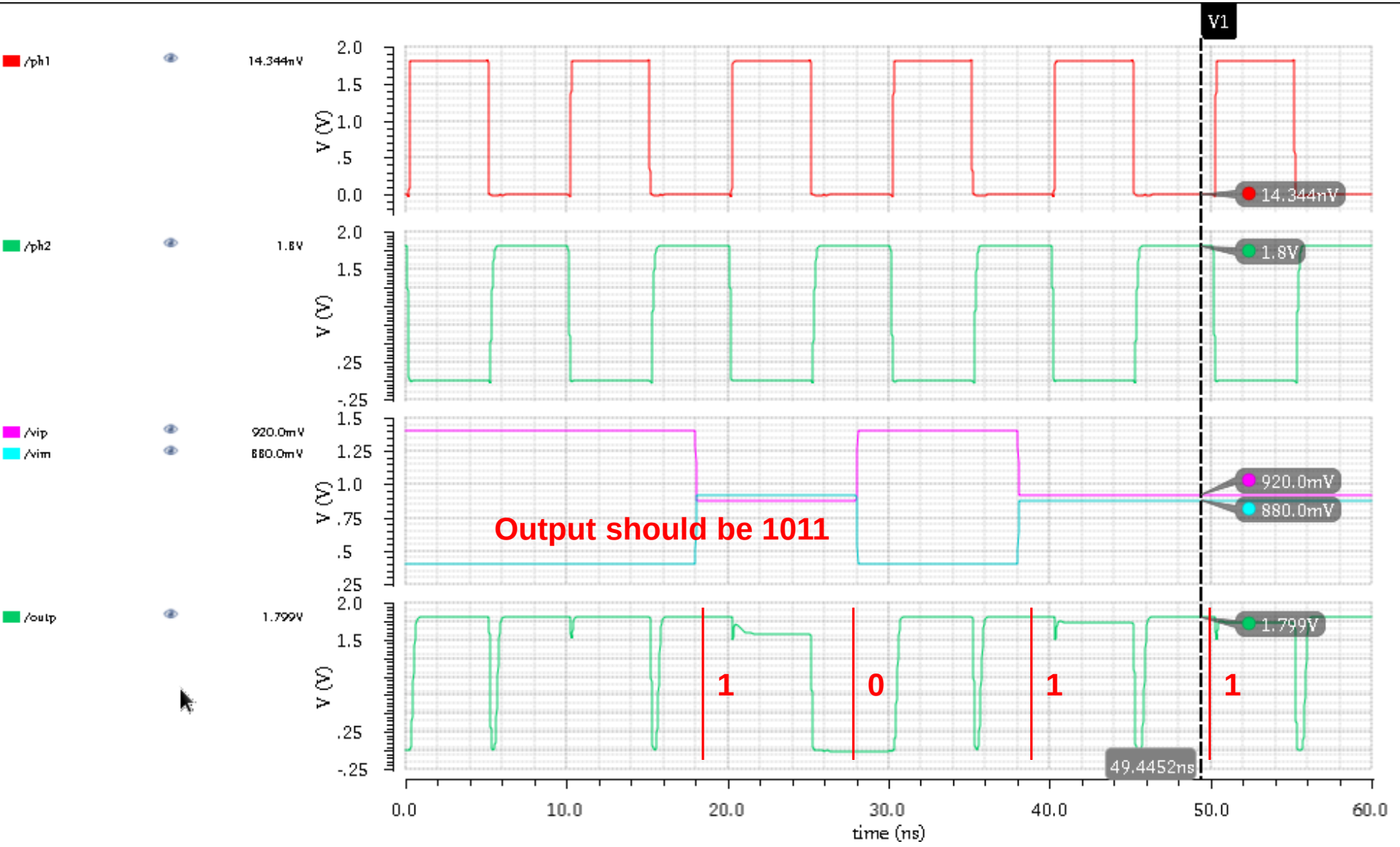
During ph2, comparator latch makes a decision.
During ph1, both comparator latch outputs (outp, outm) reset to VDD.
Then both vp1 & vm1 are low, thereby retaining previous outputs.

HW#4 : Comparator Overdrive Test Bench





Comparator Overdrive Test Result



4-bit Flash ADC Simulation Result