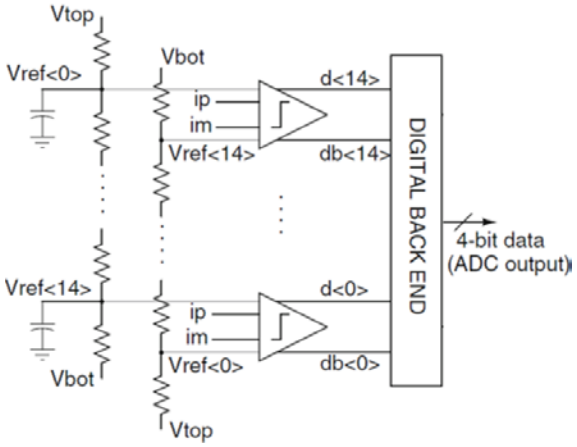
EE288 Homework #4 (5 points) Mar. 12, 2018

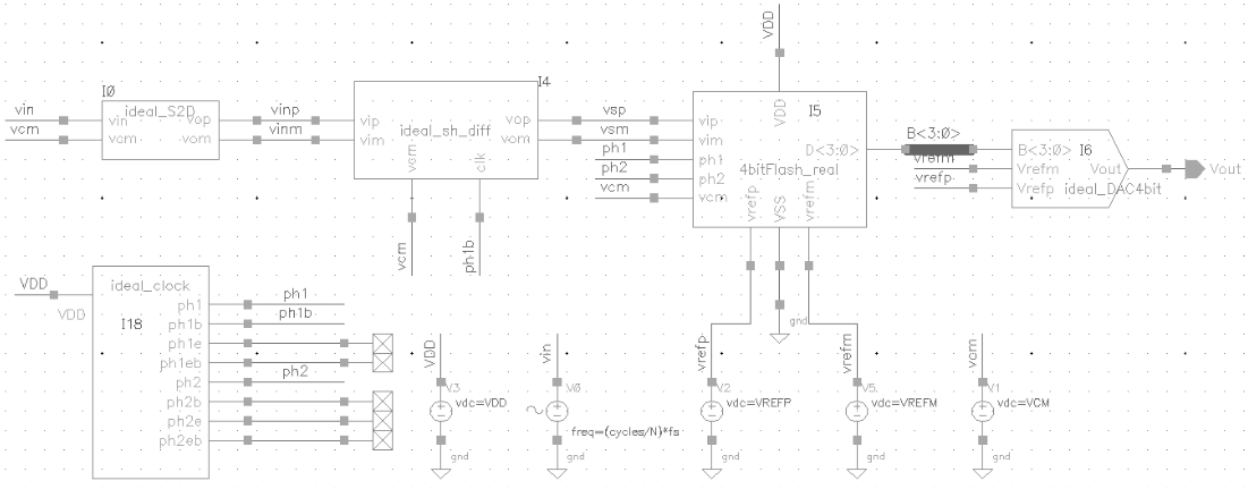
Due: April 2, 2018 6:00PM. Homework will not be received after due.
Homework submission file should be in pdf format and file name convention should be EE288HW4_yourname.

In this homework, you will build a 4-bit Flash ADC based on the following architecture where the comparator should be implemented using nmos2v and pmos2v. Your goal is to minimize the ADC Figure of Merit given by FoM = Power / (fs*2^{ENOB}).



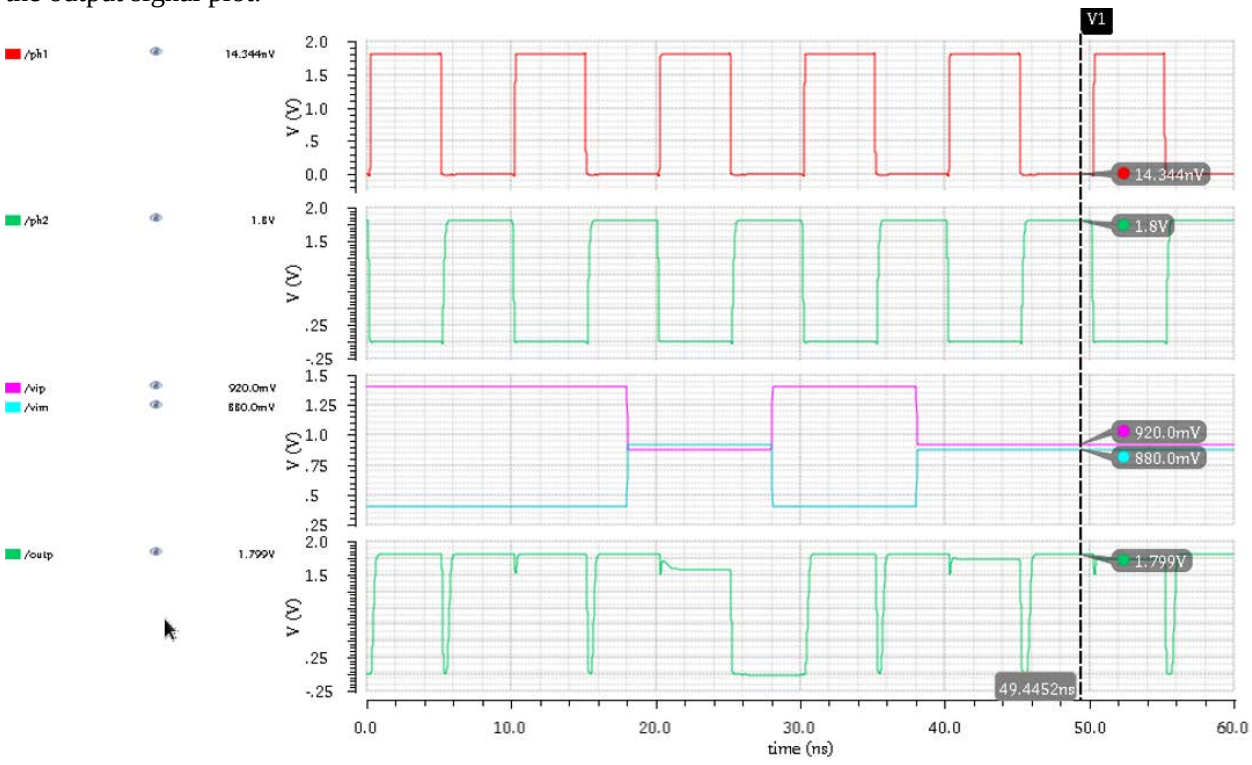
Assume the following design constraint.
VDD=1.8V
Vtop or Vrefp = 1.4V
Vbot or Vrefm = 0.4V
Input signal range 0.4V ~ 1.4V
Sampling clock pulse, fs = 100 MHz
Input signal frequency at fin = (cycles/N) * fs where cycles=7 and N=64 for 64-point FFT

Note that the input signal to the ADC is a differential signal (ip&im). Use ideal single-to-differential signal converter (ideal_S2D) and ideal S/H circuit (ideal_sh_diff) as well as ideal clock circuit (ideal_clock) in ee288lib to build a top-level schematic similar to the one shown below.



You can use ideal_swn, ideal_swp and an ideal 10 μA current source if necessary. You are free to choose any architecture to implement the comparator and the digital encoder as long as it works and helps to minimize the FoM.

To prove the functionality of the comparators used in the ADC, construct a separate comparator test bench circuit and apply a differential overdrive test signal (vip/vim) such as the one shown in below plot. The overdrive test is typically done by applying a maximum signal followed by a minimum signal with different sign. Result of the overdrive test should show an output sequence of 1011. Although the signal below shows a minimum differential signal of 40 mV (=920mV-880mV), you should try smaller differential signals to find out what the minimum signal the comparator can handle in overdrive test. Also, your comparator should be designed so that valid output is available when ph2 is high as you can see in the output signal plot.



To test the functionality of the ADC, build an ideal 4-bit DAC and apply a full-scale sinusoid to the input of the ADC and measure the result at the output of the DAC. Run a transient simulation for 700ns in Cadence Spectre and plot the transient waveforms for input and output signals along with clocks and other relevant signals in white background. Then plot a frequency spectrum of the DAC output using Cadence Spectrum measurement. Measure the power dissipation of each and every block as well as the total power dissipation of your ADC design as this is necessary to calculate the ADC FoM.

Summary of what you need to submit electronically:

1. Schematics of your design – use white background in monochrome (No color schematic)
2. Transient simulation results showing all relevant signal waveforms
3. FFT plot for the output of DAC
4. Summary of Power dissipation for each block, ENOB, SNR, SFDR, and FoM calculation result
5. Summary of what you have learned on this homework problem