# Analog IC design of high speed serial link transceiver for 10 GbaseKR standard using a 65 nm CMOS process

***Abstract*- This paper presents 10Gb/s transceiver design using 65nm CMOS process, the design is based on 10GBASE-KR standard. The transceiver employs several methods to improve the equalization. A 3-tap FFE CML transmitter is employed. An ADC based receiver is employed to optimize equalization control. Clock and data recovery is employed using a low power phase interpolator in a digital phase tracking loop. This paper also presents CTLE at the analog front end of the receiver.**

***Keywoeds*- High Speed Serial Links, Serializer, ADC, DAC, PLL, CDR, Phase interpolator**

## I. INTRODUCTION

The high demand for increasing the data transmission rate, for systems like backplanes and data routers, has introduced a lot of challenges like ISI and frequency dependent attenuation. Various equalization techniques has been introduced [1]. In order to utilize the benefits of scalability in digital design besides facing high complexity of designing analog circuits at such high rate with their hunger to power, this makes ADC based serial I/O receivers more promising solutions in the future, on the other hand designing an ADC with optimized power consumption, area and good performance is a challenging issue. After moving into the digital domain, digital signal post-processing is used to do the required FFE and DFE equalization.

In this paper, three equalization techniques are employed; 3-tap FFE is used for de-emphasis, CTLE for linear equalization and digital to analog converter for digital domain equalization.

Clock and data recovery is employed using a digital phase tracking loop. This paper presents a novel method for phase acquisition directly from the ADC comparators. A low power digital current steering phase interpolator has been used for the CDR. An LC second order PLL is used for clock generation for both the transmitter and the CDR loop of the receiver.

Section II presents the transmitter design, Section III presents the ADC based receiver and the CTLE, Section IV presents the PLL design, and Section V presents the CDR system.

## II. TRANSMITTER

A block diagram of the transmitter is shown in Fig.1. The key circuit blocks comprising a serializer block with 16 input lines at date rate 625Mb and one output lines at data rate 10 Gb, CML flip-flops, Pre-drivers and IDAC block which provides the bias current to the Final CML Output Driver stage.

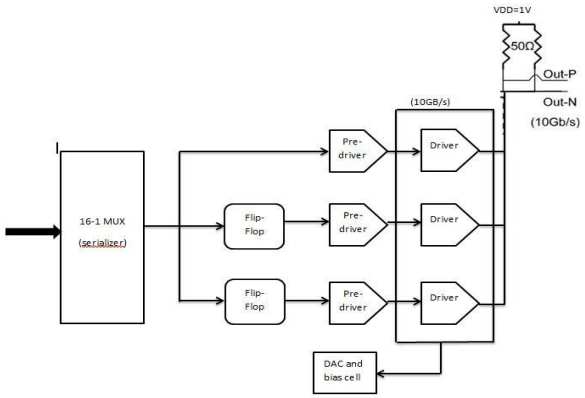



Fig.1 Transmitter block diagram

In order to achieve speeds up to 10 GB/s, a multiplexer is used. A 16-to-1 MUX is used to convert the data rate from 625 MB/s to 10 GB/s. Multiplexer is built based on the half rate architecture to reduce power consumption. Because the two data streams are shifted with simple latches instead of the master–slave flipflops required in a full-rate implementation so MUX is divided into 4 stages. All the circuits in the first three stages is implemented in CMOS technology due to low rate and in order to achieve low power. In the fourth stage the Flip-Flop and the Latch is implemented in TSPC topology to achieve 5 GB/s and the MUX is implemented with CML MUX to achieve the 10 GB/s data rate needed from the MUX. The output of the Multiplexer is fed in to 3-tap equalizer. The eye diagram of the MUX is shown below in figure.2.

The transmitter realizes 3 tap FFE function with 1 precursor tap and 1post cursor tap. The range of coefficient of pre cursor tap is from 0 to -0.175 with step size 0.025 and the range of coefficient of post cursor tap is from 0 to -.375 with 0.05. The coefficients are programmed using IDAC block to provide proper current for each tap. FFE has 26dB of frequency peaking, Attenuates DC at -26dB and passes Nyquist frequency at 0dB. The range of coefficient, equivalent current for each tap and amount of channel losses that FFE can reduce is shown in table 1.

A CML flip-flop that operates at full rate delays the output data from serialize with 1 UI and driving it to output stage. The role of that output stage is allowing a large output swing that is enough for the signal to traverse the channel with enough signal-to-noise ratios (SNR) that allows the receiver to properly detect the transmitted symbol. The drivers are a differential pairs that are bias controlled using current mode

digital to analog converters. The main advantage of using current mode drivers that it provide good common mode, immunity to noise, provide high output impedance which won't have significant effect on termination resistance and allows the operation of high speed circuits without the disadvantage of CMOS .One limitation on this operation is that the output differential pair is driving high currents, causing the drivers to have large widths that represent a large capacitive load to the CML flip flops, so pre-drivers are required that act as buffers between flip flops and output drivers. The CML drivers have been loaded with 50 ohm termination resistance (poly resistance) to minimize reflections and achieve the required return loss specified in standard. The standard waveform has a specific rise and fall time which it is within 20 to 47 ps that is prevent EMI to occur.

| ($C_{-1}$) | Pre-tap Crt. | ($C_0$) | Main_tap Crt. | ($C_1$) | Post Tap Crt. | FFE freq. peaking |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 20mA | 0 | 0 | 0 |
| -0.025 | .5mA | 0.925 | 18.5mA | -0.05 | 1mA | -1.4db |
| -0.05 | 1mA | .85 | 17mA | -.1 | 2mA | -4db |
| -0.075 | 1.5mA | .775 | 15.5mA | -.15 | 3mA | -5.1db |
| -.1 | 2mA | .7 | 14mA | -.2 | 4mA | -8db |
| -.125 | 2.5mA | .625 | 12.5mA | -.25 | 5mA | -12db |
| -.15 | 3mA | .55 | 11mA | -.3 | 6mA | -20db |
| -.175 | 3.5mA | .475 | 9.5mA | -.35 | 7mA | -26db |

Table.1 Range of coefficients

The transmit driver system outputs a maximum of 1200 mV into a 100- differential load. This eye diagram plot includes the effects of driver slew rate limit due to IC parasitic. The total channel loss at 5GHz for 16inch channel is approximately -12dB, requiring FFE settings [-.125, .625,-.25] to equalize the channel.

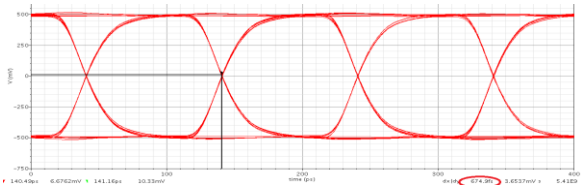


Figure.2 TX. eye diagram at 10GB/s without equalization.

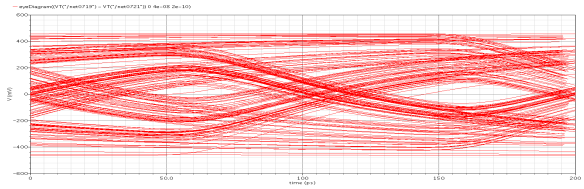


Figure.3 Eye diagram at Receiver input before Equalization.

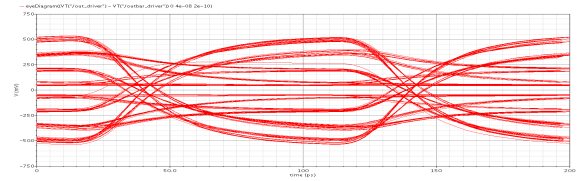


Figure.4 Transmitter Eye diagram at 10GB/s with Equalization.

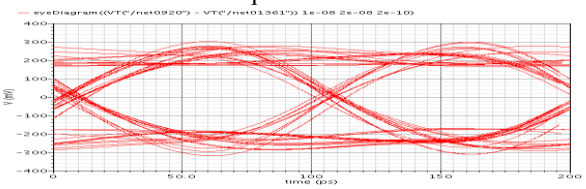


Figure5.Eye diagram at receiver input after Equalization.

## III. RECIVER

An ADC-based receiver has been employed as shown in figure.6 that uses CTLE, VGA as analog front end for the receiver, ADC- the mixed signal block - and the DSP core for processing the signal.

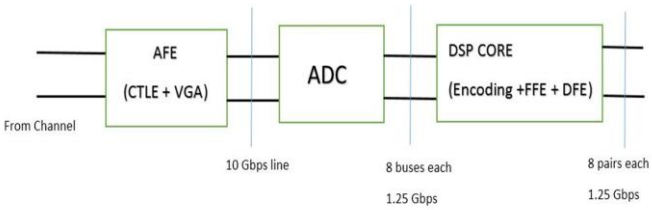
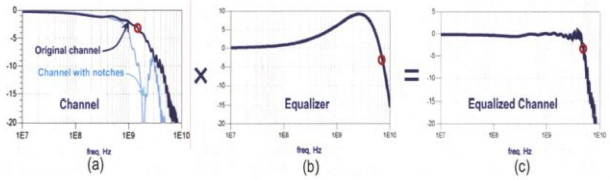



Figure6. System level of digital Receiver

### *A) CTLE:*

The channel acts as a low-pass filter, hence at the receiver the distortion must be compensated in order to reconstruct the transmitted symbols, a high-pass filter can be used.A continuous-time linear equalizer (CTLE) that provides gain peaking in order to boost up high-frequencies to counter the channel attenuation and distortion.

Fig. 7 illustrates the concept of an equalizer from a frequency domain point of view. By placing an equalizer in series with the channel.




Frequency responses of (a) the channel, (b) the CTLE, and (c) the equalized channel. (● : *-3 dB* point.)

Fig.7 Equalization idea

Poles of the CTLE are larger than the dominant pole of the channel,so the bandwidth of the equalized channel is increased. For example, the *-3dB* bandwidth of the channel, shown in previous figure, increased from 1.5 *GHz* to 4.5 *GHz.*

One of the common types of CTLE is source-coupled differential pair with source degeneration as shown in figure.8 The load resistance $R_L$ and the output parasitic capacitance $C_P$ introduce an additional high frequency pole. To obtain the desired boost, the $R_S$ value must be chosen as a trade of between the DC gain and the high frequency boost. The peaking and DC gain can be tuned through adjustment of

degeneration resistor and capacitor. The dominant pole is designed to be higher than the zero frequency to achieve high-frequency peaking gain. Simulation results for typical channel with $S_{21}$ = -17.36 dB are shown in figure 9.

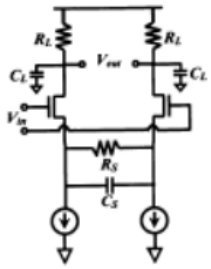



Fig.8 CTLE used topology

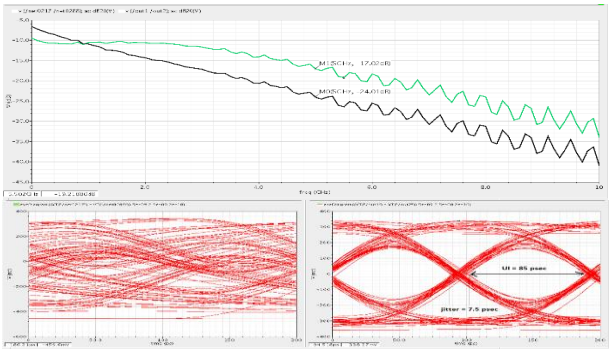


Fig.9 S21 with and without CTLE, eyediagram before and after CTLE

| Parameter | Value |
|---|---|
| Power consumption | 7.843 mW |
| Technology | 65nm |
| Supply voltage | 1V |
| Range | 0 – 10 dB |
| Data rate | 10 Bps |

Table.2 characteristics of the CTLE

*B) VGA*

The channel severely attenuates the data. So the received 10Gbps data must be amplified to a higher values suitable for operating the following stage ADC, It's supposed for this amplifier to have a very high linearity and add minimum noise to the received data. Fig.10 shows the design used. Varying the amplifier gain is done by varying the degeneration resistance to give a constant output = 1.2 Vpp.

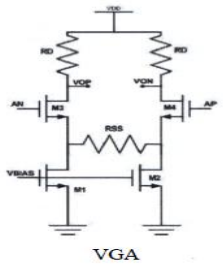



Fig. 10 VGA used topology

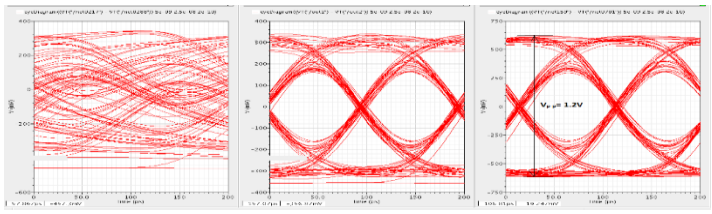


Fig. 11 Typical back plane channel after CTLE and VGA

*C) LOW POWER HIGH SPEED FLASH ADC*

i. ADC Architecture:

For data rate around 10 Gb/s, ADC-based receivers have shown sufficiently comparable power/performance to be considered a viable solution in addition to the traditional mixed-mode approach. The ADC resolution requirement for digital receivers depends on the application and link characteristics. 4.5 bits of resolution are needed in the channel with >30 dB attenuation, and a 3-bit ADC is sufficient for the channels with less than 20 dB attenuation. A 4-bit FLASH ADC has been chosen to obtain both proper resolution for 25 dB channel attenuation at Nyquist freq. (5GHz) and the required high speed. Also time interleaving principle is used to reach this high rate and reduce the power consumption taking into consideration issues of timing, offset mismatches between channels.

Used ADC architecture utilizes THA, traditional reference ladder and array of comparators, as shown in fig.12 the full architecture of one channel of the designed ADC.

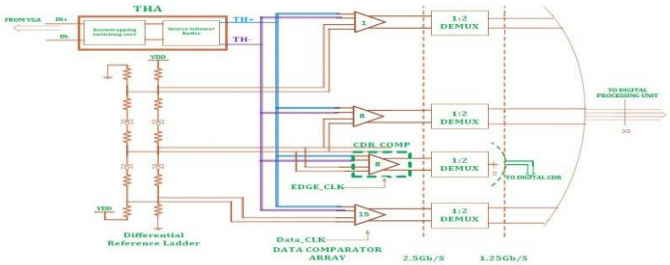



Fig.12 flash ADC system level

Track and hold circuit is used to hold signal for array of comparators to decrease the mismatch between comparators and to ensure proper operation with existence of high frequency input signal, as we designed 4 bit Flash ADC, each branch contains 15 comparator to give the output thermometer code corresponding to the input value, the output of comparators is at 2.5 Gbps , by using demux we can divide this rate in half to get two lines with 1.25 Gbps , these lines are forwarded directly to the DSP core to apply the digital processing on signal.

ii. Calculated Results:

System level design was done using MATLAB©. For the full Flash time interleaved ADC as shown in figure 13.a. Expected results for the design are shown in table 2.

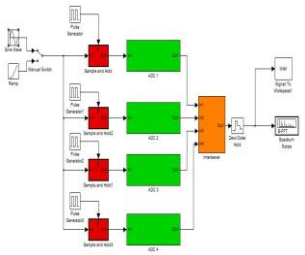


Fig.13 model for interleaved ADC

| Spec | Value |
|---|---|
| SNR_ideal | 25.84 dB |
| SINAD | 21.73 dB |
| SNR | 22.46 dB |
| SFDR | 33.4 dB |
| ENOB | 3.32 Its |

Table.3 Expected values of ADC performance

iii. THA:

THA contains two main blocks, sampling switch with bootstrap circuit and buffer to isolate the sampling core form the high input capacitance of all comparators which are connected on the same node of input.

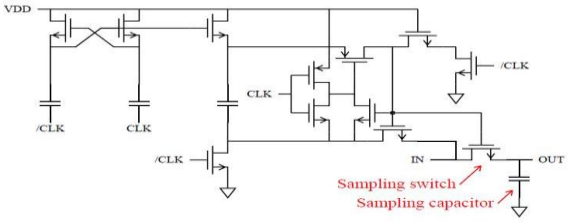



Fig. 14 bootstrapping circuit for sampling switch

Buffer is chosen to be open loop circuit to support this high bandwidth, the used topology is simple source follower (Figure 15) with advantages over differential pair to keep mismatch sensitivity low and to maintain better linearity.

iv. Comparator:

This is the main block in the ADC which decides if input signal is greater than or smaller than some defined threshold "reference", designed comparator consists of pre-amplifier, strong-arm latch and SR-latch.

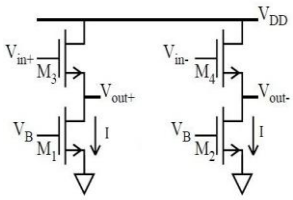



Fig. 15 pseudo differential source follower buffer

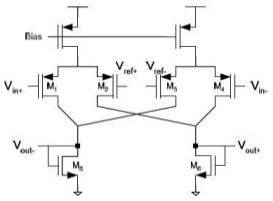



Fig.16 Preamplifier topology

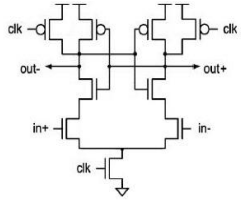



Fig.17 StrongArm latch

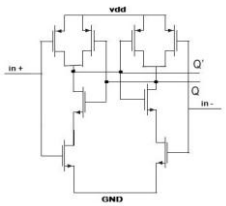



Fig.18 SR Latch

| | |
|---|---|
| SNDR | 20.42 dB |
| SFDR@ 4.961 GHz | 28 dB |
| FOM | 1.58 pJ/conv-step |
| INL | +0.25/-0.16 |
| Power | 124 mW |
| ENOB | 3.1 bits |

Table.4 ADC Final results

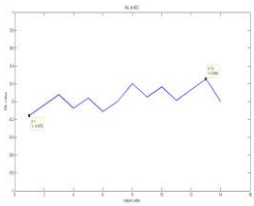


Fig. 19 INL for full ADC

Output thermometer code is forwarded directly to the DSP core for decoding and applying DFE and FFE equalization.

## IV. PHASE LOCKED LOOP

Phase locked loop is considered the main source of clocking of the whole system. The output clock of the PLL is fed to the transmitter, receiver and CDR, The used PLL used is a conventional second order charge pump PLL as shown in the figure.20

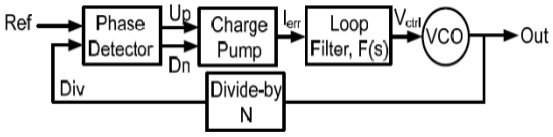



Fig.20 Conventional 2nd Order Charge Pump PLL

Loop parameters are chosen based on the transfer function for the PLL loop to be stable.

| Parameter | Value |
|---|---|
| Reference Frequency | 156.25 MHz |
| Output Frequency | 10.3125 GHz |
| N | 66 |
| $K_{VCO}$ | 753 MHz/V |
| BW | 7 MHz |
| Phase Margin | 60 degrees |
| Peaking | < 2 dB |
| C1 | 0.22 pF |
| C2 | 2.85 pF |
| R | 29.78 KΩ |
| $I_{CP}$ | 150 uA |

Table.5 Parameters and the achieved specs

i. Phase and frequency detector:

The PFD compares the divided-down signal with the reference signal and provides an error voltage. The average output, $\overline{V_{out}}$, is linearly proportional to the phase difference, $\Delta\varphi$, between its two inputs.

The implementation of the PFD is shown in Fig. 21-a. The circuit consists of two edge triggered, resettable D flip-flops. Applying a PFD can be done by many topologies. This topology's output is free from dead zone & has relatively low power consumption and area.

ii. Charge pump:

Charge pump combined with the loop filter is the part in the PLL system that gives a control voltage to the VCO, according

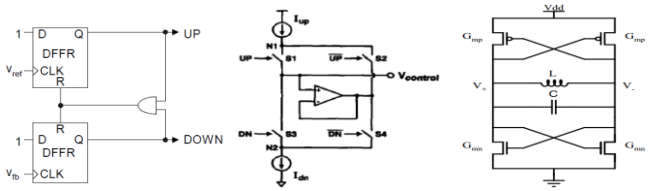
to the signal coming from the PFD, thus letting the VCO output a signal of certain frequency.

The topology used for the charge pump is shown in Fig.21-b. The current sources are kept on always & the $V_{DS}$ is kept almost constant when the switches are open using a unity gain buffer in order to decrease the current mismatch & charge sharing. The compliance curve of this topology shows that the compliance range is between 0.125V – 0.85V.

iii. Voltage controlled oscillator:

VCO is a circuit that generates a periodic output whose frequency is a linear function of a control voltage.

Since the required output jitter from the PLL is 1ps rms, we have chosen to work with the LC VCO, Fig.21-c, in order to achieve the lowest possible phase noise from the oscillator. It is noticed from the figure that the current source was eliminated from the circuit, as the preliminary simulation results showed that the current source contributed with 25% of the noise to the circuit. The phase noise at 1MHz offset is -112dBc/Hz which is enough for acquiring the desired 1ps.




(a) (b) (c)

Fig.21: (a) PFD (b) Charge pump (c) VCO

| | | | | | |
|---|---|---|---|---|---|
| NMOS | 105µm / 360nm | | | | |
| PMOS | 105µm/300nm | | | | |
| Capacitance range | 1.23pF – 1.5pF | | | | |
| Inductance | Width = 9µm | Radius = 40µm | Turns = 1 | L = 186.5pH | Q Factor = 20.6 |
| | Area width = 153µm | Area length = 147.5µm | | | |

Table.6 VCO characteristics

iv. Divider:

The divider takes the output of the VCO which is 10.3125GHz, and outputs it as a signal with 156.25 MHz. To achieve this, the dividing ratio will be 66. To get a dividing ratio of 66, it is divided by 11 as it is the first prime number which we can divide by, then divide by 3 and then 2.

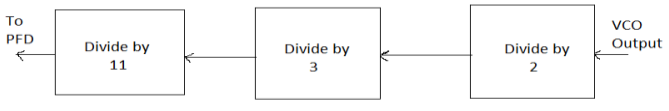



Figure.22 Proposed divider blocks

The building blocks are D-flip flops and logic gates. The D-flip flops are implemented using TSPC flip-flop. The logic gates are implemented using static CMOS gates. The total power consumption is 5.7 mW for the whole divider.

## V. CLOCK AND DATA RECOVERY

The implemented system is an ADC based dual loop phase tracking system Figure.23 based on a PLL and phase interpolator. A single loop system was avoided as due to the conflict in setting the loop bandwidth. Phase acquisition is done directly using edge and data samples of the middle comparators of the ADC using 8 clocks interleaved by 45 degrees as the system is working on quarter rate.

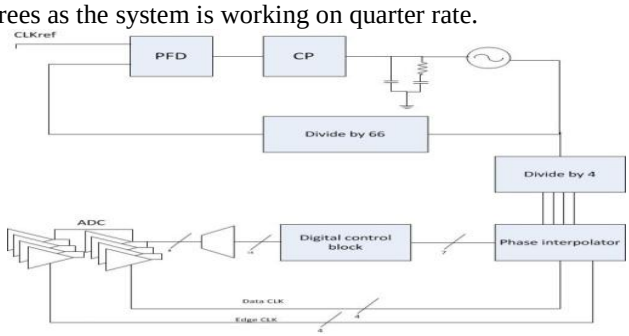



Fig.23 CDR System

A demultiplexer is added to reduce the data rate for the digital block. The digital block is responsible for processing the data samples and computing the average phase in order to feed the PI with the required code-word to get the required phases.

i. Digital block:

Digital code block is illustrated in Figure.24. The data stream is sampled at four equally spaced phases of clocks, data (center) and edge clocks. XOR gates are used to detect transition, then the edge and data samples are compared to determine if the samples are early or late. Majority voting is done to increment or decrement an accumulator. The accumulator is 7 bit, 2MSB are gray coded, and 5LSB are thermometer coded for the PI monotonicity.

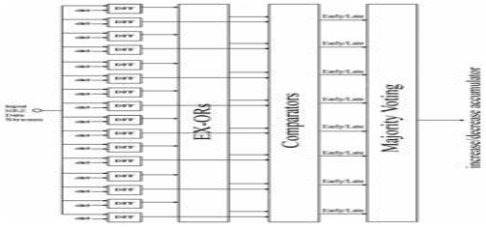



Fig.24 Simplified structure of digital block

ii. Phase interpolator:

Phase interpolator is a dual input delay buffer which receives two clocks, φ' and ψ', and generates the main clock Θ. The implemented PI interpolator is shown in Figure.25.

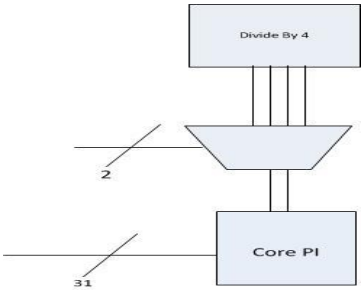
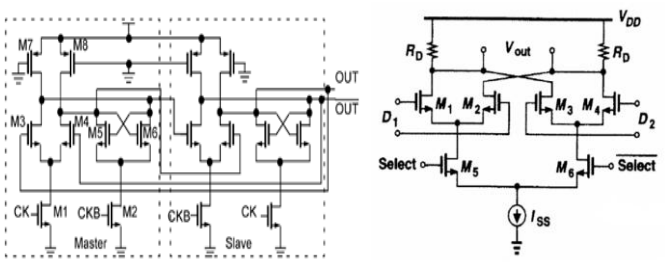



Fig.25 Implemented PI

A quadrature divider is used to get the quarter rate clock with different phases (0, 90,180,270) implemented using a pseudo differential master slave latch Figure.28.a, followed by a CML multiplexer to select the interpolating clocks, the used circuits are shown in Figure.26.




(a) (b)

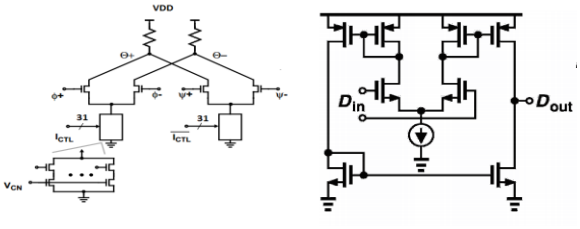
Fig.26: (a) Quadrature Divider, (b) CML MUX

The core PI consists of two differential pairs driving a resistive load. The interpolation is done using a DAC which changes the current driven from each differential pair Figure.27.a Capacitors were added to the gates of the PI in order to decrease the slew rate for proper interpolation.

The transfer function of the Phase interpolator is shown in Figure.28, showing an almost linear performance over different code words. The output waveform has a very low swing and the slew rate is very low while the ADC comparators require CMOS clocks, a CML to CMOS stage is added to generate the CMOS clocks as shown in figure.27.b followed by inverter buffer.

| Quadrature divider | |
|---|---|
| M1 – M2 | 800n/60n |
| M3 – M4 | 1u/60n |
| M5 – M6 | 1u/60n |
| M7 – M8 | 600n/60n |
| Power consumption | 0.93mW |
| Multiplexer | |
| Diff pair | 2.4µm/60nm |
| Select | 1.2µm/60nm |
| Current mirror | 29µm/240nm |
| Resistance | 1.25kΩ |
| Power consumption | 0.75mW |

Table.7 Transistor sizing and power consumption




(a) (b)

Fig.27: (a) Core PI, (b) CML to CMOS Converter

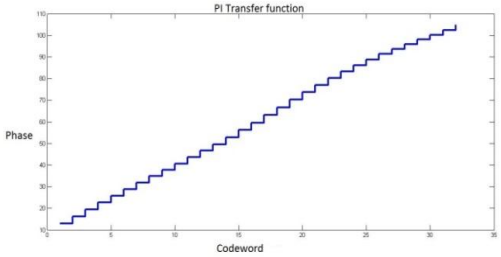



Figure.28 PI transfer function

| Phase interpolator | |
|---|---|
| Diff pair | 7µm/60nm |
| Switch transistors | 200nm/60nm |
| Current sources | 8 µm/360nm |
| Power consumption | 0.179mW |
| Multiplexer | |
| Diff pair | 23µm/60nm |
| Load transistors | 23µm/60nm |
| Current source | 130 µm/360nm |
| Inverter NMOS | 6µm/60nm |
| Inverter PMOS | 6µm/60nm |
| Power consumption | 1.6mW |

Table.8: Transistor sizing and power consumption of PI and CML to CMOS stages

## VI. REFERENCES:

[1] Kossel, M.; Menolfi, C.; Weiss, J.; Buchmann, P.; von Bueren, G.; Rodoni, L.; Morf, T.; Toifl, T.; Schmatz, M., "A T-Coil-Enhanced 8.5 Gb/s High-Swing SST Transmitter in 65 nm Bulk CMOS With << -16 dB Return Loss Over 10 GHz Bandwidth," Solid-State Circuits, IEEE Journal of , vol.43, no.12, pp.2905,2920, Dec. 2008

[2] Fabian Klass, "Semi-Dynamic Flip-Flops with Embedded Logic" IEEE, 1998.

[3] Mikael Gustavsson, J. Jacob Wikner and Nianxiong Nick Tan, "CMOS Data Converters for Communications," ISBN 0-306-47305-4.

[4] E-Hung Chen, Chih-Kong Ken Yang, "ADC-Based Serial I/O Receivers", VOL.57, NO. 9, SEPTEMBER 2010.

[5] B. Razavi, Design of Analog CMOS Integrated Circuits. New York: McGraw-Hill, 2001, ISBN 0-07-118815-0.

[6] B.Razavi, Design of Integrated circuits for optical Communications, McGraw-Hill, 2003.

[7] J.Rogers, C.Plett and F.Dai, "Integrated Circuit Design for High-Speed Frequency Synthesis" ARTECH House 2006

[8] Richard C.Walker " Designing Bang-Bang PLLs for clock and Data recovery in Serial Data Transmission"