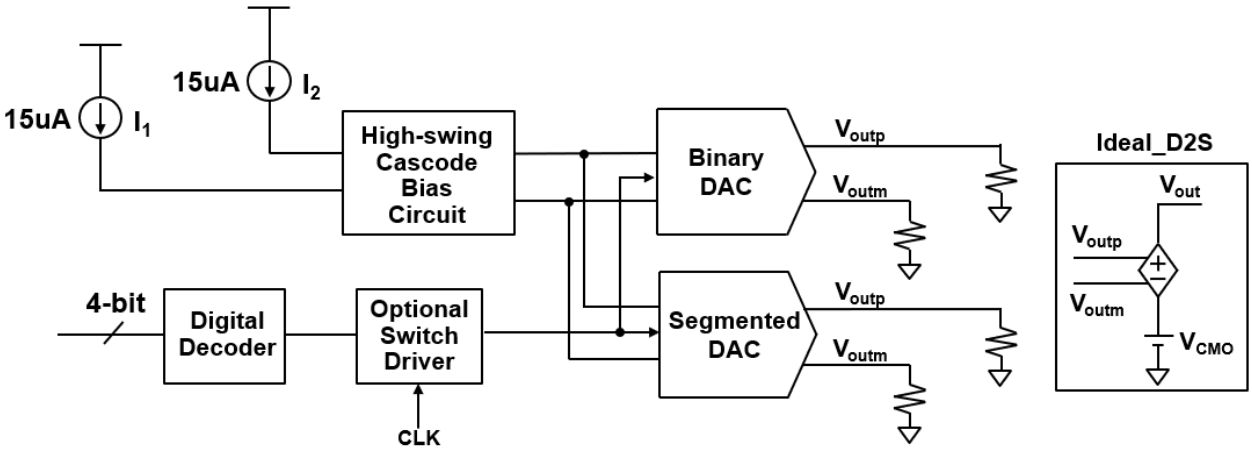
EE288 Homework #5 (5 points) Apr 9, 2018

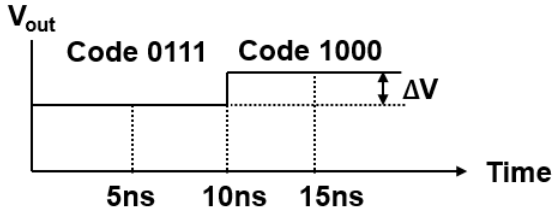
Due: April 23, 2018 6:00PM. Homework will not be received after due.
Homework submission file should be in pdf format and file name should be EE288HW5_yourname.

In this homework, you will build two 4-bit current steering DACs based on Binary and Segmented architectures using nmos2v and pmos2v at VDD=1.8V supply. You are required to use high-swing cascode current mirror structures for the current source arrays. Assume you have 2 ideal current sources of 15uA to generate bias voltages for the current source arrays as can be seen in below diagram. You will be measuring the output voltage, Vout, of the ideal differential-to-single end conversion circuit (ideal_D2S in ee288lib).



For the current source arrays used in DAC, use PMOS cascode current mirrors to get the differential output currents dumped to external 2KΩ resistor in each side. With 1-LSB current of 15uA, the full signal swing at Vout will be around 1Vppd.

The main transistor of the current source should be sized to meet the 1/8 LSB DNL requirement at major code transition. To check the DNL at major bit transition, run a transient simulation for 10ns with 0111 code followed by another 10ns with 1000 code. Then calculate the voltage difference between two codes at 5ns and 15ns as shown below.

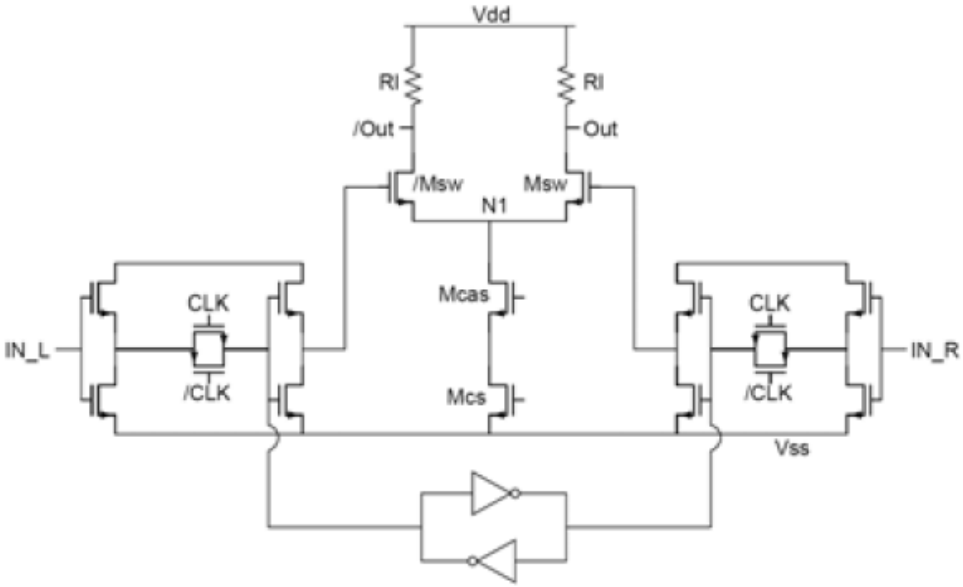


To get the statistical variations of the circuits, use 200 points Monte Carlo simulation in ADE-XL. Make sure to choose correct model file for Monte Carlo simulation. This model setup should be done in Corners Setup table in ADE XL. Click on Corners Setup icon and add new corner with “mc” model. It is desirable to create a result parameter using Calculator and run Monte Carlo simulation so that you can get the DNL variations over 200 points in the simulation. Multiply the Sigma value from the mc simulation by 5 for 5-sigma variation for the spec. This value should be less than 1/8 of 1-LSB, i.e., 7.8mV.

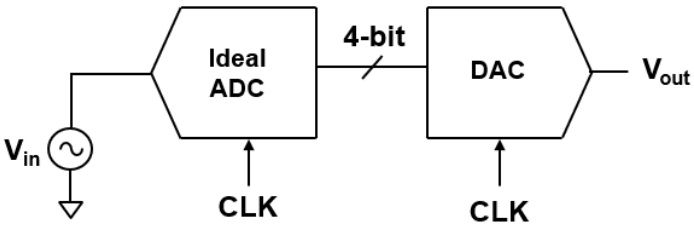
The binary DAC does not need a digital decoder, but the segmented DAC will need one. You can add an optional switch driver to see if it affects the final result or not. The optional switch driver is needed in

practice to synchronize the switch timing and to improve the dynamic linearity performance. An example switch driver circuit is shown below from the following paper

P. Palmers, Xu Wu, and M. Steyaert, \A 130 nm CMOS 6-bit full nyquist 3GS/s DAC," *IEEE Asian Solid-State Circuits Conference, ASSCC '07,* pp.348-351, 12-14 Nov. 2007.



To verify the dynamic performance of the DAC you designed, construct a test bench similar to below diagram.



The ideal 10-bit ADC you used in HW#1 can be modified to produce an ideal 4-bit ADC. Apply an input signal Vin (0.4V to 1.4V) at fin = (cycles/N) * fs where cycles=7 and N=64 for 64-point FFT. Run a transient simulation for 700ns in Cadence Spectre and plot the transient waveforms for the input and output signals along with clock and other relevant signals in white background. The sampling clock (CLK) should be fs = 100MHz and the output spectrum should be measured using Cadence spectrum analysis. Provide screen captures of the spectrum measurement showing signal measured, FFT condition, and the measurement result for both DACs.

Summary of what you need to submit electronically:

1. Schematics of your design – use white background in monochrome. (No color schematic)
2. 200-points Monte Carlo simulation results for DNL at major bit transition for both DACs
3. 700ns Transient simulation results showing all relevant signal waveforms
4. 64-point FFT plot for the output of both DACs
5. Summary of what you have learned on this homework problem