EE288 – HW5 Report

4-bit DAC design

(using 45nm CMOS Technology)

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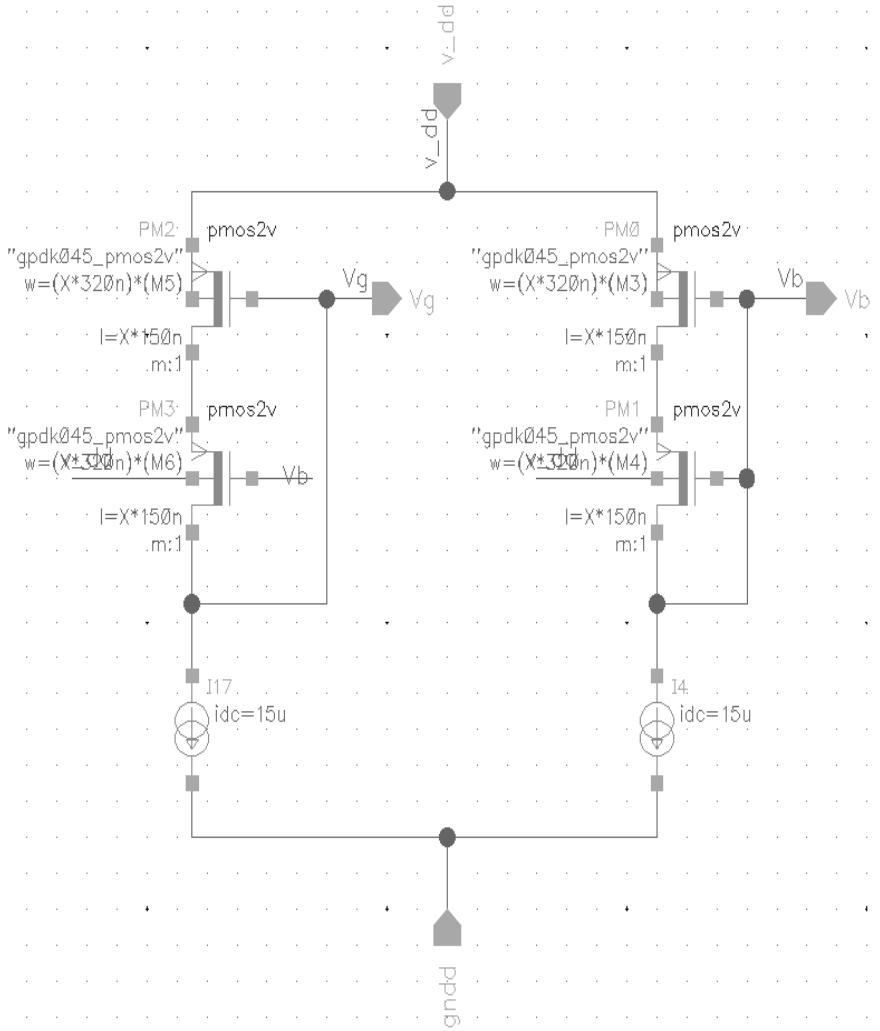
Overview

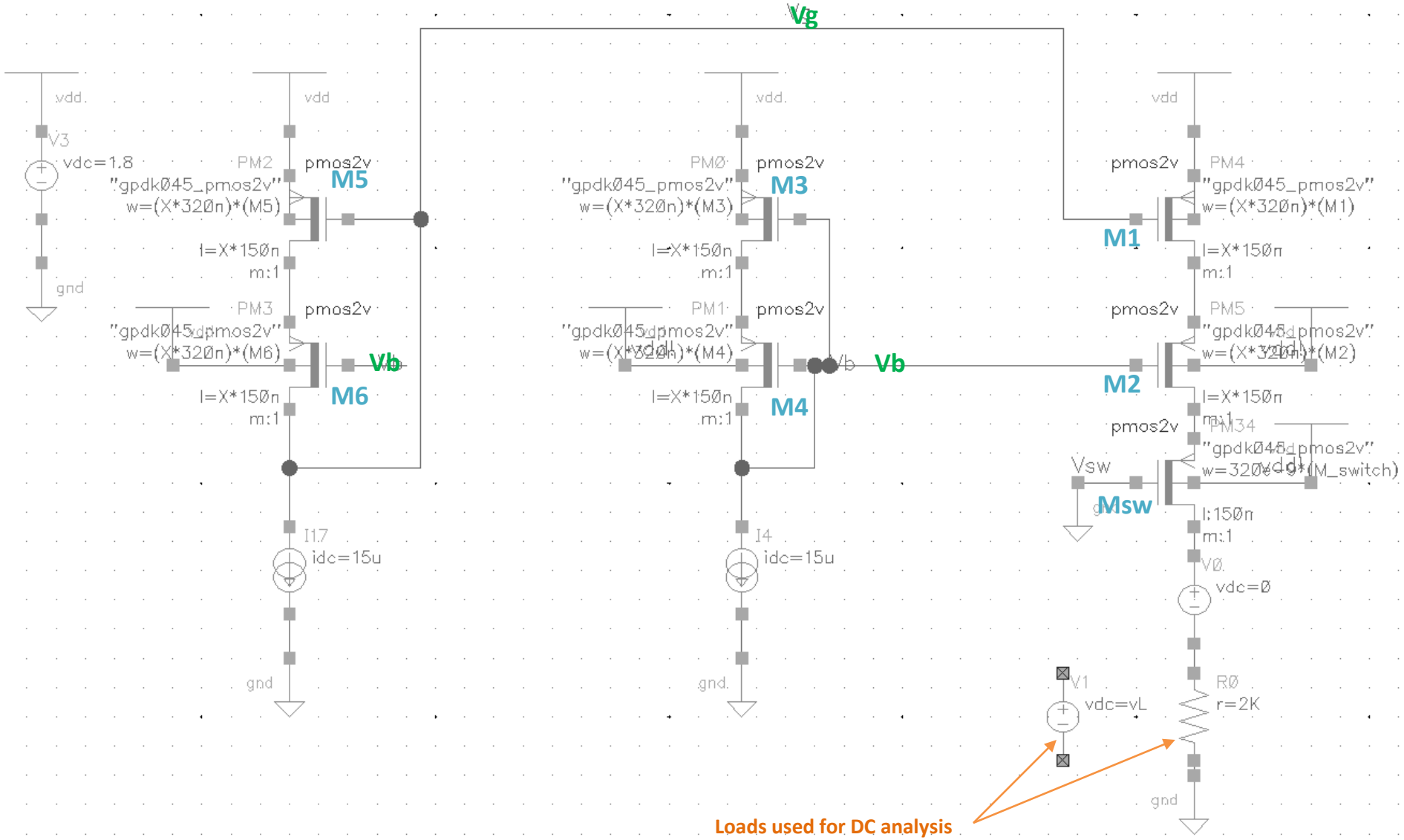
1. High-Swing Cascose Bias circuit
   - Circuit
   - Testbench
2. Current Mirror branches (1x, 2x, 4x, & 8x)
3. DAC circuits
   - Binary DAC
   - Segmented DAC
4. Monte Carlo Simulations
5. Transient Simulations
6. Results & Summary

(1)
High-Swing Cascode Bias Circuit

Circuit


v_dd
v_dd
PM2
pmos2v
"gpdk045_pmos2v"
w=(X*320n)*(M5)
l=X*150n
m:1
Vg
Vg
PM3
pmos2v
"gpdk045_pmos2v"
w=(X*320n)*(M6)
l=X*150n
m:1
Vb
I17
idc=15u
PM0
pmos2v
"gpdk045_pmos2v"
w=(X*320n)*(M3)
l=X*150n
m:1
Vb
Vb
PM1
pmos2v
"gpdk045_pmos2v"
w=(X*320n)*(M4)
l=X*150n
m:1
I4
idc=15u
gndd
gndd

Testbench


Vg
vdd
V3
vdc=1.8
gnd
PM2
pmos2v
"gpdk045_pmos2v"
w=(X*320n)*(M5)
M5
l=X*150n
m:1
PM3
"gpdk045_pmos2v"
w=(X*320n)*(M6)
M6
Vb
I17
idc=15u
PM0
w=(X*320n)*(M3)
M3
PM1
w=(X*320n)*(M4)
M4
I4
idc=15u
PM4
w=(X*320n)*(M1)
M1
PM5
w=(X*320n)*(M2)
M2
PM34
Vsw
Msw
m:1
V0
vdc=0
V1
vdc=vL
R0
r=2K
Loads used for DC analysis

Testbench

- Sizing:

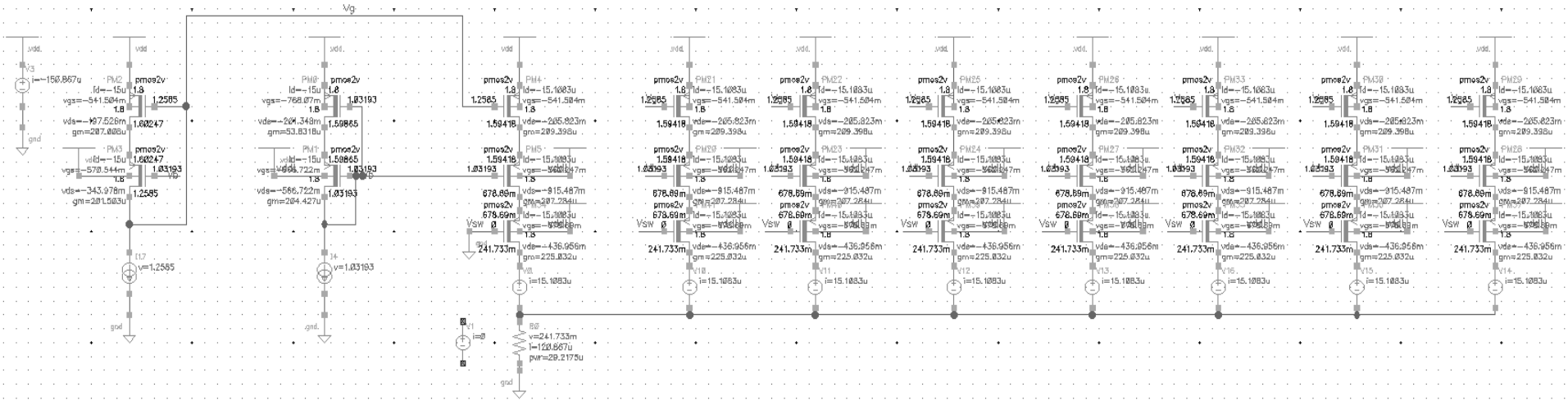
Device	Size (in terms of fingers, m)
M1	**6**
M2	**5**
M3	**1**
M4	**5**
M5	**6**
M6	**5**
Msw	**4**
Ideal Current Sources	**15 uA**

➔ The aim is to have M1 & M2 in saturation with low Vds. (Vds of both transistors is monitored in the test)

- M2, M4, M6 are sized together to have equal current densities.
- M3 is in triode. It's (W/L) is increased to decrease its Vds, which will also be equal to Vds of M5 & M1.
- M5's (W/L) is increased to decrease Vg till M1 becomes in Saturation.
- M1's (W/L) is then increased to provide a current of 15uA in the mirror branch.
- M2 & Msw's sizes must ensure the passage of the 15uA in the mirror branch.

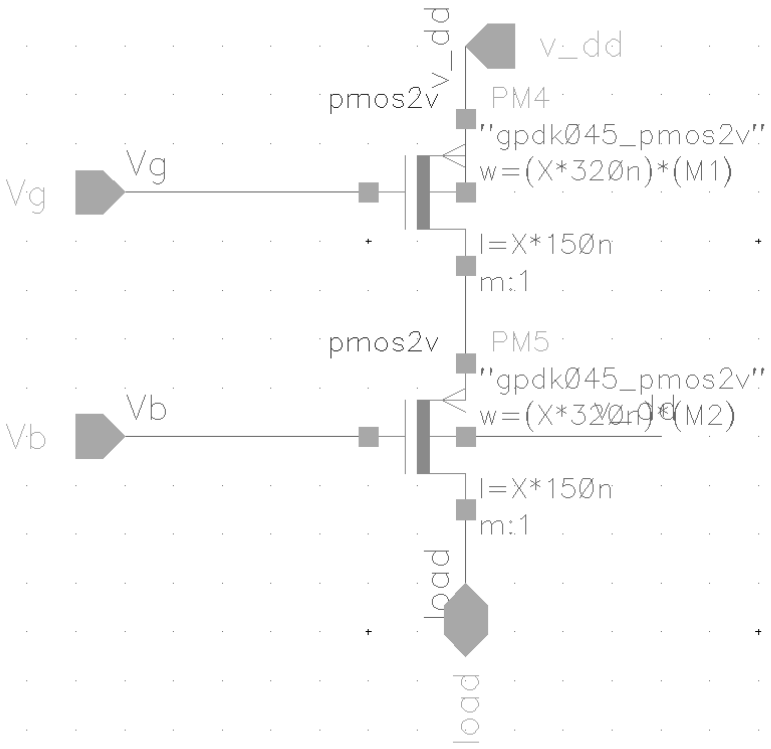
- In the testbench, besides using the 2KΩ load, a voltage source is used to make sure the mirror branch provides a 15uA at different output voltages (~0.4v-1.4v).

Testbench
(for more than 1 mirror branch)

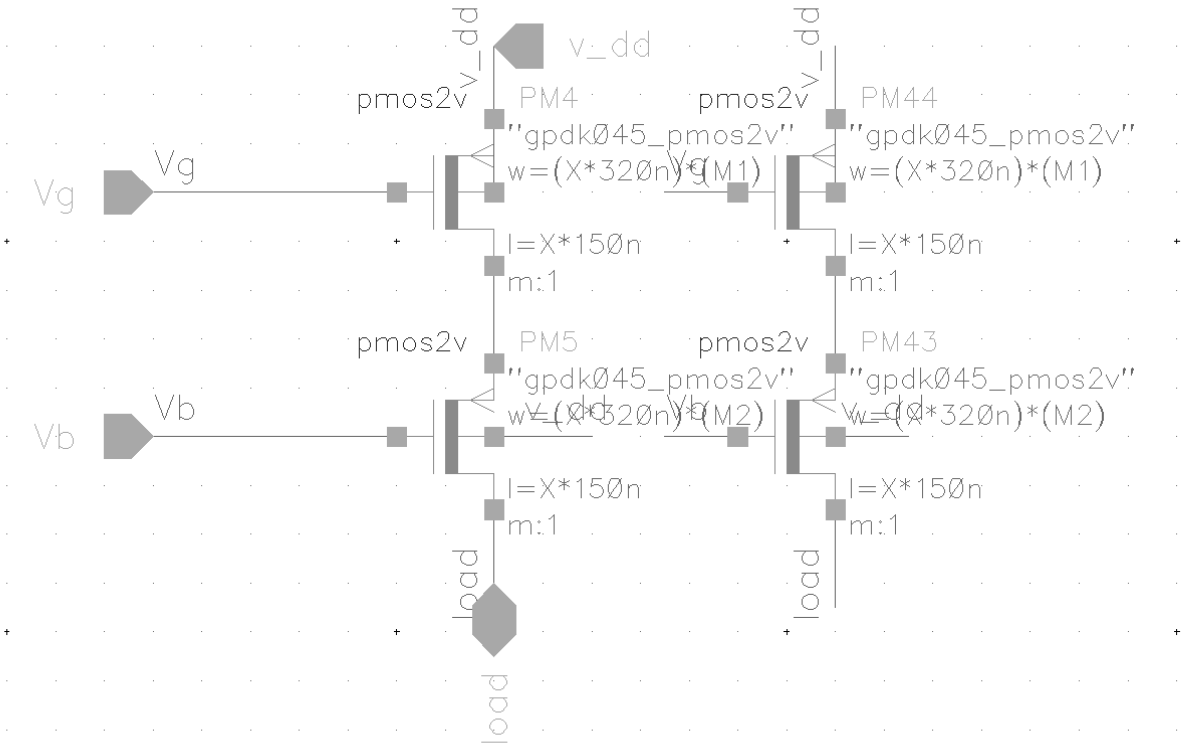


(2)
Current Mirror Branches

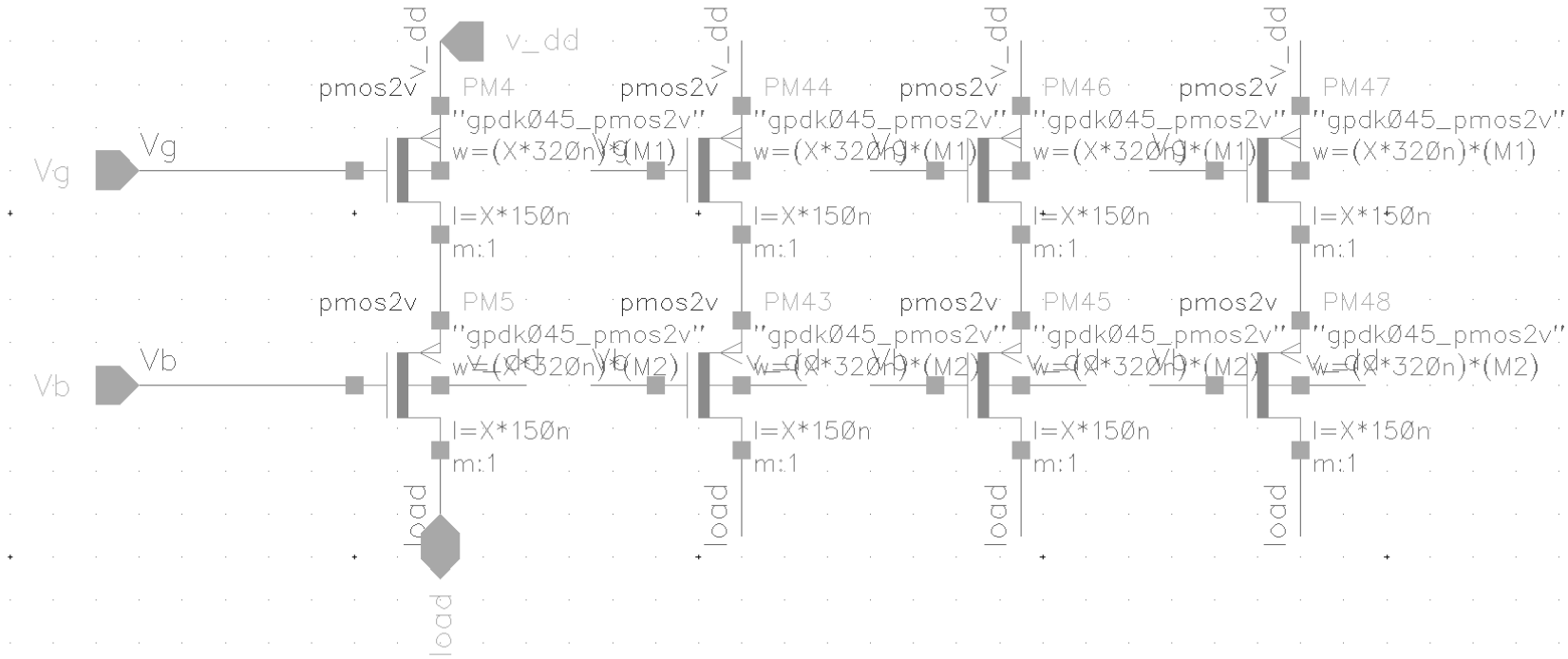
1x Current Mirror Branch



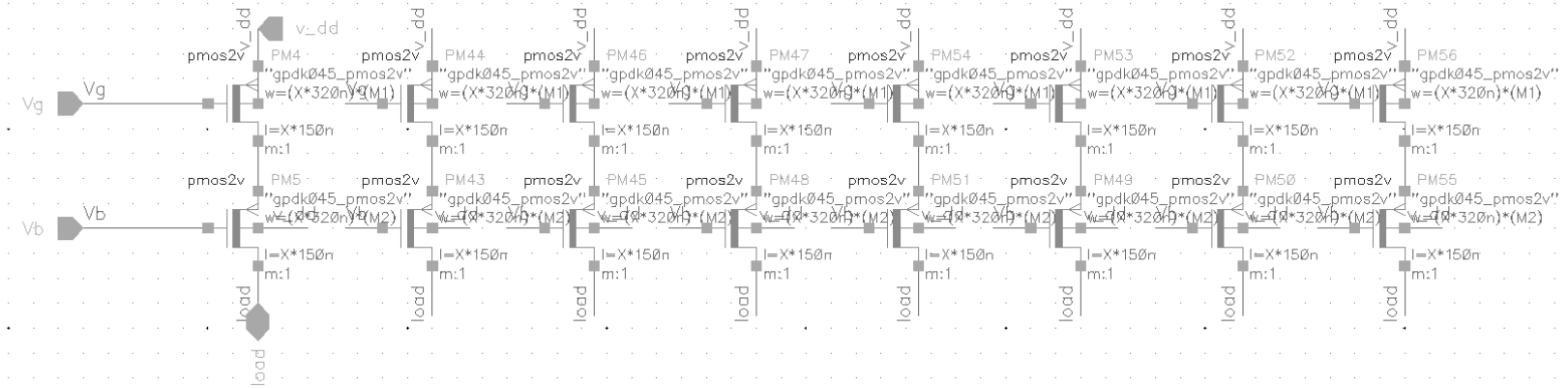
2x Current Mirror Branch



4x Current Mirror Branch

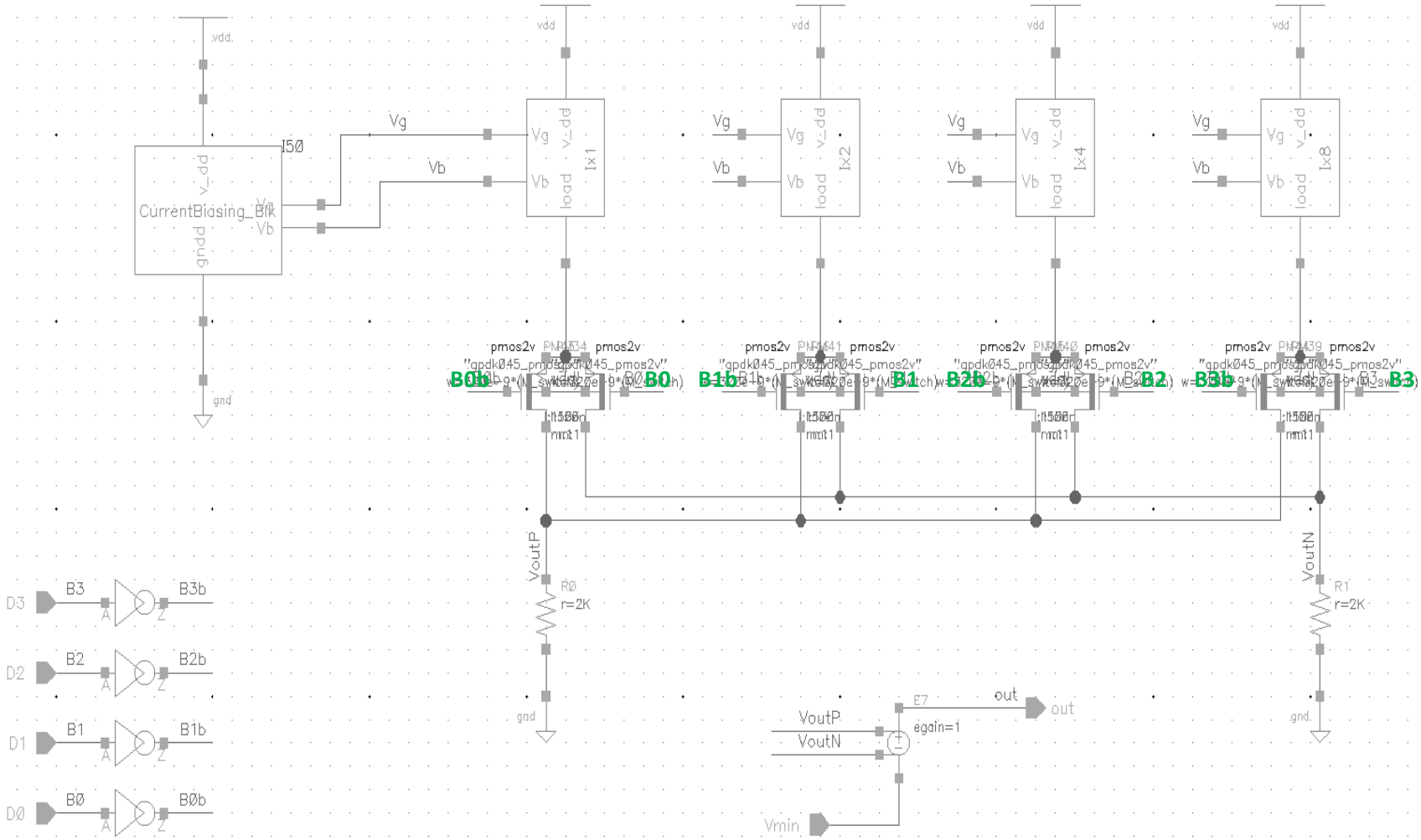


8x Current Mirror Branch

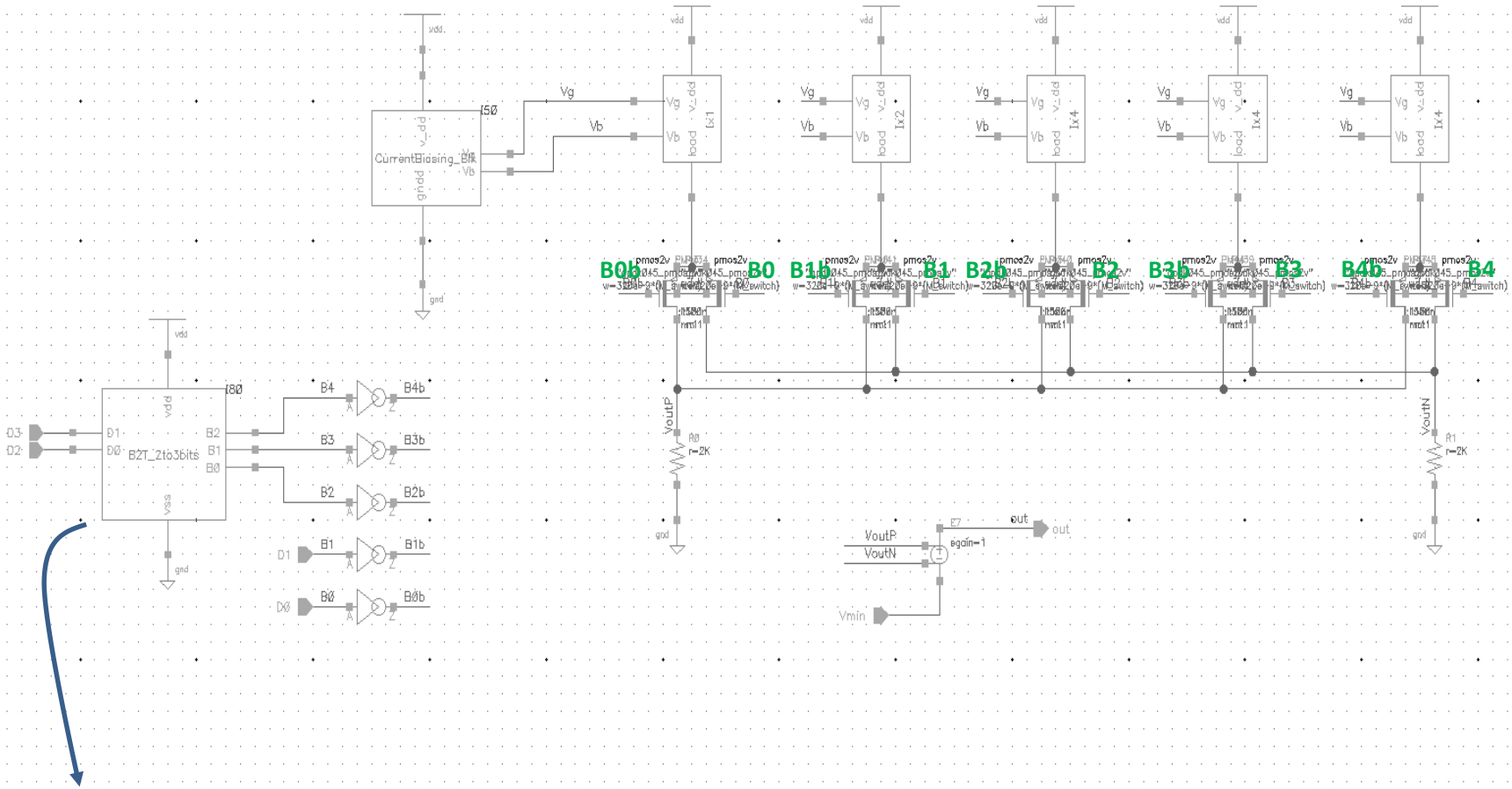


(3)
DAC Circuits

Binary DAC Circuit



Segmented DAC Circuit



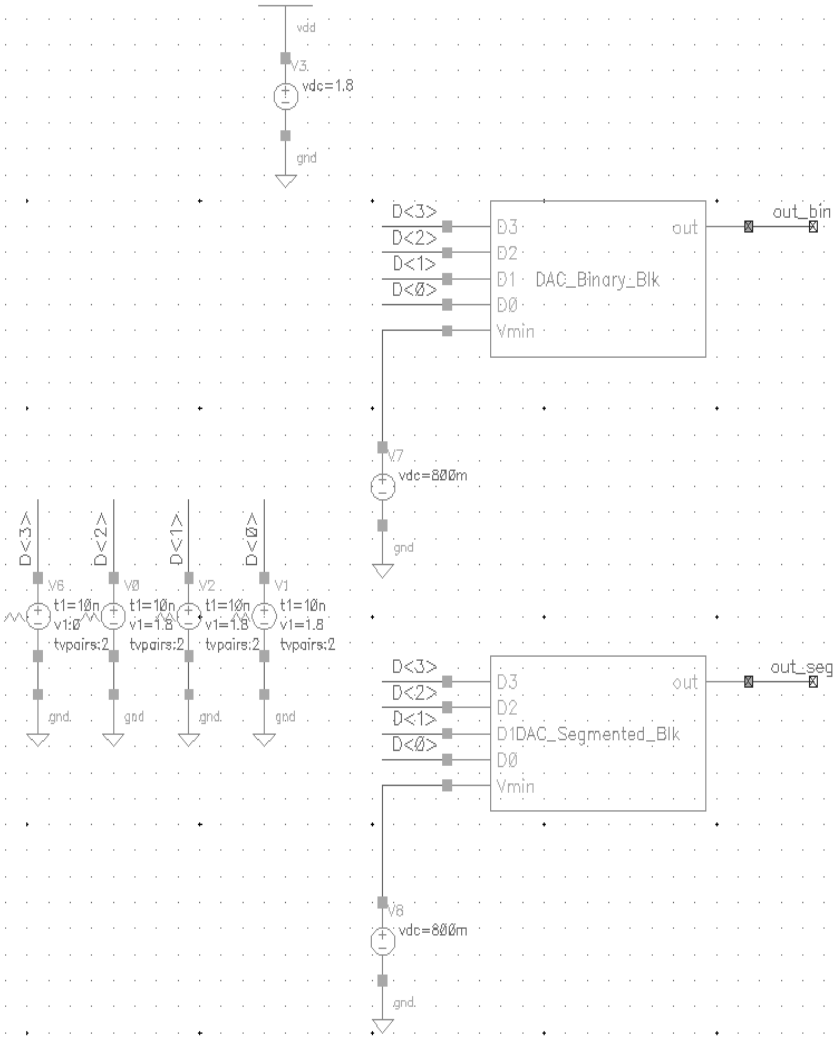
VerilogA: BinaryToThermometer Block (2-to-3 bits)

```
// VerilogA for ADC_DACs, B2T_2to3bits, veriloga

`include "constants.vams"
`include "disciplines.vams"

module B2T_2to3bits(D0,D1,B0,B1,B2,vdd,vss);

parameter real vtrans=0.5;
parameter real delay = 0;
parameter real ttime = 1p;

inout vdd,vss;
input D0,D1;
output B0,B1,B2;

electrical vdd,vss;
electrical D0,D1;
electrical B0,B1,B2;

real b_0,b_1,b_2;
```

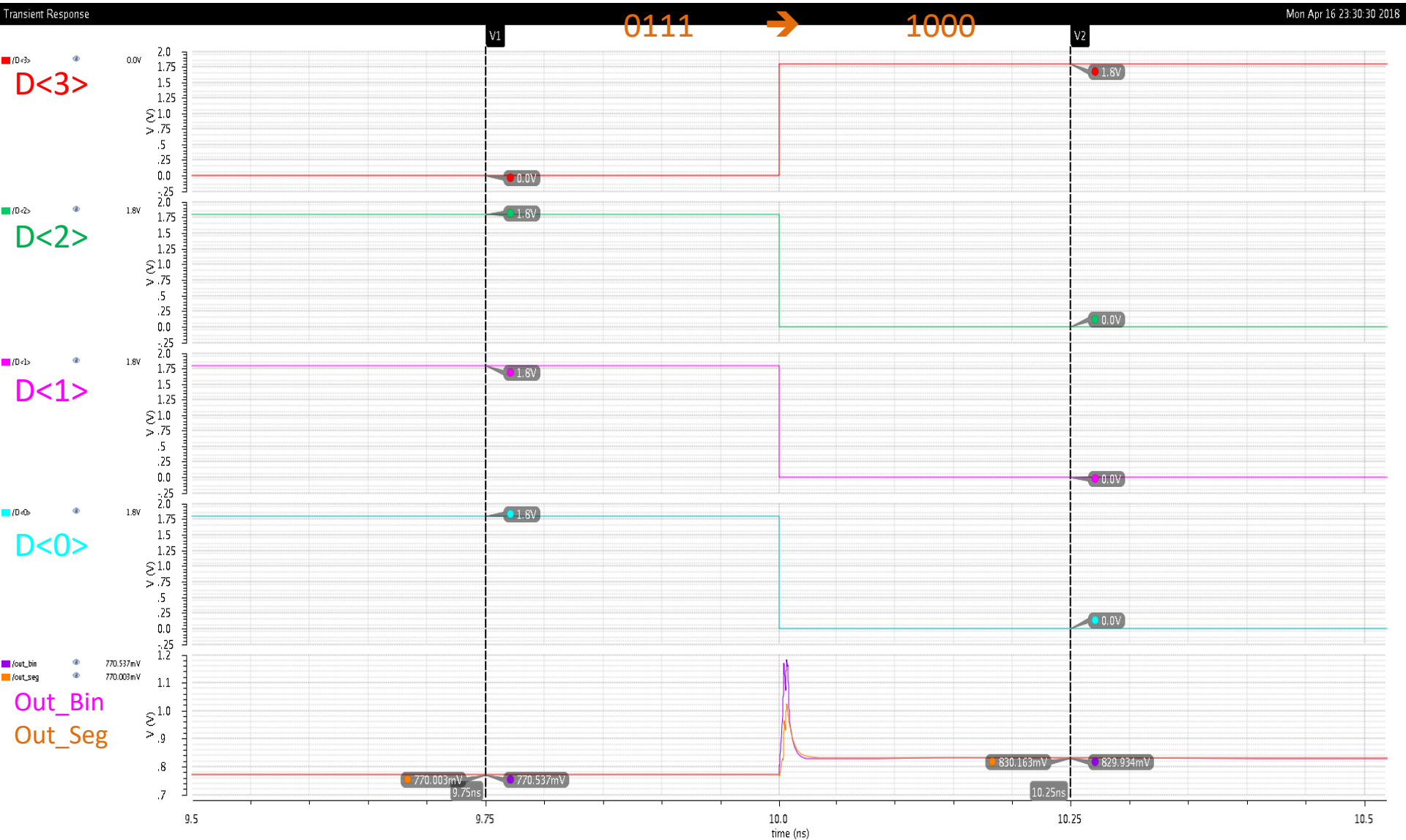
```
analog begin
        if ((V(D1)>0.9) && (V(D0)>0.9)) begin
        b_2 = V(vdd);       b_1 = V(vdd);       b_0 = V(vdd);
        end

        else if ((V(D1)>0.9) && (V(D0)<0.9)) begin
        b_2 = V(vss);       b_1 = V(vdd);       b_0 = V(vdd);
        end

        else if ((V(D1)<0.9) && (V(D0)>0.9)) begin
        b_2 = V(vss);       b_1 = V(vss);       b_0 = V(vdd);
        end

        else begin
        b_2 = V(vss);       b_1 = V(vss);       b_0 = V(vss);
        end

        V(B2) <+ transition(b_2,delay,ttime);
        V(B1) <+ transition(b_1,delay,ttime);
        V(B0) <+ transition(b_0,delay,ttime);
end
endmodule
```

(4)
Monte Carlo Simulations

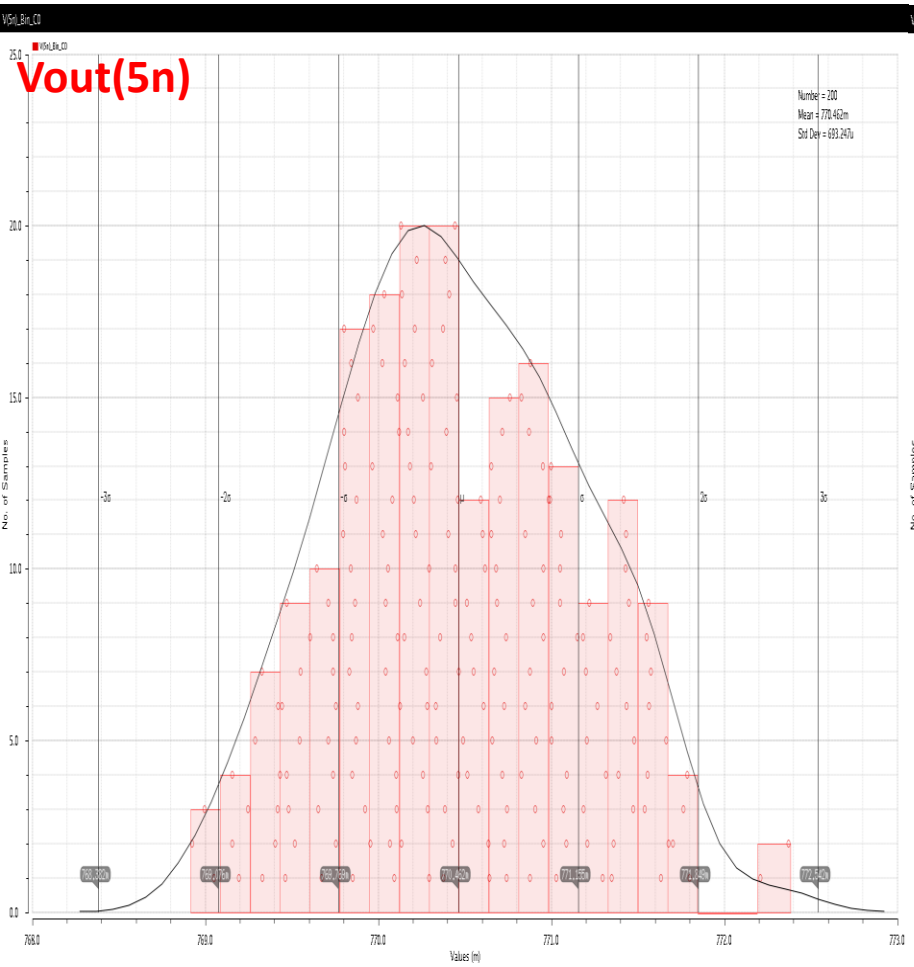
Testbench

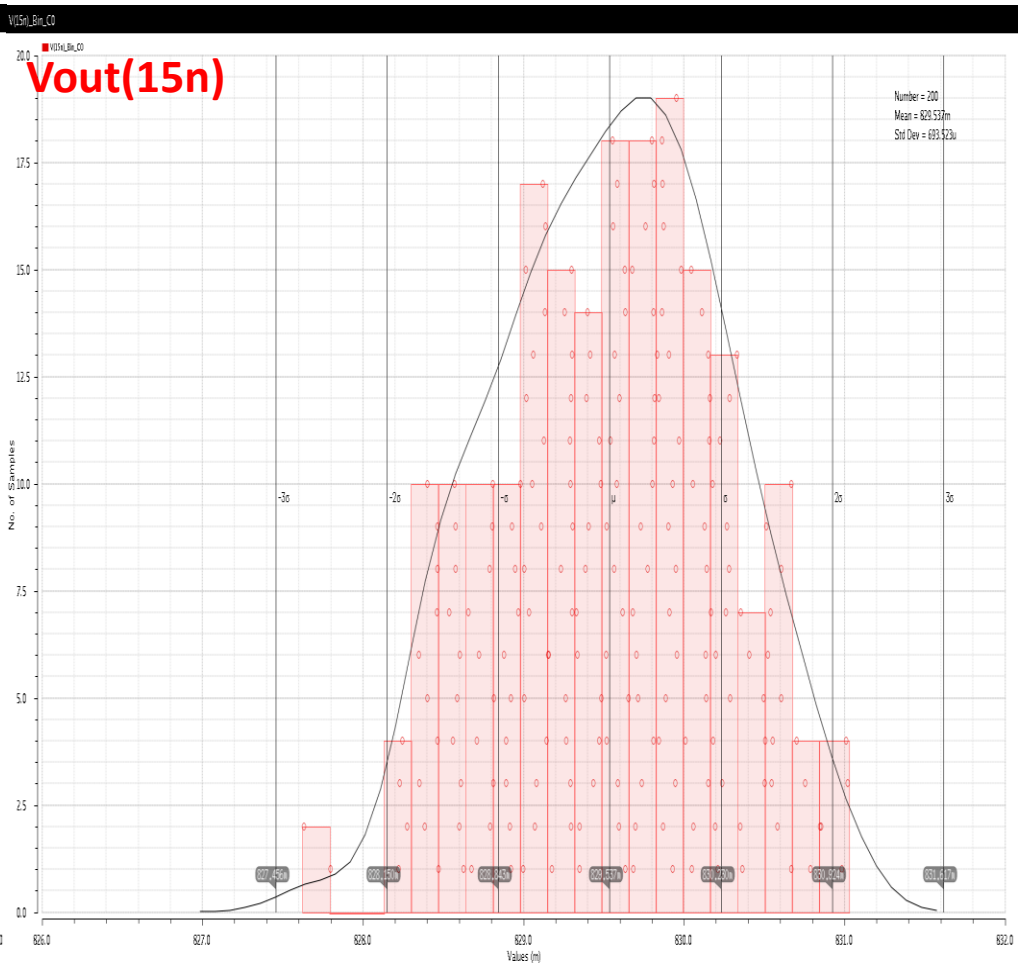

vdd
V3
vdc=1.8
gnd
D<3>
D<2>
D<1>
D<0>
D3
D2
D1
D0
Vmin
out
DAC_Binary_Blk
out_bin
V7
vdc=800m
gnd
V6
V0
V2
V1
t1=10n
v1:0
v1=1.8
tvpairs:2
gnd.
D1DAC_Segmented_Blk
out_seg
V8
vdc=800m

Transient Simulation

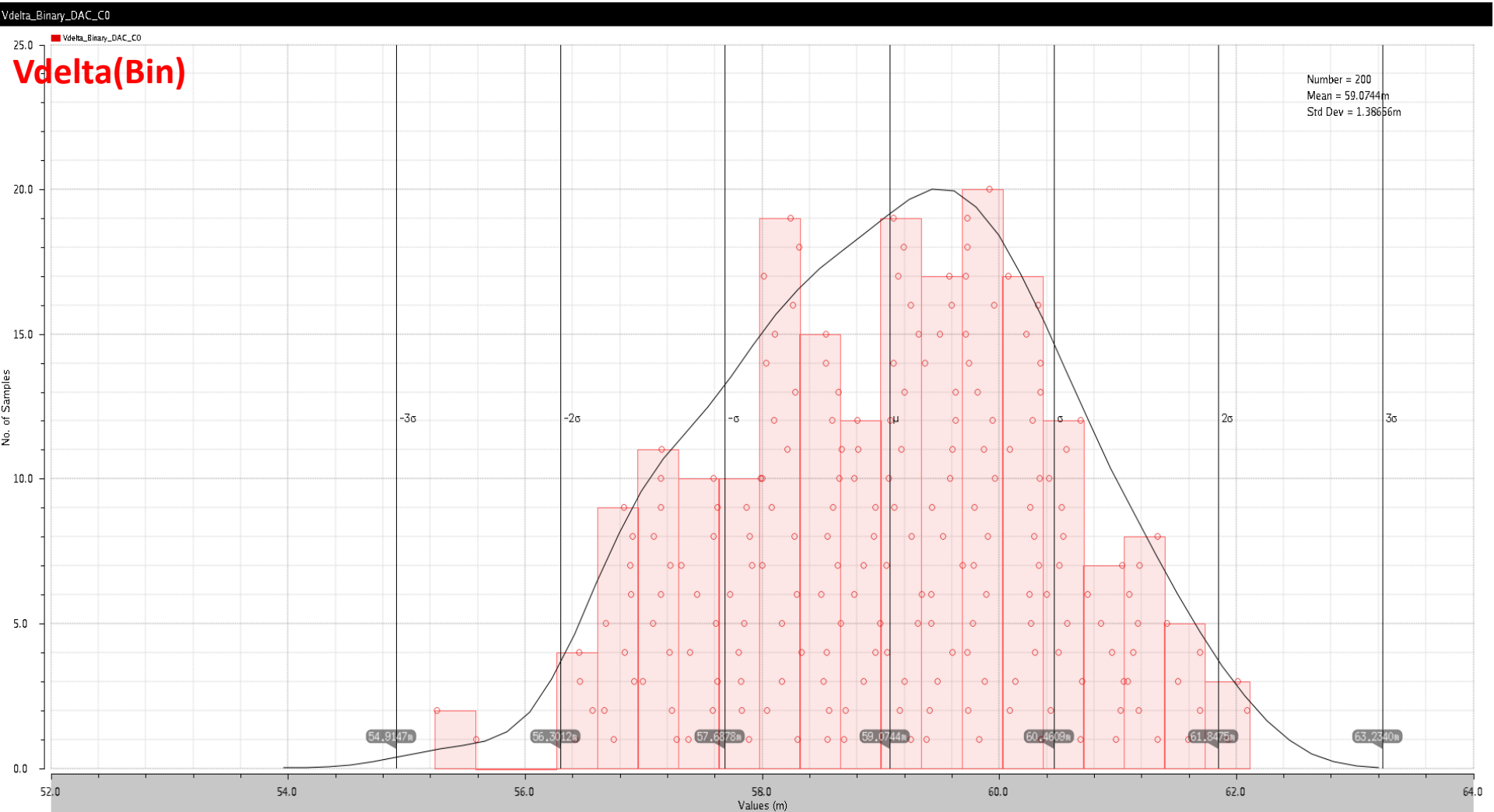


Monte Carlo Simulation (Binary DAC)

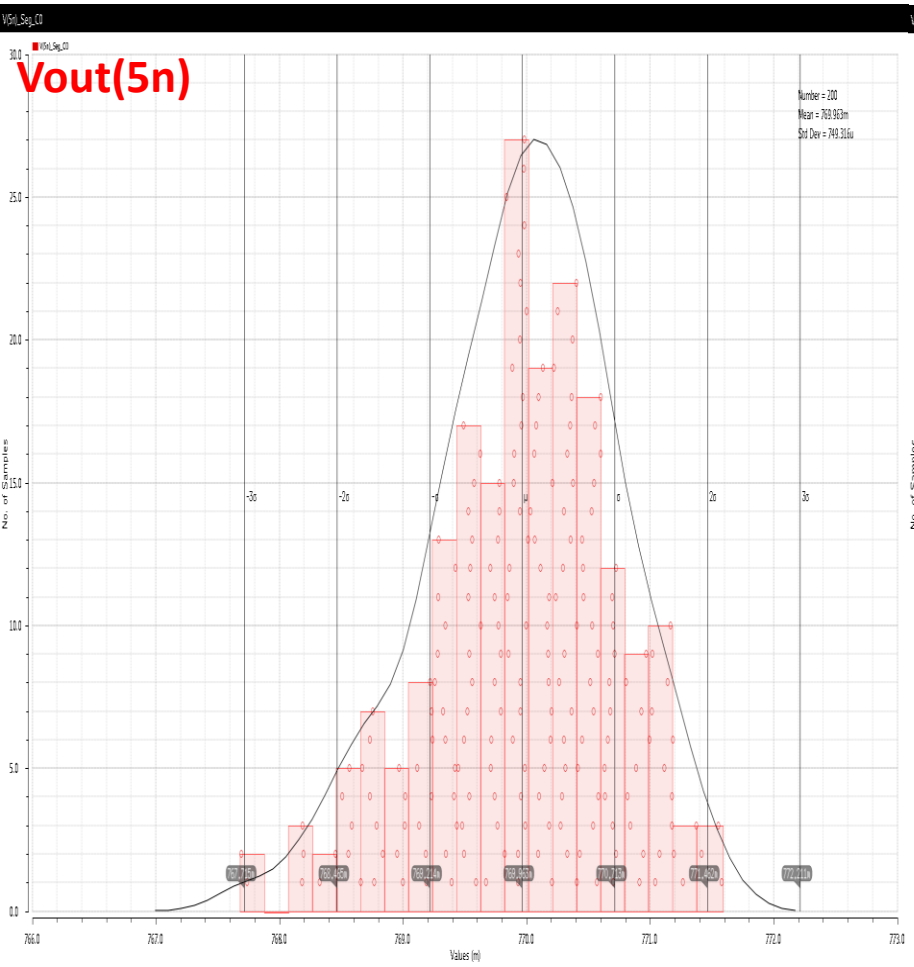


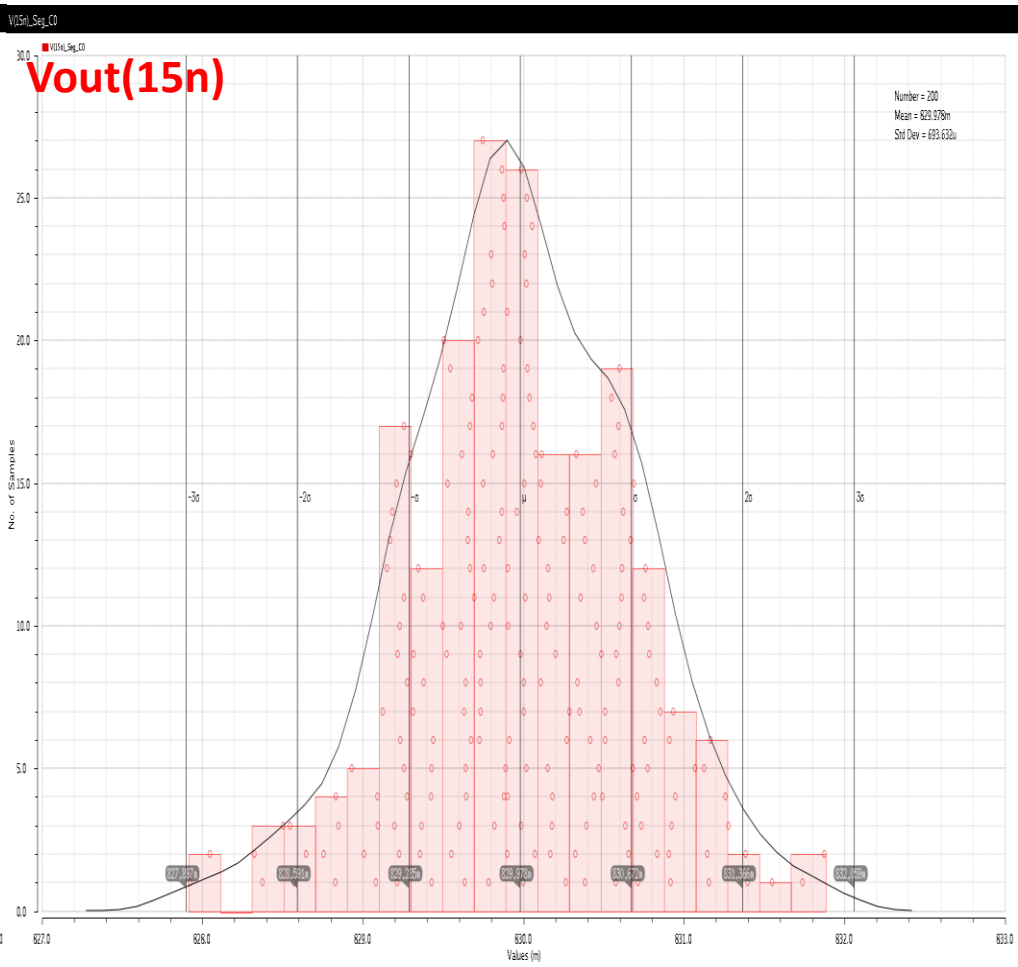


Monte Carlo Simulation (Binary DAC)

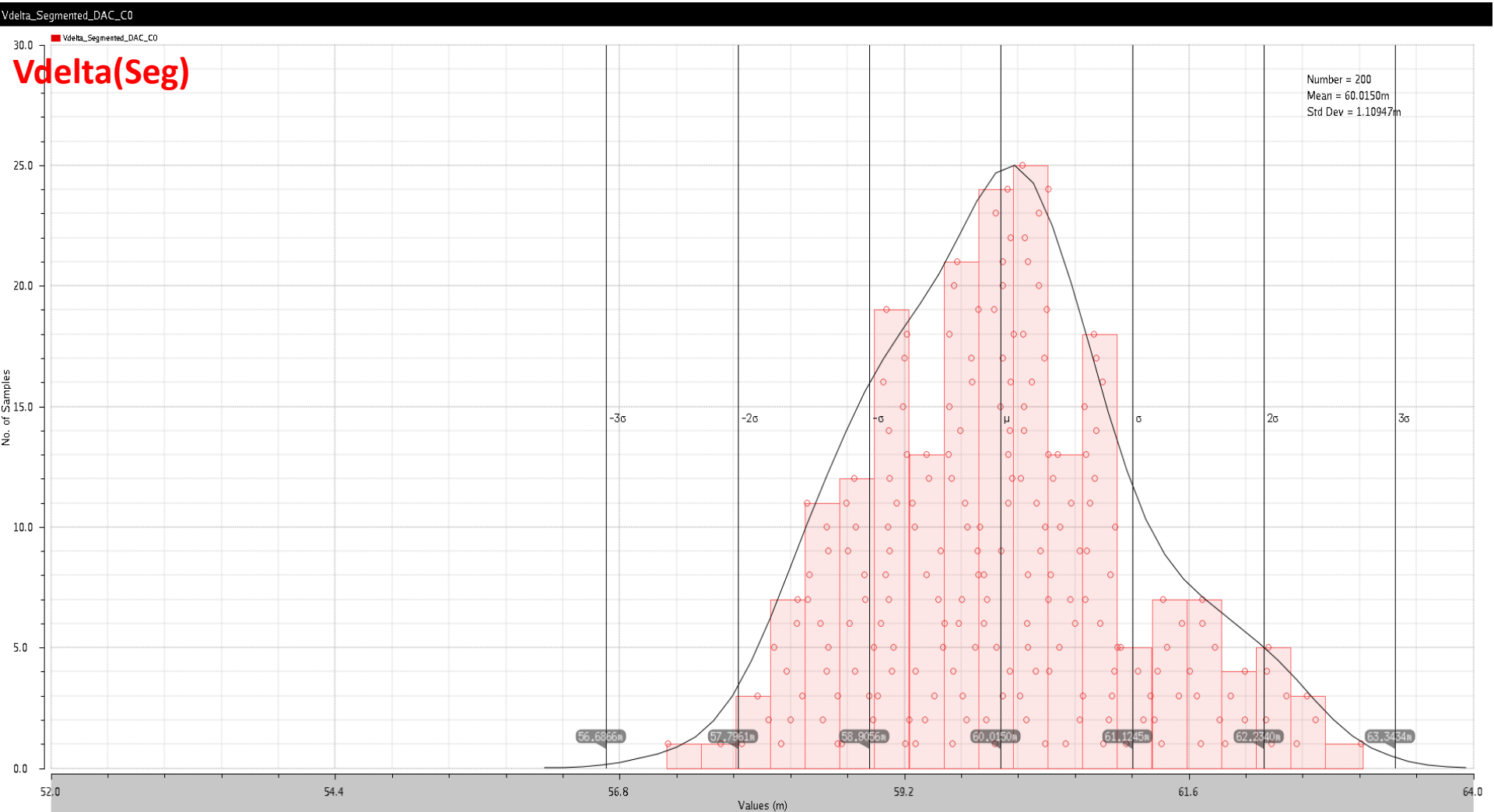


Monte Carlo Simulation (Segmented DAC)

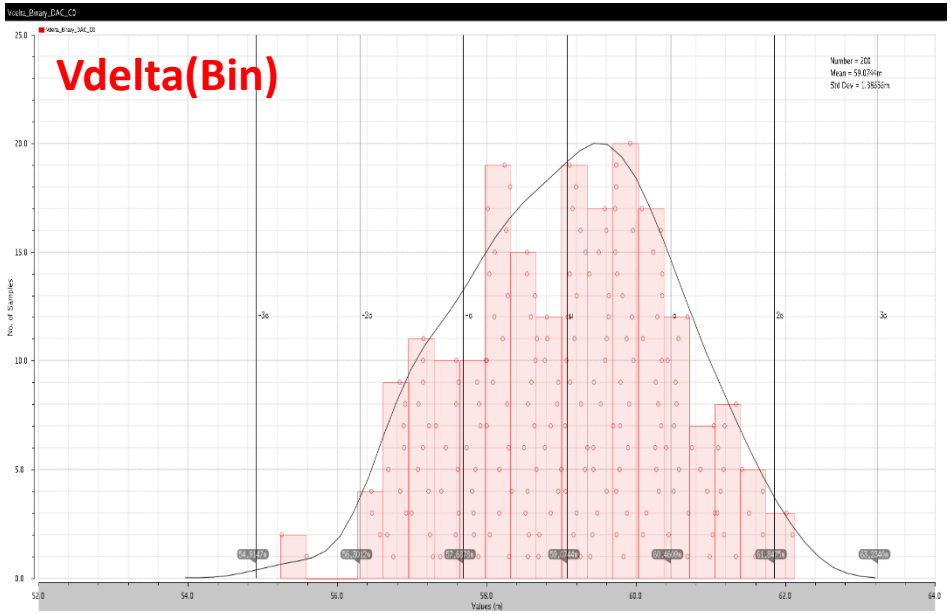


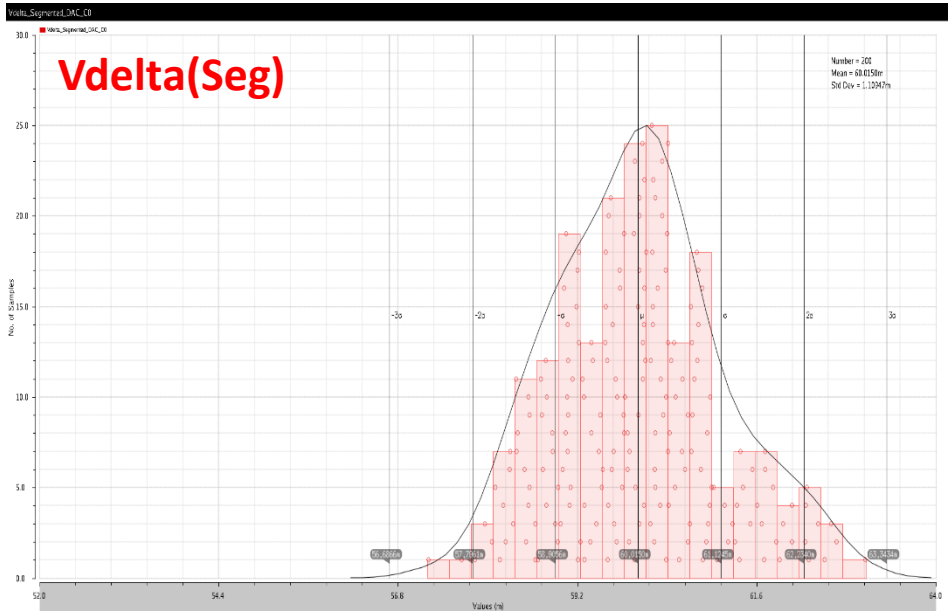


Monte Carlo Simulation (Segmented DAC)



Monte Carlo Simulation (Binary DAC VS Segmented DAC)



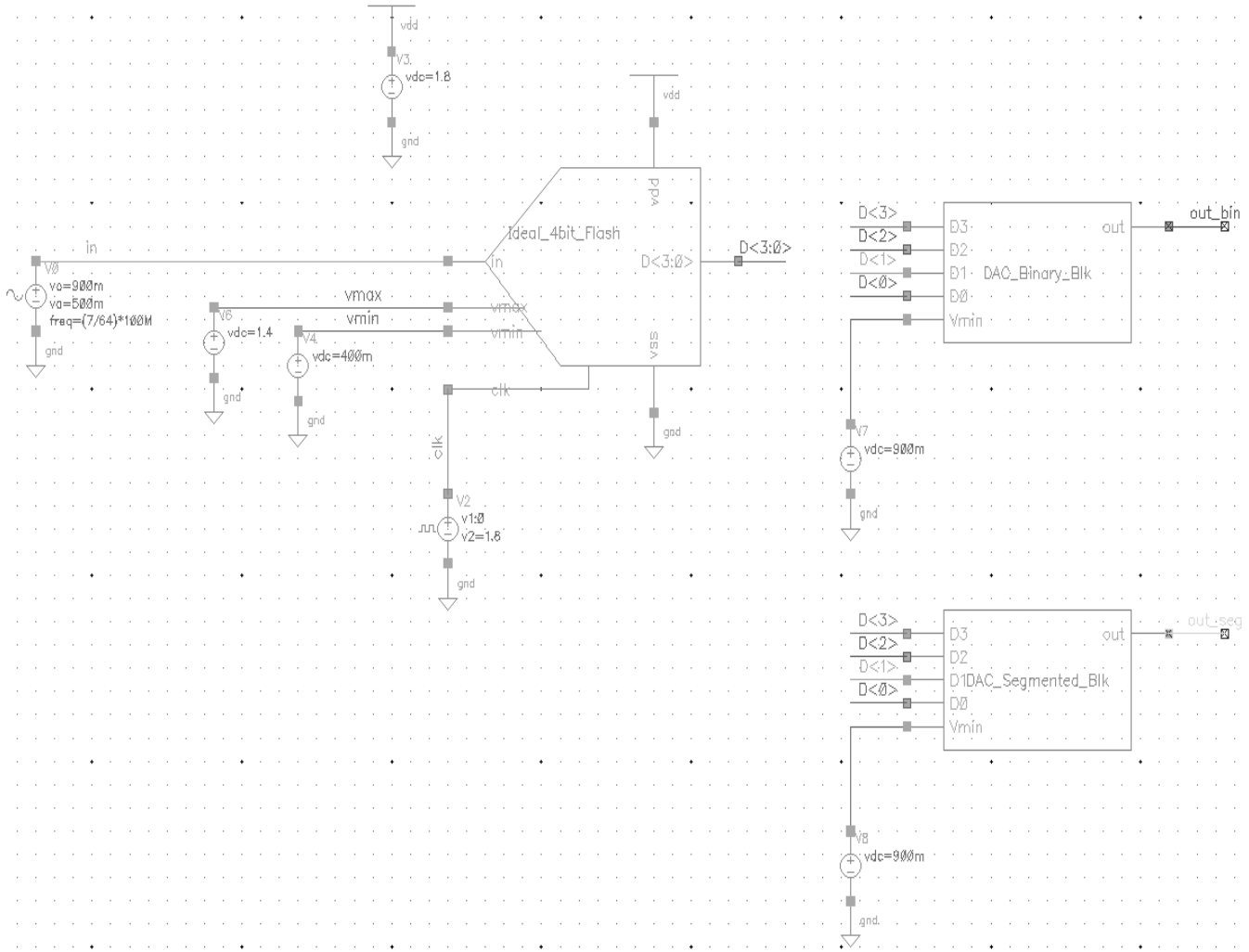


Parameter	Binary DAC	Segmented DAC
Mean (μ)	**59.074 mV**	**60.015 mV**
Standard Deviation (σ)	**1.3866 mV**	**1.1095 mV**
5 σ	**6.933 mV**	**5.548 mV**
X	**7**	**7**

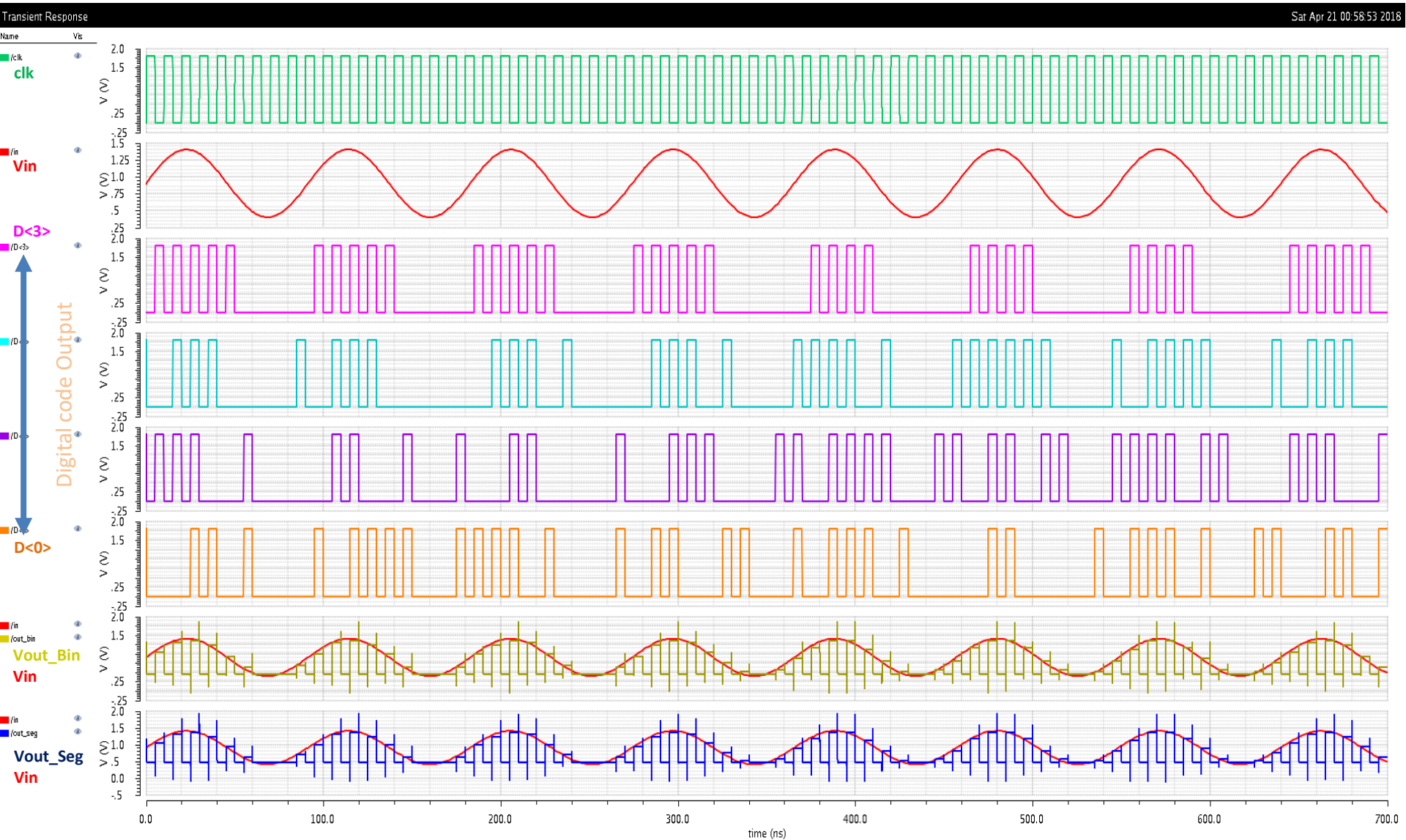
- Both 5*σ of the 2 DACs are less than 1/8 of 1 LSB (~7.8mV) by choosing X = 7, which is the factor multiplied by all Ws & Ls of the Biasing & the Current Mirrors transistors.
- The standard deviation of the segmented DAC is smaller than that of the Binary DAC, giving better DNL performance.

(5)
Transient Simulations of the Whole System

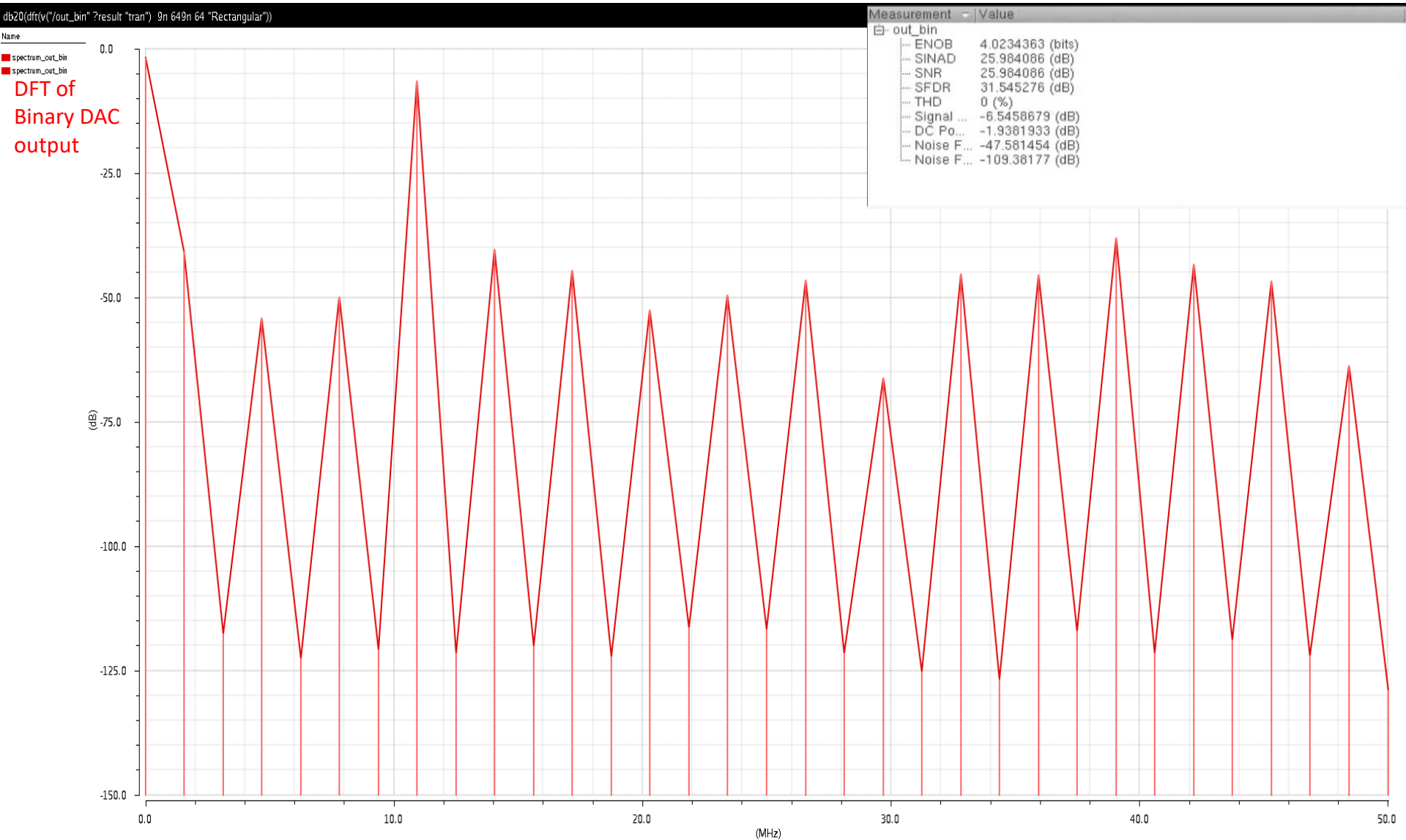
Whole System Testbench



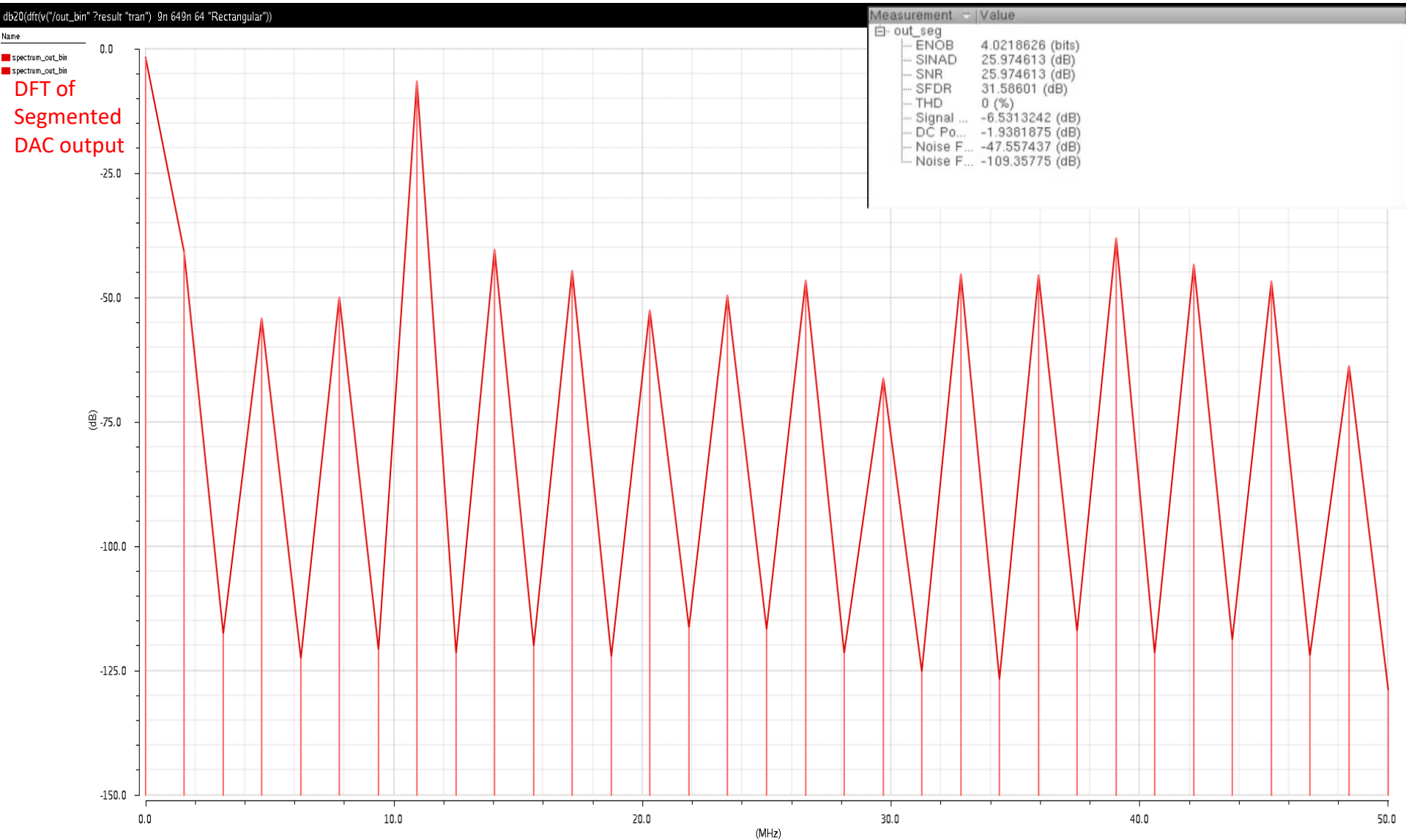
Waveforms


Transient Response
Sat Apr 21 00:58:53 2018
Name
Vis
/clk
clk
/in
Vin
D<3>
/D<3>
Digital code Output
D<0>
/D<0>
/out_bin
Vout_Bin
/out_seg
Vout_Seg
V (V)
time (ns)
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0

DFT of Binary DAC output



DFT of Segmented DAC output



SUMMARY

Summary Notes:

- When designing the high-swing biasing circuit, it is important to size the transistors such that the current mirror transistors would have a small Vds while also being in saturation, or else the variation seen in the Monte Carlo will be high.
- Increasing the W & L of the biasing & the current mirror circuits decreases the standard deviation observed in the Monte Carlo simulation, which means giving a better DNL performance.
- The Segmented DAC is shown to have smaller variation (standard deviation) than that in the Binary DAC.