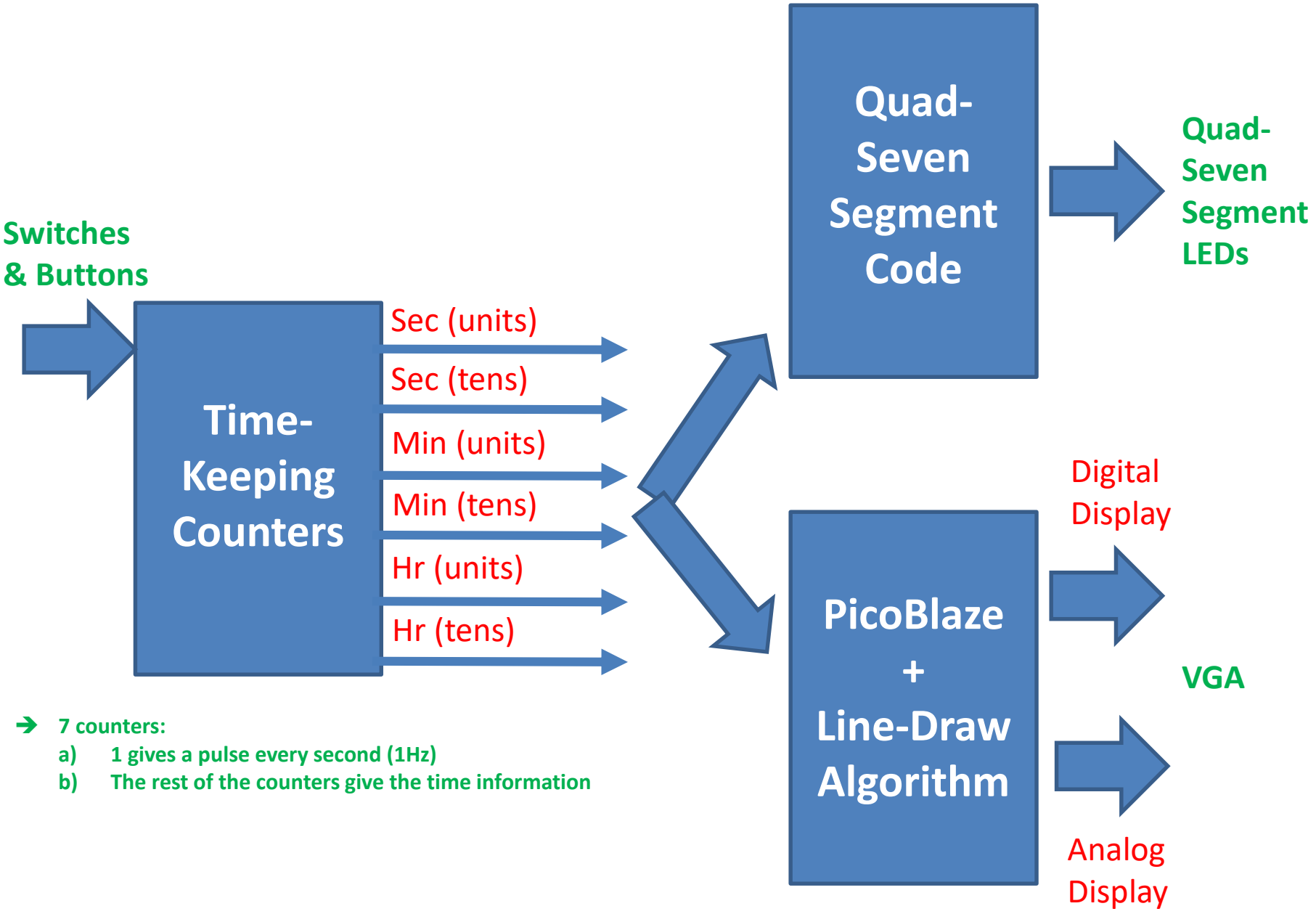
Digital & Analog Clock Display using FPGA

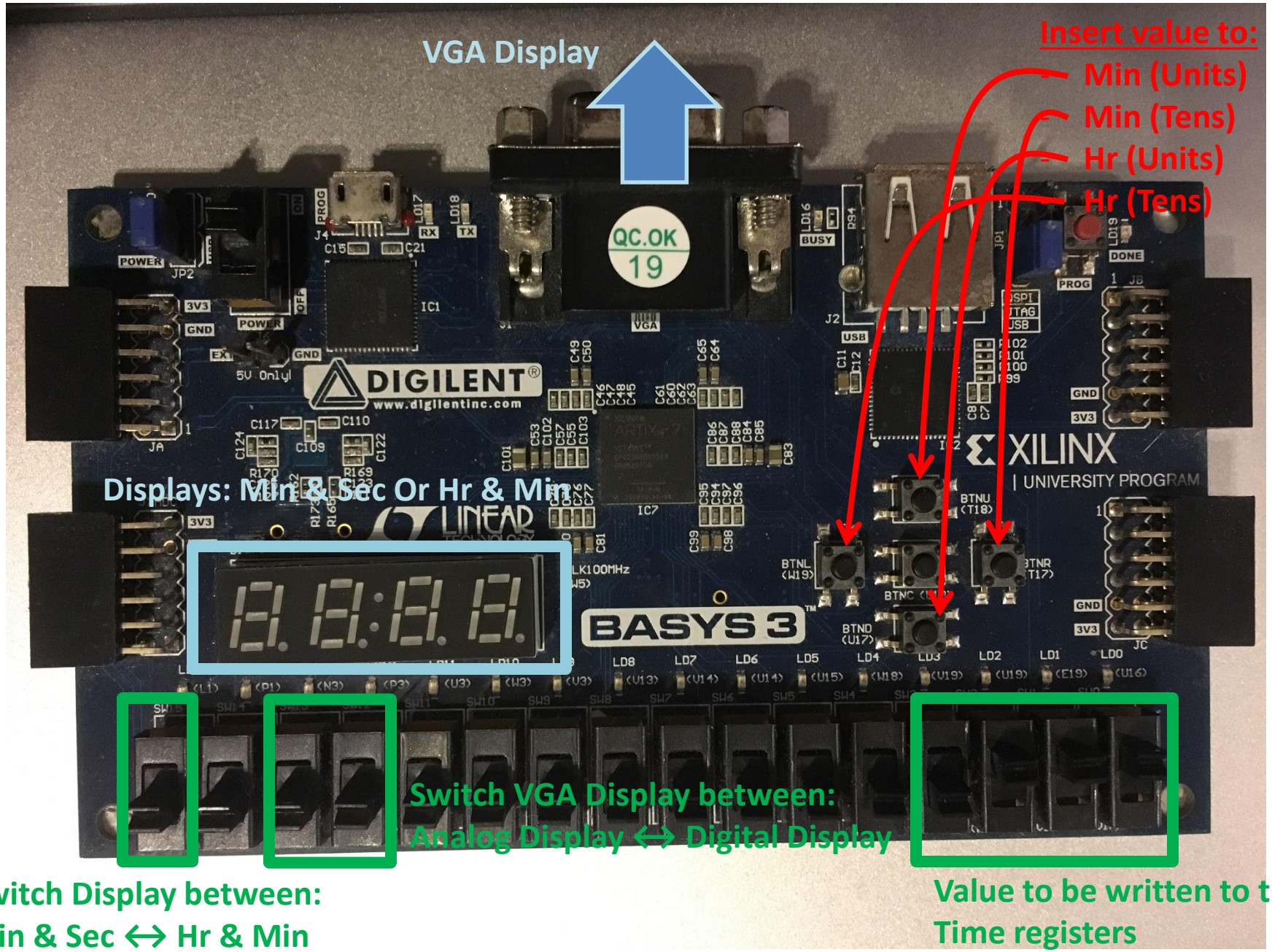
Group 4



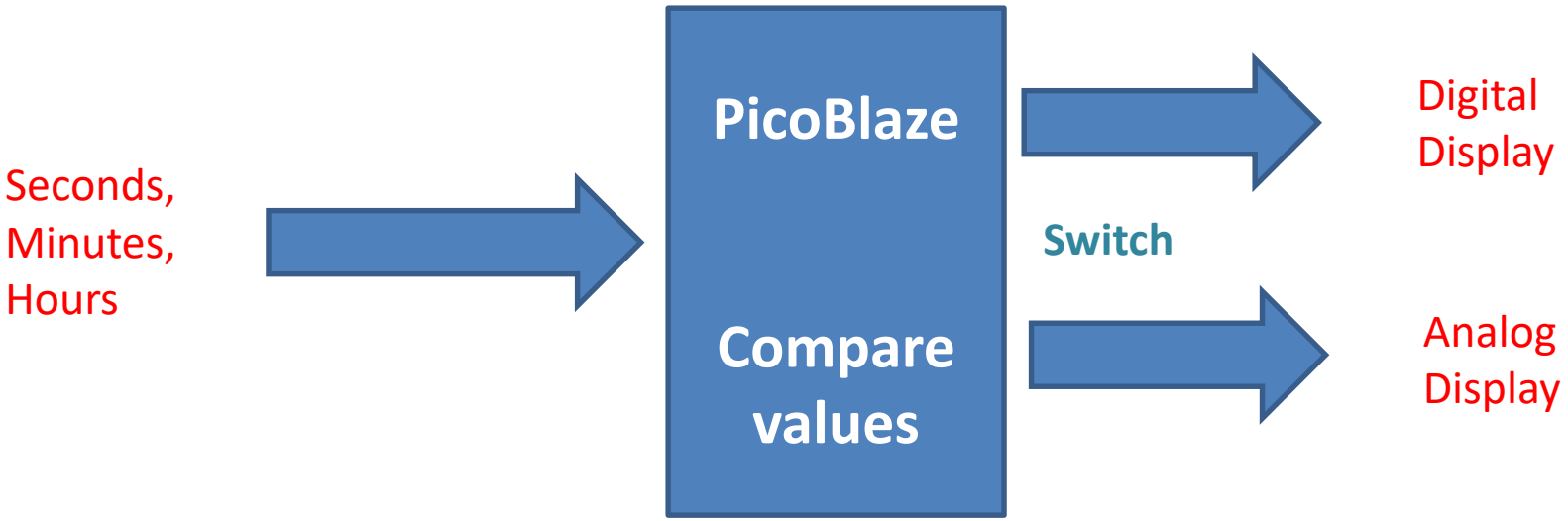
➔ 7 counters:

a) 1 gives a pulse every second (1Hz)

b) The rest of the counters give the time information


VGA Display
Insert value to:
Min (Units)
Min (Tens)
Hr (Units)
Hr (Tens)
Displays: Min & Sec Or Hr & Min
Switch VGA Display between:
Analog Display ↔ Digital Display
Switch Display between:
Min & Sec ↔ Hr & Min
Value to be written to the
Time registers

VGA Display

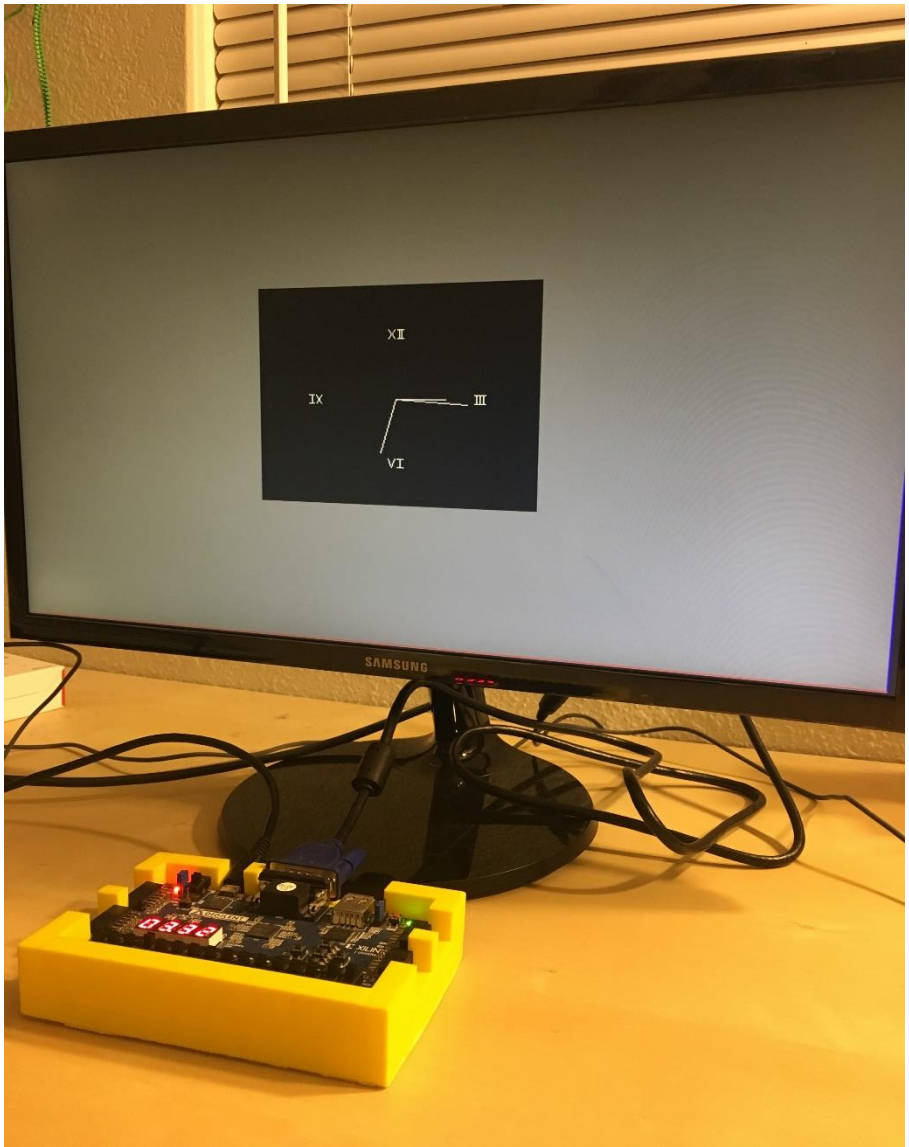


➔ **The idea is:**

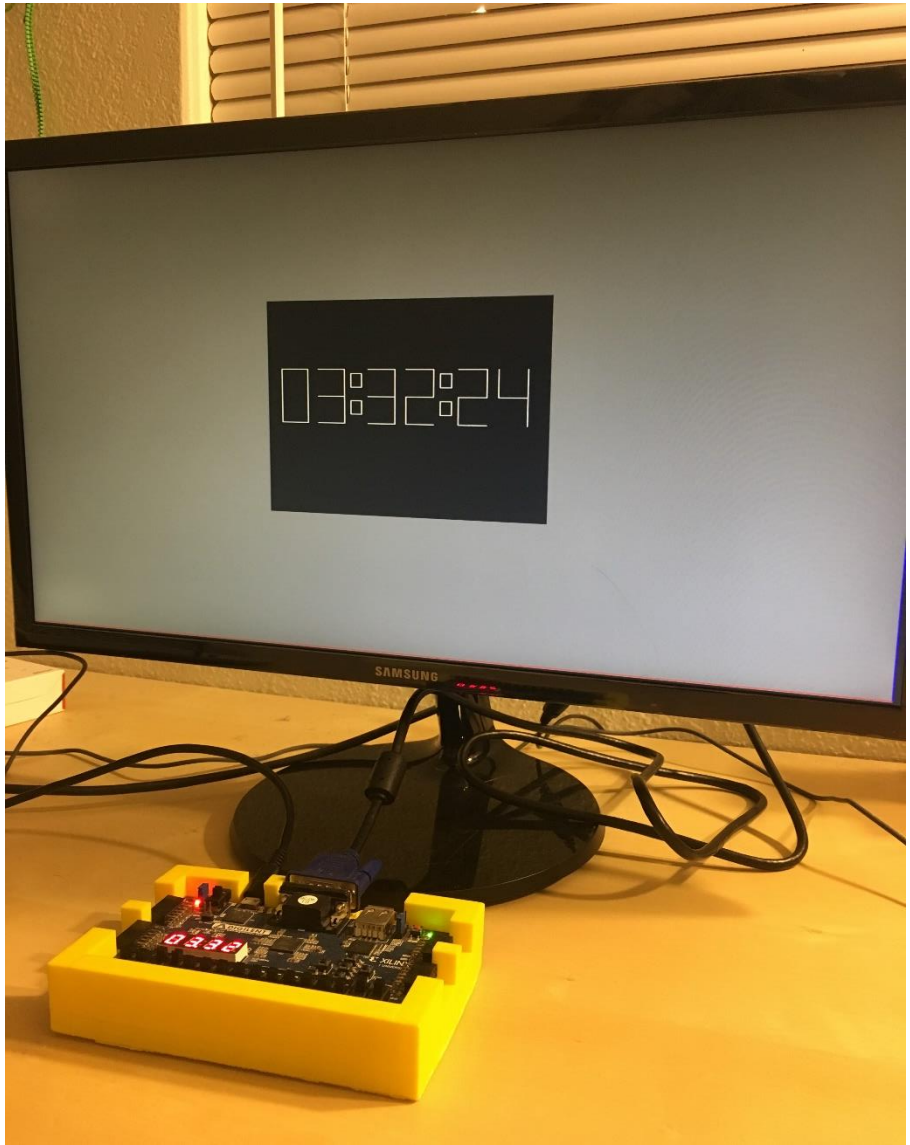
a) First, the time information are stored in 6 registers in the picoblaze.
b) Then, the "Sec-Units" is compared with all numbers 0-9.
c) According to its value, the program jumps to a certain set of code lines that draw (using the drawing algorithm code) that certain number
d) When that is done, the same will be done to "Sec-Tens", … & so on.

e) The whole frame is drawn every 1/60th of a second. There is an interrupt that comes to the picoblaze from the outside (draw line algorithm block) every 1/60th of a second.
f) The frame is erased before drawing every 1/60th of a second.

Analog Display



Digital Display



Links to the material

http://www.eric.crabill.org/

https://drive.google.com/drive/folders/1JvVr4amOXQE0dqAIHVlUzsUnugPQMXc1?usp=sharing

Project:

https://drive.google.com/drive/folders/1QCiNa7iVuNNrkJ16X37NimUBDMLxXcll?usp=sharing