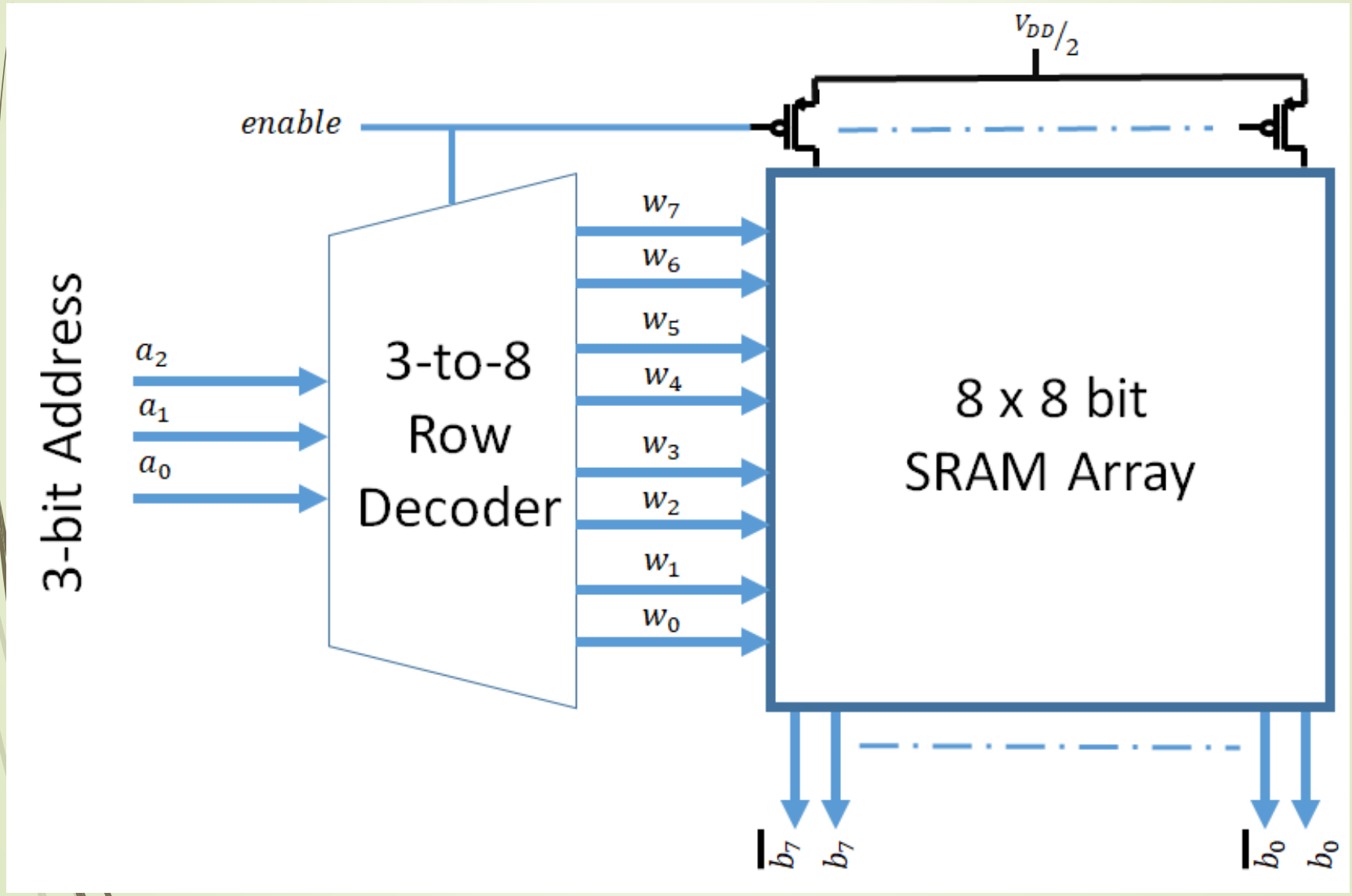
8x8 SRAM Array Design

Muhammad Aldacher

Overview

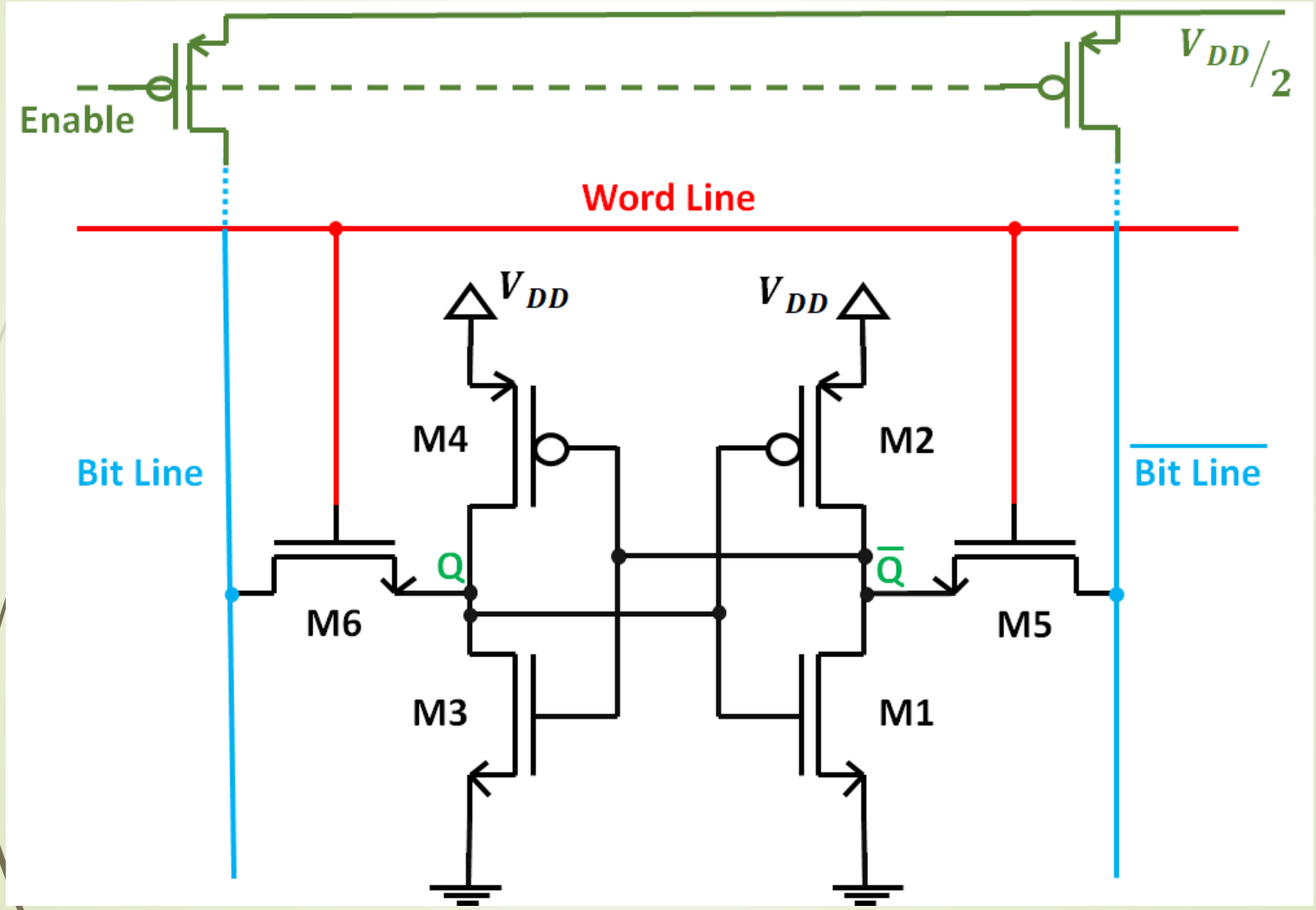
- System Block Diagram
- SRAM Cell
- Decoder Circuits
- Layout
- Final Results
- Future Work

1. System Block Diagram



2. SRAM Cell

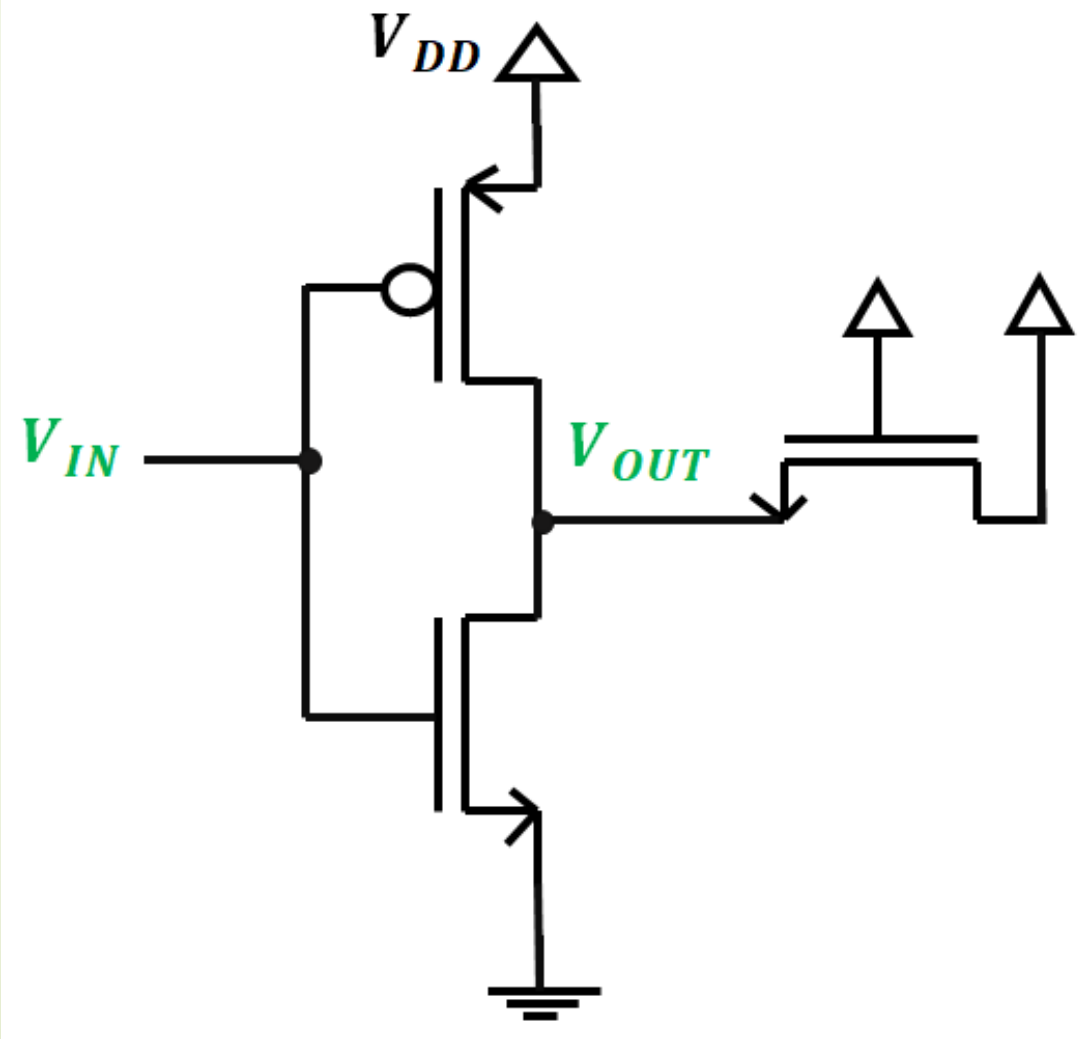
2.1. Circuit



2. SRAM Cell

2.2. Read Noise Margin

a) Testbench



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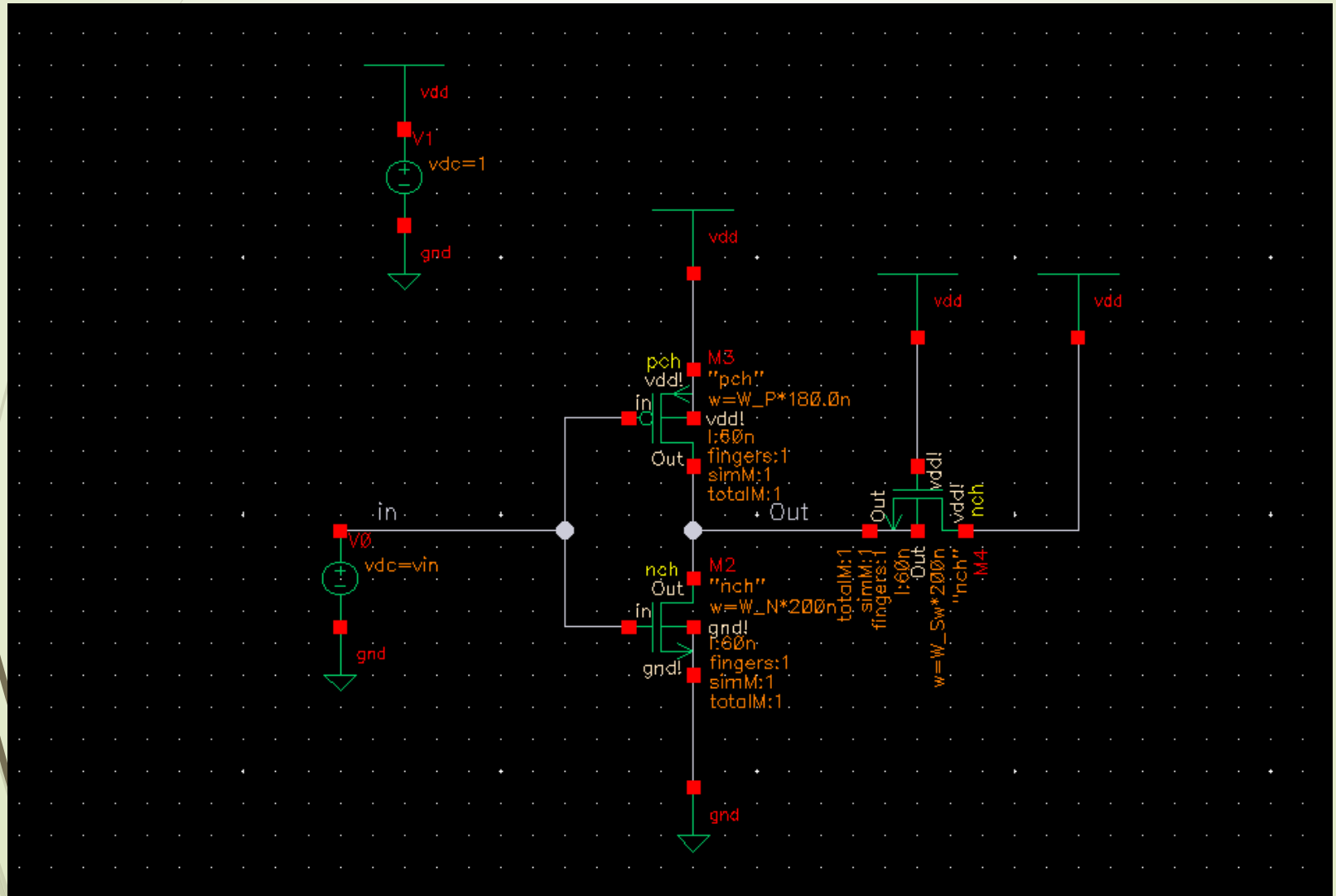
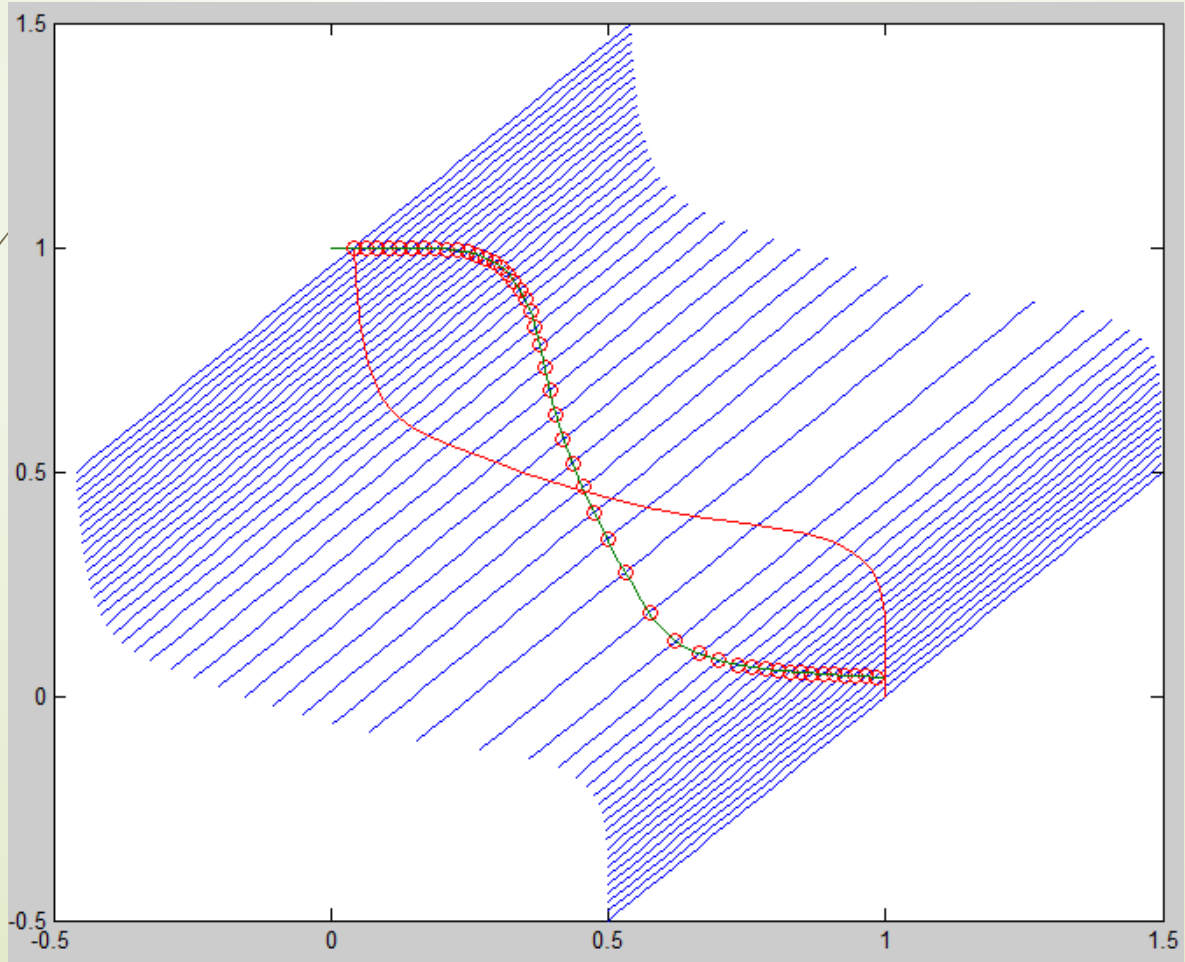


2. SRAM Cell

2.2. Read Noise Margin

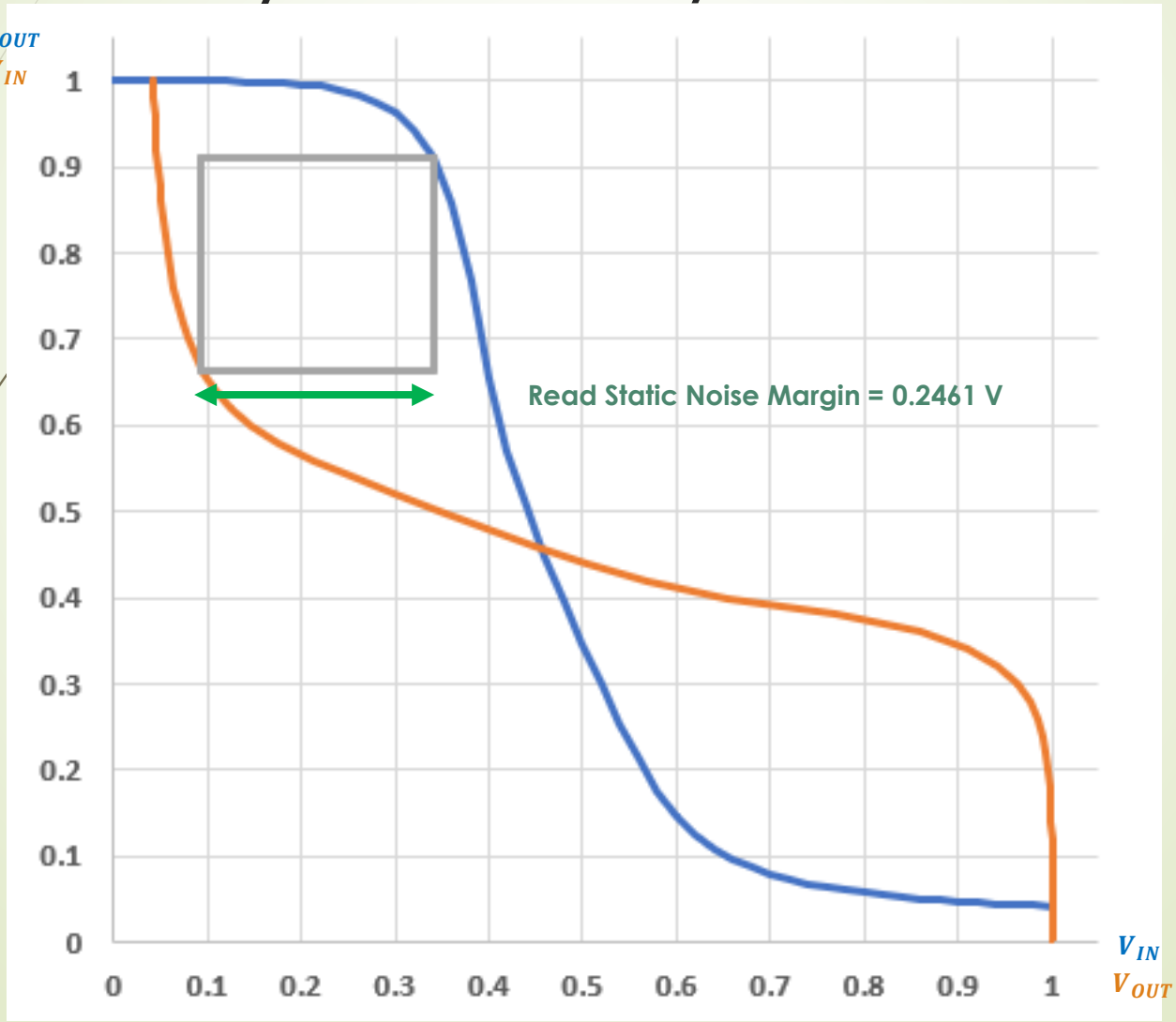
b) Finding largest diagonal (For SNM square)



2. SRAM Cell

2.2. Read Noise Margin

c) DC Analysis



2. SRAM Cell

2.3. Write Noise Margin

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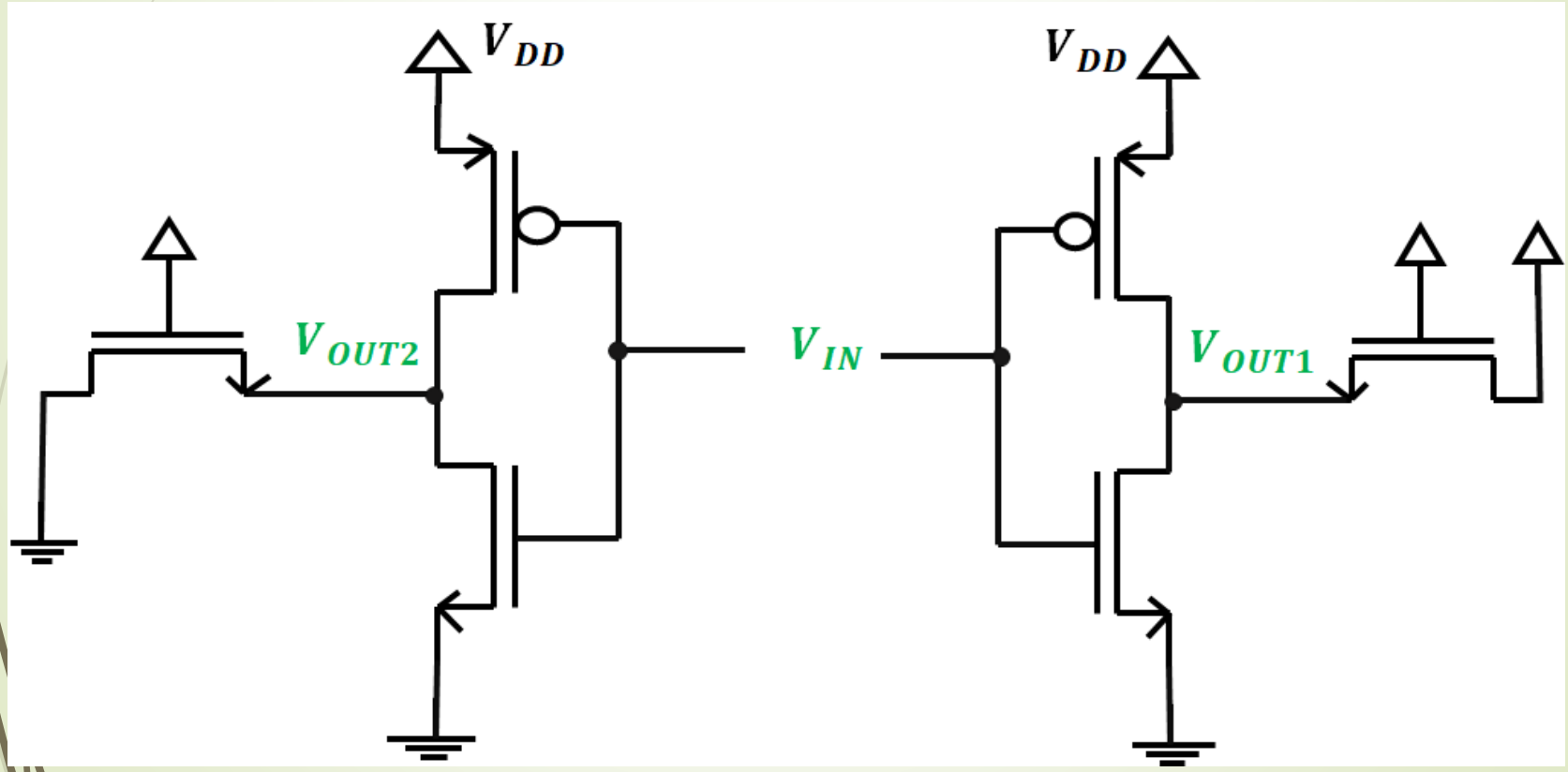

2. SRAM Cell

2.3. Write Noise Margin

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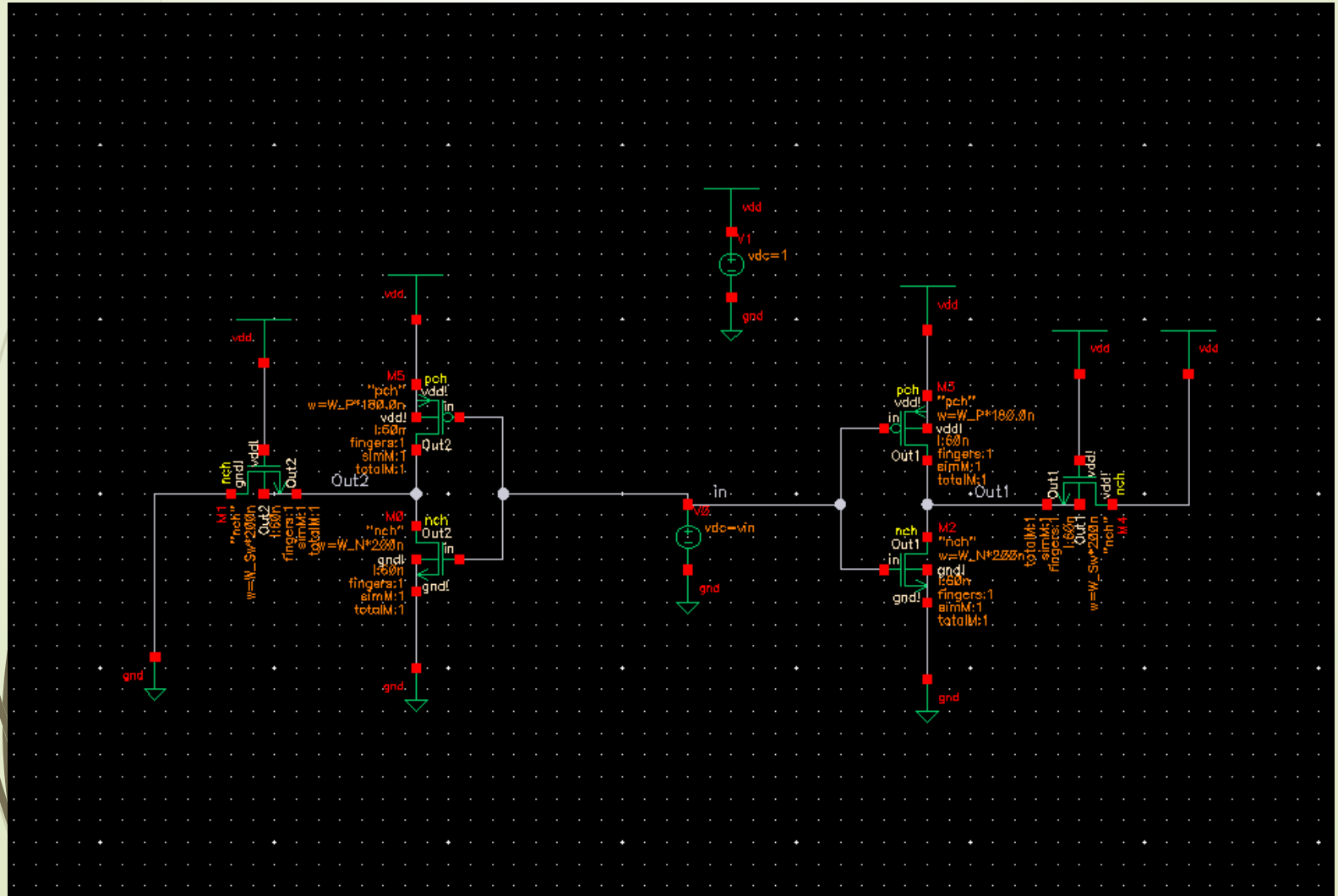

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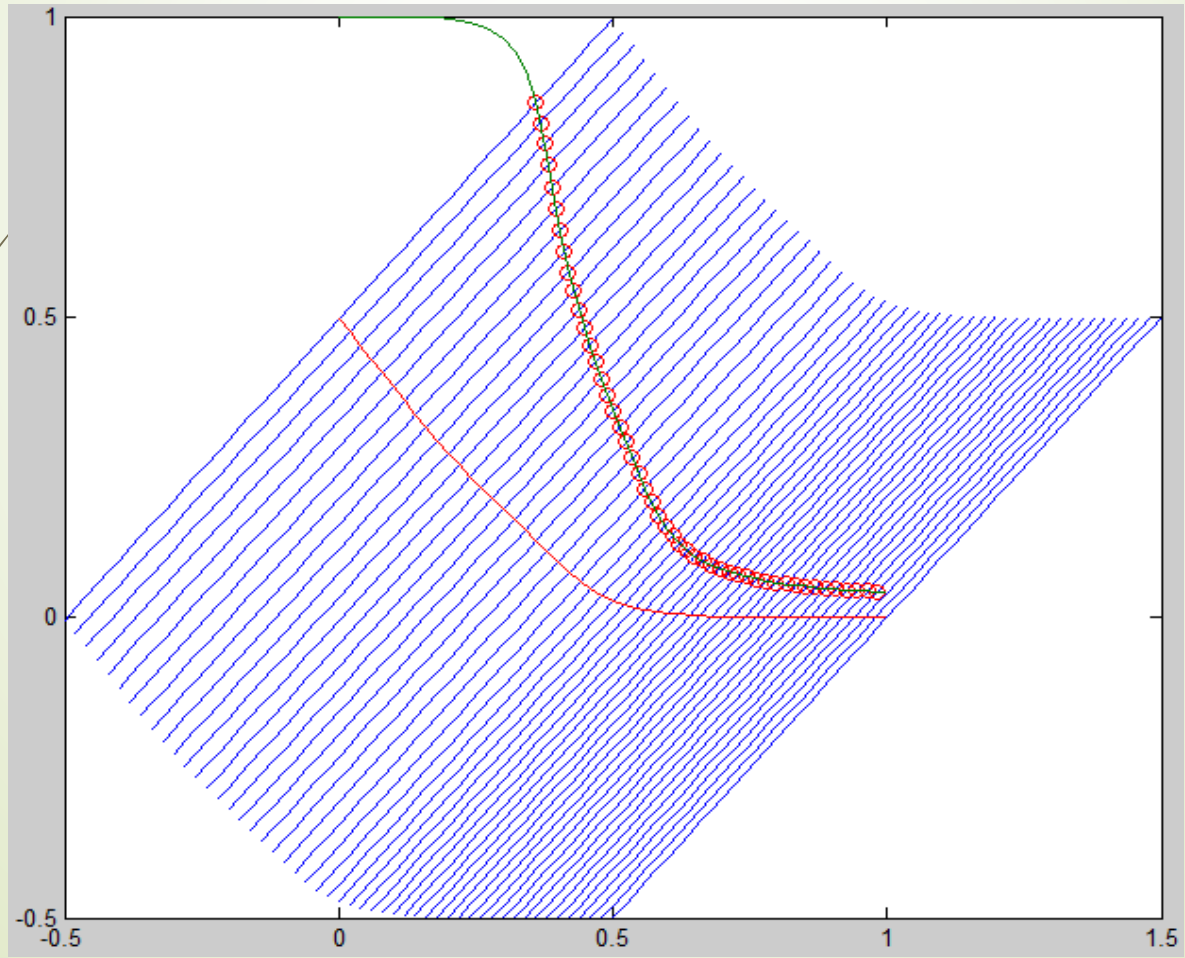
2.3. Write Noise Margin

b) Finding largest diagonal (For SNM square)



2. SRAM Cell

2.3. Write Noise Margin

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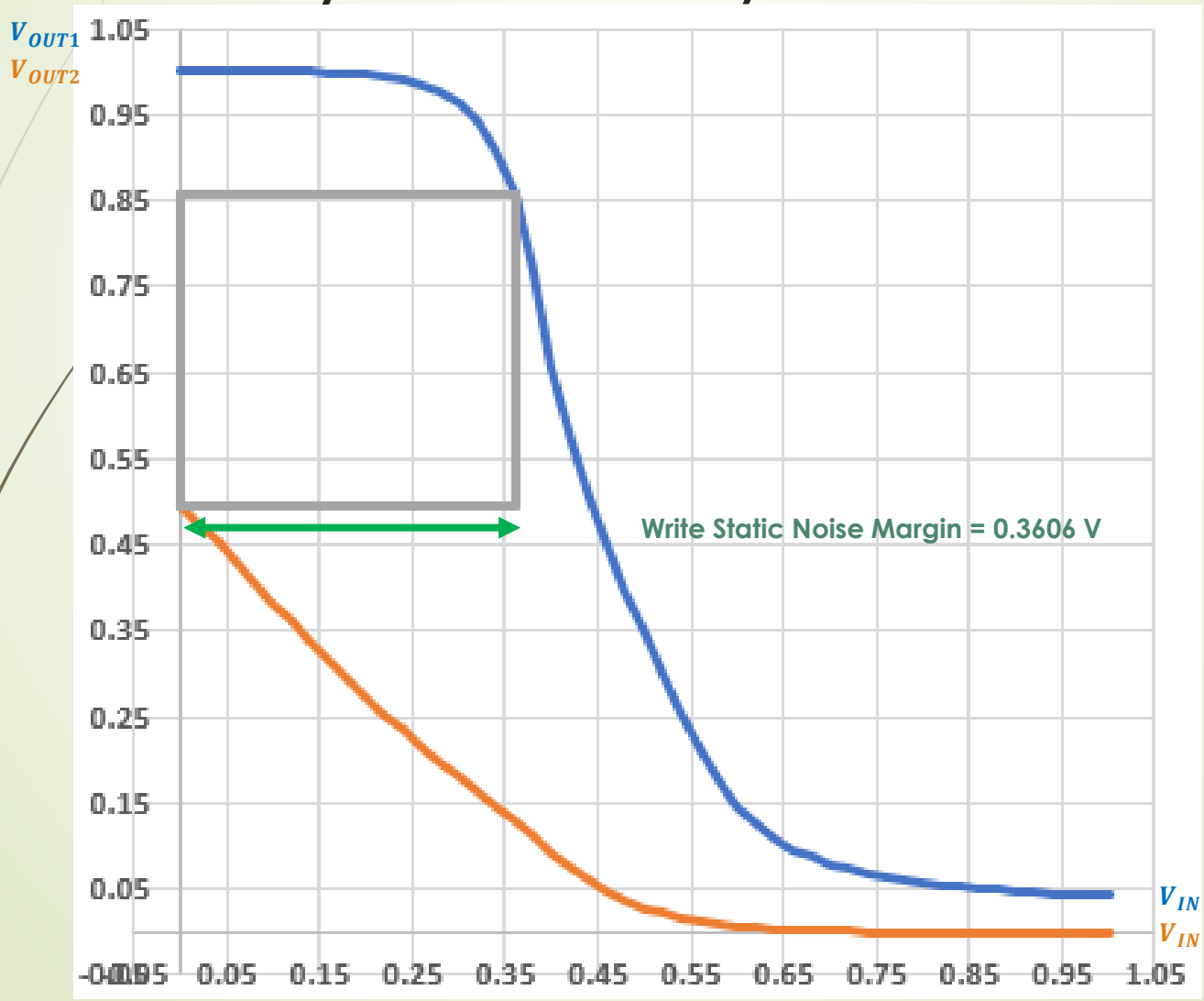
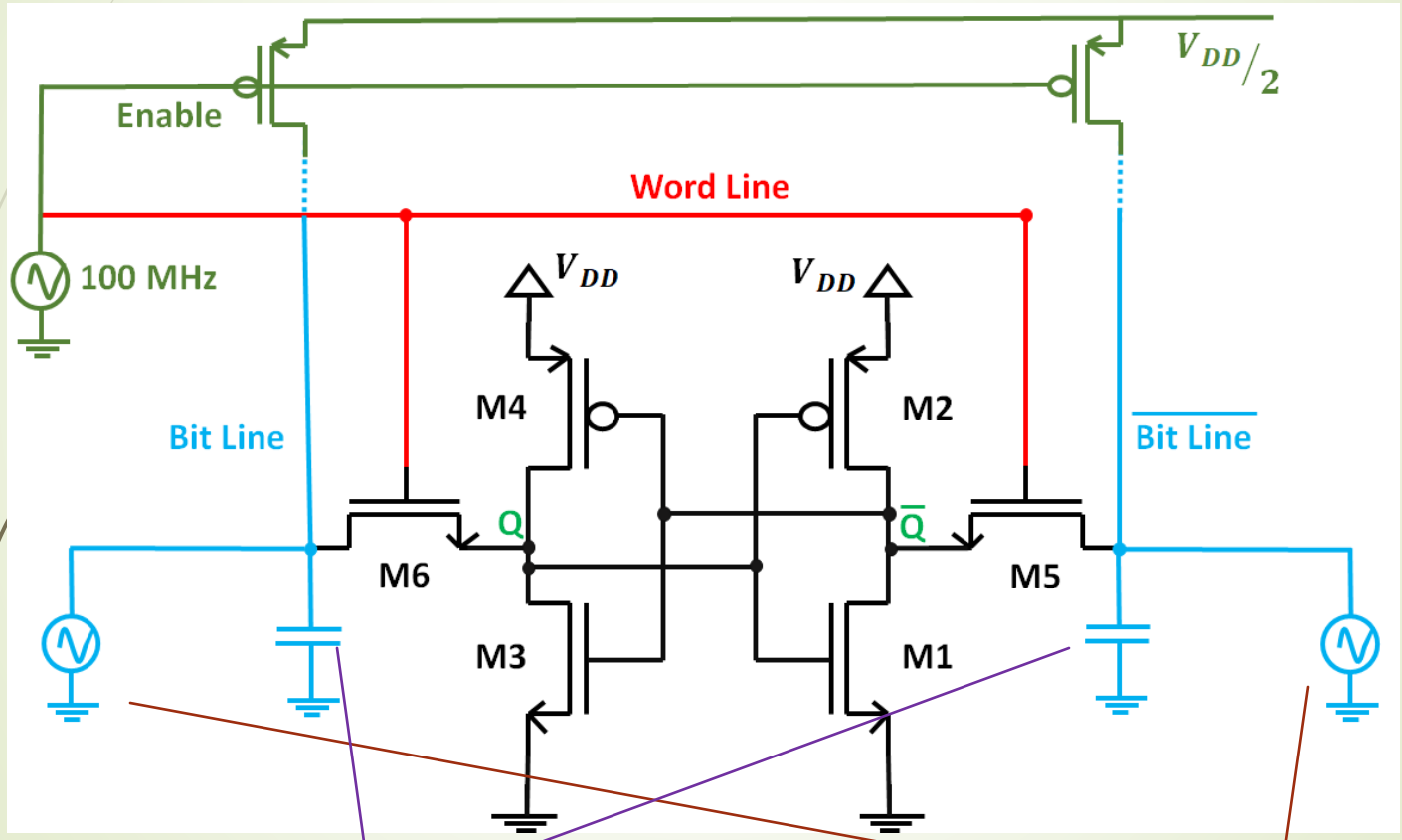


2. SRAM Cell

2.4. Transient Simulation

a) Testbench



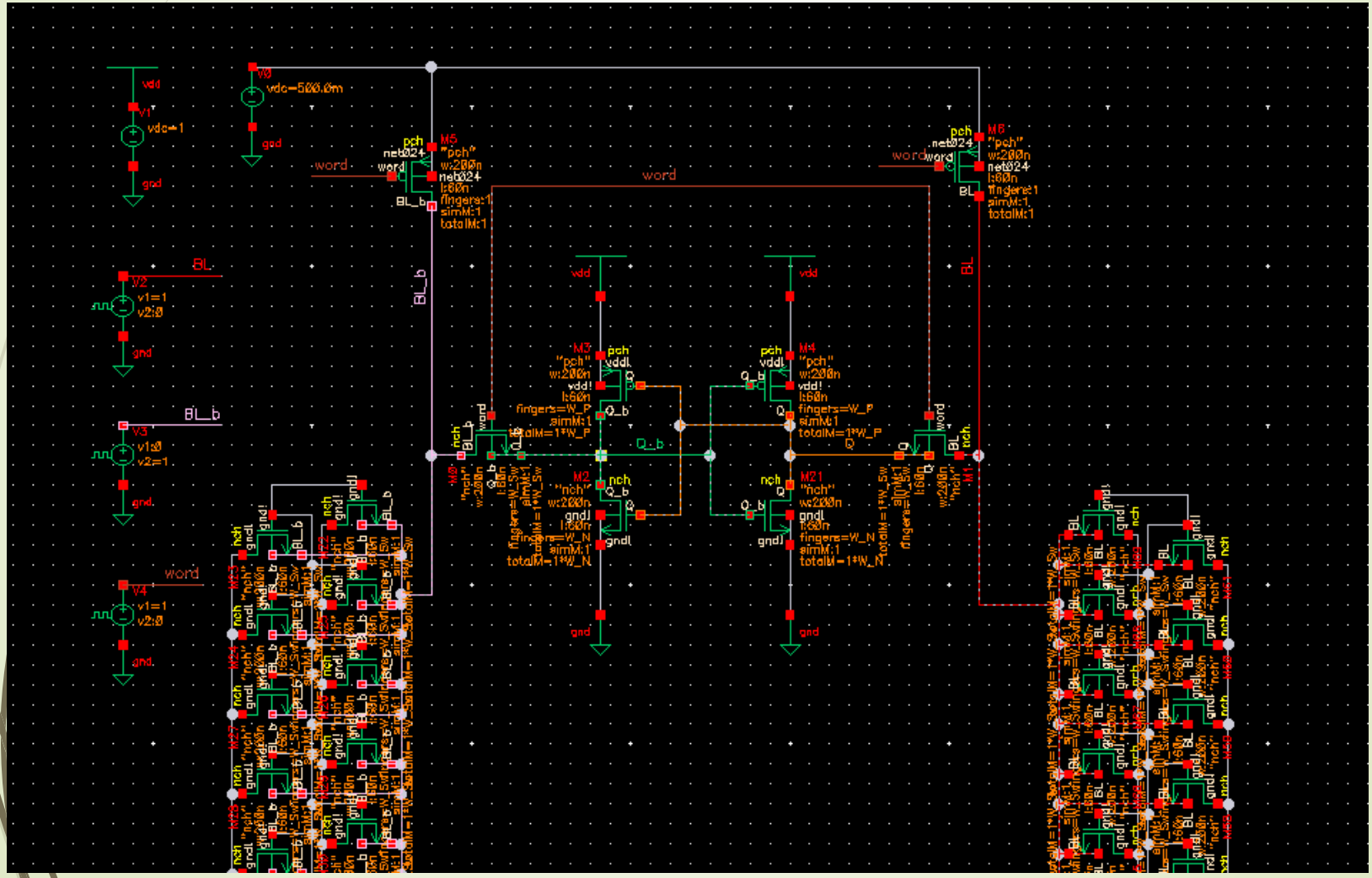
These Caps represent the other cells connected to the same bit-lines.

These sources are removed in Read Operation

2. SRAM Cell

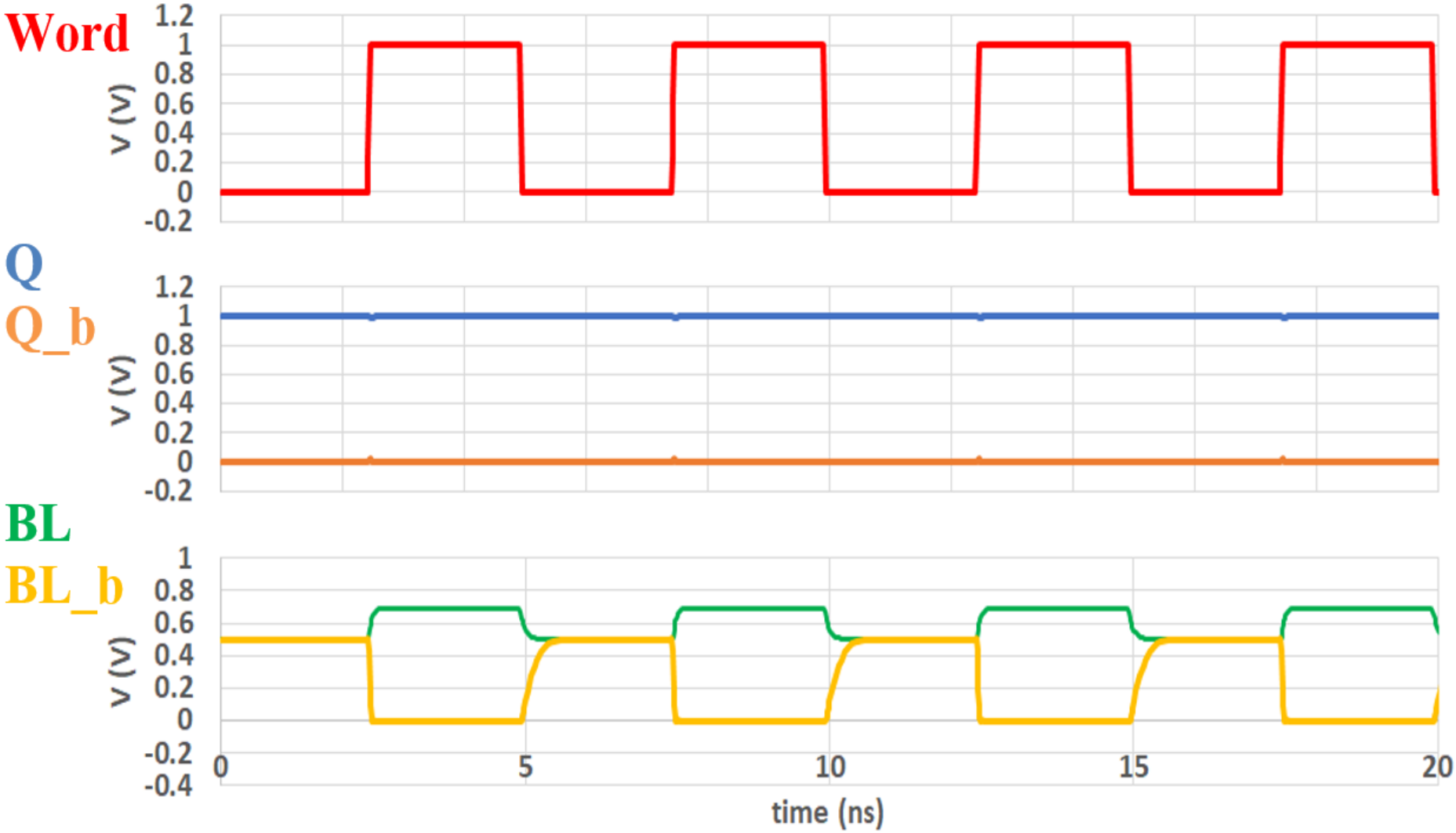
2.4. Transient Simulation

a) Testbench



2. SRAM Cell

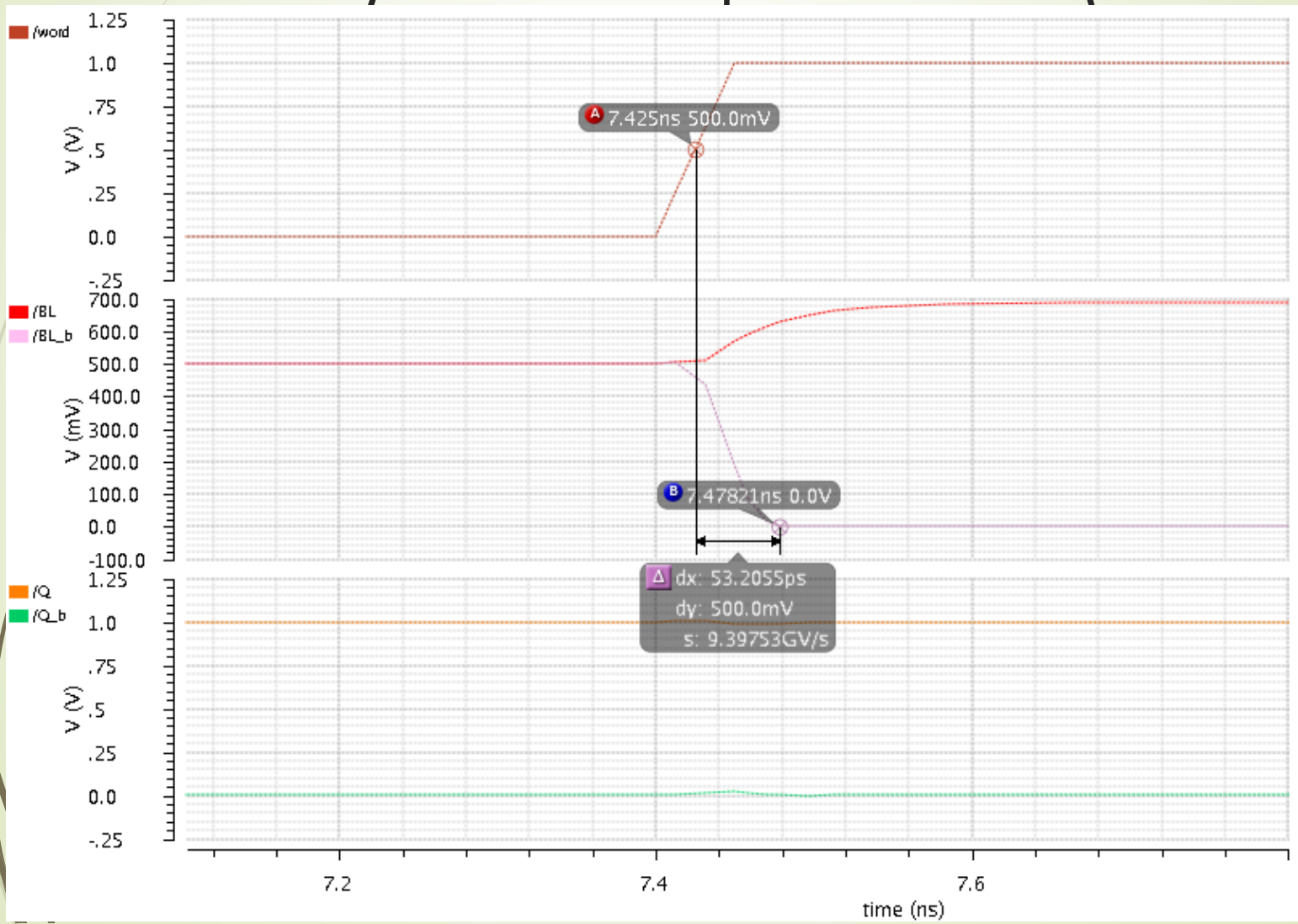
2.4. Transient Simulation
b) Read Operation



2. SRAM Cell

2.4. Transient Simulation

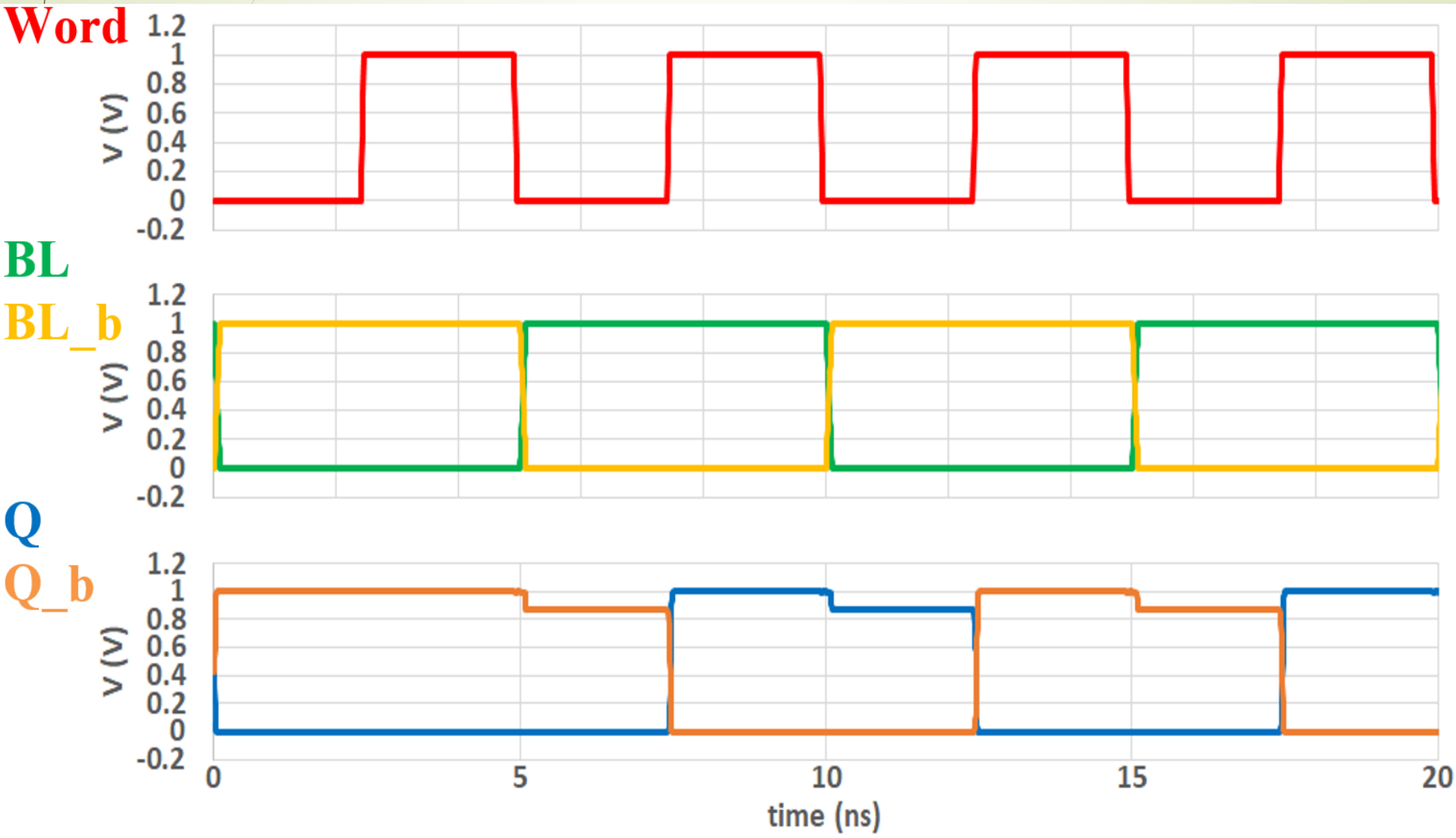
b) Read Operation (Delay)



2. SRAM Cell

2.4. Transient Simulation

c) Write Operation



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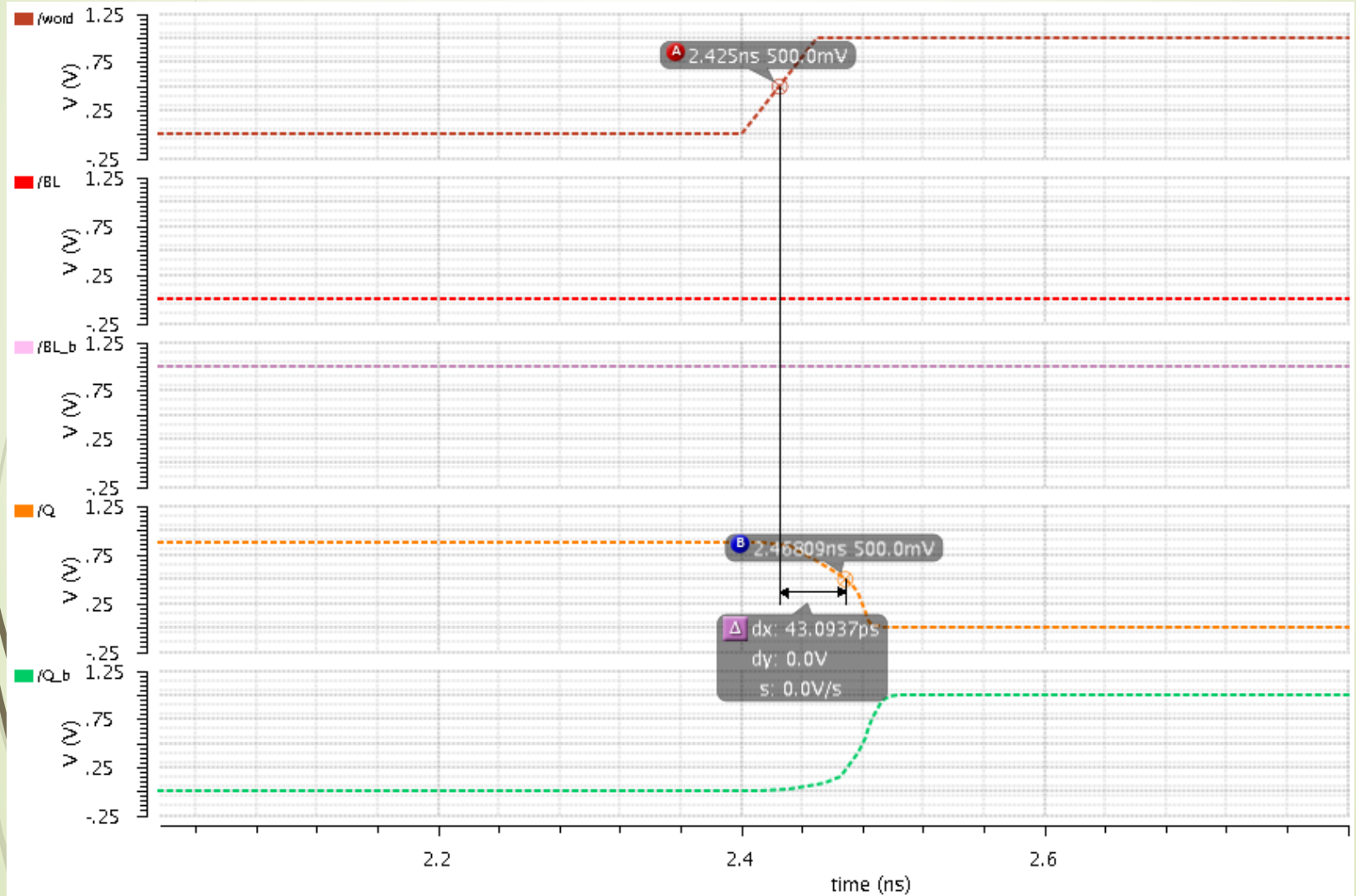
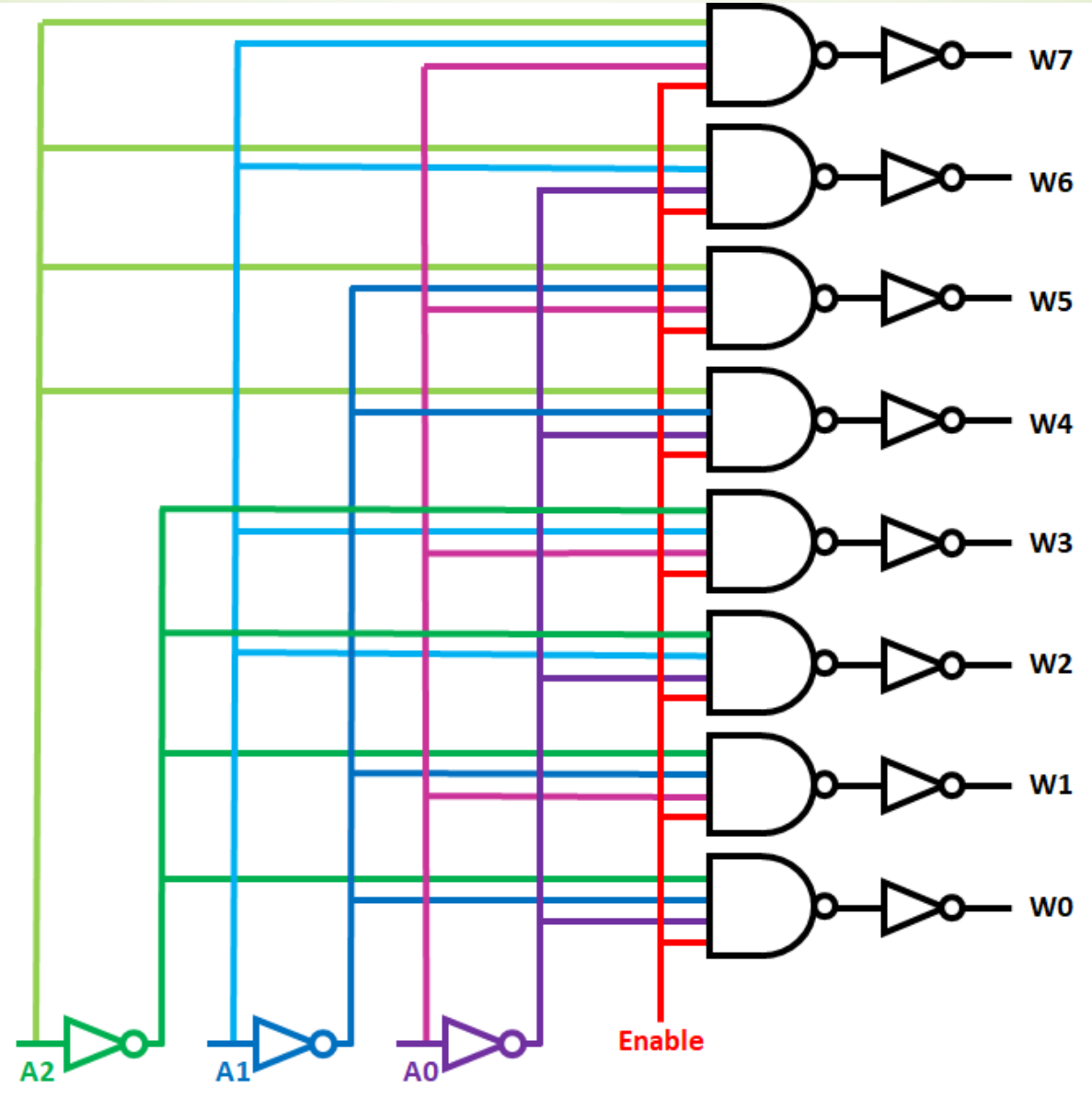
c) Write Operation (Delay)



3. Decoder

3.1. Circuit



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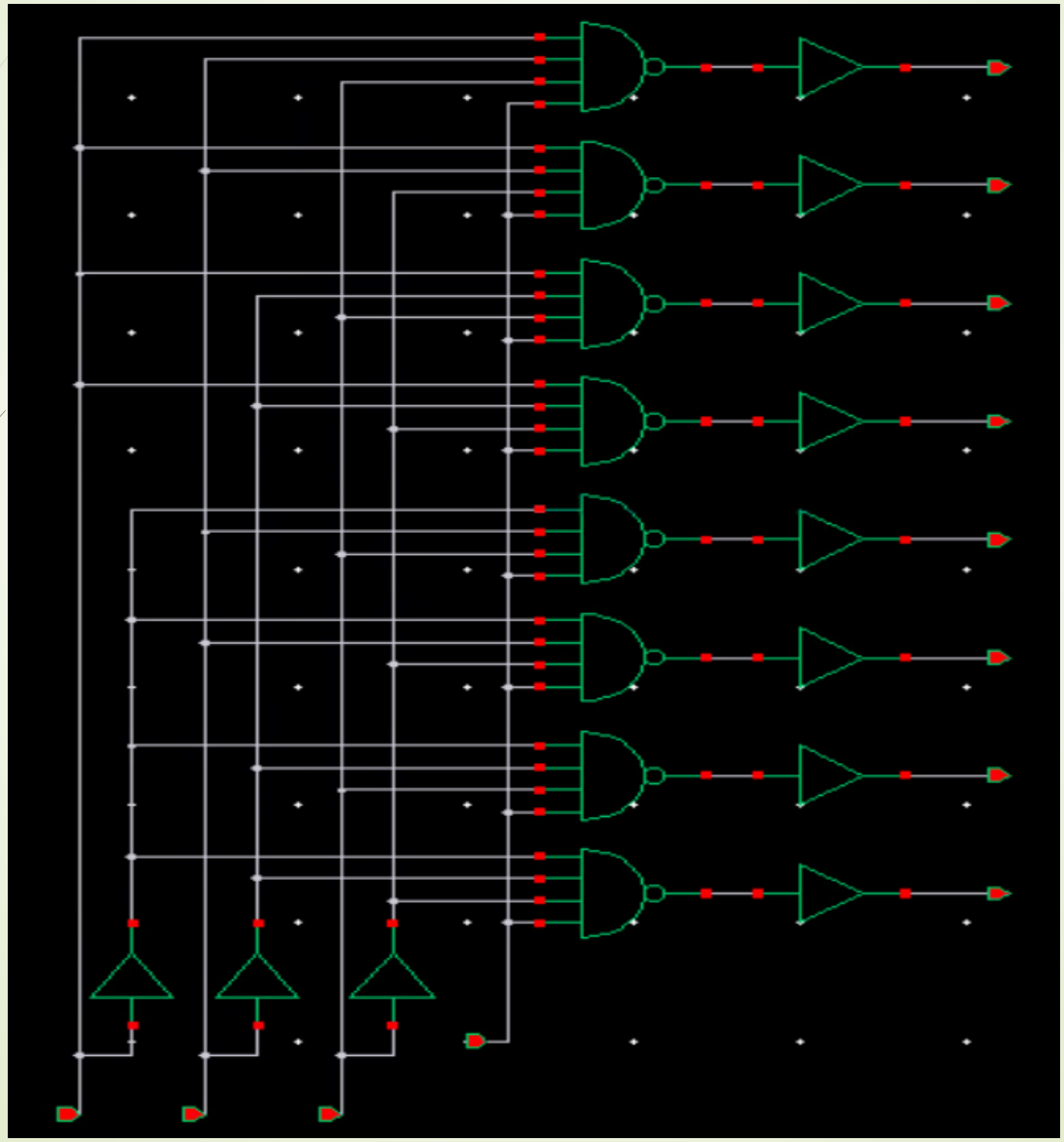
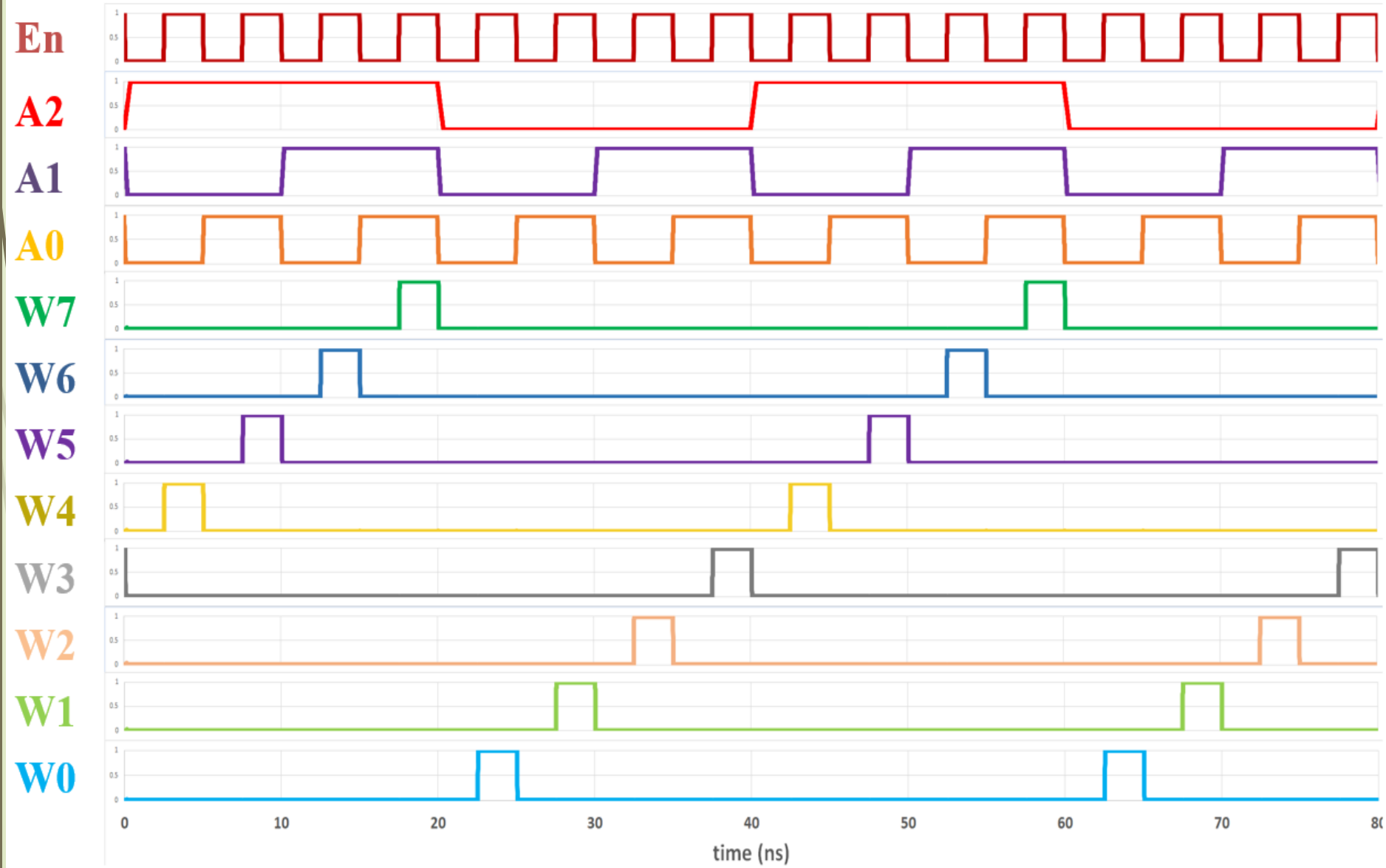


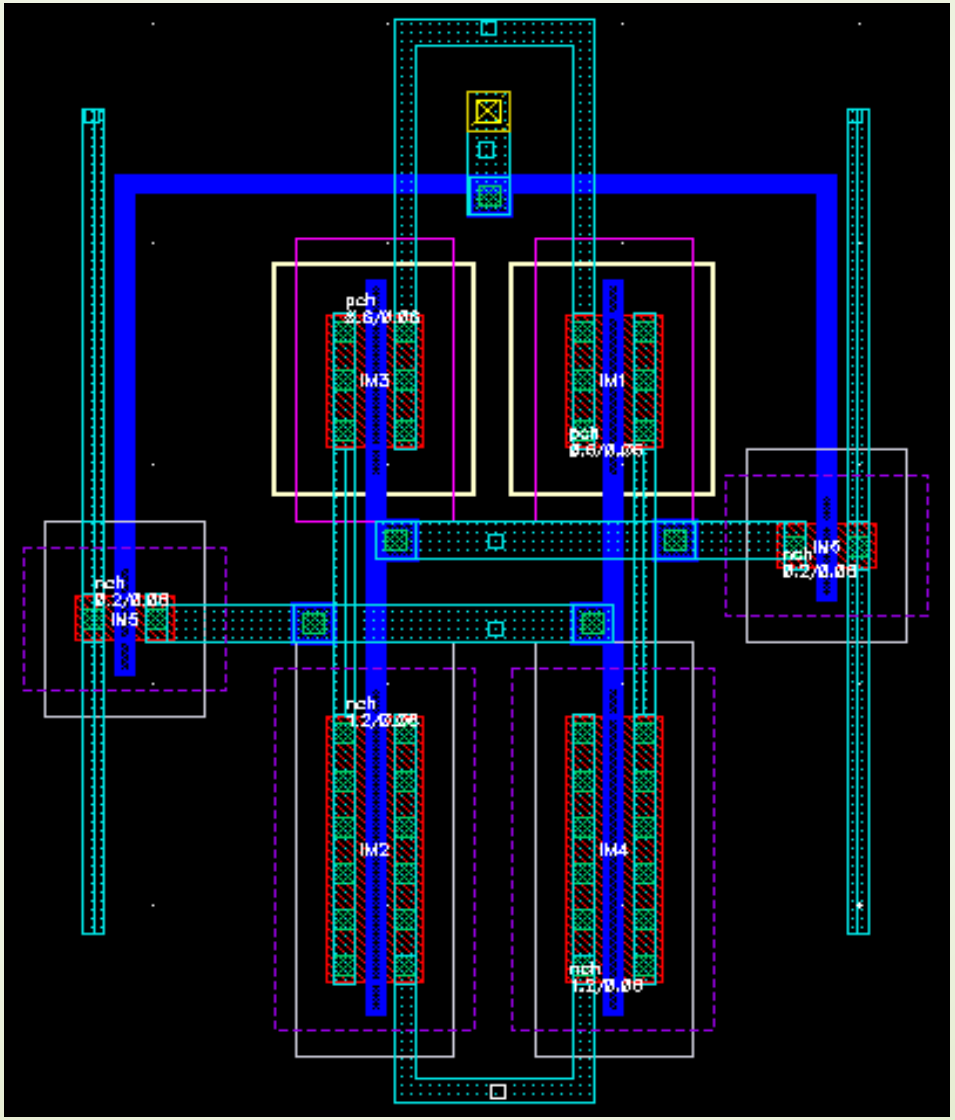
3. Decoder

3.2. Transient Simulation



4. LAYOUT

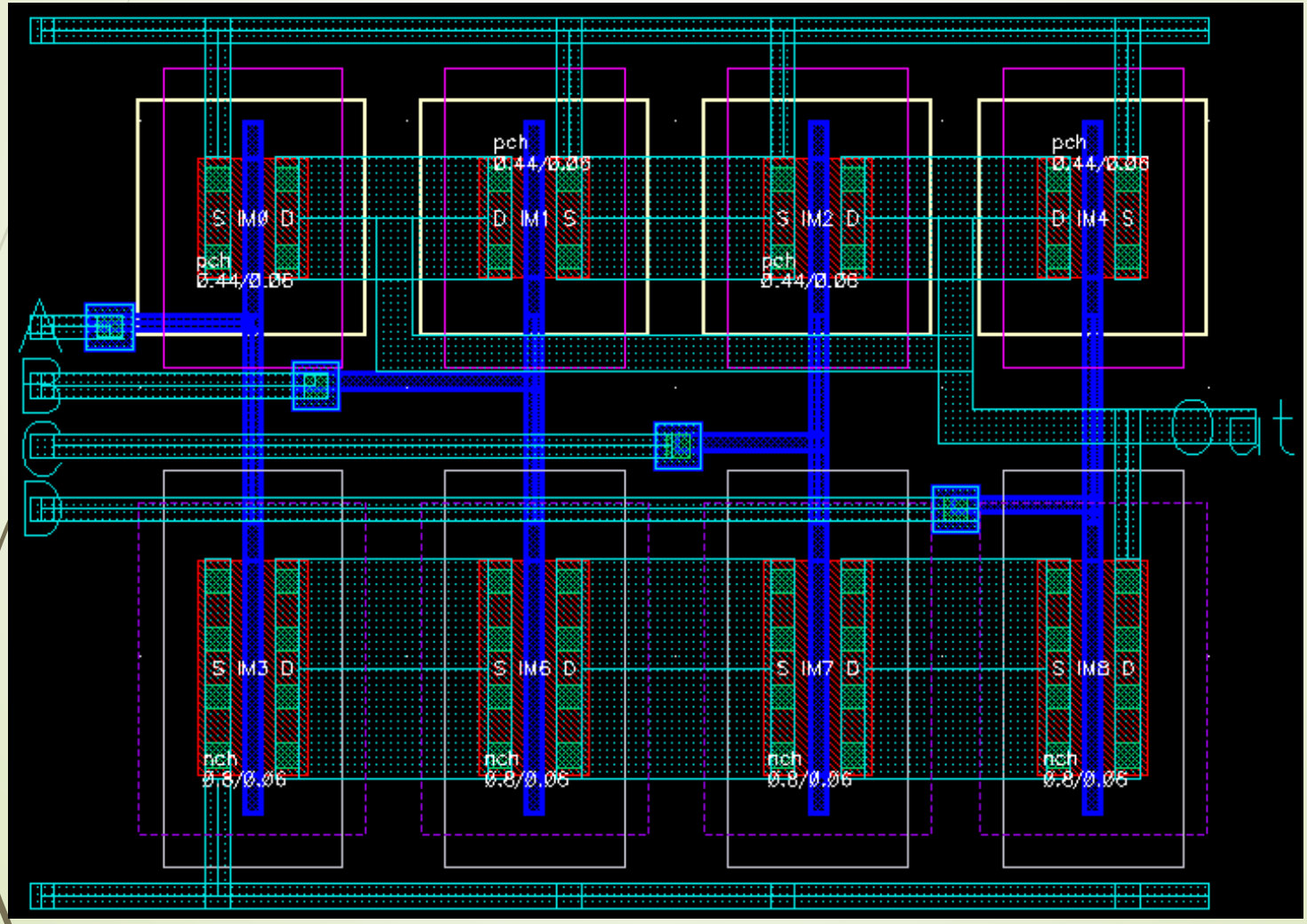
4.1. SRAM Cell



4. LAYOUT

4.2. Decoder

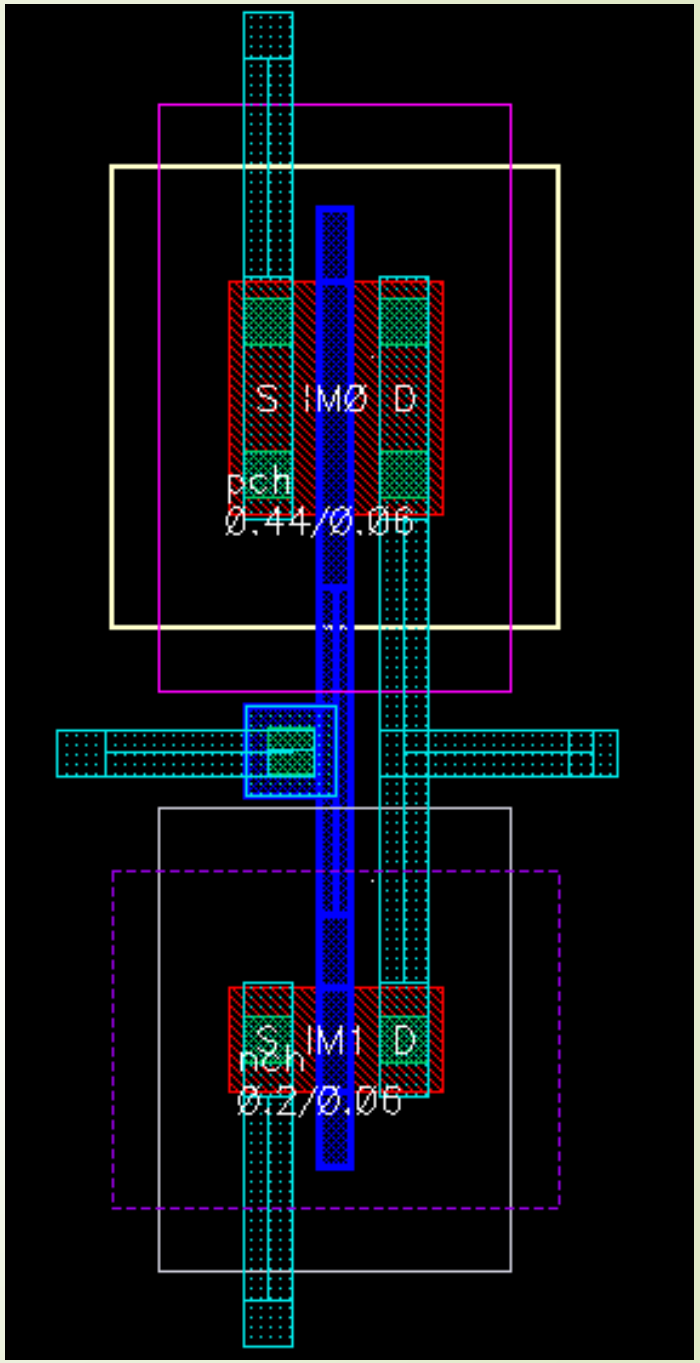
a) 4-input NAND



4. LAYOUT

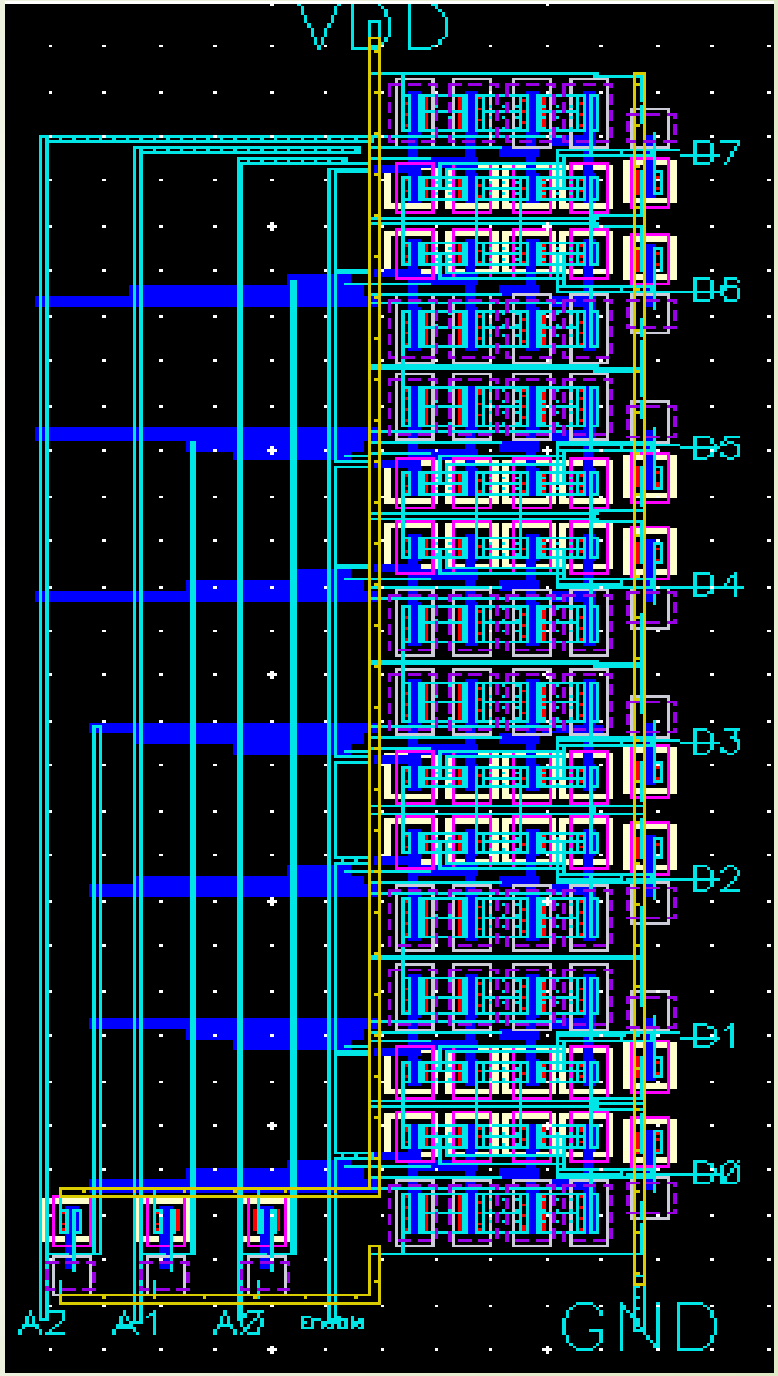
4.2. Decoder

b) Inverter



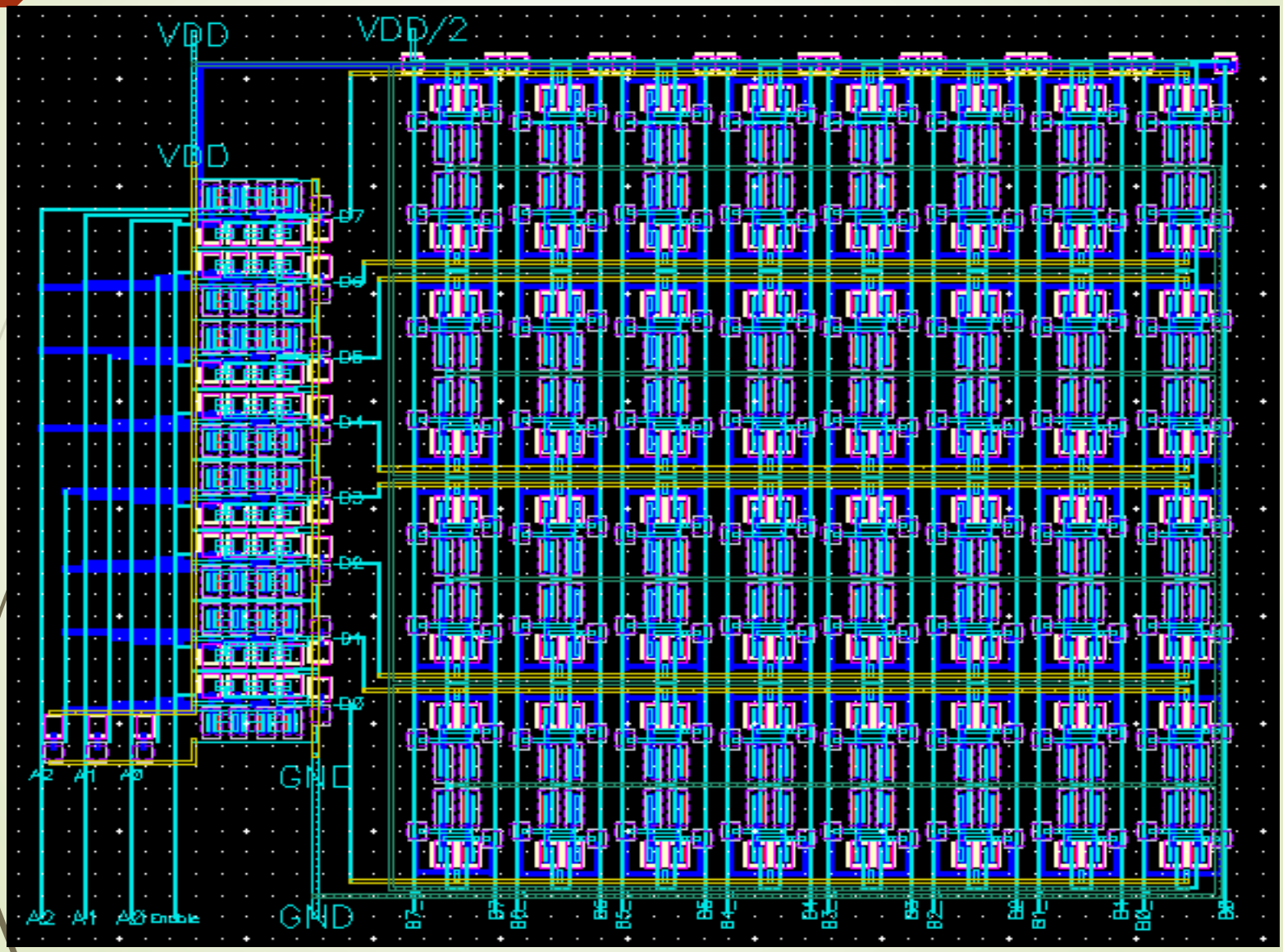
4. LAYOUT

4.2. Decoder



4. LAYOUT

4.3. Whole System

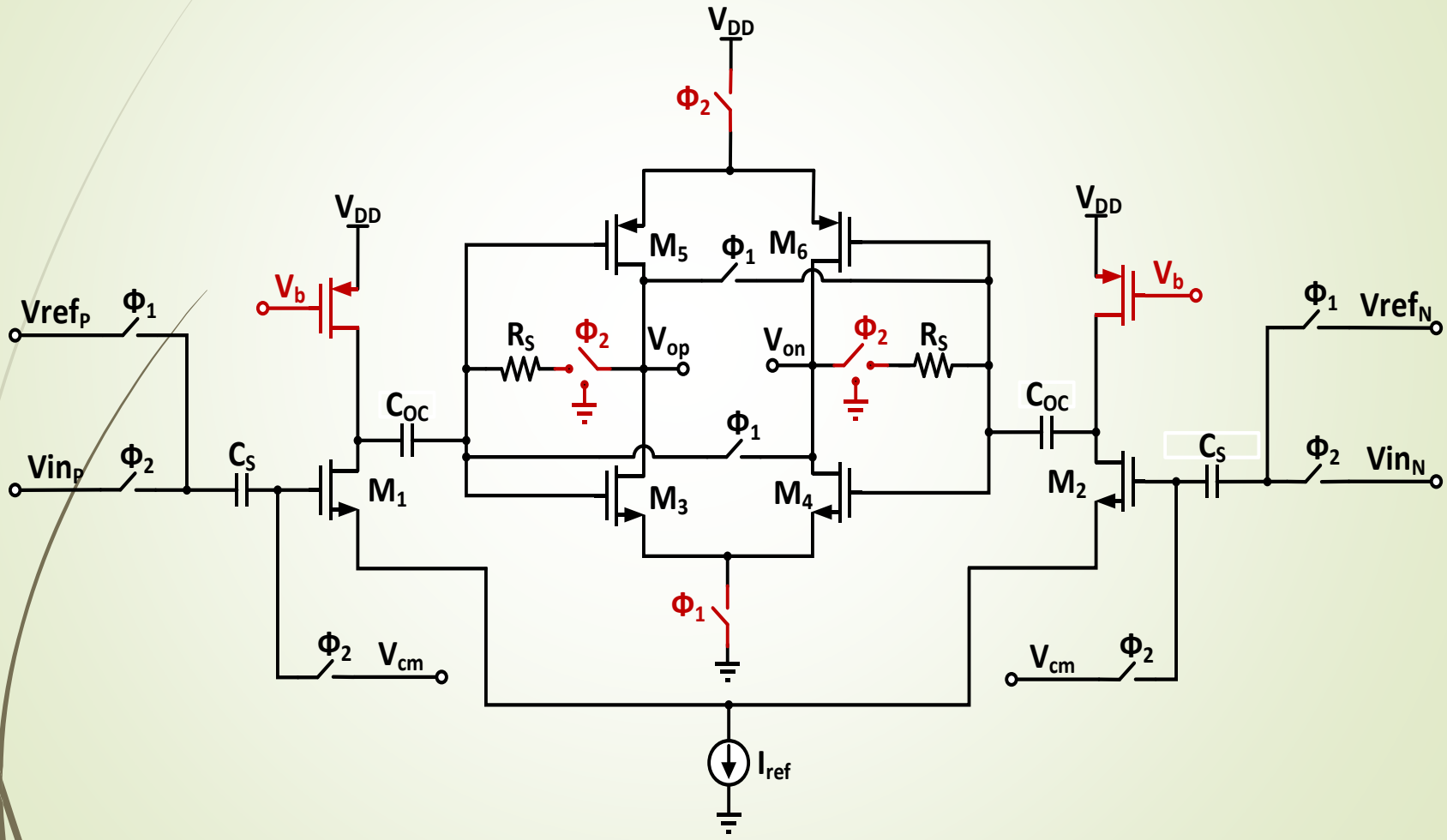


5. Final Results

Parameter		Value
Technology		65nm CMOS
Supply Voltage (V_{DD})		1 V
Frequency (f)		100 MHz
Power Consumption (P)		109.72 uW
Static Noise Margin	Read	0.2461 V
	Write	0.3606 V
Delay	Read	53.2 ps
	Write	43.1 ps
Total Area (A)		40 um x 47.077 um = 1883.08 μm^2

6. Future Work

→ Sense Amplifier (Comparator)



References

- R. Baker, "CMOS Circuit Design, Layout, and Simulation", 2nd Ed., Wiley & Sons Inc., 2007.
- R. Ruchi, and Sudeb Dasgupta, "Compact Analytical Model to extract Write Static Noise Margin (WSNM) for SRAM Cell at 45nm & 65nm nodes", IEEE Transactions on Semiconductor Manufacturing, Vol. PP, Issue 99, November 2017.
- V. Enumula, S. Gupta, R. Manchukonda, and N. Upadhyay, "Design and implementation of 16X8 SRAM in 0.25u SCMOS technology", https://pdfs.semanticscholar.org/24c8/5982c98c177e6393aef35b8891f44564e8ec.pdf
- V. Saxena, "SRAM Static Characterization", Boise State University, https://www.researchgate.net/file.PostFileLoader.html?id=54be4ae2d2fd64fb0d8b45cf&assetKey=AS%3A273675910090788%401442260829994
- J. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits – A Design Perspective", 2nd Ed., Prentice Hall, 2009.

Q & A