EE230 Homework #2 (10 points) Oct. 9, 2018

Due: Oct. 30, 2018 4:00PM
Late homework policy. 1-point deduction for each day you miss the due date.
Extra 1-point credit for the student who submitted homework first.

Goal of this homework is to learn the use of periodic steady state (pss) simulation tools in Cadence Spectre in the characterization of a VCO including its phase noise. To understand the operation of a CMOS LCVCO and analyze its performance trade-offs, use the reference design described in "VCO_simulation.pdf" that can be found in Canvas homework folder.

You are required to duplicate the materials presented in the reference document except the followings:

1. Use the device model nmos2v and pmos2v from gpdk045.
2. V_{DD} = 1.8V and you are free to change the component values, IBIAS, and the 0 < VC < 1.8 value.
3. Create a document like the reference document and answer the problem questions in the reference.

Design target is to meet the following key requirements for the LCVCO structure presented in the reference.

- fo ~ 1.9 GHz
- Tuning range 1.8 ~ 2.0 GHz
- Phase noise < -110 dBc/Hz at 1 MHz offset
- Power dissipation < 5 mW

You can use an LCVCO circuit different from the reference structure if you meet the key requirements.

You should submit the pdf file format of your homework via email to sang-soo.lee@sjsu.edu

File name should be EE230HW#3_Lastname_Firstname.pdf.

Also, the first page of the homework report should include your name. Otherwise, 1-point deduction.

Please submit just one pdf file. No Zip file or image files please!