EE230 – HW4 Report

CMOS down-conversion Mixer

(@ 1.9 GHz & using 45nm CMOS Technology)

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1. Schematic Setup:

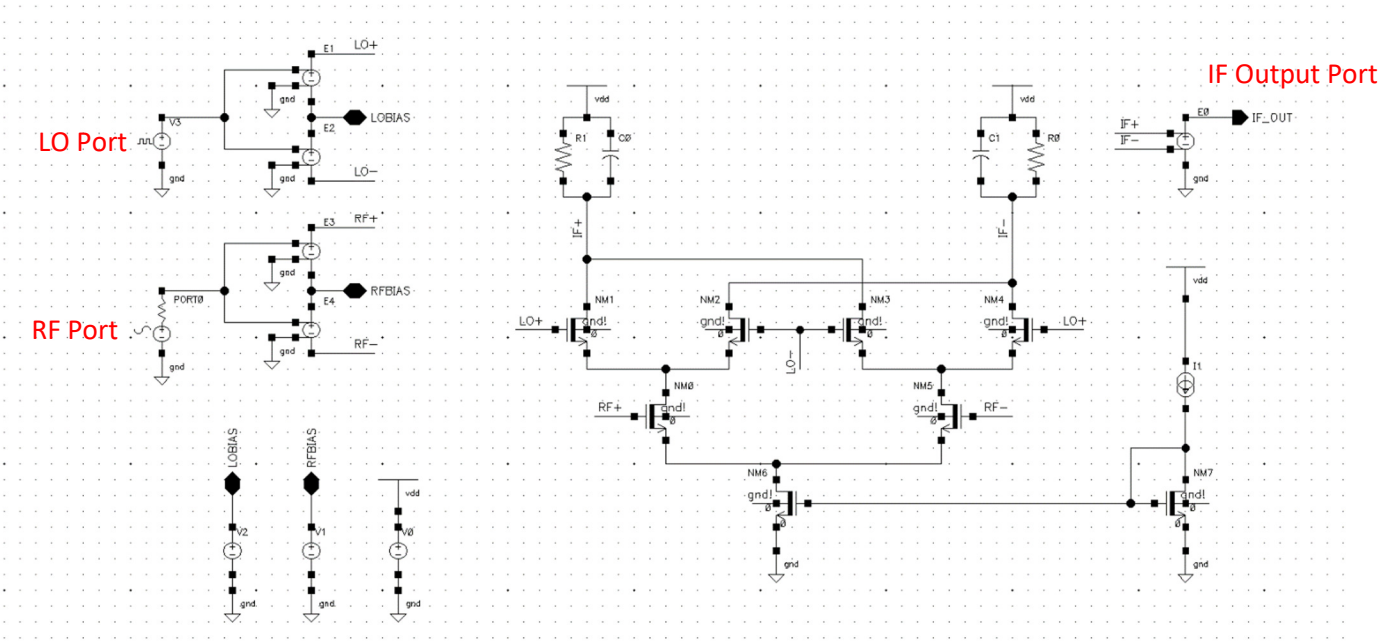


Fig. 1. Active Mixer schematic

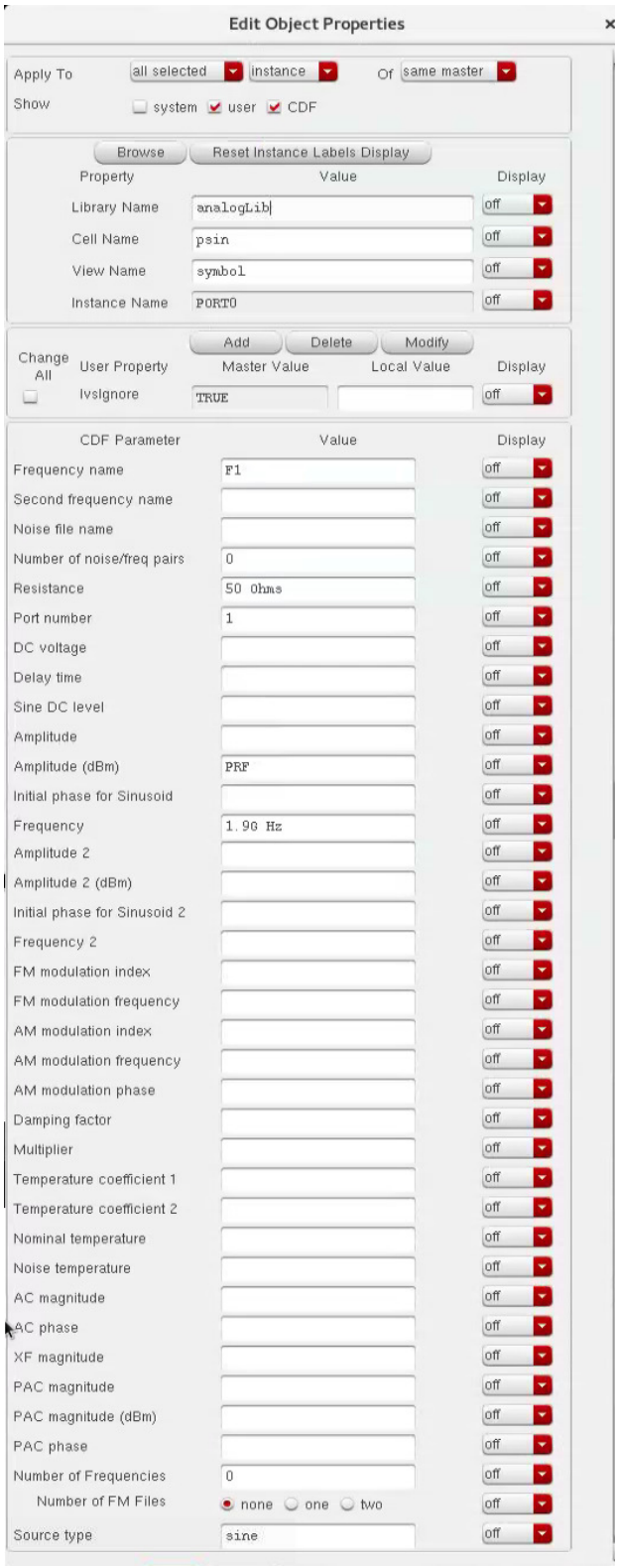
Table 1. Transistor parameters

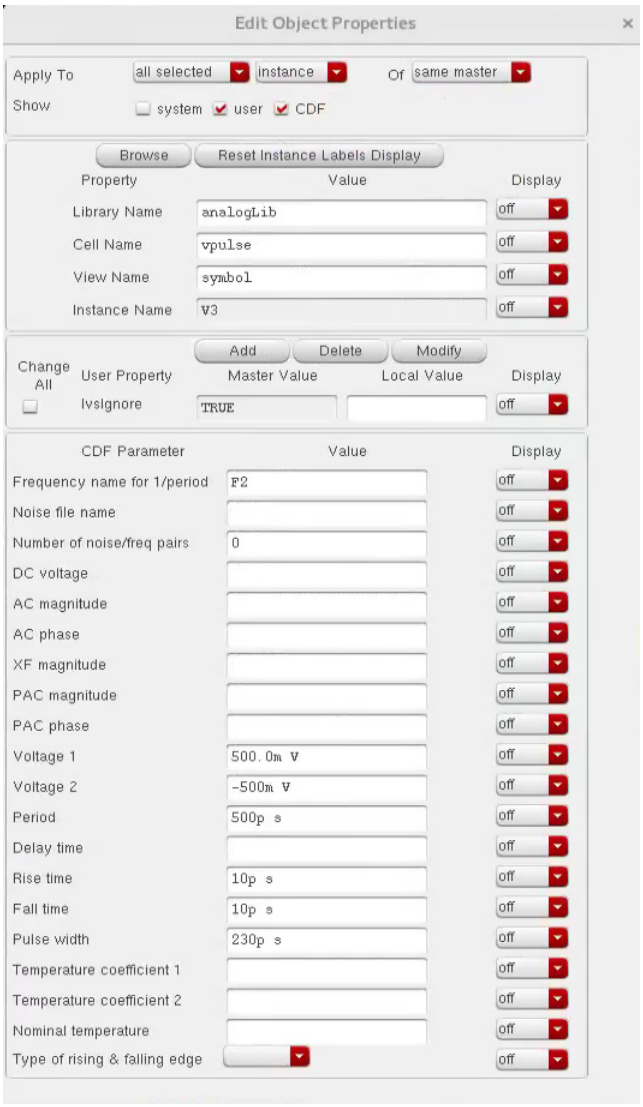
Transistor	W [um]	L [um]	Multiplicity
NM7	10	0.6	2
NM6	15	0.6	20
NM0, NM5	50	0.6	10
NM1, NM2, NM3, NM4	15	0.15	10

Table 2. Component values

Component	Value
R0, R1	600 Ohms
C0, C1	200 fF
IBIAS	250 uA
LOBIAS	0.9 V
RFBIAS	0.7 V
VDD	1.8 V
E0, E1, E2, E3, E4	0.5 V/V

Table 3. RF port (left) & LO port (right) parameters





2. DC operating points:

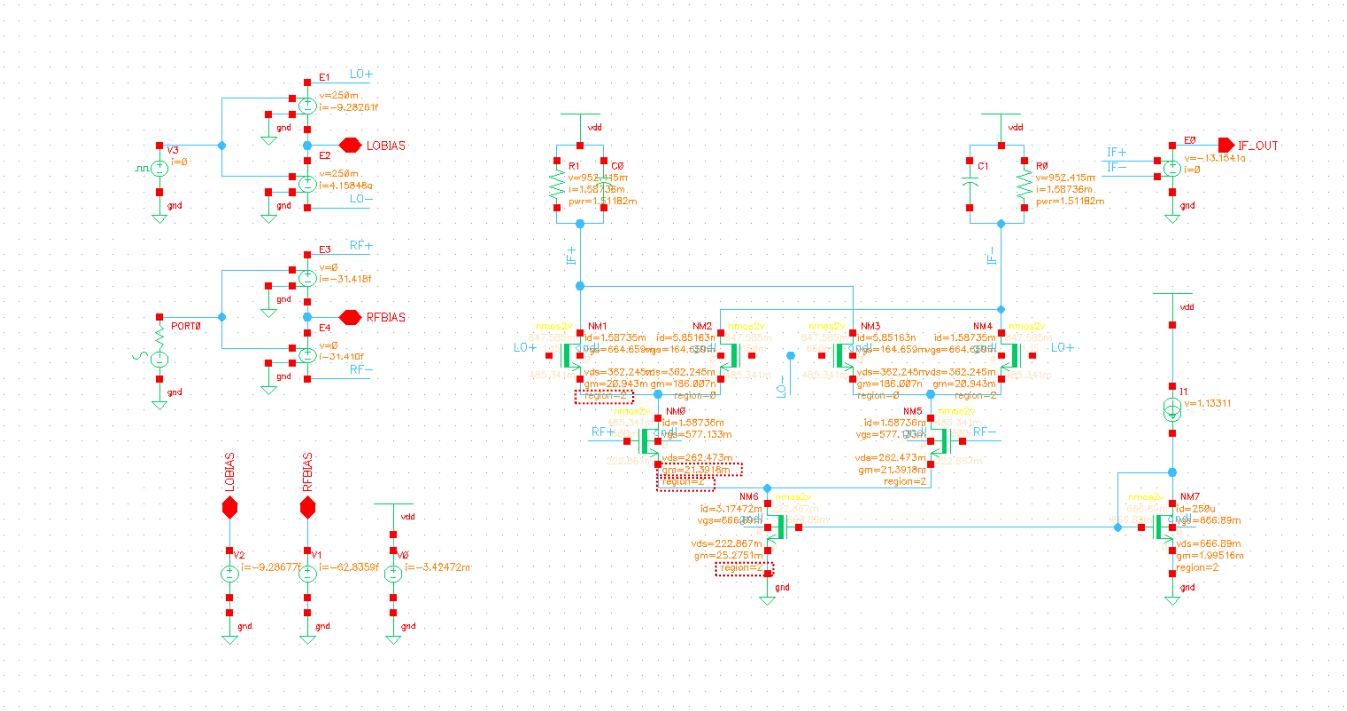


Fig. 2. DC operating points (after running dc analysis)

3. PSS Simulation:

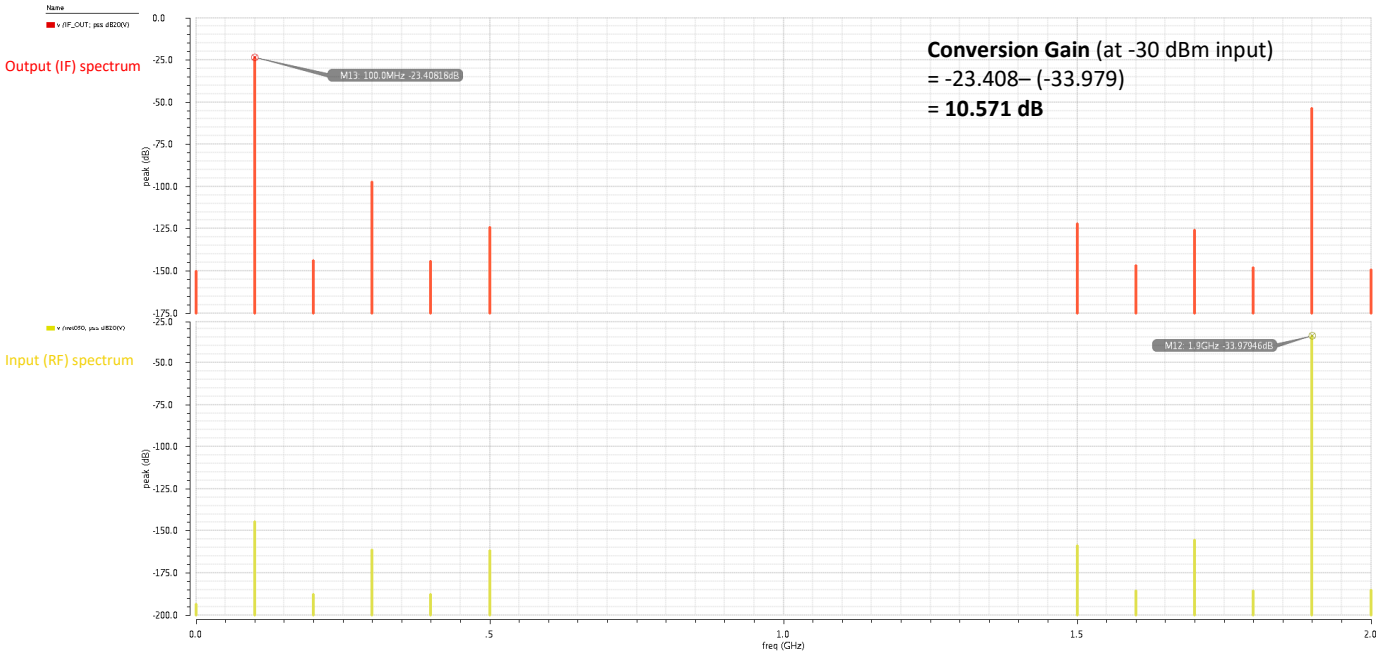


Fig. 3. Output & Input Spectrum

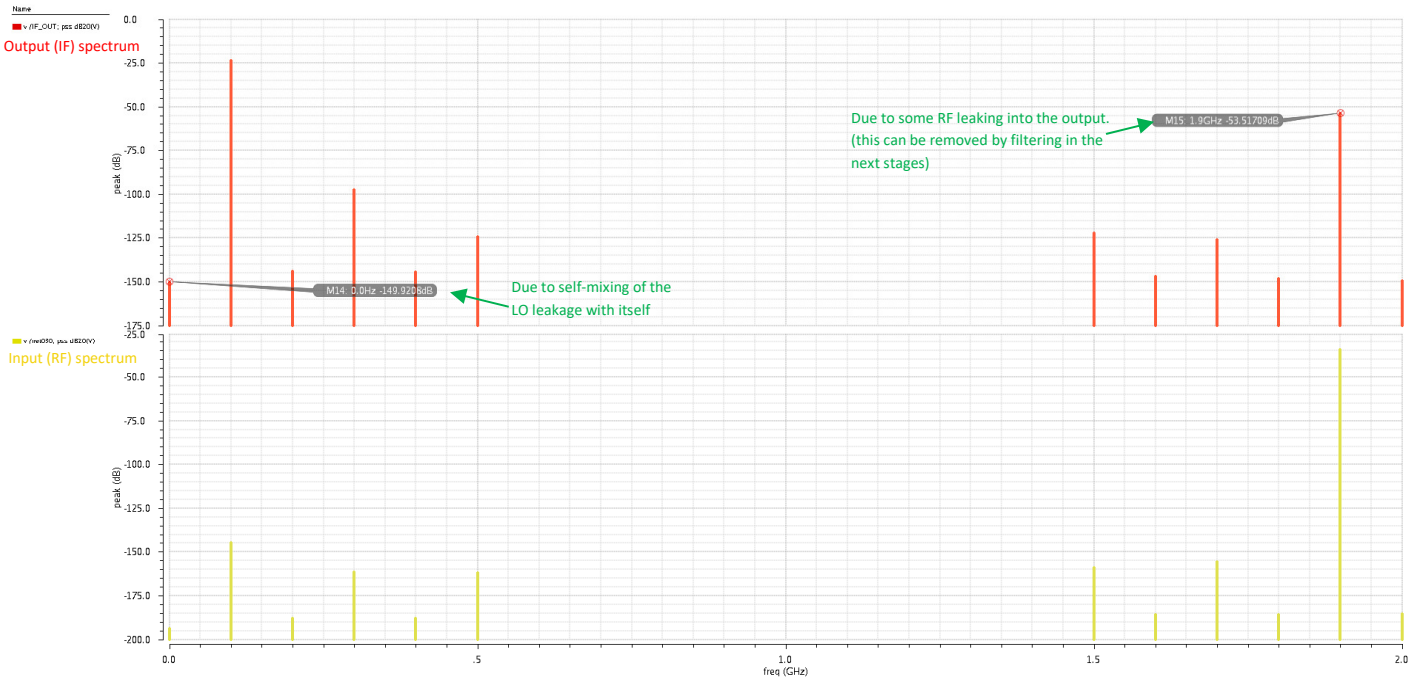


Fig. 4. Undesired Output Spectrum

4. PNoise Simulation:

5.

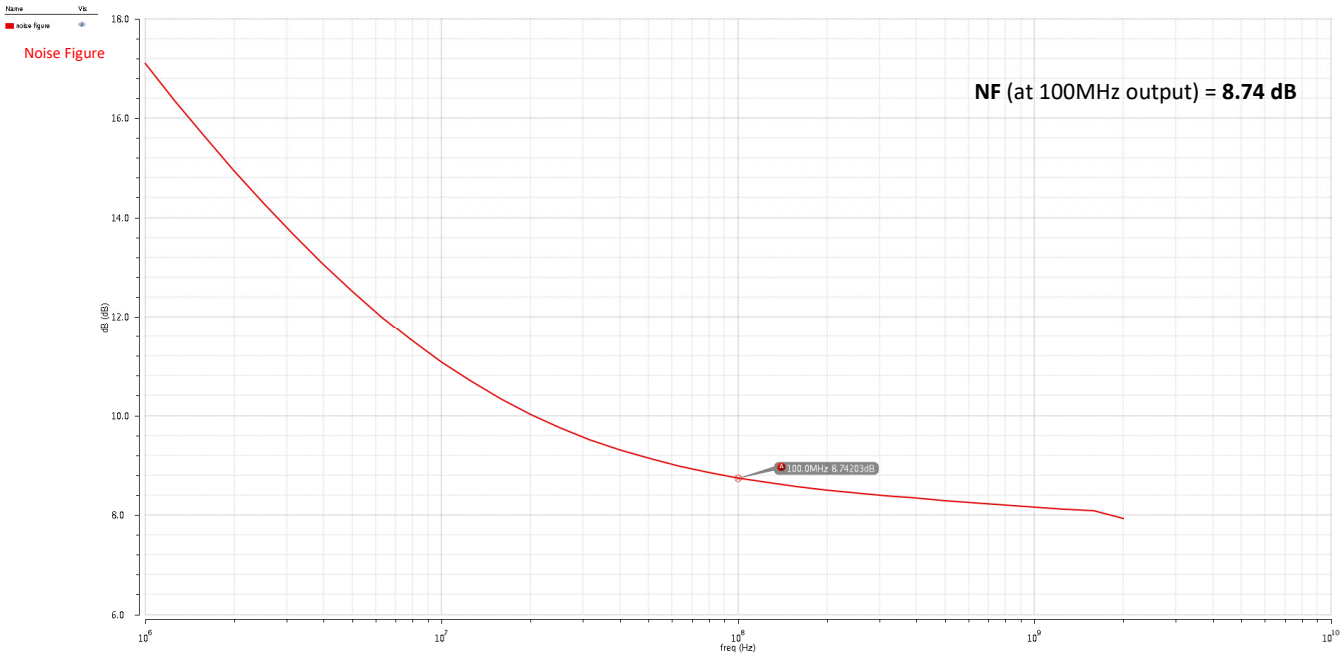


Fig. 5. Noise Figure of the Mixer

6. SPSS Simulation:

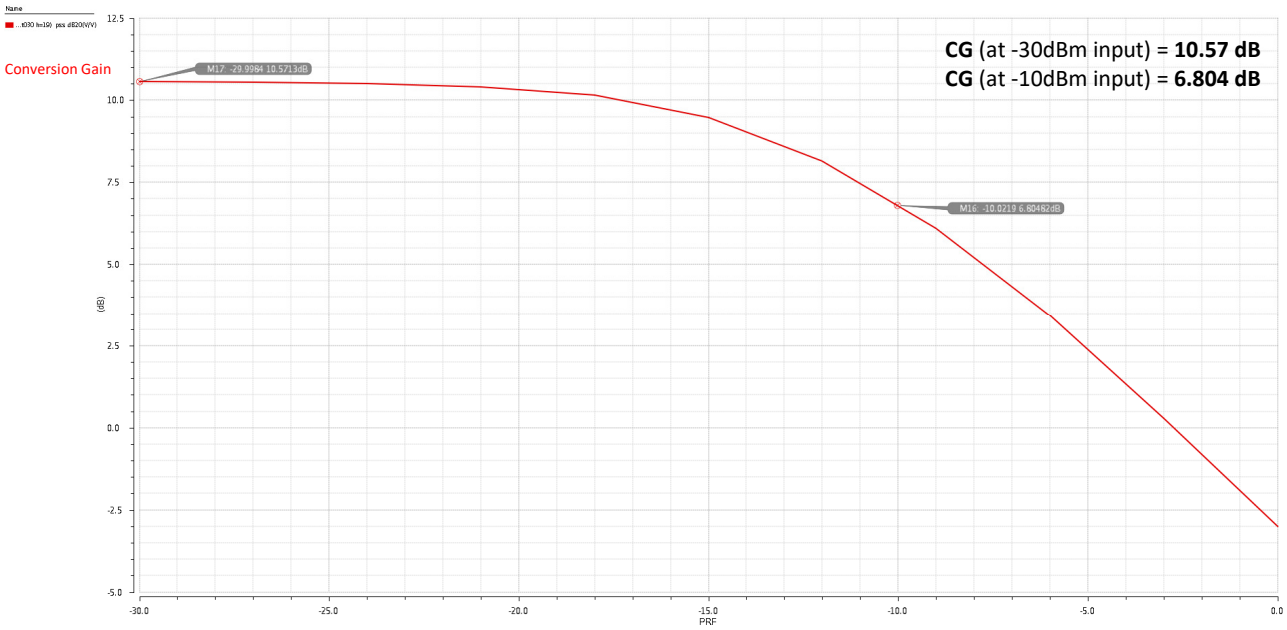


Fig. 6. Conversion Gain Vs Input Power

7. QPSS & QPAC Simulation:

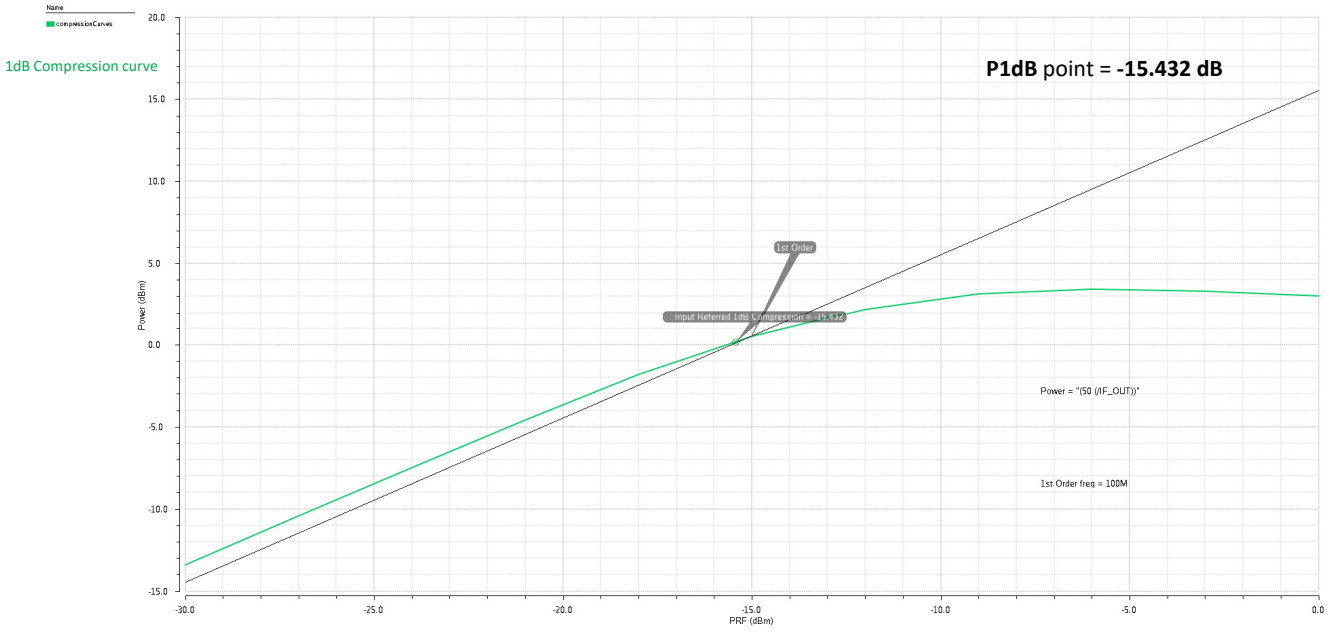


Fig. 7. Output Power Vs Input Power (Compression curve)

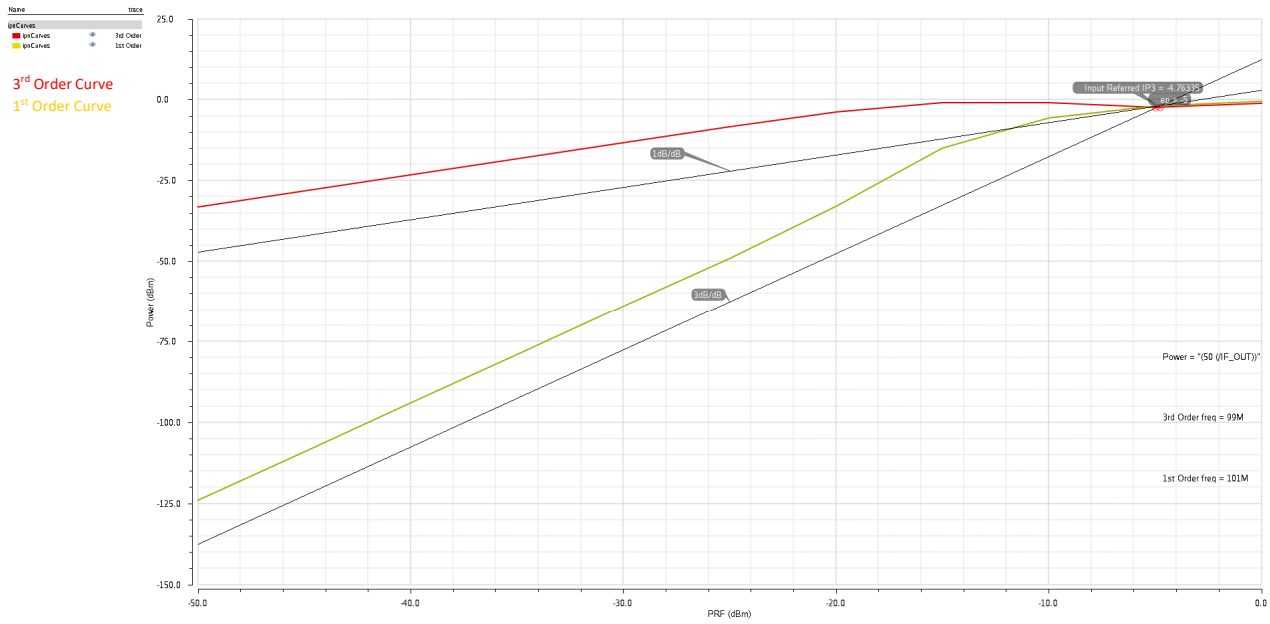


Fig. 8. Fundamental & 3rd-order Output Power Components Vs Input Power from the 2-tone test (IPN curves)

8. Summary of the results:

Parameter	Value
Power Dissipation	3.42 mA * 1.8 V = **6.16 mW**
Conversion Gain (@ -30 dBm)	**10.57 dB**
Noise Figure	**8.74 dB**
P1dB Compression Point	**-15.43 dBm**
IIP3	**-4.76 dBm**