數位系統實驗

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LAB - 03

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Digital Integrat

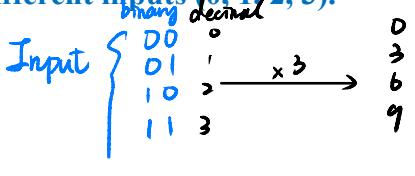
Lab I -- Constant Multiplier (1/3)

最高有效位元
MSB

- There is a 2-bit input X (represented as X1 and X0). A constant multiplier is designed to multiply the input by 3. Finally, show the result with decimal format (0, 1, 2, …..,9) on Digital Display in the breadboard.

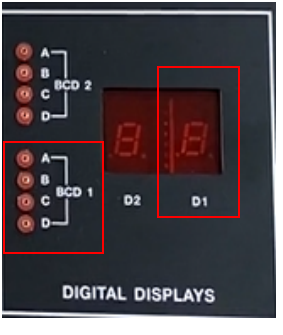
Hint-1:

The output digital number is 0, 3, 6 or 9, respectively, for four different inputs (0, 1, 2, 3).



Lab I -- Constant Multiplier (2/3)

Hint-2:
Function of the Digital Display in the breadboard is as follows.



D	C	B	A	DIGITAL DISPLAY
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Lab I -- Constant Multiplier (3/3)

Please

(a) draw the truth table of the constant multiplier where two input bits are X1 and X0, and four output bits are A, B, C and D, respectively.

(b) simplify the circuit with K-map (SOP format) and draw the simplified circuit diagram of the constant multiplier.

(c) implement the circuit on the breadboard.

(a)

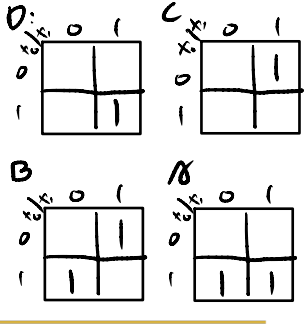
X_1	X_0		D	C	B	A
0	0	0	0	0	0	0
0	1	1	3	0	0	1	1
1	0	2	6	0	1	1	0
1	1	3	9	1	0	0	1

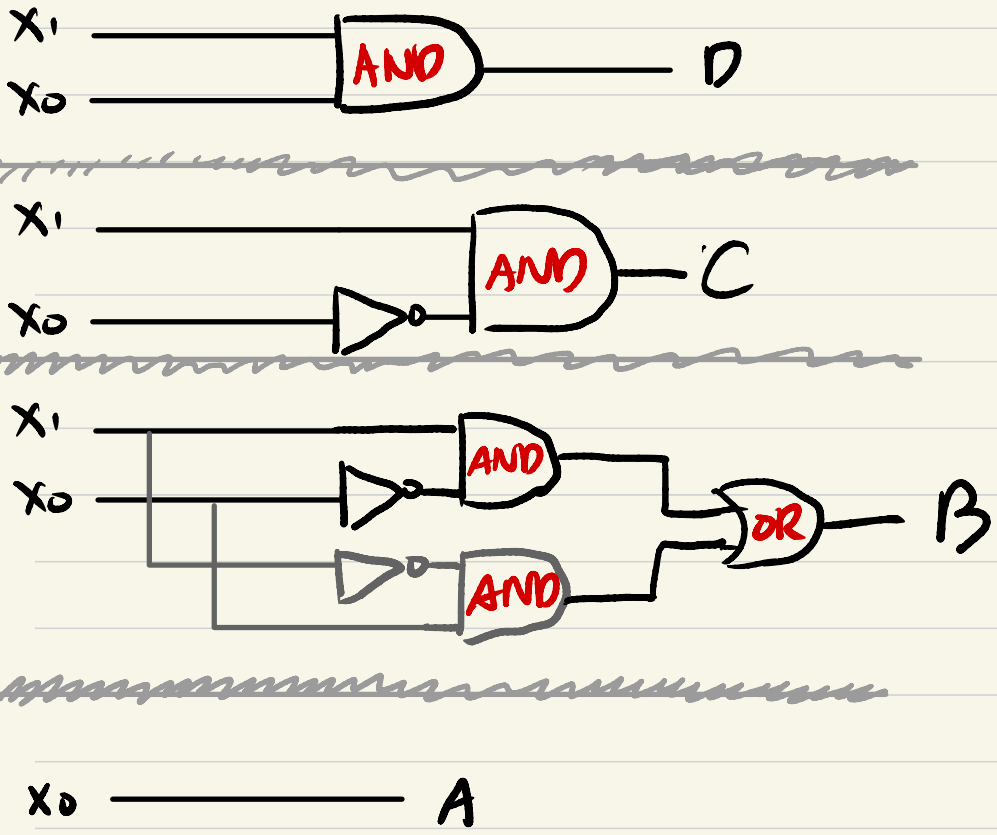
$D = X_1X_0$

$C = X_1X_0'$

$B = X_1X_0' + X_1'X_0$

$A = X_0$




X1
X0
AND
D
X1
X0
AND
C
X1
X0
AND
AND
OR
B
X0
A

Components needed for LAB I

Names	Amount
Solerless Breadboard	×1
74LS04 NOT	×1
74LS08 AND	×1
74LS32 OR	×1

Lab II – Comparator(1/2)

- There are a 3-bit input X (represented as X2, X1 and X0) and two 1-bit outputs A and B. The comparator is designed to let output A be 1 if X>3 and output B be 1 if X>4.
- The function of the comparator is described as follows.

MSB LSB

$$A = \begin{cases} 1 & , if\ X\ is > 3 \\ 0 & , else \end{cases}$$

$$B = \begin{cases} 1 & , if\ X\ is > 4 \\ 0 & , else \end{cases}$$

Lab II – Comparator(2/2)

Please

(a) draw the truth table of the comparator where three input bits are X2, X1 and X0, and two output bits are A and B, respectively.

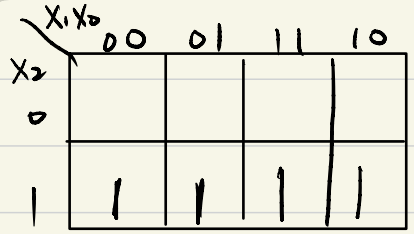
(b) simplify the circuit with K-map and draw the simplified SOP-format circuit diagram of the constant multiplier. Finally, implement the circuit on the breadboard.

(c) repeat (b) by using the POS format.

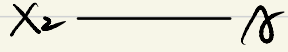
SOP

X_2	X_1	X_0		A	B
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	2	0	0
0	1	1	3	0	0
1	0	0	4	1	0
1	0	1	5	1	1
1	1	0	6	1	1
1	1	1	7	1	1

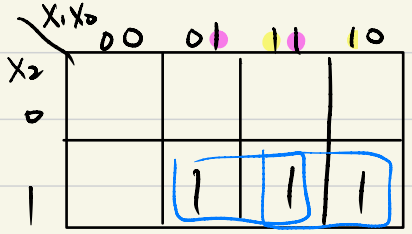
A:



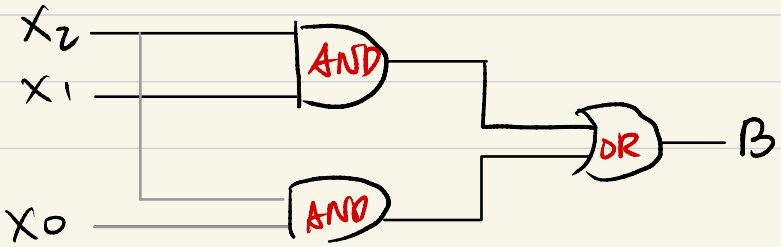
$A = X_2$



B:



$B = X_2X_0 + X_2X_1$



POS

A:

X_2 \ X_1X_0	00	01	11	10
0	0	0	0	0
1	1	1	1	1

$A' = X_2'$

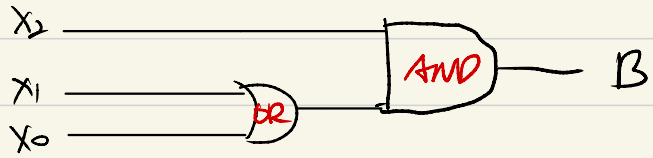
$A = X_2$

B:

X_2 \ X_1X_0	00	01	11	10
0	0	0	0	0
1	0	1	1	1

$B' = X_2' + X_1'X_0'$

$B = (X_2' + X_1'X_0')' = X_2(X_1 + X_0)$

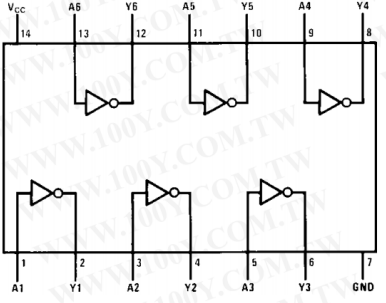


Components needed for LAB II

Names	Amount
Solerless Breadboard	×1
74LS08 AND	×1
74LS32 OR	×1

74LS04

Connection Diagram



Function Table

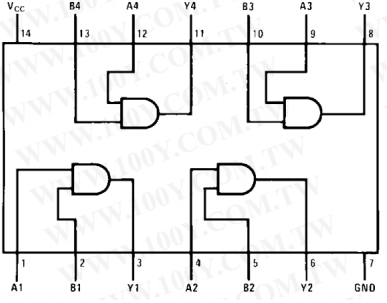
$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

74LS08

Connection Diagram



Function Table

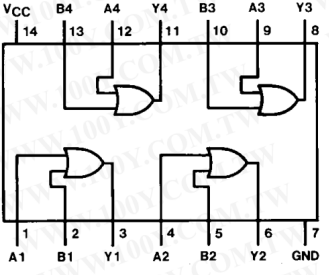
$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

74LS32

Connection Diagram



Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Logic Level
L = LOW Logic Level