LAB - 09

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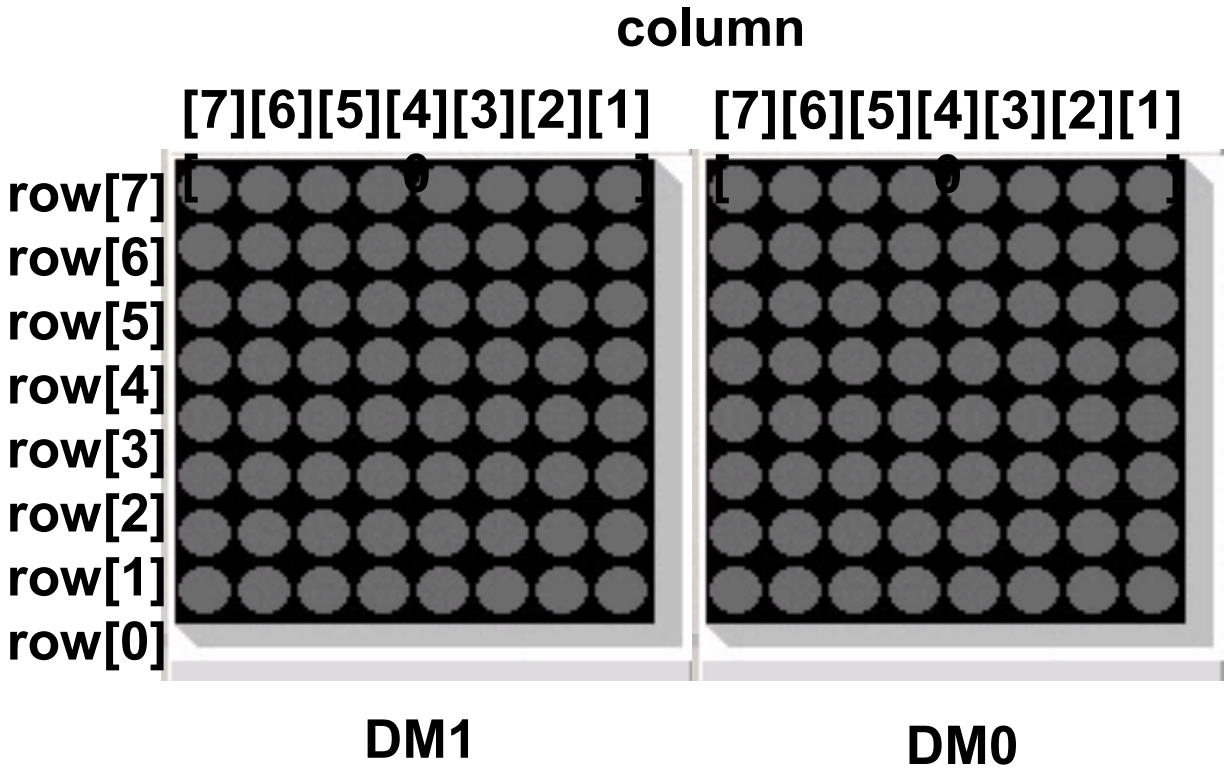
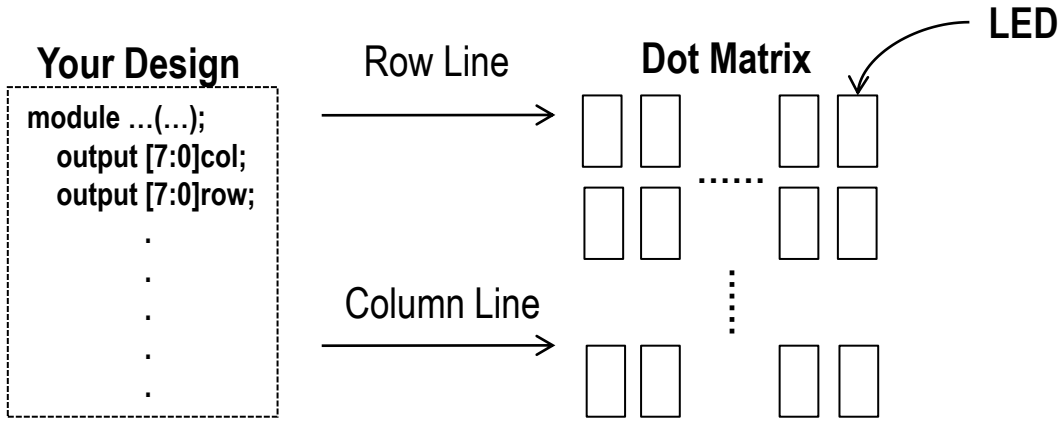
LED Dot Matrix Display (1/3)

- In DE0-CV external board

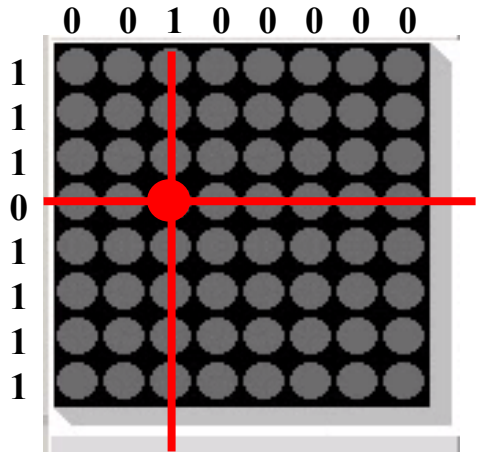


LED Dot Matrix Display (2/3)

- 點矩陣由8 bits的row訊號及8 bits的column訊號控制
- 當row訊號第i個bit為0，column訊號的第j個bit為1，則第(i, j)個位置之點矩陣會被點亮

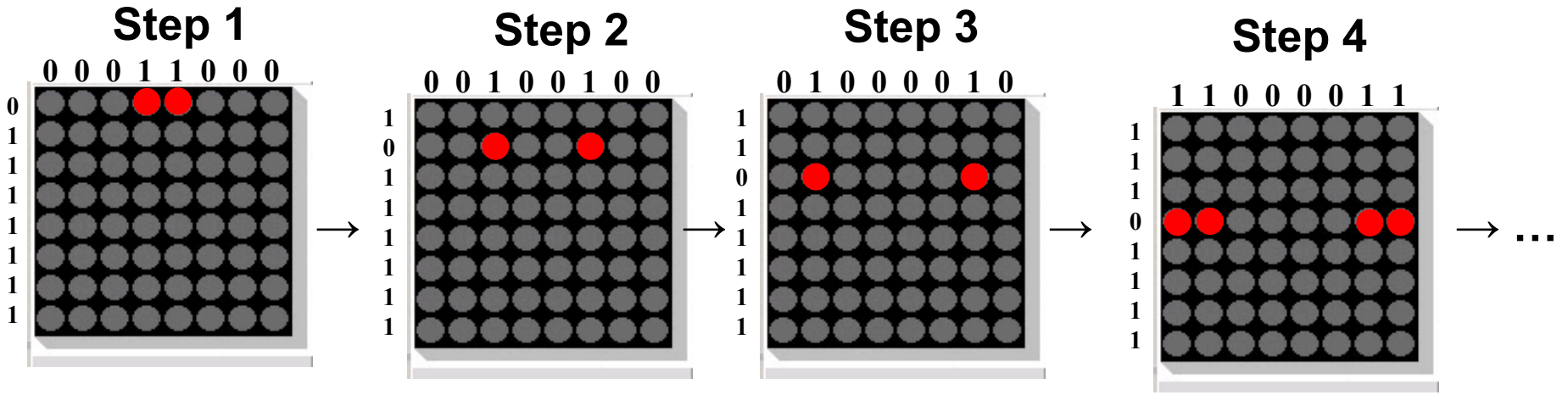


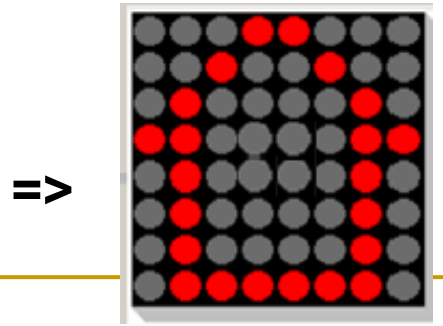
row[4] = 0
column[5] = 1



LED Dot Matrix Display (3/3)

- 快速地將row控制訊號的每個bit輪流設為0
- 根據目前要顯示的row來判斷column訊號的哪些bits要設為0
- 藉由視覺暫留，達到一次顯示8列的視覺效果

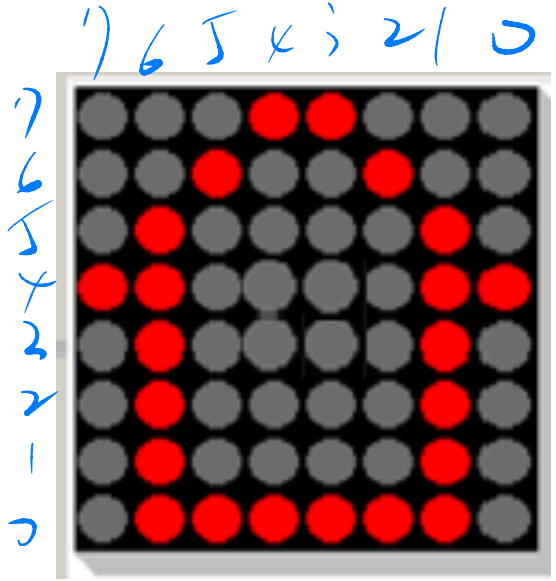




Clock must be as 10000 Hz for display !!!

Lab I – Dot matrix display controller

- 請設計一點矩陣控制電路，在點矩陣顯示右側圖像
- 電路腳位
  - Input: clock(CLOCK_50)、reset(reset button)
  - Output: dot_row(8 bits)、dot_col(8 bits)



- 本電路採低位準非同步reset
  - 按下reset button時，點矩陣須維持全暗
- 除頻後的clock頻率須為10000Hz

Example for dot matrix controller

```
always@ (posedge clk_div or negedge rst ) begin
        if (~rst) begin
            dot_row <= 8'b0;
            dot_col <= 8'b0;
            row_count <= 0;
        end
        else begin
            row_count <= row_count + 1;
            case (row_count)
                3'd0: dot_row <= 8'b01111111;
                3'd1: dot_row <= 8'b10111111;
                3'd2: dot_row <= 8'b11011111;
                3'd3: dot_row <= 8'b11101111;
                3'd4: dot_row <= 8'b11110111;
                3'd5: dot_row <= 8'b11111011;
                3'd6: dot_row <= 8'b11111101;
                3'd7: dot_row <= 8'b11111110;
            endcase
            case (row_count)
                /*
                    design col signals here
                */
            endcase

        end
    end
```

Notice

- 請勿命名中文或數字開頭的資料夾
- Device family 請確認與 FPGA Chip 符合 (5CEFA4F23C7)
- Top module name & Project name 需要一致
- 在組合電路中，case、if…else…若沒有寫滿，合成後會產生latch