- Bit 13 CONT
  - 0: single conversion mode, 1: continuous conversion mode
- Bits 9 to 6 L

ADC_ISR

- Reset value = 0
- Bit 0 ADRDY (ADC Ready, set to 1 by HW when ADC is enabled and ready)
- Bit 2 EOC
  - When EACH CHANNEL conversion ends, this bit is set by hardware
  - Means data is available at ADC_DR
  - If SW reads ADC_DR, this bit is AUTOMATICALLY CLEARED
  - 0: Conversion not complete, 1: Conversion complete
- Bit 3 EOS
  - When ALL CHANNELS conversion ends, this bit is set by hardware
  - Means data is available at ADC_DR
  - 0: Conversion not complete, 1: Conversion complete

PRELAB 9

- Try changing the sampling rate from ADC_SAMPR1
- ADC global register map