AN934
APPLICATION NOTE

TIMEKEEPER® Calibration

INTRODUCTION

The term “quartz accurate” has become a familiar phrase used to describe the accuracy of many time keeping functions. Quartz oscillators provide an accuracy far superior to other conventional oscillator designs, but they are not perfect. Quartz crystals are sensitive to temperature variations. Figure 1 shows the relationship between accuracy (acc), temperature (T), and curvature (K) for the 32,768Hz crystal used on STMicroelectronics TIMEKEEPER® products. The curves follow this general formula:

$$acc = K \times (T - T_O)^2$$

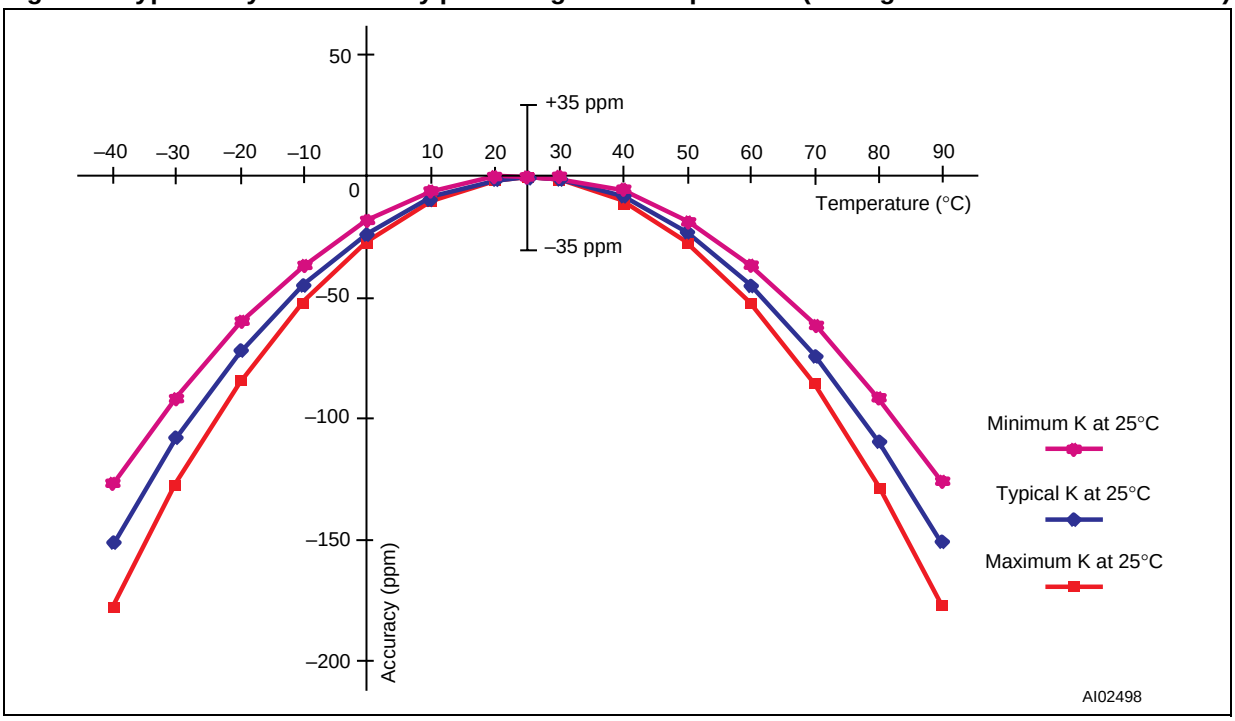
where T_O = 25°C ± 5°C and K = –0.036 ppm/°C^2 ± 0.006 ppm/°C^2.

The clocks used in most applications require a high degree of accuracy, and there are several factors involved in achieving this accuracy. Typically most crystals are compensated by adjusting the load capacitance of the oscillator. This method, while effective, has several disadvantages:

1. It requires external components (trim capacitors); and
2. it can increase oscillator current (an important factor in battery-supported applications).

STMicroelectronics replaced this crude analog method with a digital calibration feature. This method gives the user software control over the calibration procedure which makes it user friendly.

Figure 1. Typical Crystal Accuracy plotted against Temperature (and against Different Values of K)



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METHODOLOGY

The STMicroelectronics TIMEKEEPER® products are driven by a quartz crystal-controlled oscillator with a nominal frequency of 32.768kHz. The crystal is mounted in either a 600mil DIP CAPHAT™ package, 600mil DIP Hybrid, 300mil SOIC Embedded Crystal, or in a 330mil SOIC SNAPHAT® package, along with the battery. A typical TIMEKEEPER device is accurate within ±1.53 minutes (±35 ppm - parts per million) per month at 25°C without calibration.

Two sources of clock error are:

– temperature variation

– crystal variation

As mentioned previously, most clock chips compensate for crystal frequency and temperature shift error with cumbersome “trim” capacitors. The TIMEKEEPER design, (with the exception of the M48T86 device, which does not have the calibration register), employs periodic counter correction. The digital calibration circuit adds or subtracts counts from the oscillator divider circuit at the 256Hz stage (see Figure 2).

Figure 3 shows how extra clock pulses are added (by clock splitting) or removed (by clock blanking). The number of times the pulses are split (added during positive calibration) or blanked (subtracted during negative calibration) depends upon the value that has been loaded into the least significant five bits of the Control Register. Adding counts speeds the clock up while subtracting counts slows the clock down.

Figure 2. Oscillator Divider Chain

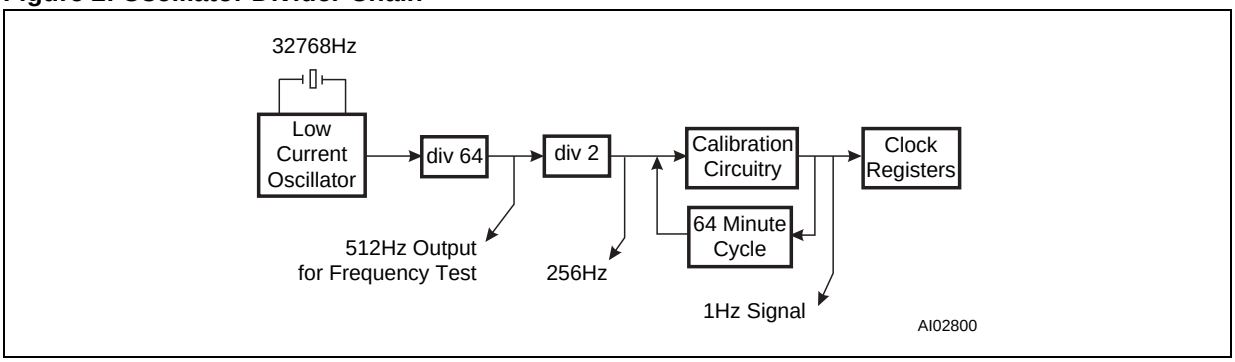
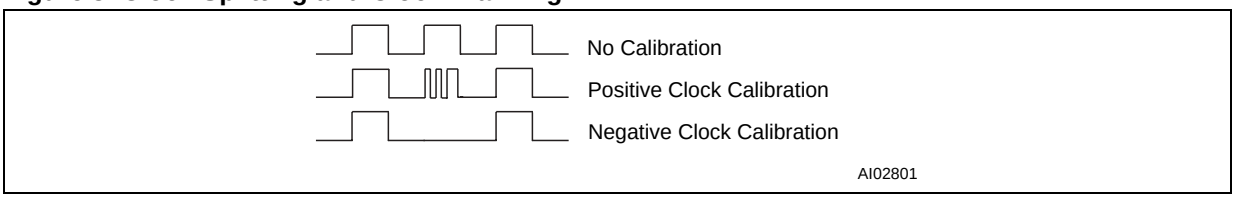


Figure 3. Clock Splitting and Clock Blanking

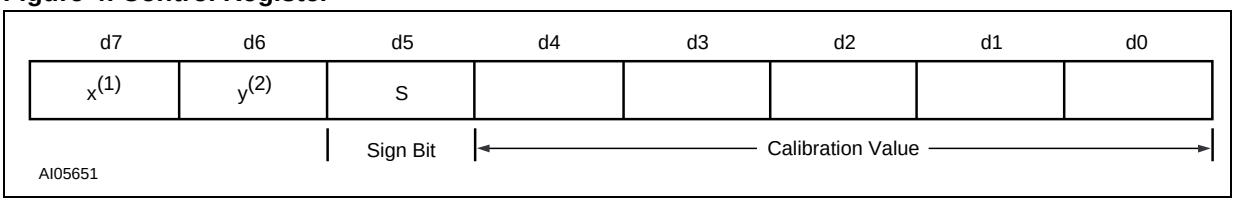


The calibration byte occupies the five lower order bits in the Control Register, as shown in Figure 4. These bits represent the binary value between 0 and 31. Table 1., page 5 shows how many seconds (or ppm) each bit represents in real time for the TIMEKEEPER® product line. The sixth bit is a sign bit. A binary '1' indicates a positive calibration (added pulses), and a binary '0' indicates a negative calibration (blanked pulses). Calibration occurs within a 64-minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64-minute cycle are modified; if a binary “6” is loaded, the first 12 minutes are affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles (64 minutes x 60 seconds/minute x 32,768 cycles/second). That is, +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is running exactly at 32.768kHz, each of the 31 increments in the calibration byte represent +10.7 or –5.35 seconds per month, which corresponds to a total range of +5.5 or –2.75 minutes per month.

As can be seen from Figure 1., page 1, the peak of the curve corresponds to approximately 25°C. This is known as the “turnover temperature.” As the temperature rises or falls from room temperature, the oscillator slows down. Typically the turnover point on the graph is very close to 32.768kHz (no error). However, variations from one crystal to another may cause the turnover point to be slightly above or below 32.768kHz. The frequency variation for an uncalibrated device is a function of the crystal frequency variation for the given load capacitance (C_L). Thus, if the crystal has a C_L that is different from the actual internal load capacitance of the device, then the oscillator frequency will run faster or slower than the 32.768kHz (±1Hz). At STMicroelectronics, the real-time clock has an internal capacitance of 12.5pF (except for the M41T6x device, which has an internal capacitance of 6pF) across the crystal input pins. For this reason, the calibration feature can be programmed to adjust for both negative and positive variations. Entering a value into the 6-bit calibration field of the Control Register will shift the entire curve up or down according to the values found in Table 1., page 5.

Figure 4. Control Register



Note: 1. x = W (Parallel device); OUT (Serial device)
2. y = R (Parallel device); FT (Serial device)

Table 1. Calibration Table: Compensation Values in seconds per month (30 days) and in ppm

Calibration Value (Binary)	Value in Seconds Per Month (30 days) Rounded to the Nearest Second		Value in ppm Rounded to the Nearest ppm	
	Plus	Minus	Plus	Minus
00000	0	0	0	0
00001	11	5	4	2
00010	21	11	8	4
00011	32	16	12	6
00100	42	21	16	8
00101	53	26	20	10
00110	63	32	24	12
00111	74	37	28	14
01000	84	42	33	16
01001	95	47	37	18
01010	105	53	41	20
01011	116	58	45	22
01100	127	63	49	24
01101	137	69	53	26
01110	148	74	57	29
01111	158	79	61	31
10000	169	84	65	33
10001	179	90	69	35
10010	190	95	73	37
10011	200	100	77	39
10100	211	105	81	41
10101	221	111	85	43
10110	232	116	89	45
10111	243	121	93	47
11000	253	127	98	49
11001	264	132	102	51
11010	274	137	106	53
11011	285	142	110	55
11100	295	148	114	57
11101	306	153	118	59
11110	316	158	122	61
11111	327	163	126	63
In general:				
N	337*N/32	169*N/32	337*N/(32*2.592)	169*N/(32*2.592)

CALCULATING THE NEEDED AMOUNT OF CALIBRATION

There are two methods for establishing how much calibration are required in a given application.

The first method can be easily implemented in the user environment simply by setting the clock to a known accurate reference and then storing the time in some unused location in the RAM. Over a period of time (30 days), the reference time is compared to the current time (the average ambient temperature should be considered as well). This will tell the user how fast or slow the clock operates for a period of 30 days. While it may seem crude, it allows the designer to give the end user the ability to calibrate the clock according to the specified environment. The ability to calibrate the clock can also be accomplished even after the final product is packaged in a non-user serviceable enclosure by providing a simple utility to access the calibration byte.

Table 1., page 5 provides a direct look-up table for calibration values based upon the number of seconds lost or gained during a one month (30 day) period. For example, if the system were to lose 20 seconds during one month, the needed calibration would be +20 seconds. The user could look up a +20 second value in the table under the appropriate column. In this case, the nearest value is +21. The appropriate sign bit in this case is a logical '1,' indicating the clock needs to speed up to compensate for the lost time. This yields a calibration value of “100010.” In this example, the inaccuracy would be reduced from –20 seconds per month to +1 second per month.

The second approach is better suited for a manufacturing environment, and involves the use of a special test mode (as described in the section entitled, “ENABLING THE FREQUENCY TEST FUNCTION (FT), page 9” which derives a 512Hz signal from the clock divider chain, as indicated in Figure 2., page 3. This signal can be used to measure the accuracy of the crystal oscillator. The right-hand pair of columns in Table 1., page 5 provides a look-up table similar to that in the left-hand pair of columns, except that the error values are expressed in “ppm” units instead of seconds per month. The error in ppm can be quickly calculated by dividing the measured error from 512Hz by 512 and multiplying the result by 1 million. For example, if the frequency measured during the test mode is 511.998Hz, the delta is –0.002. Dividing by 512 and multiplying by 1 million, the result is –3.906 ppm. In this case, the nearest compensation value is a +4.068. The appropriate sign bit in this case is a logical '1,' indicating the clock needs to speed up to compensate for the lost time. This yields a calibration value of “100001.”

CALCULATING CALIBRATION OVER A TEMPERATURE RANGE

The calibration procedure described so far has centered around calculating the correction for a specific temperature. This section considers the procedure for minimizing the frequency error over a wider temperature range. This involves adjusting the frequency curve so that there is an equal amount of error above and below the zero (0) ppm point. Figure 5 shows how the frequency error can be minimized over a given temperature range.

The variables in the equation (see INTRODUCTION, page 1) are as follows:

K = Curvature characteristic = –0.036 ppm/°C^2 ± 0.006 ppm/°C^2

acc = Accuracy, in ppm, of the frequency, at the turnover temperature

T_O = Turnover temperature, in degrees Celsius = 25°C ± 5°C

T = Working temperature, in degrees Celsius

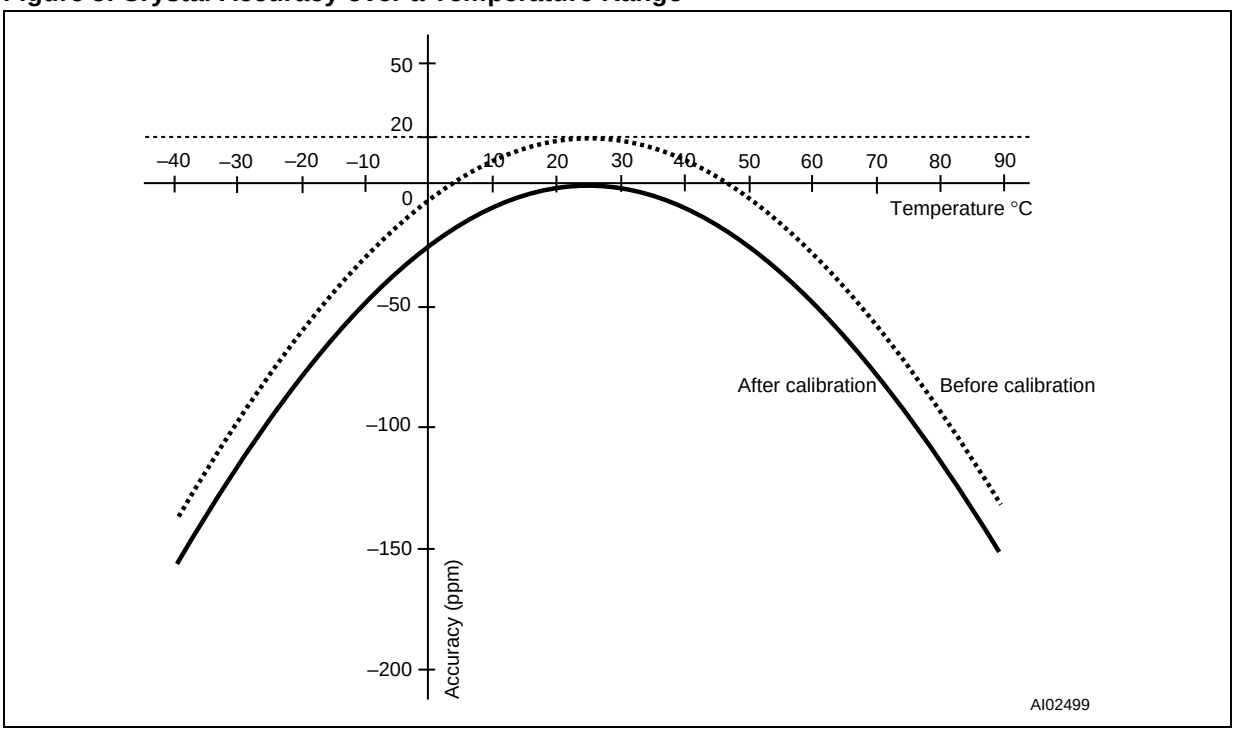
For example, if a device is in error by +20 ppm at room temperature, but will actually operate at –20°C in the application, the equation on page 1 may be used to calculate the required calibration value as follows:

acc = 20 ppm + (–0.036ppm/°C^2) * (–20°C – 25°C)^2

acc = –52.9 ppm

Since the unit will be slow by 52.9 ppm, the required correction is +52.9ppm, and this can be looked up in Table 1., page 5; the nearest value is a +53. The appropriate sign bit in this case is a logical '1,' indicating the clock needs to speed up to compensate for the lost time. This yields a calibration value of “101101.”

Figure 5. Crystal Accuracy over a Temperature Range



CALCULATING THE CALIBRATION FOR MULTIPLE OPERATING TEMPERATURES

For applications that spend significant time at more than one temperature, the following equation may be used to calculate the appropriate amount of calibration required:

$$t = \sum_{i=1}^{N} t_{PERi}(acc + K \times (T_i - T_o)^2) \times 10^{-6}$$

where:

K = Curvature characteristic = –0.036 ppm/°C^2 ± 0.006 ppm/°C^2

acc = Accuracy, in ppm, of the frequency, at the turnover temperature

T_O = Turnover temperature, in degrees Celsius = 25°C ± 5°C

T_i = Working temperature, in degrees Celsius

t_{PERi} = Amount of time it is in the temperature range (in seconds)

t = Amount of time lost during t_{PERi}

N = Number of temperature ranges

Consider a piece of portable equipment used outdoors for 8 hours per day, then stored at room temperature for the remainder of the day. The equation below calculates the calibration value at –20°C for a period of 8 hours and then room temperature for the rest of the day for a device that is currently in error by +5 ppm at room temperature:

$$8\,hours = 28800\,seconds$$

$$16\,hours = 57600\,seconds$$

$$= \{[(28800\,secs) \times (5 + ((-0.036\,ppm/°C^2) \times (-20°C - 25°C)^2))] + [(57600\,secs) \times (5 + 0)]\} \times 10^{-6}$$

$$t = -1.67\,secs/day$$

The unit is losing 1.67 seconds per day (or 50 seconds per month). The appropriate sign bit in this case is a logical “1,” indicating the clock needs to be sped up to compensate for the lost time. This yields a calibration value of “100101.”

ENABLING THE FREQUENCY TEST FUNCTION (FT)

Figure 4., page 4 and Figure 6 show the location of the Frequency Test (FT) Bit, DQ6, of the Day-of-the-Week register for the parallel device or DQ6 in the control register for the serial device. Setting the FT Bit to a '1' turns on the frequency test mode. The user needs to make sure that the Stop (ST) Bit in the second register, is set to a '0.' Exactly where the 512Hz signal is output depends on which TIMEKEEPER® device is being used, as indicated in Table 2. On the M48T02, M48T12, M48T08, M48T18, and M48T35 devices, the 512Hz signal is output on the DQ0 pin when the device is reading the Seconds register. The address and control signals must be valid during the measurement process, as shown in Figure 7., page 9.

On the M41T62, M41T63, and M41T64, the 512Hz signal is output on the SQW pin. To enable the 512Hz signal, the SQWE Bit = 1 (DQ6 of the alarm month register), RS3 = 0, RS2 = 1, and RS1 = 0 (DQ7-DQ4 in the day register). The SQW output pin is an open drain output for M41T64 and a full CMOS output for the M41T62 and M41T63.

For all other devices listed in Table 2., page 10, the 512Hz signal is output on the FT/OUT, FT, $\overline{IRQ}$/FT, and $\overline{IRQ}$/FT/OUT pins. These outputs are open drain, and require a pull-up resistor. A 500Ω to 10kΩ resistor is recommended in order to control the rise time. Measurement should be taken from negative edge to negative edge due to the slow rise time on the positive edge. If the $\overline{IRQ}$ function is enabled, the FT function is inhibited.

Note: Setting or changing the calibration byte does not affect the frequency test output frequency as the adjustment is made at the 256Hz stage.

Once the amount of calibration has been determined, either from the test mode or by monitoring it over a period of time, the user can enter the values from the calibration tables into the Control Register.

Figure 6. A Day of the Week Register (for Parallel Devices)

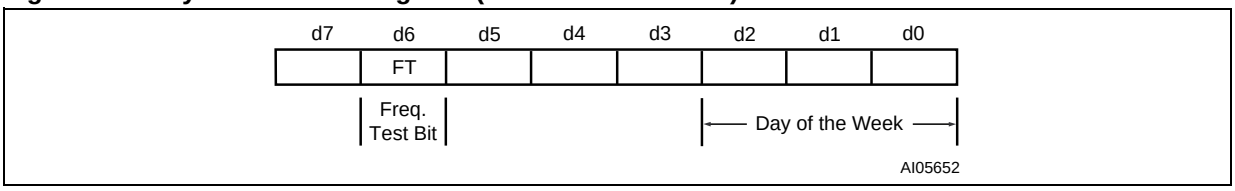
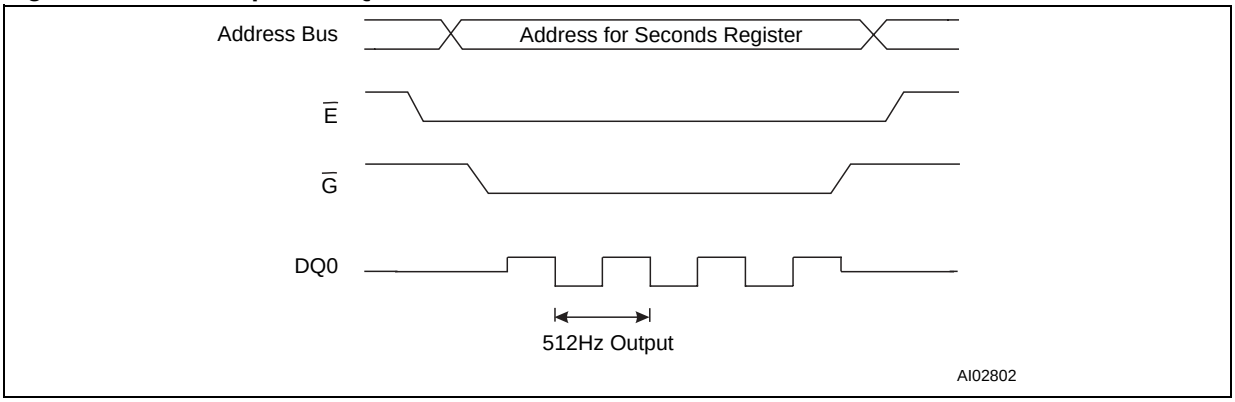


Figure 7. 512Hz Output to DQ0



Note: Care should be taken when writing to the Control Register so as not to overwrite the calibration value.

Table 2. 512Hz Output Pin

Device	Pin Name
M41T00, M41T00S, M41T11, M41T56	FT/Out
M48T02/12, M48T08/18, M48T35	DQ0
M41T256, M41T60, M48T58	FT
M48T59, M48T559, M48T37, M48T201, M48T212, M48T212A	$\overline{\text{IRQ}}$/FT
M41ST84, M41ST85, M41ST87, M41ST95, M41ST97, M41T65, M41T81, M41T81S, M41T94	$\overline{\text{IRQ}}$/FT/OUT
M41T62, M41T63, M41T64	SQW

CONCLUSION

Software calibration is a convenient feature which allows the user to adjust the clock accuracy during manufacturing (or later) at minimal cost. This feature also provides a method whereby “drift” (due to temperature variation) can be corrected and/or anticipated.

See **http://www.st.com/nvram** for additional details as well as an online calibration calculation tool.

REVISION HISTORY

Table 3. Document Revision History

Date	Version	Revision Details
December 1998	1.0	First Edition
20-May-03	1.1	Clarify compensation required (Table 1, 2); add Conclusion
16-Feb-04	2.0	Update web reference information
11-Nov-04	3.0	Reformatted; updates to content (Figure 4, 6; Table 2)

If you have any questions or suggestions concerning the matters raised in this document, please refer to the MPG request support web page:

http://www.st.com/askmemory