

Module pos ○

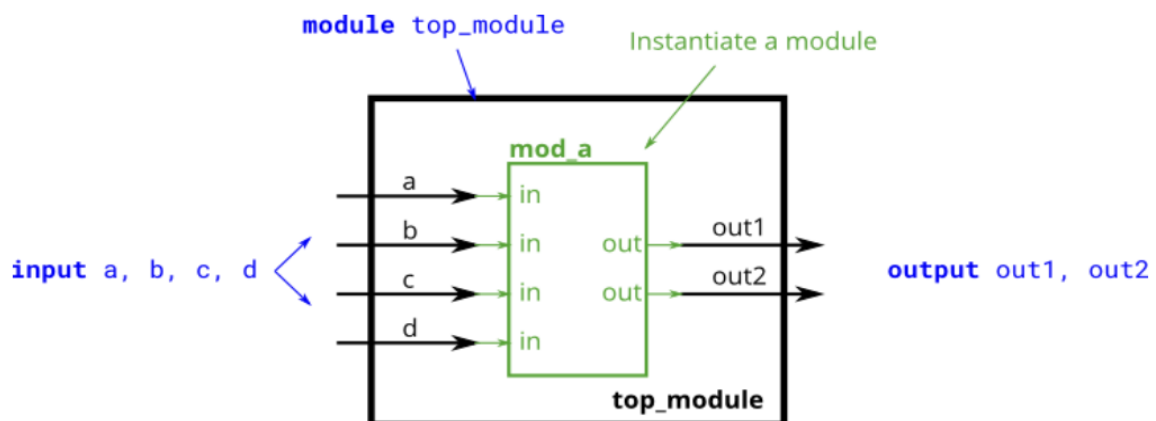
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This problem is similar to the previous one (module ✓). You are given a module named `mod_a` that has 2 outputs and 4 inputs, in that order. You must connect the 6 ports *by position* to your top-level module's ports `out1`, `out2`, `a`, `b`, `c`, and `d`, in that order.

You are given the following module:

```
module mod_a ( output, output, input, input, input, input );
```



Expected solution length: Around 1 line.

설명

- 이름의 의한 포트 매핑을 연습한다. Mod_a는 주어짐.

코드 및 실행 결과

module_pos — Compile and simulate

Running Quartus synthesis: [Show Quartus messages...](#)
Running ModelSim simulation: [Show Modelsim messages...](#)

Status: Success!

You have solved 21 problems. [See my progress...](#)

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The 'Mismatch' trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).

The timing diagram displays waveforms for inputs `a`, `b`, `c`, and `d`, and outputs `out1` and `out2`. It also includes a 'Mismatch' trace at the bottom, which shows a series of 0s and 1s indicating the correctness of the outputs over time.

```
HDLBits > Module > 2_Module_pos.v
1  module top_module (
2      input a,
3      input b,
4      input c,
5      input d,
6      output out1,
7      output out2
8  );
9
10     mod_a instance1(
11         out1,
12         out2,
13         a,
14         b,
15         c,
16         d
17     );
18 endmodule
19
```

코멘트

이름에 의한 포트 맵핑이니까, 하위 모듈 인스턴스의 이름을 알 필요가 없음(이 코드 한정).