Module name

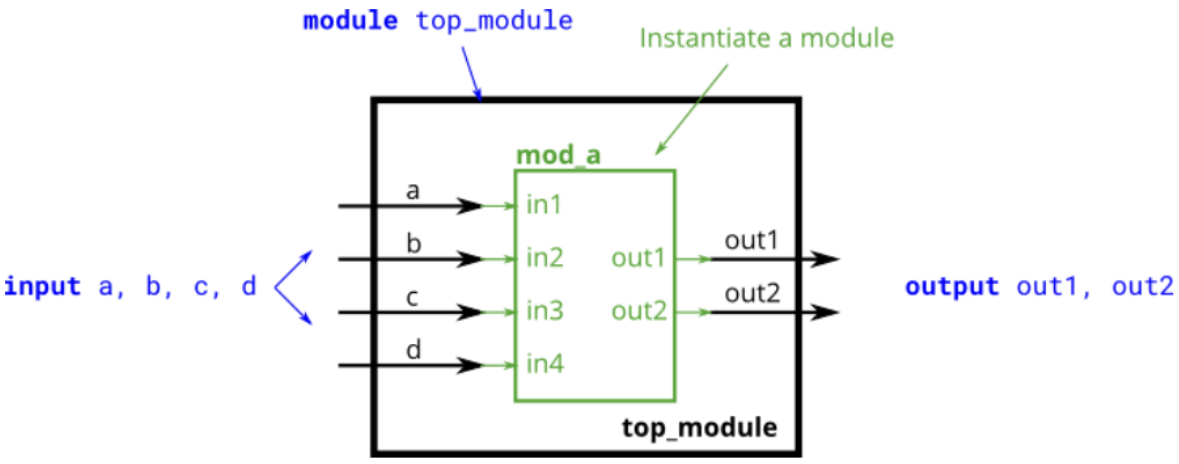
module_pos Previous Next module_shift

This problem is similar to module. You are given a module named `mod_a` that has 2 outputs and 4 inputs, in some order. You must connect the 6 ports *by name* to your top-level module's ports:

Port in `mod_a`	Port in `top_module`
`output out1`	`out1`
`output out2`	`out2`
`input in1`	`a`
`input in2`	`b`
`input in3`	`c`
`input in4`	`d`

You are given the following module:

```
module mod_a ( output out1, output out2, input in1, input in2, input in3, input in4);
```

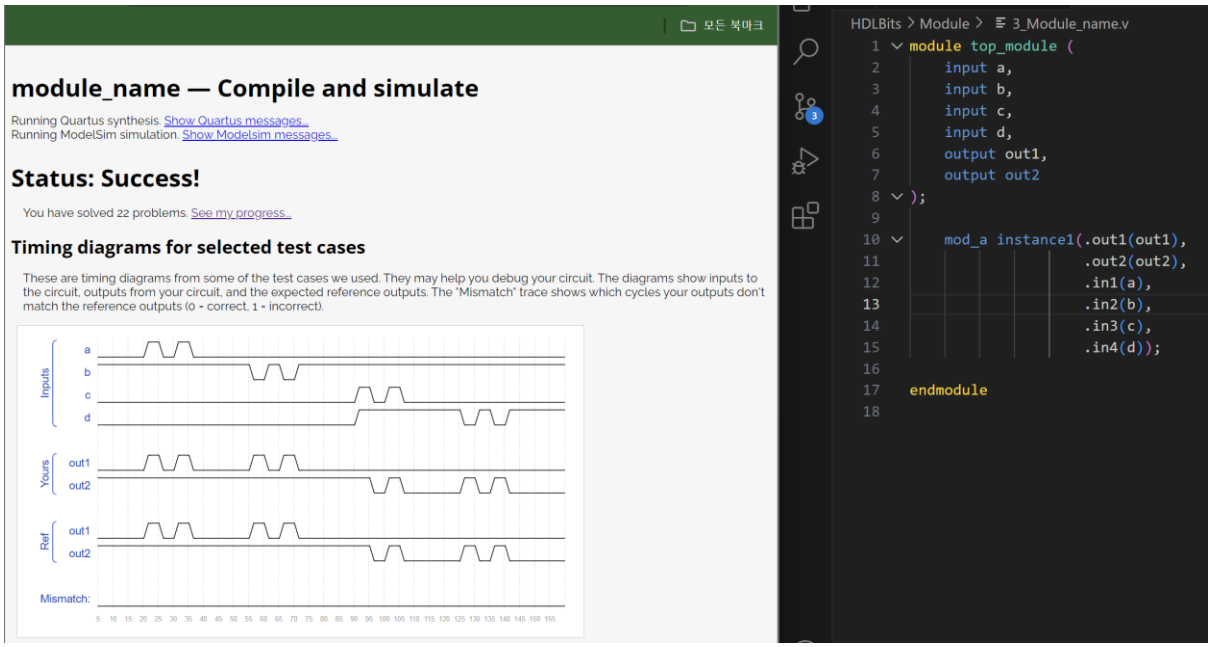


Expected solution length: *Around 1 line.*

설명

- 이름에 의한 포트 매핑을 연습한다.

코드


모든 북마크
module_name — Compile and simulate
Running Quartus synthesis. Show Quartus messages...
Running ModelSim simulation. Show Modelsim messages...
Status: Success!
You have solved 22 problems. See my progress...
Timing diagrams for selected test cases
These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 - correct, 1 - incorrect).
Inputs
a
b
c
d
Yours
out1
out2
Ref
out1
out2
Mismatch:
HDLBits > Module > 3_Module_name.v
module top_module (
input a,
input b,
input c,
input d,
output out1,
output out2
);
mod_a instance1(.out1(out1),
.out2(out2),
.in1(a),
.in2(b),
.in3(c),
.in4(d));
endmodule