A Frequency Adaptive Three-Phase Sequence Detector Synchronization System for Power Systems Applications

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***Abstract*—This paper presents a Sequence Detector Synchronization System (SD-SS) capable of extracting the positive, negative and zero sequence components of a three phase signal. The system is frequency adaptive, and provides real time frequency, phase and amplitude estimations of the extracted positive sequence component. The SD-SS is able to operate over a wide range of frequencies (40-2000Hz), and in the presence of significant input signal distortion (THD as high as 100%). The SD-SS dynamically compensates for DC offsets and is capable of achieving parameter estimations in compliance with the IEEE Std.C37.118-2011 for synchrophasors. The system employs an adaptive FIR filtering technique that offers a high degree of immunity to harmonics and notch-types disturbances over the full operating range of frequencies. In the event of input transients such as balanced/unbalanced amplitude sags and swells, balanced/unbalanced phase steps and positive or negative frequency ramps (up to 700Hz/sec), the system achieves a worst case transient response time of 2 cycles of the input period. The SD-SS is implemented as a proof of concept on a Field Programmable Gate Array (FPGA) platform.**

***Index Terms* – synchrophasor, PMU, Std.C37.118-2011, positive sequence tracking, dynamic frequency range, fast transient recovery.**

I. Introduction

In analyzing the operation of power systems and detecting faults, three phase signals are usually decomposed into the positive, negative and zero sequence components. The extracted positive sequence component is a vital piece of information used in the control and operation of grid connected devices such as DC-AC converters, static VAR compensators, active power filters [1], as well as isolated power systems employed in the aerospace industry and off-shore communities. The negative and zero sequence components can be used for protection control [2], or for determining the type and location of a fault appearing in a power network [3]. The supply of high quality power requires power measurement systems capable of extracting the sequence components from a three phase input signal and tracking them in real time.

A. Grid Connected Applications

The need for developing synchronization systems with better dynamic response has increased in recent years due to emerging power applications such as distributed generation systems based on grid connected inverters and power compensators [4]-[5]. The emphasis placed on the development of the smart grid in recent years has also created the need for the deployment of smart measurement devices within the grid, such as Phasor Measurement Units (PMUs) [6]. The future addition of more intermittent distributed generation to the grid such as wind and solar farms will also create larger variations in frequency and voltage magnitude within the power system. More recently, the IEEE C37.118-2005 synchrophasor standard has been updated to include dynamic performance testing such as amplitude/phase steps and frequency ramps. The performance of several PMUs based on these new dynamic tests was recently presented [7]. The conclusion was that all tested PMUs failed the dynamic performance assessment, specifically the dynamic frequency ramp tests ($\pm$1Hz/sec for $\pm$5Hz range). These results demonstrate the need for measurement units with better frequency ramp tracking capabilities and dynamic response for grid connected synchrophasor estimation.

B. Isolated and Aerospace Applications

Power systems that are isolated from the main power grid, such as islanded microgrids, aerospace power systems or isolated generators, have larger operating frequency ranges (360-800Hz for the aerospace industry [8]) and can experience much larger frequency ramps (up to 250Hz/sec). In recent years, the aerospace community has been driving for a "More Electric Aircraft", which entails the removal of hydraulic power generation and increasing the use of power electronics [9]. This trend has promoted the development of more efficient/lightweight DC-AC converters [10] and measurement systems with better fundamental frequency estimation [11]. The monitoring and control of aerospace systems require synchronization systems that can operate over a wide frequency range, have good dynamic response to transients, and extract the sequence components in

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the presence of harmonic distortion, wideband noise and DC-offsets.

An increasing number of papers that claim to offer better solutions for synchronization have appeared in the literature over the past decade. Table I presents several of the most widely cited three phase schemes which appear in recent publications (2006-2011) and have frequency adaptive capabilities. The table displays the frequency range each system can operate under, the transient recovery time for amplitude and/or phase steps, and the frequency tracking capabilities of each device in terms of frequency steps and frequency ramps. The numbers provided in table I are extracted from the references cited for each system. If no tests or information was presented with respect to a certain dynamic feature, then "N/P" has been placed in the appropriate column for the given system.

TABLE I
DYNAMIC PERFORMANCE OF DIFFERENT SYNCHRONIZATION SYSTEMS

Synchronization System	Frequency Operating Range	Transient Resp. Time	Frequency Step Limit	Maximum Frequency Ramp Rate
PMU [12]	50-70Hz	200ms	1Hz	N/P
DSOGI-PLL [13]	40-60Hz	50ms	10Hz	N/P
EDCS-PLL [14]	40-60Hz	40ms	N/P	0.5Hz/sec
E-PLL [15]	30-90Hz	50ms	5Hz	1Hz/sec
FRF-PLL [16]	38-62Hz	50ms	15Hz	N/P

As seen from table I, no three phase synchronization system has a wide frequency range of operation to accommodate isolated power systems, due to the use of fixed frequency filtering techniques. Furthermore, few papers present frequency ramp transient results, and when presented, they are small in magnitude. While small frequency ramp tests ($\pm$1Hz/sec) are sufficient for main grid operation, these ramps are orders of magnitude lower than the ones encountered when dealing with isolated power systems, such as aerospace generators. Based on the current literature, no synchronization system operates over a large input frequency range while providing fast transient response and the ability to track positive and negative frequency ramps in the presence of signal distortion.

The Sequence Detector - Synchronization System (SD-SS) proposed in this paper is a three phase digital device that extracts the positive, negative and zero sequence of a three phase input signal and estimates the amplitude, phase and frequency of the positive sequence component over the full frequency range (40-2000Hz). Operability over such a large fundamental frequency range is achieved with the help of an adaptive FIR filtering technique. The SD-SS can recover from input transient events such as amplitude sags/swells and positive/negative phase steps in two fundamental cycles and can track positive/negative frequency ramps as high as 700Hz/sec. Finally, the system was verified to be compliant with the IEEE C37.118.1-2011 Standard for synchrophasors and can be operated as a stand alone Phasor Measurement Unit (PMU).

The paper is organized as follows. Section II presents the design of the SD-SS, section III details the hardware implementation of the system and section IV shows test results which outline the performance of the SD-SS, including the C37.118.1-2011 synchrophasor tests. Finally, section V concludes the article with a summary of the overall system performance.

II. SYSTEM DESIGN

The block diagram of the SD-SS system is shown in figure 1. The three phase input signal is discretized using

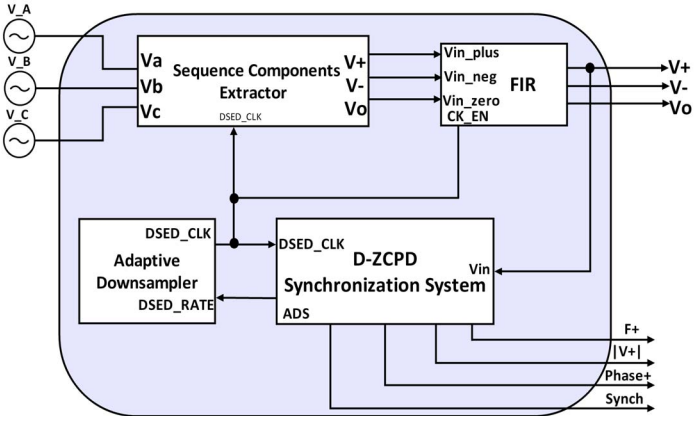

Fig. 1. SD-SS Block Diagram

three A/D modules and fed into the Sequence Components Extractor (SCE) block. The purpose of the SCE block is to extract the positive, negative and zero sequence components of the incoming wave signal. The extracted sequence components are fed into an adaptive FIR filter block that is used to attenuate signal distortions such as harmonics and wideband noise. The filtered positive sequence signal, denoted as V_+, is fed into a single phase synchronization system based on a DC compensated zero-crossing and peak detection (D-ZCPD) algorithm [17]. The purpose of the D-ZCPD is to generate magnitude ($|V_+^*|$), frequency (f_{EST}), and phase (θ_+) estimates of the positive sequence component. The D-ZCPD system also generates an Adaptive Downsampling (ADS) feedback signal that is fed into the Adaptive Downsampler block. This block uses the ADS rate to generate a downsampled clock denoted as f_{ADS}. The f_{ADS} clock is used to maintain a fixed ratio between the input fundamental frequency and the sampling frequency. This fixed ratio ensures that the bandpass of the FIR block is maintained around the nominal input frequency and that the SCE coefficients do not need to be adapted. The following three subsections present design details for the SCE, FIR and D-ZCPD blocks that are displayed in figure 1.

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A. Sequence Components Extractor

The conventional Symmetrical Components method for extracting sequence components suffers from inaccurate estimations during transient events and introduces large computational delays. Reference [18] outlines the derivation of the patented Fast Retrieval Technique used in the SD-SS. For this technique, the sequence components are extracted from a three phase discrete input signal. The main advantage of the Fast Retrieval Technique is that it lends itself to discrete time implementations with minimal hardware requirements. The output is generated with only one sample delay, removing the need for large memory resources. The sequence components are extracted as a function of the three input phases (V_a, V_b, V_c) based on the following discrete time formulas:

$$3V_+[k] = V_a[k] + P_bV_b[k] - Z_bV_b[k-1] - P_cV_c[k] + Z_cV_c[k-1] \quad (1)$$

$$3V_-[k] = V_a[k] - P_cV_b[k] + Z_cV_b[k-1] + P_bV_c[k] - Z_bV_c[k-1] \quad (2)$$

$$3V_0[k] = V_a[k] + V_b[k] + V_c[k] \quad (3)$$

where Pb, Pc, Zb, and Zc are coefficients dependent on the sampling rate and the fundamental frequency. By maintaining a fixed ratio of the sampling and fundamental frequency, the SCE coefficients do not have to be adapted, and equations (1), (2) and (3) are easily implemented in hardware. The frequency ratio is kept constant using the ADS rate, which is used to downsample the discretized three phase input.

B. Adaptive Downsampler

The ADS rate is computed within the D-ZCPD block, twice per cycle, based on the following formula:

$$ADS = round\left(\frac{f_{A/D}}{N \cdot f_{EST}}\right) \quad (4)$$

where $f_{A/D}$ is the A/D sampling frequency, N represents a fixed number of ADS samples recorded in one fundamental cycle and f_{EST} is the fundamental frequency estimation. The ADS rate is fed back into the Adaptive Downsampler block, which generates a downsampled clock denoted as f_{ADS}. The advantages of driving the SCE and FIR blocks with the f_{ADS} clock are as follows:

- The SCE coefficients are maintained constant.
- The FIR filter block maintains its frequency response characteristics over a wide frequency range (40-2000Hz).

C. FIR Filter

The purpose of the FIR filter block is to output the fundamental component of the positive, negative and zero sequences, while attenuating input disturbances such as harmonics, interharmonics and wideband noise. This is achieved using a serial-parallel (hybrid) lowpass FIR filter implementation with an order of 180, for each sequence component. The downsampled f_{ADS} clock is used to adaptively adjust the normalized fundamental frequency and maintain it within the passband of the filter. The normalized fundamental frequency f_{norm} is derived using:

$$f_{norm} = 2\pi \cdot \frac{f_{ADS}}{f_{A/D}} \quad (5)$$

where $f_{A/D}$ is downsampled by N=180 to obtain f_{ADS}. This ensures a fixed attenuation at all frequency harmonics, irrespective of the input signal frequency. Based on equation 5, the normalized fundamental frequency is located at $\frac{\pi}{90}$ $rad/sample$. Figure 2 displays the magnitude response of the 180 order filter. The fundamental frequency is located at $\frac{1}{90} \cdot \pi$ $rad/sample$ with an attenuation of -0.155dB. The third harmonic is located at $\frac{1}{30} \cdot \pi$ $rad/sample$ and is attenuated by approximately -50dB. The filter was generated using the Filter Design & Analysis (FDA) tool box available in MATLAB, and has the following design specifications:

- Fir Least Square Implementation.
- Direct-form symmetric FIR.
- Hybrid implementation using 6 multipliers.
- 16-bit precision for input/output signals.
- W_{pass} = 0.011 $\pi \cdot rad/sample$.
- W_{stop} = 0.033 $\pi \cdot rad/sample$.

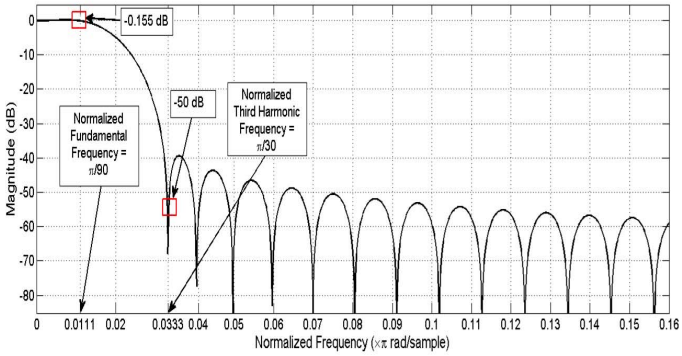

Fig. 2. Magnitude response of lowpass FIR filter

D. D-ZCPD Block

The detailed diagram of the D-ZCPD synchronization system is shown in figure 3. The D-ZCPD block is used to generate frequency, amplitude and phase estimates of the positive sequence component.

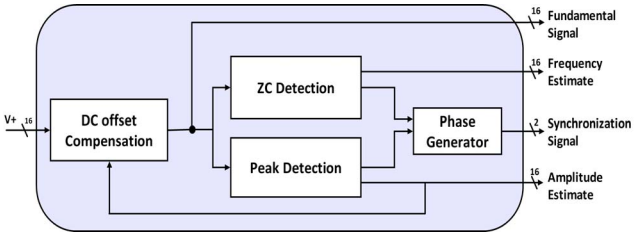

Fig. 3. D-ZCPD Block Diagram

The frequency of the input wave is estimated using a zero-crossing technique. A counter denoted as $Samp_{ZC}$ is used to record the number of A/D samples between two successive x_{ZC} samples. This counter is equal to:

$$Samp_{ZC} = m \cdot ADS \tag{6}$$

where 'm' is a positive integer. Figure 4 displays the zero-crossing samples x_{ZC} , the $Samp_{ZC}$ counter along with a DC offset. In steady state operation, the value of m is equal

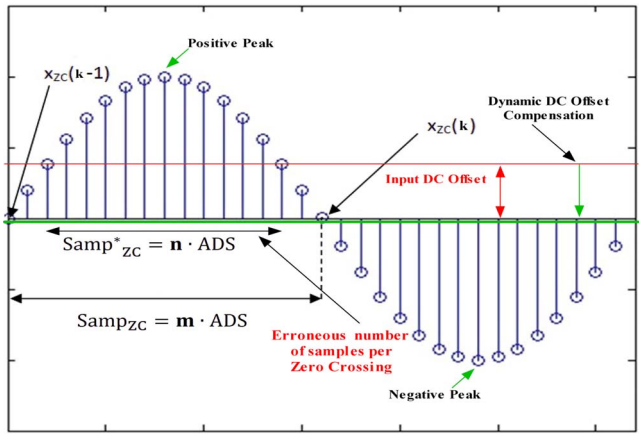

Fig. 4. Zero-crossing detection and DC-offset compensation

to either $N/2$ or $N/2 \pm 1$. An auxiliary term, denoted as $Samp_{adj}$, is added to the $Samp_{ZC}$ counter to compensate for the mismatch between the fundamental frequency and the A/D sampling frequency, thus improving the accuracy of the frequency estimation:

$$Samp_{adj} = ADS \cdot \frac{|x_{ZC}[k]| - |x_{ZC}[k-1]|}{x_{FIR}[n] - x_{FIR}[n-1]} = ADS \cdot \frac{\Delta x_{ZC}}{\Delta x_{FIR}} \tag{7}$$

where Δx_{FIR} is the difference between two successive samples output from the FIR. The adjusted counter is used to obtain the fundamental frequency estimation, f_{EST}:

$$f_{EST} = \frac{f_{A/D}}{2 \cdot (Samp_{ZC} + Samp_{adj})} \tag{8}$$

The amplitude estimation of the input signal is based on a peak detection algorithm. Consecutive amplitude estimations are fed back to the dynamic DC Offset Compensation block (DOC) to determine the input signal DC bias magnitude. As can be seen in figure 4, a DC offset results in incorrect fequency estimations due to inaccurate $Samp_{ZC}$ counter values. To fix this problem, the DOC block identifies the negative and positive peak amplitudes of the signal and recursively adjusts the ground level to maintain a zero offset. This adjustment allows the frequency estimation to be measured accurately in the presence of DC offsets. The positive sequence phase estimate, denoted as θ_+, is extracted with the help of the frequency estimation. The phase estimate is generated every A/D clock cycle from 0 to 2π in one fundamental cycle, by using the ratio between the estimated frequency and the fixed A/D frequency:

$$\theta_+ = 2\pi \frac{f_E ST}{f_{A/D}} \cdot \left(n + ADS \cdot \frac{x_{ZC}[k]}{\Delta x_{FIR}} \right) \tag{9}$$

where n is the value of a counter which is incremented every A/D clock cycle and reset once $\theta_+ = 2\pi$.

III. Hardware Implementation of SD-SS

The system is implemented on a PMC-AX3065 Acromag board which has 4 A/D modules, 2 D/A modules, and a Virtex II FPGA core with 32,256 logic cells. The PMC-AX series ships with a built in C program that facilitates the synchronized flow of data from the input A/D modules to the output D/A modules. The software eliminates the need to perform direct low-level manipulations of the piping registers. The main disadvantage of this software-hardware hybrid approach, is that it limits the data collection and processing capabilities of the system. Because of this limitation, a hardware-only approach was developed. The hardware-only approach is implemented in synthesizeable VHDL and uses a Mealy Finite State Machine (FSM) to setup the memory FIFO registers and perform the data piping. The FSM is clocked at 64 MHz, and achieves a data transmission rate of up to 900 kHz, the maximum rate supported by the D/A modules. Figure 5 outlines the states,

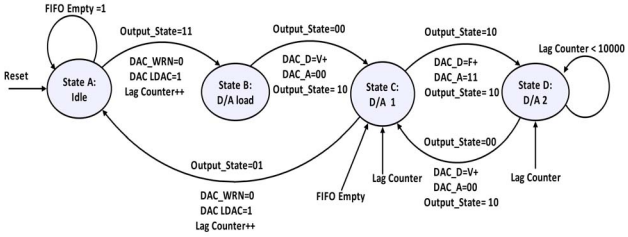

Fig. 5. Hardware Data piping Finite State Machine

the transition signal and the output at each state. The state transition is displayed above the arrow, while the output is displayed below it. The output is computed directly after an input change. The FSM consists of 4 states encoded with the Output_State transition signal.

IV. Experimental Setup and Results

The implementation block diagram of the SD-SS system is shown in Figure 6. The SD-SS three phase inputs were generated using two different methods: (a) three synchronized function generators and (b) a three phase power system lab setup. In most power circuit tests, the three phase generators used were rated at 115Vrms line to line, at 60Hz. The A/D input signals were stepped down through voltage sensors with an input to output ratio of 70V/1V. The experimental results obtained are presented in the following subsections.

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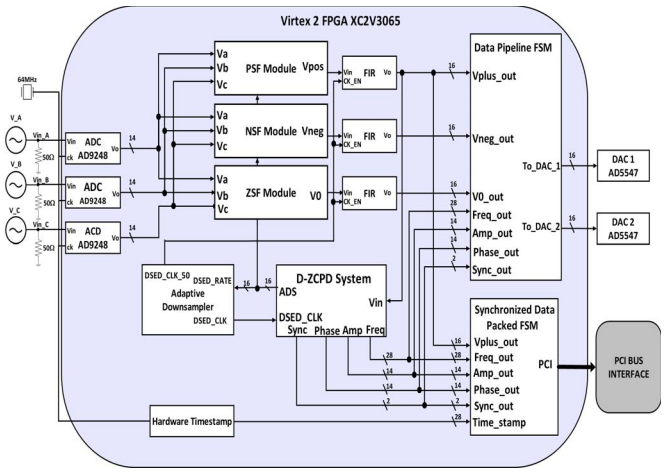

Fig. 6. SD-SS Implementation

The experimental results are divided into two categories: (a) steady state tests and (b) dynamic tests. The steady state tests outline the frequency range of operation, as well as the filtering capabilities of the system. The dynamic tests present the capability of the system to recover from faults such as balanced and unbalanced phase/amplitude steps and frequency ramps.

A. *Steady State Operation*

The SD-SS system was tested with a range of frequencies (40-2000Hz) and nominal amplitudes (0.1-2pu) with THD values greater than 100% and 3rd harmonics as large as 40%. This is exemplified in figure 7 which displays a square

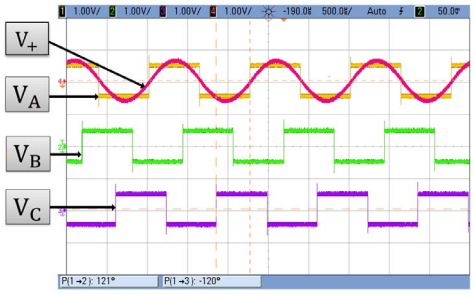

Fig. 7. Balanced Three Phase Square Wave Input at 800Hz

wave input at 800Hz, along with the positive sequence estimation, denoted as V_+. The positive sequence signal has the harmonics attenuated, and is synchronized with phase A. For the power system tests, the three phase generators were connected to a balanced three phase load, through a series inductance on each phase.

Figure 8(a) displays the three phase input signal obtained from the power system lab setup, while part (b) shows the positive sequence estimate V_+. The synchronization signal, denoted as Sync, shows that the positive sequence estimate is synchronized in real time with the three phase input signal.

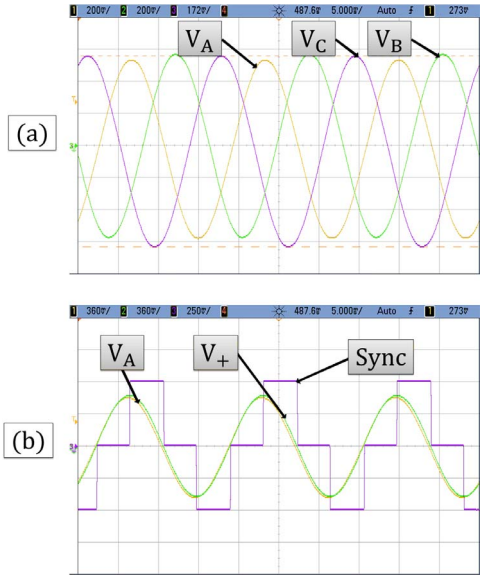

Fig. 8. Balanced Three Phase Input

The SD-SS system is also able to extract the frequency, phase and amplitude of a Sinusoidal Pulse Width Modulated (SPWM) signal. Figure 9 shows Phase A connected to the

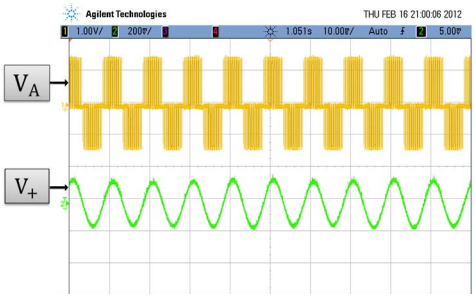

Fig. 9. PWM Positive Sequence

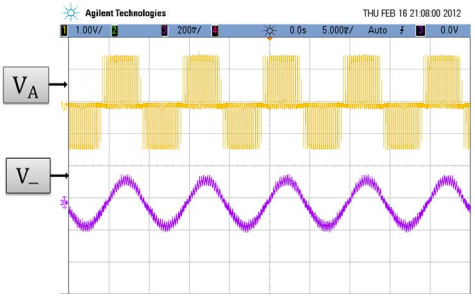

Fig. 10. PWM Negative Sequence

output of a SPWM Voltage Source Converter (VSC). The extracted positive sequence component, denoted as V_+, has the harmonics attenuated and is synchronized with the input wave. Figure 10 displays the extracted negative sequence component, denoted as V_-, for the same SPWM input.

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B. Dynamic Tests

The dynamic tests are divided into two categories: (a) amplitude and phase step transients and (b) dynamic frequency ramps. The amplitude and phase step transients were generated by balanced and unbalanced load switching events, and by generating single phase outages in the system. The frequency ramps were generated by creating single phase frequency ramp events with a function generator or with the help of a permanent magnet synchronous machine.

1) Amplitude and Phase Steps: Single and three phase loads were connected/disconnected from the power system in order to generate balanced/unbalanced amplitude and phase steps. Balanced three phase load switching events are shown in figures 11 and 12. In both presented cases (for one and two consecutive load switching events), the positive sequence estimation recovers within two fundamental cycles from the transient event.

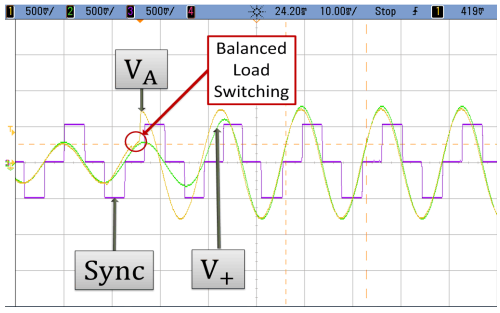

Fig. 11. Three phase balanced load switching of output load

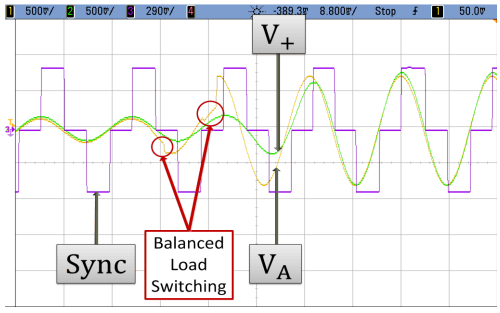

Fig. 12. Two sequential balanced load switching events

Figure 13 shows the result of three subsequent load switching events on phase A only. As expected, the magnitude of V_A is reduced, along with a decrease in the amplitude of the positive sequence estimation. The phase estimate, θ_+, remains synchronized to V_+. In figure 14, the system is initially unbalanced with the negative sequence component denoted as V_- displayed along with V_+. Load switching on phases B and C re-balance the output load, and as a result, V_- diminishes and V_+ increases to the nominal

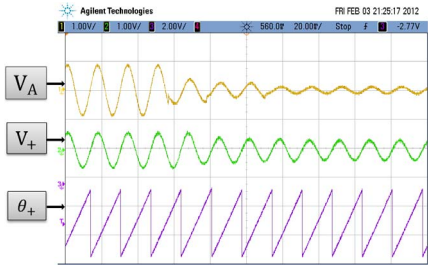

Fig. 13. Sequential unbalanced load switching for Phase A

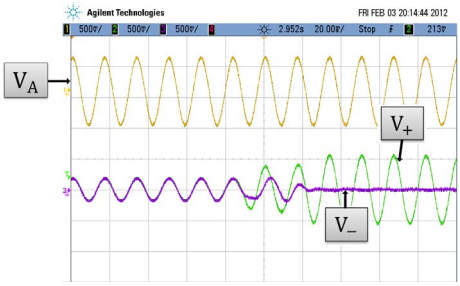

Fig. 14. Positive and negative sequence estimations for an unbalanced to balanced three phase transition

balanced value. Finally, figure 15 displays the positive and negative sequence estimates obtained from a momentary heavy loading of phase C. As can be seen, the SD-SS is able to track the changes of the positive and negative sequences in real time.

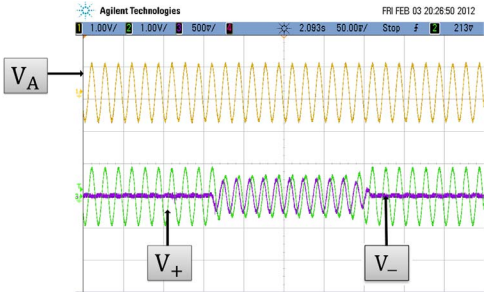

Fig. 15. Positive and negative sequence estimations for a momentary unbalance in the three phase input signal

In all amplitude and phase step transient tests and simulations, the SD-SS system was able to recover from the disturbance and re-synchronize with the positive sequence within two cycles. The fast transient response of the system was tested for a variety of phase and amplitude steps (range of $\pm 60^\circ$ phase changes and 0.1 - 2.0pu amplitude changes). Regardless of the severity of the transient events, the transient recovery time remains below two fundamental cycles.

2) Frequency Ramps: The SD-SS is able to track any sequence component through positive and negative frequency

ramps as large as 700Hz/sec. Figure 16 presents the results of a 690Hz/sec positive frequency ramp. This ramp was generated with a function generator connected to phase A. The frequency estimation displayed on the oscilloscope capture shows that the synchronization device is able to track the steep frequency ramp.

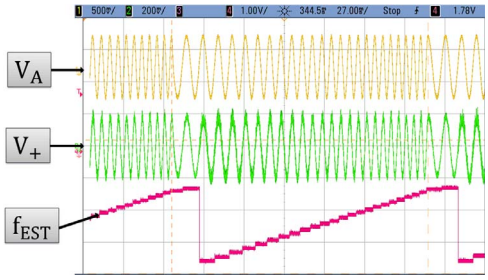

Fig. 16. Frequency ramp of 690Hz/sec from 80Hz to 210Hz

The frequency tracking capabilities of the SD-SS were also tested using a three phase, 6 pole, permanent magnet synchronous machine. The generated negative frequency ramp of approximately 84Hz/sec is shown in figure 17. The SD-SS was able to track this three-phase frequency ramp, even in the presence of input signal harmonics and with an associated negative amplitude ramp.

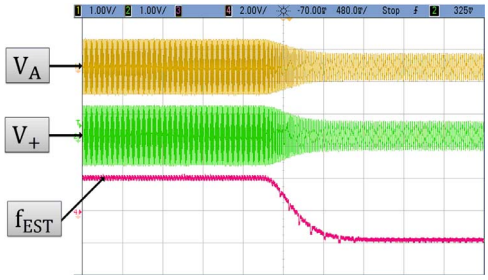

Fig. 17. PM-SM stator output with a -84Hz/sec frequency ramp

C. Operation as a Phasor Measurement Unit

The Sequence Detector - Synchronization System can operate as a stand alone Phasor Measurement Unit. The SD-SS operation is compliant with the IEEE Synchrophasor Standard C37.118.1-2011. The PMU simulations presented in this section were calibrated with the results obtained from the experimental setup. The calibration consisted of including the appropriate wide-band noise and quantization levels of the internal signals in the simulation setup, in order to obtain approximately the same error ranges as with the hardware implementation. The experimental setup was modified to include a rate of change of frequency measurement (ROCOF), and a hardware-based data acquisition block, as seen in figure 6. The onboard 64 MHz clock is used as a common reference time base that emulates a GPS time stamp. The accuracy of the of onboard crystal clock is within 0.5μs. This approach is implemented in synthesizeable VHDL and uses a Finite State Machine (FSM) to acquire synchronized data frames relating to the amplitude, frequency, phase and rate of frequency change of the extracted positive sequence component. The FSM is clocked at 64 MHz, and has a variable data transmission rate, from 10 to 120 samples per second.

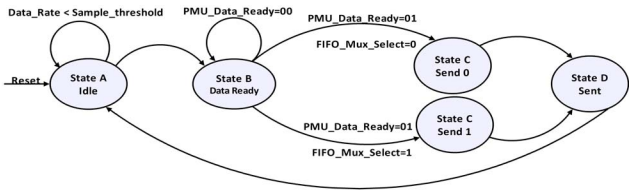

Fig. 18. Synchronized Data Packets Finite State Machine

Figure 18 outlines the states, the transition signal and the output at each state. The FSM consists of 4 states encoded with the PMU_Data_Ready transition signal. The FSM is in the PMU Idle state at Reset or when the data is not ready to be sampled. Once the sampling instance is detected the FSM toggles to State B where the frequency, ROCOF, amplitude and phase measurement frames are recorded. The sampled data is then interlaced with 4 data FIFOs available on the Acromag board. Once a data frame is sampled, time stamped and relayed to the FIFOs, the FSM reaches State D and the cycle is repeated.

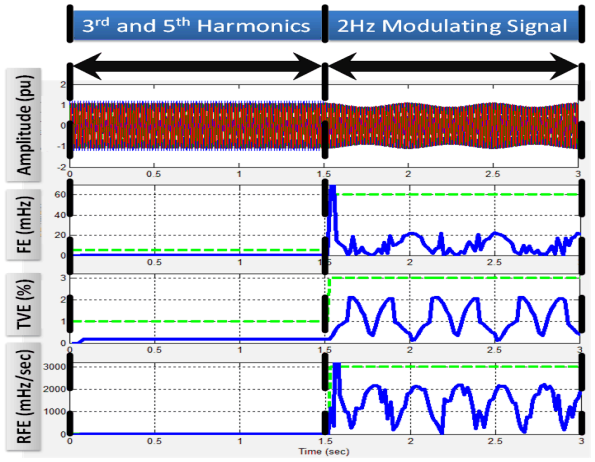

Fig. 19. 10% 3rd and 5th harmonics and 2Hz modulating signal

Figure 19 shows a set of steady state simulation results. The Total Vector Error (TVE), Frequency Error (FE) and Rate of Frequency Error (RFE) of the SD-SS estimations are displayed for a three phase input signal with 10% third and fifth harmonic (0-1.5sec) and for a 2Hz 10% phase and amplitude modulating signal (1.5-3sec). The SD-SS is able to generate the required measurements within the error limits, for the frequency/amplitude ranges and harmonics/modulating signal levels provided in the synchrophasor standard. The allowed error limits are represented by the dashed horizontal lines. The SD-SS system is also able

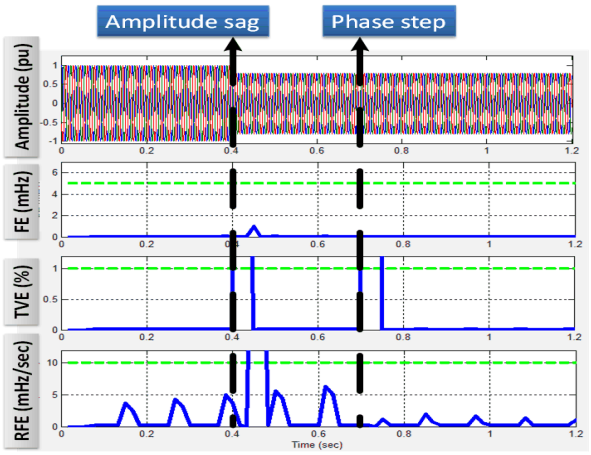

Fig. 20. 0.8pu amplitude sag and 20° positive phase shift

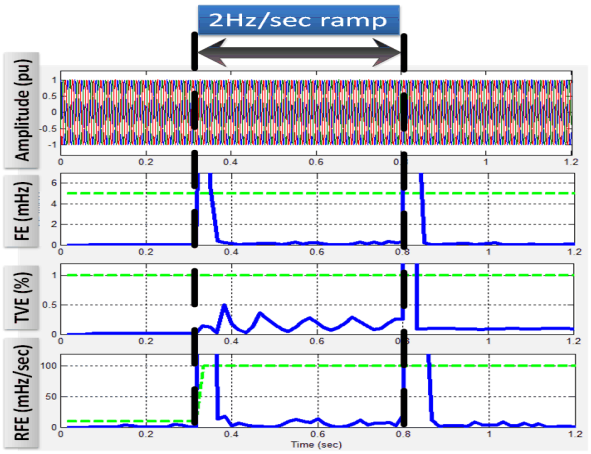

Fig. 21. 2Hz/sec positive frequency ramp

to maintain TVE, FE and RFE within the given limits for all dynamic tests required. Figure 20 presents the dynamic response of the system to a 20% amplitude sag at 0.4 seconds and a positive 20 degrees phase shift at 0.7 seconds, while figure 21 presents a 2Hz/sec frequency ramp from 0.3 to 0.8 seconds. Note that figures 20 and 21 show transient tests which are twice as large as the maximum required by the IEEE C37.118.1-2011 standard. Despite doubling the severity of the transients, the SD-SS system is able to maintain operation within the given error limits.

Table II displays the largest error limits obtained for the tests outlined in the first column. The SD-SS system is able to provide accurate measurements for a variety of test conditions, as outlined by the C37.118.1-2011 standard, and can be used as a stand-alone PMU unit.

V. Conclusion

The proposed Sequence Detector - Synchronization System can extract and track any of the three sequence components and generate phase (θ_+), frequency (f_{EST}) and amplitude ($|V_+|$) estimates from a wide variety of

TABLE II
PMU Performance Metrics

Test	TVE	FE (mHz)	RFE (mHz/sec)	TVE resp time	Frequency resp time
$55-65Hz$	0.35	0.3	6	N/A	N/A
10% harmonics	0.39	0.3	6.5	N/A	N/A
0.1-2Hz mod signal	2.1	22.3	2300	N/A	N/A
20% ampl step	0.48	0.3	7.4	2 cycles	2 cycles
20° shift	0.42	0.3	6	1 cycle	2 cycles
5Hz/sec freq ramp	0.51	1.6	13.1	2 cycles	3 cycles

power networks ranging from grid-connected applications to aerospace power systems. This flexibility comes from the ability of the system to operate over a large frequency range while providing fast signal transient tracking time and high accuracy measurements of frequency and amplitude. The system is compliant with the IEEE C37.118.1-2011 Standard for synchrophasors and can therefore be operated as a Phasor Measurement Unit. The system is implemented as a proof of concept on a FPGA platform and is synthesizeable into an application specific integrated circuit for high volume production. The SD-SS was validated under both steady state and transient conditions. The results indicate that the SD-SS is capable of achieving the following:

- Operate over a wide frequency range (40-2000Hz) suitable for utility and non utility applications. The frequency range is constratined by the available hardware resources and is not a hard limit of the system design.
- Achieve synchronization after amplitude sags and swells from 0.1pu - 2.0pu and phase shifts of $-60°$ to $60°$ within two fundamental cycles.
- Track positive and negative frequency ramps of up to 700Hz/sec, in the presence of harmonic distortion and amplitude ramps.
- Operate as a stand alone PMU in compliance with the C37.118.1-2011 Standard for synchrophasors.
- Achieve low steady state estimation error for amplitude, phase and frequency over the full fundamental frequency range.

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