FPGA based implementation of Network-on-chip for efficient distributed computing

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***Abstract*—The abstract goes here.**

***Index Terms*—IEEE, IEEEtran, journal, LaTeX, paper, template.**

I. Introduction

Fpga

II. NoC Architecture

Network-on-chip is a 2D mesh based architecture with switches and processing elements(PE). A PE could be a processor core or a dsp core or an IP block etc. Each PE is connected to a switch and each switch is connected to four neighbouring switches. A PE cannot communicate directly with other PE's. It can only send and recieve packets directly from its corresponding switch. We have implemented a parameterized NoC architecture without any packet loss . In this architecture a switch can receive packets from left or bottom swithces or its PE and it can only send packets to its right or top switches or its PE. Data is routed over the network in a packet-switched style.Each packet carries two fields. 1) Address of the destination 2) data payload.We have implemented a deflection based routing system where ,if a switch gets packets from two of its neighbouring switches at the same clock edge such that both the packets have to be routed in the same direction our routing system makes sure that the switch deflects one of these packets.

III. Results

Subsection text here.

1) : The following table contains the results for Noc that has both switch and Pe

Resource Utilization			
Size of architecture	Size of Input in bits	Total number of LUT's used	Total Number of flip-flops used
2x2	8	242	156
2x2	32	487	444
2x2	64	871	828
2x2	256	3204	3132
4x4	8	1060	816
4x4	32	2222	1968
4x4	64	3767	3504
4x4	256	13117	12720
8x8	8	4897	4032
8x8	32	9905	8640
8x8	64	16141	14784
8x8	256	53609	51648

Timing Report		
Size of architecture	Size of Input in bits	Minimum Period Required(ns)
2x2	8	0.750
2x2	32	0.750
2x2	64	0.750
2x2	256	0.750
4x4	8	0.750
4x4	32	0.750
4x4	64	0.750
4x4	256	0.750
8x8	8	0.750
8x8	32	0.750
8x8	64	0.750
8x8	256	0.750

2) : The following table contains the results for Noc that has only switch

Resource Utilization			
Size of architecture	Size of Input in bits	Total number of LUT's used	Total Number of flip-flops used
2x2	8	57	39
2x2	32	111	111
2x2	64	194	207
2x2	128	360	399
2x2	256	680	783
4x4	8	73	51
4x4	32	135	123
4x4	64	214	219
4x4	128	374	411
4x4	256	694	795
8x8	8	83	63
8x8	32	145	135
8x8	64	225	231
8x8	128	385	423
8x8	256	705	807

Timing Report		
Size of architecture	Size of Input in bits	Minimum Period Required(ns)
2x2	8	0.750
2x2	32	0.750
2x2	64	0.750
2x2	128	0.750
2x2	256	0.750
4x4	8	0.750
4x4	32	0.750
4x4	64	0.750
4x4	128	0.750
4x4	256	0.750
8x8	8	0.750
8x8	32	0.750
8x8	64	0.750
8x8	128	0.750
8x8	256	0.750

IV. Conclusion

The conclusion goes here.

Appendix A

Appendix one text goes here.

Appendix B

Appendix two text goes here.

Acknowledgment

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