**PROJECT REPORT**

**(August-November, 2017)**

**SIMULATION AND FABRICATION OF**

**MULTI LEVEL INVERTER**

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**(Deemed University)**

(August-November, 2017)

**DECLARATION**

I hereby declare that the project work entitled “**SIMULATION AND FABRICATION OF MULTI LEVEL INVERTER**” is an authentic record of my own work carried out at **PEC University of Technology** a requirements of four months project of the 5th semester for the award of degree of B.Tech. Electrical Engineering, PEC University of Technology (Deemed University), Chandigarh, under the guidance of **Dr. Jagdish Kumar** (Faculty Mentor), during **August to November, 2017**.

Date: \_\_\_\_\_\_\_\_\_\_\_\_

Certified that the above statement made by the students is correct to the best of our knowledge and belief.

**Dr. Jagdish Kumar**

Assistant Professor

(Faculty Coordinator)

**ACKNOWLEDGEMENT**

It gives us immense pleasure to take this opportunity to thank **PEC University of Technology** for giving us such a great opportunity to do this project. We deem it our privilege to have carried out this dissertation work under this well-known institution.

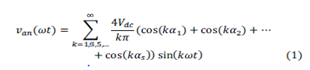
The success and final outcomes of this project required a lot of guidance and assistance from many people and we are very fortunate that so many people came to lend us a helping hand and make us learn so many new things and gave us a chance to revise our old technical concepts and at the same time helping us to understand the importance of cooperation and team work.

We would like to thank our Head of the Department, Dr. Tilak Thakur for including Minor Project in out college curriculum. We would also like to express our sincere gratitude and indebtedness to our mentor **Dr. Jagdish Kumar** for his invaluable guidance and enormous help and encouragement, which helped us to complete our project successfully. His way of working was a constant motivation throughout the semester.

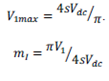
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|  | 1. **SUMMARY**   We were assigned this project as a part of our college curriculum for the time interval August to November, 2017. Thanks to this project, we got a chance to get familiar with MATLAB Simulation, electronics components, hardware fabrication and learnt about design and control of Seven Level Convertor by giving DC as input and obtaining modified sine wave as output.   * 1. **Project Title:**   Fabrication of Simulation of Multi Level Inverter   * 1. **Objectives:** * To make an AC supply from DC with **THD (Total Harmonic Distortion) less than or equal to 5%** in the final output waveform. * **MATLAB Simulation** of 3 Level Inverter, 11 Level 1-phase Inverter, 11 Level 3-phase Inverter. * **Hardware Fabrication** of 7 Level Inverter with Cascaded H-Bridge topology.   1. **Background:**     The project covers particularly the operating principle, physical fabrication, gate firing circuits, of inverter with Cascaded H-Bridge topology. The H-Bridges will be made using MOSFETs for hardware fabrication while IGBTs for MATLAB simulation.  The project is presented in two domains -  ● **MATLAB Simulation** - It is used to compute the values of parameters like Firing angles of IGBTs for different H Bridges used in inverter associated with model and to safely debug it before implementing on hardware.  ● **Hardware Model** - The hardware model has been developed on the basis of simulation done earlier. The Cascaded H-topology is used as this method helps to form different output voltage levels, increasing the total inverter output voltage and also its rated power and reducing the Total Harmonic Distortion (THD) in the output waveform. The method will be brought in use with the use of MOSFETs for switching purposes . The modulation  Fig 4: H-bridge unit  and firing pulses will be issued using Arduino microcontroller.  In the development of this model, our main intent had been to enhance our knowledge about inverters as the generation from most of the renewable sources is in the form of DC for example solar and wind power plants. This DC output has to be converted to AC for use in conventional systems and already prevalent systems in use.  Current advantages of this Project :-   * Higher power quality of output voltage. * Lower Harmonic content in output voltage waveform. * Reduced filtering requirements. * Used in machines requiring high power AC for operation. * Improved conversion efficiency due to lower switching losses.   1. **Tools Used** * Research Paper * MATLAB  1. **INTRODUCTION**   An **Inverter** is an electrical power device which is used to convert direct current (DC) into alternating current (AC). We can get AC at any required voltage and frequency, using appropriate control circuit. It can be used to convert DC power coming from solar panels, batteries, supercapacitors or medium voltage sources.  There are different types of inverters available these days. Few most commonly used inverter types are: Square wave inverter, Modified sine wave inverters, Multilevel inverters, Pure sine wave inverters etc. In household application, modified sine wave and pure sine wave inverters are used. The only difference being that, pure sine wave inverters have additional filtering circuitry and use techniques to make the output waveform a pure sine wave, with least possible value of THD, and that’s why they are comparatively expensive. On the other hand, Square wave inverter are cheaper than modified or pure sine wave inverters, but there is humming noise in inverter and in electrical appliances, as it operates; the value of THD is quite high and it leads to less safety and decreased life of appliances.    Fig 1: Modified and Pure Sine wave Inverters  We have designed an **11 level Cascaded Multilevel Inverter**, which falls in the category of Modified sine wave inverters.   * 1. **Topologies For Multilevel Inverter**   Based on mechanism of switching and the source of input voltage to the multilevel inverters, several topologies of multilevel inverters available-  **2.1.1 Diode Clamped Multilevel Inverter**- In this diode acts as a clamping device, while switches and capacitors are also present in the circuit. Output voltage is obtained across the capacitors. And for making ‘n’ levels, (n-1) capacitors are required in the circuit.    Fig 2: Diode Clamped Multilevel Inverter  **2.1.2 Flying Capacitor Multilevel Inverter**- In this capacitor acts as a clamping device, while switches are also present in the circuit.  Both these topologies are suitable to make 3 Level inverter only, due to capacitor charge balancing issues. Also, the clamping device transfers only a limited amount of voltage, due to which, in both cases, Maximum output voltage waveform=½(Input DC voltage).    Fig 3: Flying Capacitor Multilevel Inverter  **2.1.3 Cascaded H-bridge Multilevel Inverter-** In this, power scaling is easy. The circuit simply consists of switches which may be (MOSFET/ IGBT). To simulate an 11 Level inverter and to fabricate a 3 Level inverter, we have used this topology.   * 1. **Advantages Of Multilevel Inverter** * Higher power quality of output voltage, lesser value of THD. * Lower Harmonic content in output voltage waveform. * Reduced filtering requirement and thus saves cost. * Used in machines requiring high power AC for operation. * Improved conversion efficiency due to lower switching losses.   1. **Cascaded H-Bridge Multilevel Inverter**   A number of H-bridge inverter units with separate dc source for each unit are is connected in cascade or series.  Each H-bridge can, produce three different voltage levels: +Vdc, 0, and –Vdc by connecting the dc source to ac output side by different combinations of the four switches *S1*, *S*2, *S3*, and *S4*. Depending on firing pulses issued to the the four switches, which may be MOSFETs or IGBTs, we obtain a particular level in the output voltage.  The graph below shows the firing pulses given to the four switches: S1, S2, S3 and S4. When switches S1 and S4 are ON, we get +Vdc at output, while when switches S2 and S3 are ON, we get -Vdc at output. And when either S1 and S2 are ON or S3 and S4 are ON, then we obtain 0 Volt at output. This is how we obtain 3 Levels of voltage from a single H-bridge.    Fig 4: H-bridge unit    Fig 5: Waveform for single H-bridge unit  Also, at all times, the firing pulses issued to S1 and S3 will be complement of each other.  Similarly, for S2 and S4 as well. This is done to prevent short circuit of source voltage Vdc.    Fig 6: 5 Cascaded H-bridge units  In a cascaded H-bridge circuit, several H-bridges are connected in series such that the synthesized output voltage waveform is the sum of all of the individual H-bridge outputs. For a 11-level output phase voltage waveform using five H-bridges, magnitude of the ac output phase voltage is given by  **Van = Va1+Va2+Va3+Va4+Va5**    Fig 7: Waveform when 5 H-bridge units are cascaded  Every switch (MOSFET/ IGBT) is ON for 180° of the cycle i.e. half of the time period. For an 11 Level inverter, we fire 5 H-bridges at 5 different firing angles α1, α2, α3, α4, α5; these have been calculated using Newton-Raphson Method.  For a **1-phase** Inverter,  Number of levels in output waveform of 1-phase cascaded H-bridge inverter= **2n+1**  Example, for n=5, we obtain 11 levels in a 1-phase cascaded H-bridge Inverter.    Fig 8: 11 Level for a Single phase inverter  For a **3-phase** Inverter,  Number of levels in output waveform of 3phase cascaded H-bridge inverter= **4n+3**  Example, for n=5, we obtain 23 levels in a 3-phase cascaded H-bridge Inverter.    Fig 9: 11 Level for a Three phase inverter  Where, n= number of H-bridges cascaded in the circuit.  As we keep on increasing ‘n’ i.e. number of H-bridges in series, we obtain more number of levels in the output waveform and Total Harmonic Distortion (THD) decreases. |

**2.4 Mathematical Models Of Switching Angles and SHE Equations**

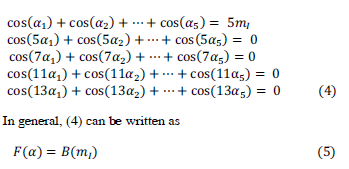
In general, the Fourier series expansion of the staircase output voltage waveform is given by



Where *s* is the number of H-bridges connected in cascade per phase. For a given desired fundamental peak voltage *V1*, it is required to determine the switching angles such that 0 ≤ a1 < a2 < …. < a5 ≤ pie/2 and some predominant lower order harmonics of phase voltage are zero.In three-phase power system, triplen harmonics are cancel out automatically in line-to-line voltage as a result only non-triplen odd harmonics are present in line to line voltages.The **modulation index,** m1, is the ratio of the fundamental output voltage V1 to the maximum obtainable fundamental voltage V1(max). The maximum fundamental voltage is obtained when all the switching angles are zero i.e.



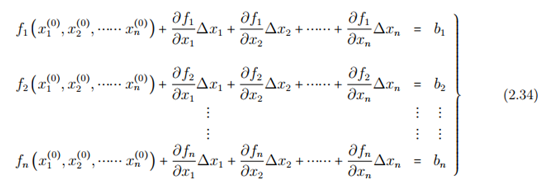
For an 11-level cascade inverter, there are five H-bridges per phase i.e. *s* = 5 or five degrees

of freedom are available.

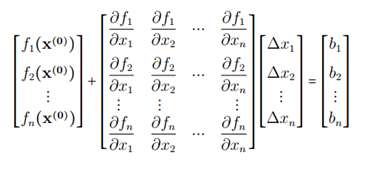
The (4) is a system of five transcendental equations, known as **(SHE) selective harmonic elimination equations,** in terms of five unknowns a1, a2, a3, a4, a5. For the given values of m1 (from 0 to 1), it is required to get complete and all possible solutions of (4) when they exist with minimum computational burden and complexity.All possible solutions for any number of levels can be computed by proper implementation of the **Newton-Raphson method** without knowing any specific initial guess and range of modulation index for which solutions exist.

**2.5 Newton Raphson Method**

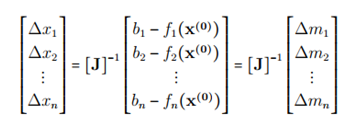
Let there be ‘n’ equations in ‘n’ unknown variables x1, x2, ⋯⋯ xn as given,

To solve equation, first we take an initial guess of the solution . Subsequently, first order Taylor’s series expansion (neglecting the higher order terms) is carried out for these equation around the initial guess of solution

Equation (2.34) can be written as



The matrix containing the partial derivative terms is known as the Jacobin matrix (J). As can be seen, it is a square matrix.



1. **MATLAB SIMULATION**
   1. **Single Phase 3-Level Inverter**

Shown below is the MATLAB model for 3-level inverter.

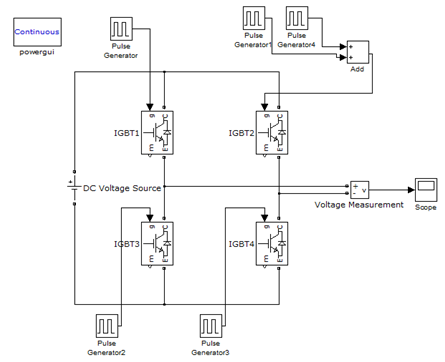
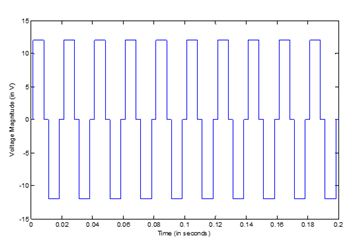


Fig 10: MATLAB model for 3-level inverter

Shown below is the Output Waveform for 3-level inverter.



Graph 1: Plot of Output Voltage v/s Time for 3-Level Inverter

FFT Analysis: The THD comes out to be 48.12% which is quite large. As we increase the number of levels the value of THD decreases.

* 1. **Calculating Firing Angles of 11-Level Inverter**

**3.2.1 Algorithm**

1) Assume any random initial guess for switching angles (say a0 ) such as 0 ≤  α1  <  α2  <   
 …….<  α5  ≤   pi/2

2) Set m= 0.8. (Modulation index chosen for finding switching angles with low THD)

3) Calculate F(α0), B(m1), and Jacobian J(α0).

4) Compute correction Δα during the iteration using relation-  
 Δα=Jacobian (inverse of (α0))\*(B(m1)-F(α0))).

5) Update the switching angles i.e. α(k+1) = α(k)+ Δα(k)

6) Perform α(k+1)=cos⁻¹((abs(cos(α(k+1))))) transformation to bring switching angles in

    feasible range

7) Repeat steps (3) to (6) for sufficient number of iterations to attain error goal of 0.001   
 radians.

**3.2.2 MATLAB Code**

clc

clear

m=0.8; %setting up of modulation index

i=1;

a\_m=[18; 28; 38; 48; 58]; %setting of initial angles

delta(5,1)=0; %delta matrix represent change after every   
 iteration

i\_matrix(:,1)=0;

a1\_matrix(:,1)=0;

a2\_matrix(:,1)=0;

a3\_matrix(:,1)=0;

a4\_matrix(:,1)=0;

a5\_matrix(:,1)=0;

while true

jacob=[-sind(a\_m(1,1)) -sind(a\_m(2,1)) -sind(a\_m(3,1)) -sind(a\_m(4,1))   
 -sind(a\_m(5,1));...

-5\*sind(5\*a\_m(1,1)) -5\*sind(5\*a\_m(2,1)) -5\*sind(5\*a\_m(3,1))   
 -5\*sind(5\*a\_m(4,1)) -5\*sind(5\*a\_m(5,1));...

-7\*sind(7\*a\_m(1,1)) -7\*sind(7\*a\_m(2,1)) -7\*sind(7\*a\_m(3,1))   
 -7\*sind(7\*a\_m(4,1)) -7\*sind(7\*a\_m(5,1));...

-11\*sind(11\*a\_m(1,1)) -11\*sind(11\*a\_m(2,1))   
 -11\*sind(11\*a\_m(3,1)) -11\*sind(11\*a\_m(4,1))  
 -11\*sind(11\*a\_m(5,1));...

-13\*sind(13\*a\_m(1,1)) -13\*sind(13\*a\_m(2,1))   
 -13\*sind(13\*a\_m(3,1)) -13\*sind(13\*a\_m(4,1))   
 -13\*sind(13\*a\_m(5,1))];

B\_func=[5\*m; 0; 0; 0; 0];

F\_func=[cosd(a\_m(1,1))+cos(a\_m(2,1))+cosd(a\_m(3,1))+cosd(a\_m(4,1))+cosd(a\_m(5,1));...

cosd(5\*a\_m(1,1))+cosd(5\*a\_m(2,1))+cosd(5\*a\_m(3,1))+cosd(5\*a\_m(4,1))+cosd(5\* a\_m(5,1));...

cosd(7\*a\_m(1,1))+cosd(7\*a\_m(2,1))+cosd(7\*a\_m(3,1))+cosd(7\*a\_m(4,1))+cosd(7\* a\_m(5,1));...

cosd(11\*a\_m(1,1))+cosd(11\*a\_m(2,1))+cosd(11\*a\_m(3,1))+cosd(11\*a\_m(4,1))+cos d(11\*a\_m(5,1));...

cosd(13\*a\_m(1,1))+cosd(13\*a\_m(2,1))+cosd(13\*a\_m(3,1))+cosd(13\*a\_m(4,1))+cos d(13\*a\_m(5,1))];

delta=jacob\(B\_func-F\_func);

a\_m=acosd(abs(cosd(a\_m+delta)));

i\_matrix(i,1)=i;

a1\_matrix(i,1)=a\_m(1,1);

a2\_matrix(i,1)=a\_m(2,1);

a3\_matrix(i,1)=a\_m(3,1);

a4\_matrix(i,1)=a\_m(4,1);

a5\_matrix(i,1)=a\_m(5,1);

if max(abs(delta))<0.057 %less than 0.001 radian

break

end

i=i+1;

end

display(sort(a\_m));

plot(i\_matrix,a1\_matrix,i\_matrix,a2\_matrix,i\_matrix,a3\_matrix,i\_matrix,a4\_matrix,i\_matrix,a5\_matrix)

a=a\_m(1,1); %final angles linked to the model

b=a\_m(2,1);

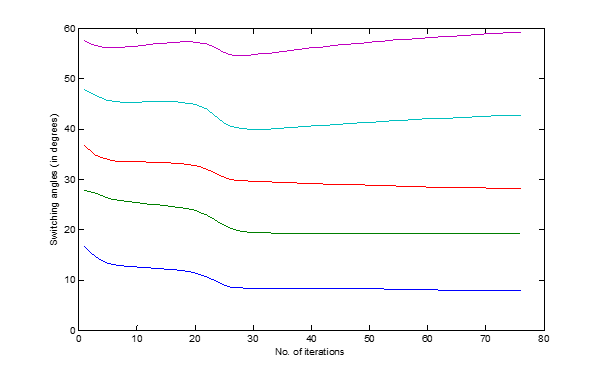
c=a\_m(3,1);

d=a\_m(4,1);

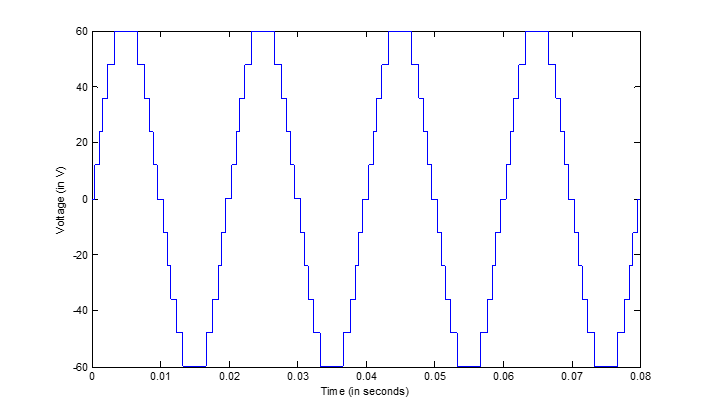
e=a\_m(5,1);

t=0.02; %time period corresponding to the model

**3.2.3 Results**

As a result, the following results were obtained on running the code. The graph shows the variation of switching angles with number of iterations till error goal is reached.  
 

Graph 2: Plot of switching angles v/s number of iterations

α1 = 7.7374  
α2 = 19.19  
α3 = 28.0234  
α4 = 42.7203  
α5 = 59.1368  
  
These Firing Angles calculated are further used in the MATLAB model to provide firing pulses to the IGBT/MOSFET.

Graph 2: Plot of variation of switching angles with number of iterations for 11-Level Inverter

Graph 3: Plot of Output Voltage v/s Time for 11-Level 1-Phase Inverter

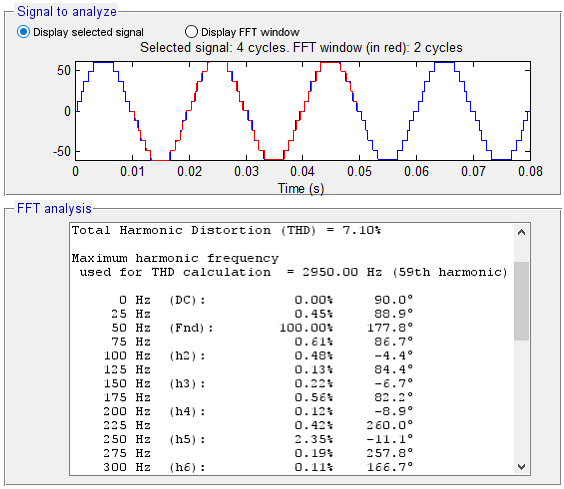
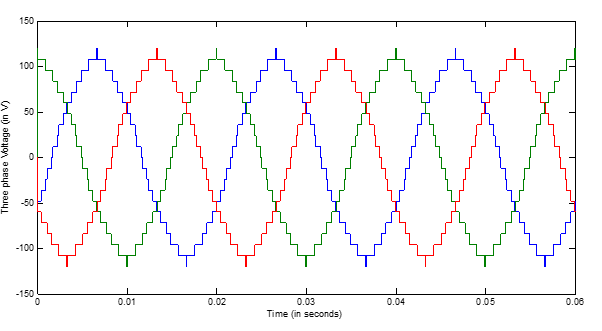


Fig : FFT analysis of the output voltage of 11-level 1-phase Inverter



Graph 4: Plot of Output Voltage (line to line) v/s Time for 11-Level 3-Phase Inverter

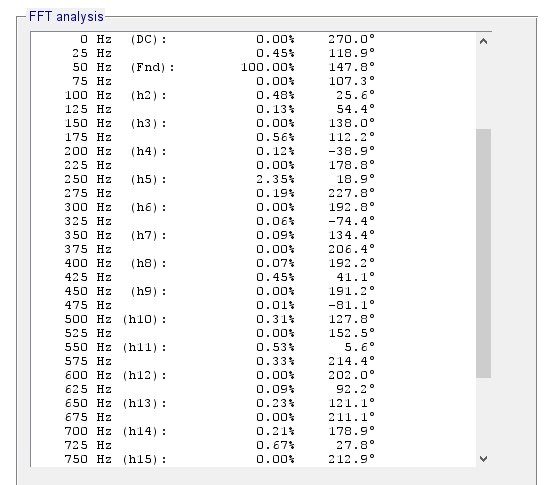


Fig : FFT analysis of the output voltage (line to line) of 11-level 3-phase Inverter

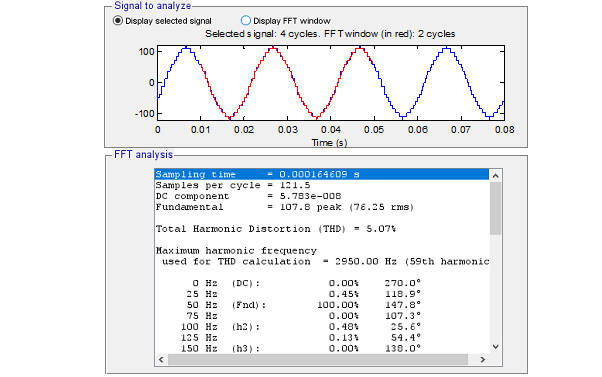
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Fig : Triplen Harmonics removed in 3-phase 11 level inverter voltage output (line to line)

* 1. **Calculating Firing Angles of 7-Level Inverter**

[For hardware implementation]

We have done hardware implementation of 7-level inverter and for that we have calculated the firing angles for the same using MATLAB code.

**3.3.1 MATLAB Code**

clc

clear

m=0.6; %setting up of modulation index

i=1;

a\_m=[10; 30; 60]; %setting of initial angles

delta(3,1)=0; %delta matrix represent change after every iteration

i\_matrix(:,1)=0;

a1\_matrix(:,1)=0;

a2\_matrix(:,1)=0;

a3\_matrix(:,1)=0;

while true

jacob=[-sind(a\_m(1,1)) -sind(a\_m(2,1)) -sind(a\_m(3,1));...

-5\*sind(5\*a\_m(1,1)) -5\*sind(5\*a\_m(2,1)) -5\*sind(5\*a\_m(3,1));...

-7\*sind(7\*a\_m(1,1)) -7\*sind(7\*a\_m(2,1)) -7\*sind(7\*a\_m(3,1))];

B\_func=[3\*m; 0; 0];

F\_func=[cosd(a\_m(1,1))+cos(a\_m(2,1))+cosd(a\_m(3,1));...

cosd(5\*a\_m(1,1))+cosd(5\*a\_m(2,1))+cosd(5\*a\_m(3,1));...

cosd(7\*a\_m(1,1))+cosd(7\*a\_m(2,1))+cosd(7\*a\_m(3,1))];

delta=jacob\(B\_func-F\_func);

a\_m=acosd(abs(cosd(a\_m+delta)));

i\_matrix(i,1)=i;

a1\_matrix(i,1)=a\_m(1,1);

a2\_matrix(i,1)=a\_m(2,1);

a3\_matrix(i,1)=a\_m(3,1);

if max(abs(delta))<0.057 %less than 0.001 radian

break

end

i=i+1;

end

display(sort(a\_m));

plot(i\_matrix,a1\_matrix,i\_matrix,a2\_matrix,i\_matrix,a3\_matrix)

a=a\_m(1,1); %final angles linked to the model

b=a\_m(2,1);

c=a\_m(3,1);

t=0.02; %time period corresponding to the model

**3.3.1 Results**



Graph 2: Plot of variation of switching angles with number of iterations for 7-level inverter

Corresponding angles that were obtained from the code are –

α1 = 10.5770  
α2 = 26.4472  
α3 = 57.7424

These angles were used in the hardware implementation and the corresponding FFT analysis gives the following result.

Fig : FFT analysis of the output voltage of 7-level 1-phase Inverter

1. **HARDWARE CIRCUIT**

**4.1 Turning ON of an N-channel MOSFET**

The conducting channel is lightly doped or even undoped making it non-conductive. This results in the device being normally “OFF” (non-conducting) when the gate bias voltage, VGS is equal to zero. For the n-channel enhancement MOS transistor a drain current will only flow when a gate voltage ( VGS ) is applied to the gate terminal greater than the threshold voltage ( VTH ) level in which conductance takes place making it a transconductance device. The application of a positive (+ve) gate voltage to a n-type MOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing (hence its name) the thickness of the channel allowing more current to flow. This is why this kind of transistor is called an enhancement mode device as the application of a gate voltage enhances the channel. In other words, for an n-channel enhancement mode MOSFET: +VGS turns the transistor “ON”, while a zero or -VGS turns the transistor “OFF”. Then, the enhancement-mode MOSFET is equivalent to a “normally-open” switch.

This is required because when the positive charges will come at gate, the holes in the p substrate will be repealed and a channel of negative ions will form. Now this channel will work as a path for the conduction of the electrons when a voltage is applied between drain and source terminals.



Fig : N-channel MOSFET

**4.2 Turning ON of an P-channel MOSFET**

The reverse is true for the p-channel enhancement MOS transistor. When VGS = 0 the device is “OFF” and the channel is open. The application of a negative (-ve) gate voltage to the p-type MOSFET enhances the channels conductivity turning it “ON”. Then for an p-channel enhancement mode MOSFET: +VGS turns the transistor “OFF”, while -VGS turns the transistor “ON”.

This is required because when the negative charges will come at gate, the holes in the p substrate will be repealed and a channel of positive ions will form. Now this channel will work as a path for the conduction of the electrons when a voltage is applied between drain and source terminals.

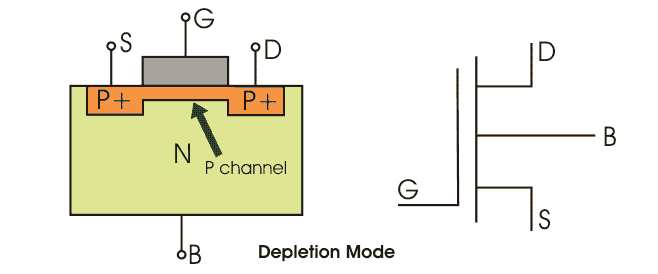


Fig : P-channel MOSFET

**4.3 Symbol of N and P MOSFET**

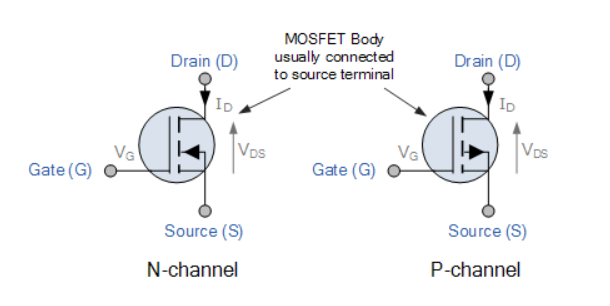


Fig : Symbol of N and P-channel MOSFET

The only difference between the symbol of the N and P channel MOSFET is that of the direction of the arrow on the base terminal. The arrow is point inwards in N channel MOSFET and outside in P channel MOSFET.

**4.4 Switching of MOSFETs**

1. When the MOSFET is to be turned on or off, the gate must be driven high or low with sufficient current so as to charge or discharge the gate capacitance quickly enough so that the MOSFET spends minimal time in the linear region and is quickly turned fully on or off. This is true especially for high speed switching when time period is small. This point is of high importance as if the MOSFET will take time to switch on and off there is a high probability that 2 MOSFET of the same branch will get turn on at same time and short circuit the battery.
2. On Increasing the positive gate voltage, channel resistance decreases further causing an increase in the drain current (Id) through the channel. Due to this instead of giving direct pulses of 5V of arduino we are giving pulses of 12V using optocoupler.

**4.5 MOSFET as Low Side Switch**

In this type of switching,current travels from load through mosfet to ground. Since the source terminal is grounded, this implies that the gate voltage must be 10 to 20V. This voltage level can be easily generated by having the input voltage of order of 10-20V and does not pose any challenge for gate driver circuit.

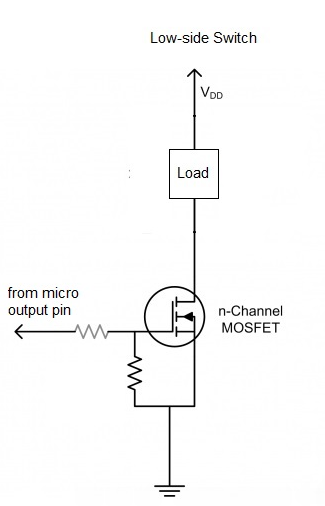


Fig : N-channel MOSFET used as Low Side Switch

**4.6 MOSFET as High Side Switch**

In this type of switching, current travels from supply through MOSFET to load and then to ground .This type of switching is harder using N channel MOSFET as the drop across MOSFET is small as drain and source are approximately at source voltage so we have to keep gate voltage even higher in order to turn on the MOSFET. This high voltage could lead to damage of MOSFET and other hardware components. This high voltage is also difficult to handle.

So now instead of using a N channel MOSFET we will make use of P channel MOSFET as high side switch as this problem can be easily rectified using it because it requires a negative Vgs to turn on as shown below. So, P-Channel MOSFET is preferred as high side switch.



Fig : P-channel MOSFET used as High Side Switch

**4.7 PULL-DOWN and PULL-UP Resistor at MOSFET’s Gate**

MOSFET/ IGBTs are voltage controlled devices, once gate voltage is applied, the MOSFET stays in its conducting state.The gate of a MOSFET behaves like a capacitor due presence of Silicon dioxide as dielectric with charges on both of its faces. When gate voltage is applied, the device turns on and the gate capacitor gets charged. Even when the gate voltage is removed, the charged capacitor keeps the device on. Pull-down resistor is needed to discharge this inherent capacitor as this could lead to false switching of the MOSFET and could also make it the digital pin to float.

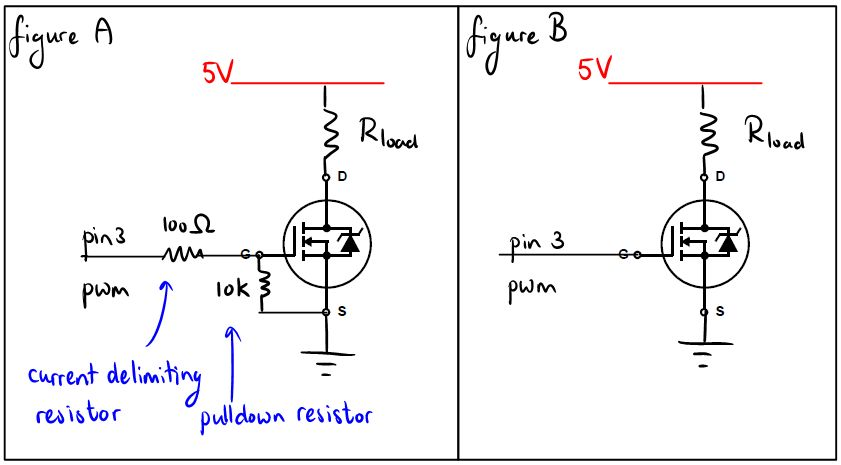


Fig : Pull-down resistor at MOSFET’s Gate

In the figure shown above the 10k resistor is working as pull down resistor. When the MOSFET will turn off the gate capacitance will discharge through the pull down resistor to ground.

**4.8 Circuit Diagram of Single cell H-Bridge**

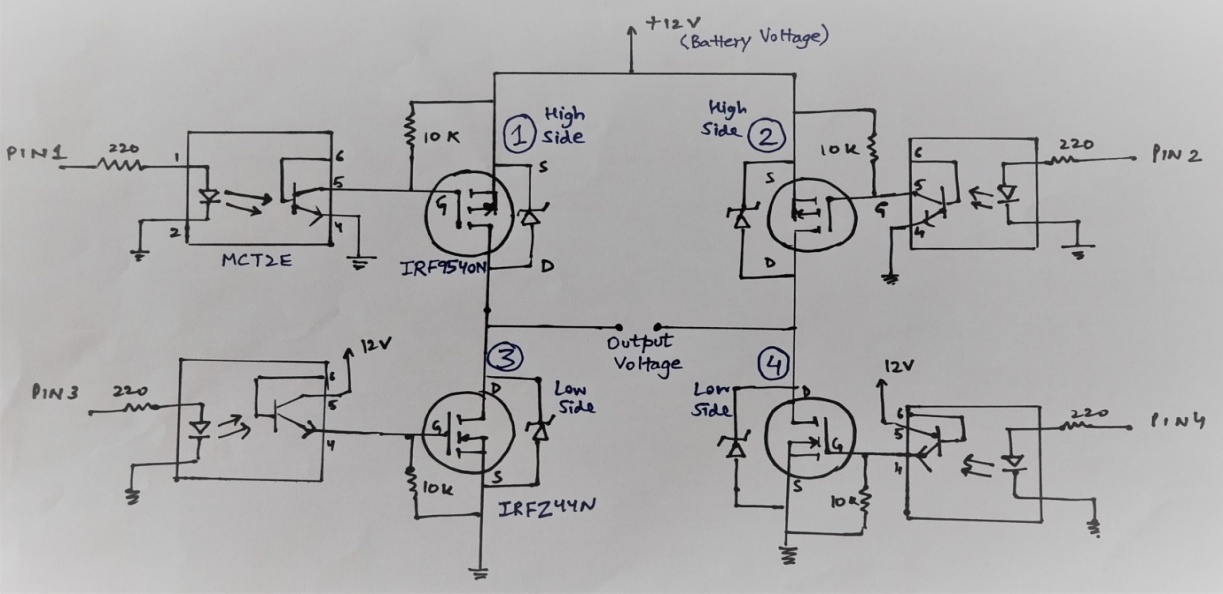
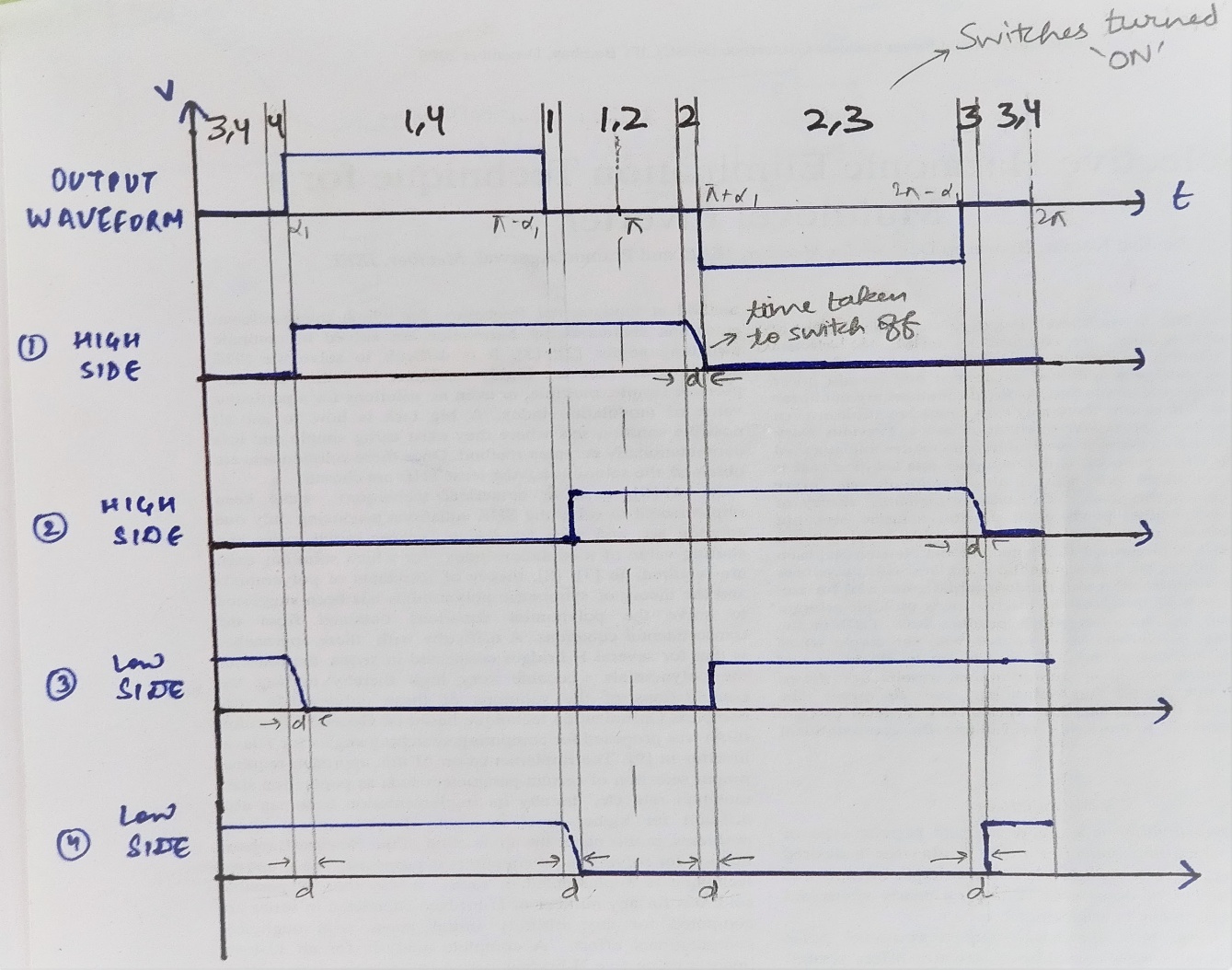
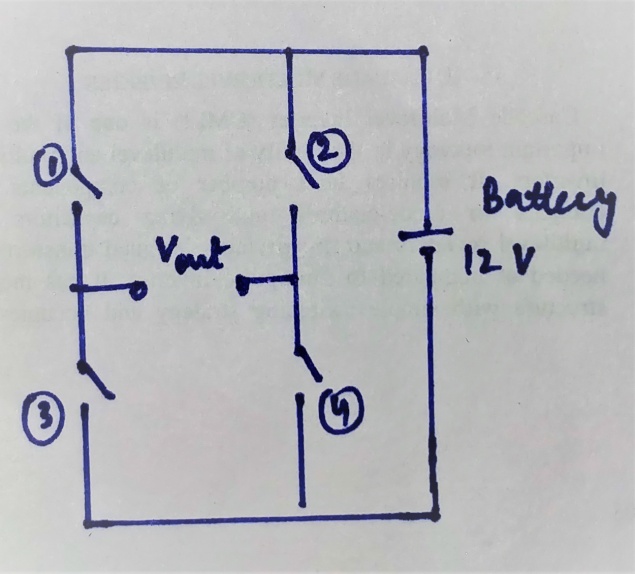
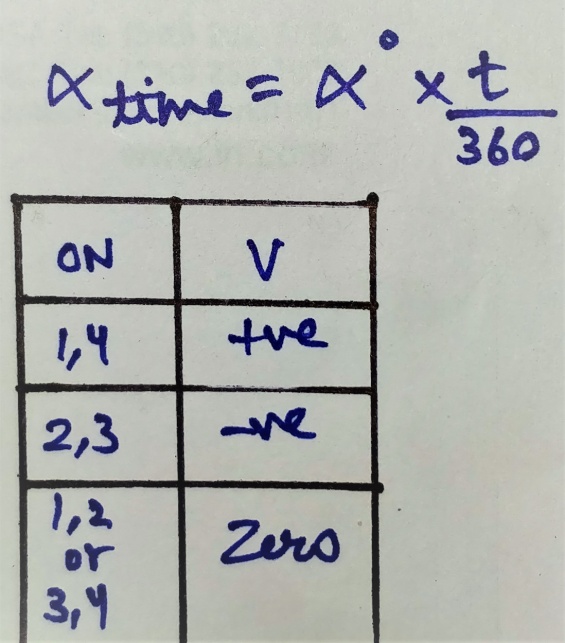


Fig : Circuit Diagram of Single Cell H-bridge

**4.9 Firing Sequence Diagram**

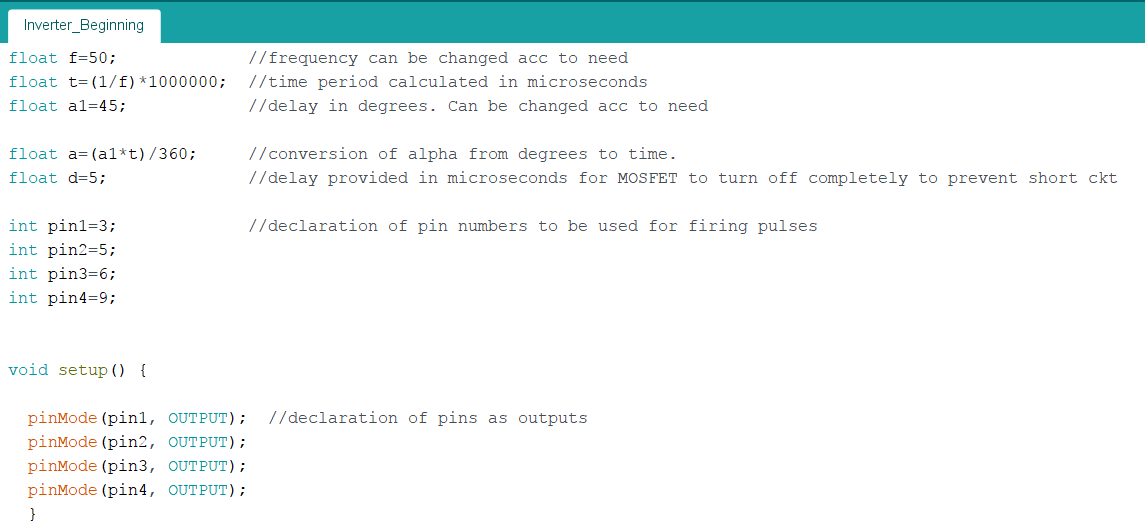


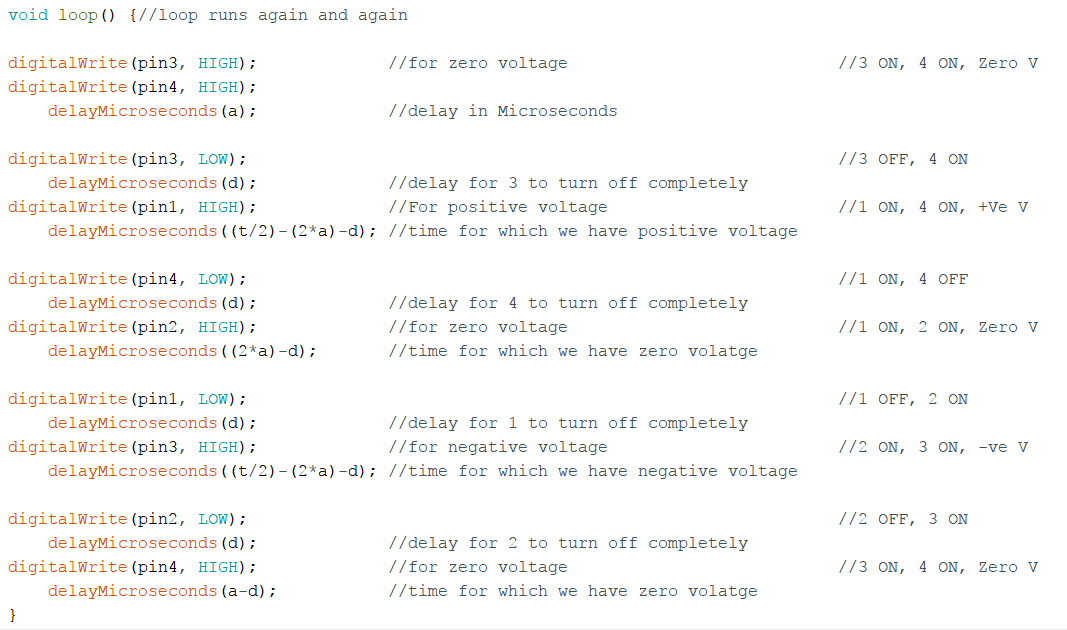


Basic Ckt Diagram Formula for converting Alpha from degrees to time

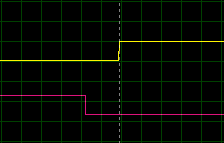
And voltage obtained on switching on different switches

**Arduino Code for 3 level H-bridge Inverter**

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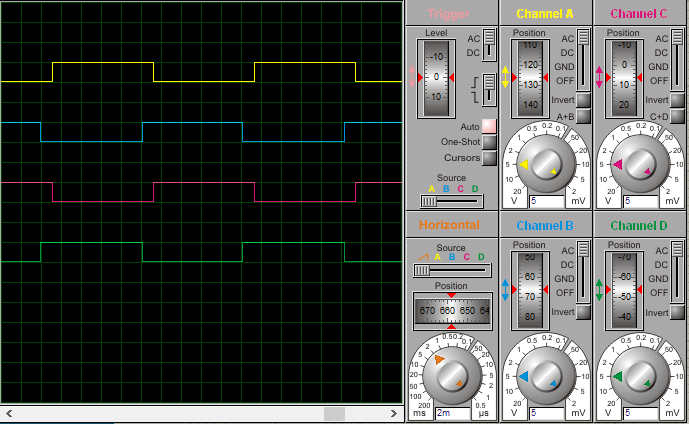
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* Firing Pulses issued by Arduino, have software delay, to prevent Short Circuit of voltage source during switching of MOSFETs.

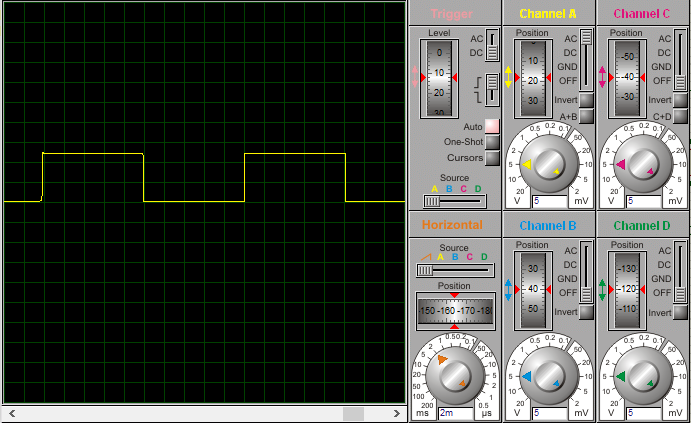


Delay given to turn on MOSFET 1(yellow) to ensure MOSFET 3(magenta) can turn off (Zoomed in)

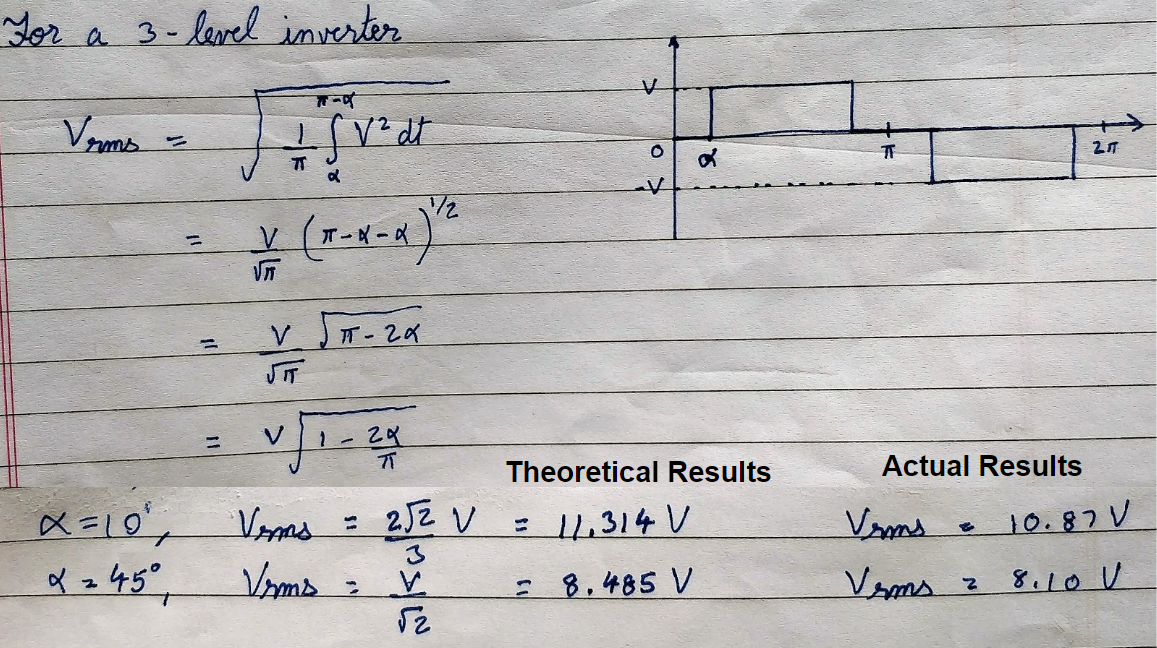
Arduino pulses as seen on Oscilloscope



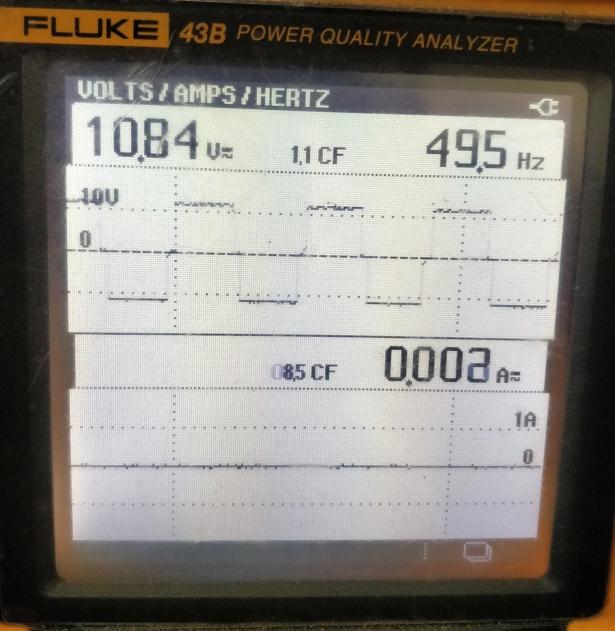
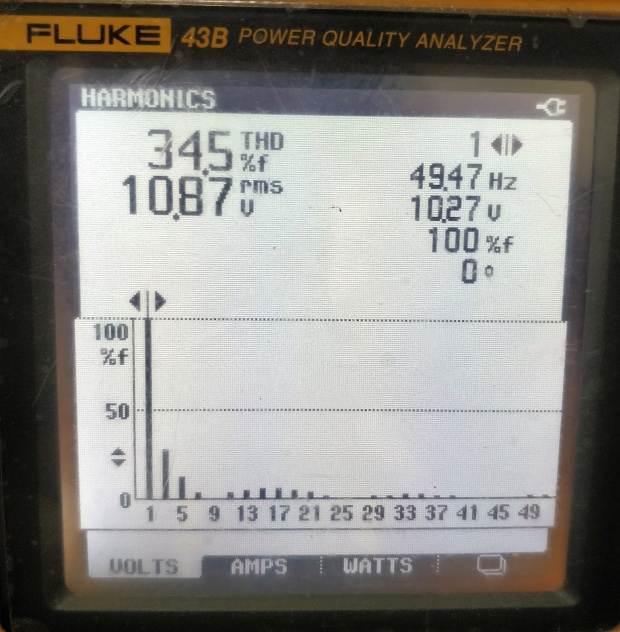
Waveform of Output voltage



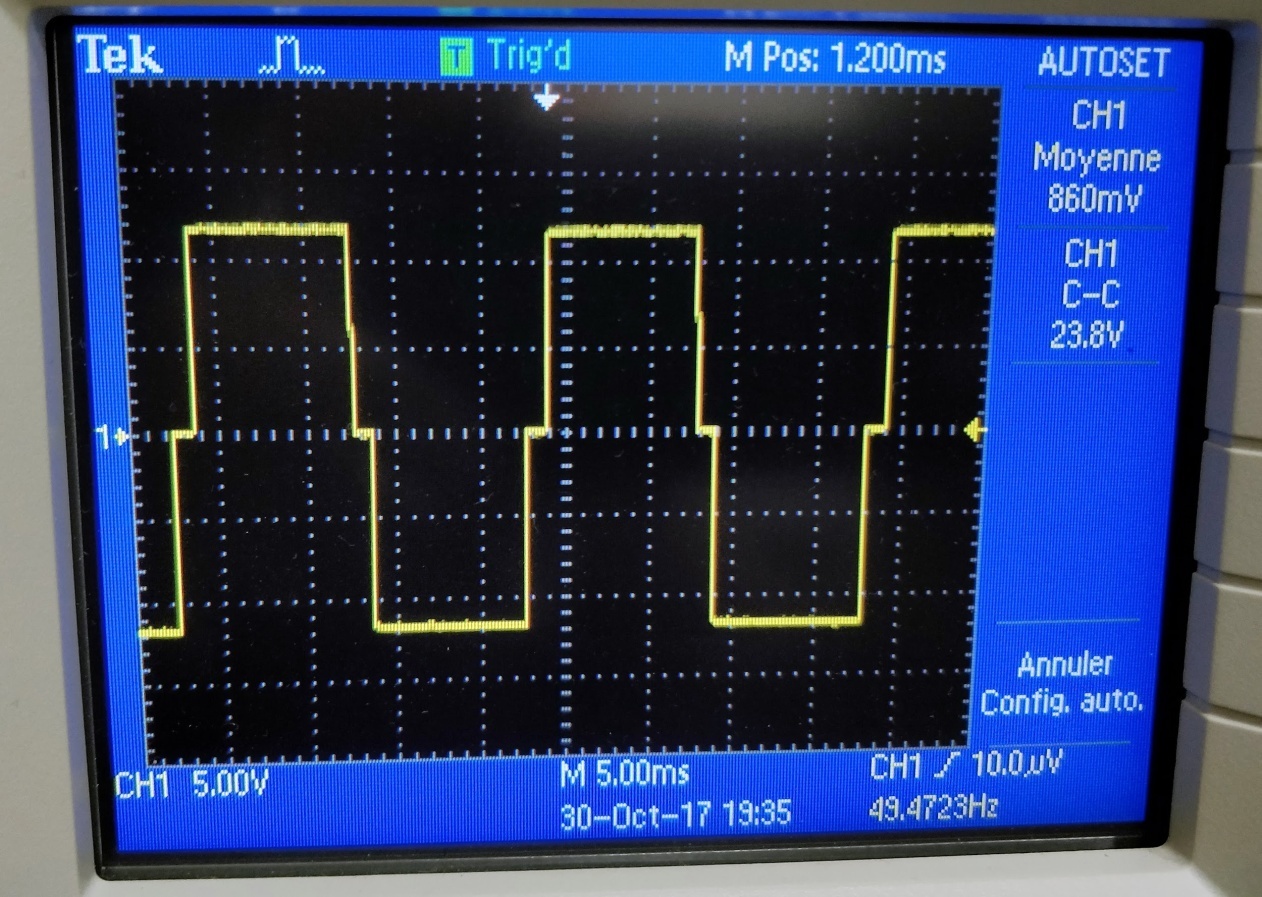
Theory vs Actual results



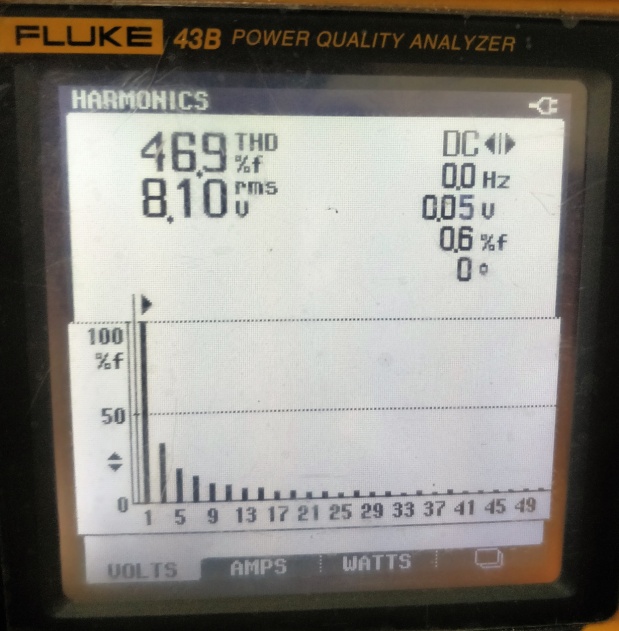
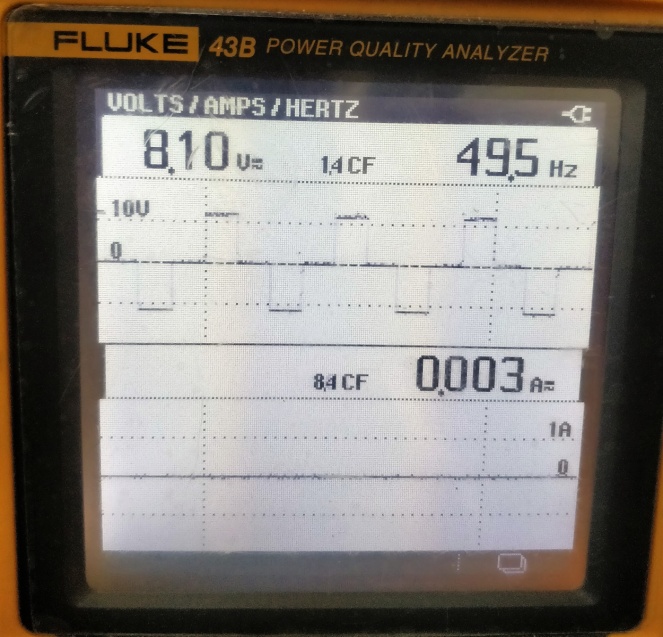
At Alpha = 10 degrees (THD=34.5%, Vrms=10.87V, f=49.5Hz)



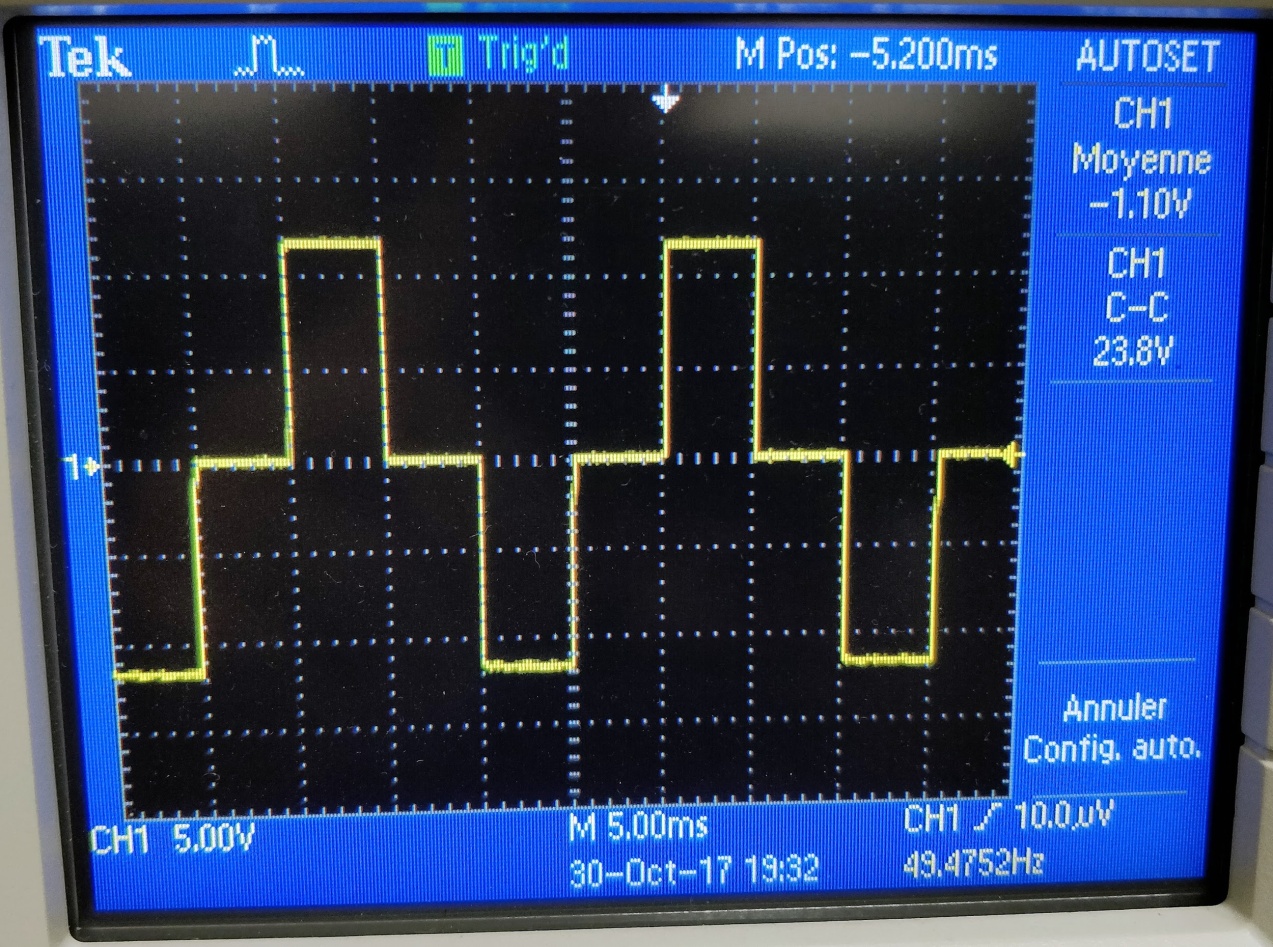
Waveform at Alpha = 10 degrees



At Alpha=45 degrees (THD=46.9%, Vrms=8.1V, f=49.5Hz)



Waveform at Alpha = 45 degrees



* References:-
* Selective Harmonic Elimination Technique for a Multilevel Inverter byJagdish Kumar, Biswarup Das, Senior Member, IEEE, and Pramod Agarwal, Member, IEEE.
* Voltage Regulation of Power Systems using Cascaded Multilevel STATCOM by Jagdish Kumar, Biswarup Das, Senior Member, IEEE, and Pramod Agarwal, Member, IEEE.
* Control of Harmonics using 15-Level Cascade Multilevel Inverter by Jagdish Kumar, Biswarup Das, Senior Member, IEEE, and Pramod Agarwal, Member, IEEE.
* https://www.youtube.com/watch?v=408qlS2z6ys
* Links for the datasheet of the components:-

1. <https://goo.gl/o3Jgb3> (N Channel MOSFET)
2. <https://goo.gl/wA66eK> (P Channel MOSFET)
3. <https://goo.gl/st3rGw> (Optocoupler)