Voltage Regulation of Power Systems using Cascaded Multilevel STATCOM

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***Abstract*—A simple control strategy is proposed to regulate load bus voltage of power systems using static synchronous compensator (STATCOM) based on a cascade multilevel inverter. Indirect control scheme is employed for voltage regulation using a single controller which can regulate the load bus voltage irrespective of causes of voltage disturbances. The proposed control strategy is implemented at high modulation index with constant switching angles. A new technique based on optimization is proposed to compute the switching angles; these computed switching angles are used for generating the output voltage of STATCOM which has minimum harmonic distortion in injected voltage to the power systems. A rotating switching scheme is used to keep the capacitor voltages balance. Digital simulation of 11-level cascade multilevel inverter based STATCOM operating under different operating points is presented using MATLAB Simulink power system block sets.**

***Index Terms*—Cascade multilevel inverter, static synchronous compensator, indirect control scheme, sequential quadratic programming.**

I. Introduction

VOLTAGE control in an electric power system is important for proper operation of electric power equipment to prevent damage such as overheating of generators and motors, to reduce transmission losses and to maintain the ability of the system to withstand disturbances and prevent voltage collapse. One of the major causes for voltage disturbances in power systems is reactive power drawn/supplied by various components of power systems, such as inductors, condensers, non-linear loads, power electronic converters etc. With the use of sophisticated loads based on power electronic converters such as battery charger, computers, televisions etc. has put two fold problems on power systems: one is that these loads create more problems to power quality issues (voltage fluctuations, harmonic distortions etc) and second, they also require good quality of electric power. In order to maintain proper level of voltage at load buses reactive power compensation is must [1], [2].

Since right from the beginning of electric power generation, some types of reactive power compensating devices such as fixed capacitors, inductors, synchronous condensers were in use. With the advent of power electronics based switches such as power diodes, thyristors etc has developed a new generation in the field of reactive power compensating devices; and these devices were named as flexible alternating current transmission systems (FACTS) devices. Some of the important of them are thyristors-switched capacitor (TSC) and thyristor controlled reactor (TCR) [2]-[4]. One or more problems associated with above mentioned reactive power compensating devices are: less accuracy of compensation, slow response, less flexibility, more cost, operating dependency on system voltage etc.

In the last decade, commercial availability of power electronics based switches with high power handling capacity such as GTO thyristors, IGBTs etc have led to the development of power electronic converters. A second generation FACTS device, using key component as voltage source inverter (VSI), has made significant impact in the field of reactive power compensation, and is known as static synchronous compensator (STATCOM). The STATCOM almost overcomes all the issues related with reactive power compensation and voltage regulation. One of the important merits of the STATCOM is that it has the capability to operate under very low voltage i.e. when the need of voltage regulating devices is more (while the most of other voltage compensating devices fail to do so) [4].

II. Static Synchronous Compensator

A. Basics

The basic STATCOM model consists of a voltage source inverter, DC side capacitors (C) with voltage V_{dc} on each capacitor, and a coupling reactor (L_C) or a transformer. The AC voltage difference across the coupling reactor produces reactive power exchange between the STATCOM and the power systems at the point of common coupling (PCC). If the output voltage of the STATCOM (V_C) is more than the system voltage (V_L) then reactive powers is supplied to the power system and reverse happen if V_C is less than that of V_L. The output voltage of the STATCOM can be controlled in two ways: i) by changing the switching angles while maintaining the DC capacitor voltage at a constant level (inverter type I control); ii) in type II control scheme, switching angles are kept constant while DC voltage of capacitor is varied according to requirement of reactive power generation or absorption [5]-[6], and this is simply achieved by varying the phase angle of V_C with respect to V_L. If V_C lags V_L, there is more transfer of active power from power systems to STATCOM side, resulting in more charge

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on capacitor, as V_C is proportional to capacitor DC voltage hence V_C increases. Advantage of type II control over type I is that, the switching angles can be selected in such a way that harmonic distortions in V_C can be kept at minimum level, thereby injecting nearly sinusoidal voltage to the power system [5]; but its response time is slower than that of the type I inverter control. The basic operating configuration of the STATCOM is shown in Fig. 1.

From view point of topology used for voltage source inverter, the STATCOM can be classified into two categories: i) multipulse type and ii) multilevel type. In multipulse inverter topology, six-pulse inverter units are connected through a specially designed zigzag transformer to achieve high pulse inverter (i.e. 12, 24, 48-pulse) for better waveform (less harmonic distortion) and high power applications. One major problem with multipulse type STATCOM topology is that the necessity of zigzag transformer which occupies more space and makes the configuration more complex [7]-[8]. The other topology is multilevel inverters; and these are further classified into three subcategories: diode-clamped type, flying capacitors type, and cascade or isolated series H-bridges type. The different multilevel inverter topologies have their own merits and demerits depending on the number of components requirement, applications, configuration, cost, space requirement, modularity etc. From most points of view, cascade multilevel inverter (CMLI) is considered most suitable topology for STATCOM as used for power systems voltage regulation application [8]-[12].

B. Cascade Multilevel Inverter

The CMLI consists of a number of H-bridge inverter units with separate DC source for each unit and is connected in cascade or series as shown in Fig. 2. Each H-bridge can produce three different voltage levels: $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to AC output side by different combinations of the four switches S_1, S_2, S_3, and S_4. The ac output of each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all of the individual H-bridge outputs [9]-[12].

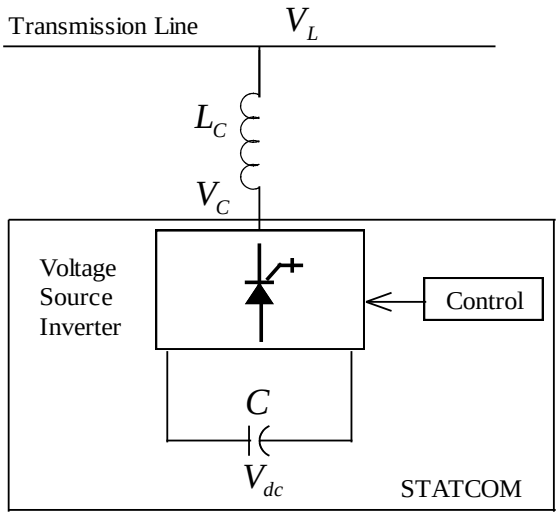


Fig. 1. STATCOM configuration.

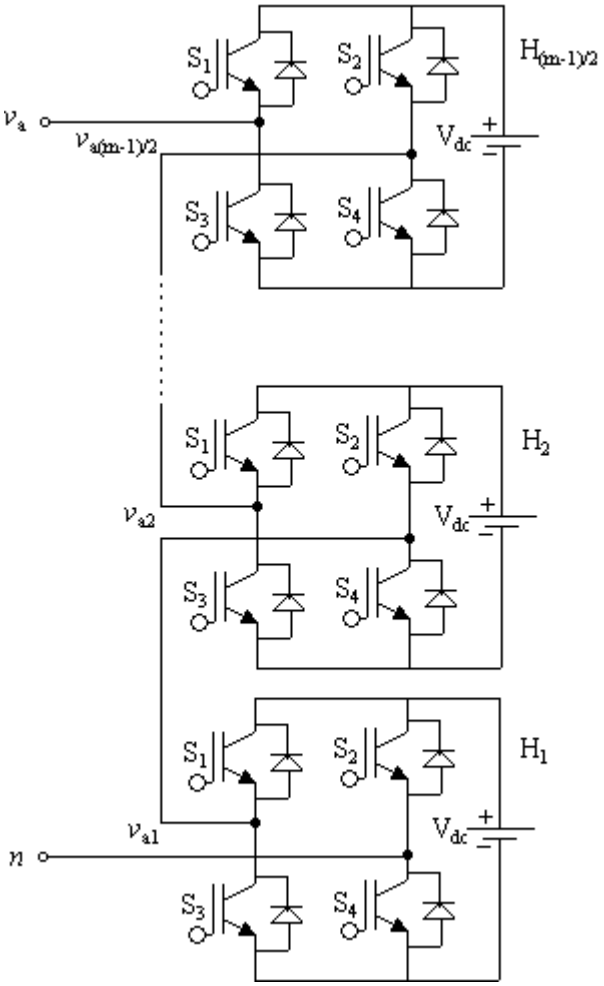


Fig. 2. Configuration of single-phase cascade multilevel inverter.

By connecting the sufficient number of H-bridges in cascade and using proper modulation scheme, a nearly sinusoidal output voltage waveform can be synthesized. The number of levels in the output phase voltage is $2s+1$, where s is the number of H-bridges used per phase. Fig. 3 shows an 11-level output phase voltage waveform using five H-bridges, where angles α_1, α_2, α_3, α_4, and α_5 are switching angles of H-bridges H_1, H_2, H_3, H_4, and H_5 respectively. The magnitude of the ac output phase voltage is given by $v_{an} = v_{a1}+v_{a2}+v_{a3}+v_{a4}+v_{a5}$ [10].

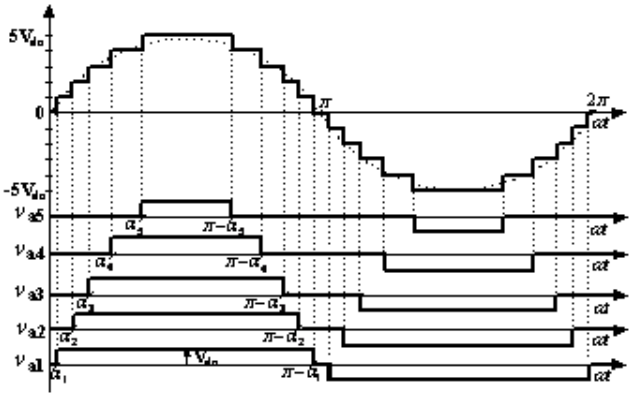


Fig. 3. Output voltage waveform of an eleven-level CMLI at fundamental frequency switching scheme.

C. Switching Angles Selection

To synthesize multilevel AC output voltage using different levels of DC inputs, the semiconductor devices must be switched on and off in such a way that desired fundamental voltage obtained is nearly sinusoidal i.e. having minimum harmonic distortions. Different switching techniques are available for computing switching angles for the semiconductor devices [13]. For power systems applications, generally fundamental frequency switching scheme is considered more suitable; in this scheme the devices are switched on and off once in every cycle, thereby producing less switching losses (more efficiency) [10]-[13]. Generally, the switching angles at fundamental frequency are computed by solving a set of nonlinear equations known as selective harmonic elimination (SHE) equations [12]-[16]. In SHE technique, in general, lower order harmonics are eliminated at the cost of generation of higher order harmonics, thereby increasing the total harmonic distortion (THD) in V_C. In the present work, an optimization technique is proposed to compute the switching angles which minimize THD due to all the harmonic components up to 49th order. By applying proposed technique for switching angles computation, significant amount of THD reduction in V_C can be achieved as compared with SHE technique.

In general, the magnitude of voltages produced by 11-level CMLI is given by following relation [12]:

$$V_n = \sum_{n=1,3,5}^{\infty} \frac{4V_{dc}}{n\pi} (\cos(n\alpha_1) + \ldots + \cos(n\alpha_5)) \quad (1)$$

The magnitude of fundamental voltage produced is given by (1) as follows:

$$V_1 = \frac{4V_{dc}}{\pi} (\cos(\alpha_1) + \ldots + \cos(\alpha_5)) \quad (2)$$

Where n is the order of harmonic components and $\alpha_1 \ldots \alpha_5$ are switching angles for five H-bridges such that $0 \le \alpha_1 < \alpha_2 < \ldots < \alpha_5 \le \pi/2$. In three-phase power system, triplen harmonic components are absent in line to line voltages, therefore, only non-triplen odd harmonic components of V_C are considered for THD optimization.

The objective function is formulated as follows:

$$\Phi(\alpha_1, \alpha_2, \alpha_3, \alpha_4, \alpha_5) = \sqrt{V_5^{\,2} + V_7^{\,2} + \ldots + V_{49}^{\,2}} \quad (3)$$

The objective function (3) is minimized with equality constraints given by (2) and $0 \le \alpha_1 < \alpha_2 < \ldots < \alpha_5 \le \pi/2$. It is to be noted that, the sequential quadratic programming (SQP) method [17] has been used and been implemented by using MATLAB optimization toolbox [18].

The THD produced by switching angles computed with above method for different values of modulation index (*m*) is computed, and the switching angles corresponding to minimum THD are selected. The *m* is defined as the ratio of fundamental output voltage to maximum obtainable voltage (maximum voltage is obtained when all α's are zero).

The THD computed is least at *m* = 0.9240 and it is 2.28%. If SHE technique were used to calculate the switching angles, in that case, value of THD would have been 5.20% i.e. net decrease in value of THD is about 3% in the proposed method as compared to existing techniques. The switching angles (in radians) at *m* = 0.9240 are selected for operation of CMLI, and is given in Table I.

TABLE I

m	α_1	α_2	α_3	α_4	α_5
0.924	0.056	0.169	0.281	0.474	0.668

D. Rotating Switching Scheme

One major issue associated with multilevel inverter is the problem of charge balance of capacitors used in different H-bridges for each phase leg. The main causes of this problem are that, there is continuous power loss in switches and capacitors, and conduction duration of each H-bridge is different due to switching of semiconductor devices at different instants. It can be seen from the Table I that, H_1-bridge conducts form α_1 to π-α_1 for positive cycle while H_5-bridge conducts from α_5 to π-α_5 for the same cycle, this creates charge unbalance on capacitors associated with individual H-bridges. A scheme suggested in [12] is implemented for capacitor charge balancing. In this scheme, switching angles are rotated among different H-bridges of each phase leg after every half cycle i.e. during first positive cycle, switching angle for H_1 is α_1, in negative cycle, switching angle for H_1 is α_2, during next positive cycle, switching angle for H_1 is α_3 and so on. The same pattern is followed for other H-bridges also. Fig. 4 shows the scheme implemented as discussed above.

III. PROPOSED CONTROL SCHEME

There are two control schemes for voltage regulation or reactive power compensation using STATCOM and these are: i) direct control, and ii) indirect control [5], [13], [19]. In direct control scheme, reactive current reference is derived by a PI controller according to the difference between reference voltage and actual voltage of power systems; this reference current is compared with actual reactive current, the error between these two reactive currents is processed by another PI controller which varies *m*, accordingly, reactive power is injected to or drawn from the power systems. In case of indirect voltage control scheme, control signal is derived in a similar way as above using two PI controllers, but in this case, instead of varying *m*, capacitor voltages are varied and accordingly the reactive power is compensated.

On contrary to using two PI controllers, in proposed scheme, a single PI controller is employed for voltage regulation purpose. The error between reference voltage and actual system voltage is processed by a single PI controller. The output of the PI controller is used to vary the capacitor voltages by phase shifting V_C with respect to V_L by an angle (theta). Due to phase shift between V_C and V_L, magnitude of capacitor voltages are varied, and accordingly variation in reactive power is achieved. The proposed control scheme, as simulated in MATLAB Simulink [18], is shown in Fig. 5.

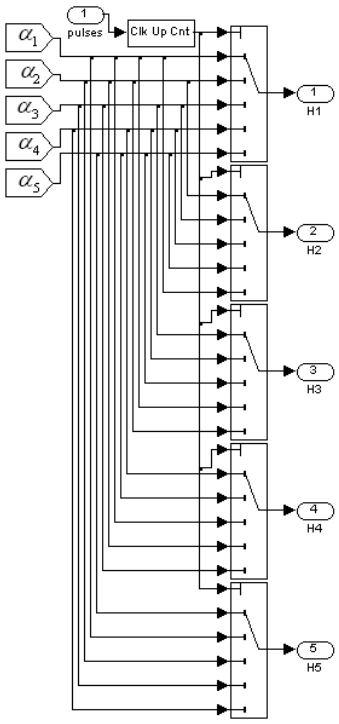


Fig. 4. Rotating switching scheme.

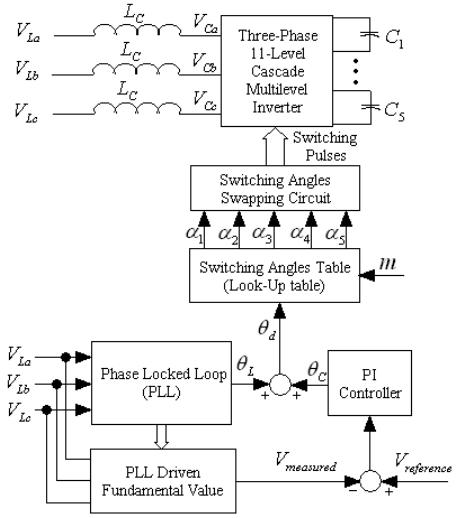


Fig. 5. Proposed control scheme.

IV. DIGITAL SIMULATION

To demonstrate the effectiveness of proposed controller, the simulation is carried out by using the MATLAB/Simulink and power system block set [18] under different loading and source voltage variations for the configuration shown in Fig. 6. The digital simulation results are given as shown in Fig. 7. The various parameters selected for simulation are shown in Table II.

TABLE II

System voltage	240V	DC capacitor	2000μf
Base voltage	240V	T/L R(pu)	0.05
Base power	1000VA	T/L X(pu)	0.10
Operating frequency	50Hz	Coupling reactor (pu)	0.15

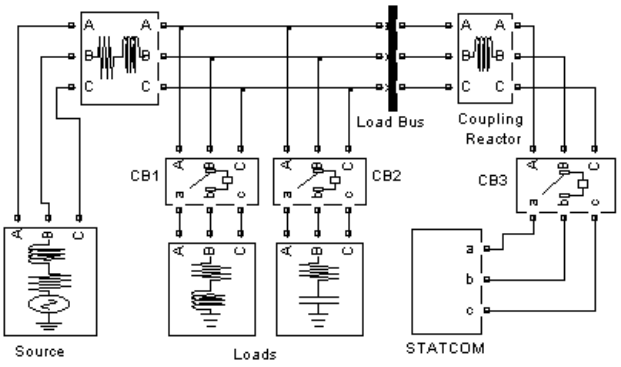


Fig. 6. Configuration for study of the STATCOM operation.

The following sequences are tested:

Step 1) the STATCOM is switched and connected to the power system at t = 0.2s by switching on the circuit breaker CB3. Before connecting the STATCOM to the power systems, DC capacitors are charged using a pre charging circuit.

Step 2) an inductive load (P = 0.15 (pu), Q = 0.50 (pu)) is connected at load bus by switching on the circuit breaker CB1 from t = 0.5s to t = 3s.

Step 3) a capacitive load (P = 0.10 (pu), Q = 0.50 (pu)) is connected at load bus by switching on the circuit breaker CB2 from t = 2s to t = 4. Corresponding load bus voltage variations for above load and d-q current components of STATCOM are shown in Figs. 7(a) and 7(b) respectively.

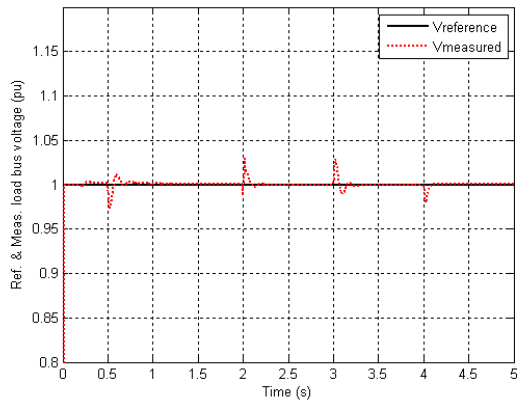
Step 4) a 5% voltage drop in source voltage is produced, by using a programmable voltage source, from t = 1s to t = 2s. In this case no load is connected to the load bus, results for load bus voltage variation and d-q current components are shown in Figs. 7(g) and 7(h)).

By observing the results shown in Fig. 7, whenever there is a drop in load bus voltage, the STACOM generates reactive power by injecting reactive current (I_q) into the power systems, thereby restoring the load bus voltage to its nominal value. Internally, this operation is accomplished by more charging of DC capacitors by phase shifting (lagging) of V_C with respect to V_L. In case of rise in load bus voltage due to capacitive load, the STATCOM again regulates the load bus voltage to its reference value by absorbing the reactive power from the power systems.

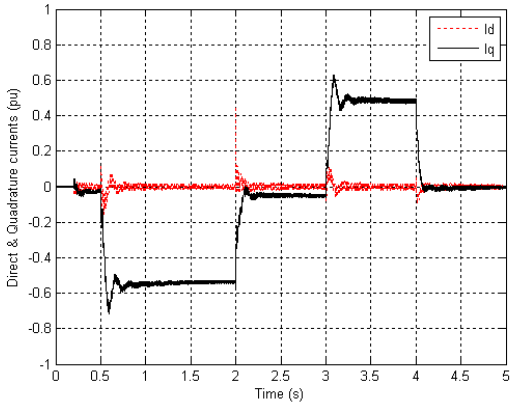
From Figs. 7(a) and 7(g), it is clear that the STATCOM responds very quickly in regulating the load bus voltage irrespective of causes for load bus voltage variations. The corresponding d-q current components are shown in Figs. 7(b) and 7(h).

Three-phase load bus and STATCOM voltages are shown in Figs. 7(c) and 7(d) at and around t=2s where a capacitive load is connect to the bus. These figures show that control is achieved in 1-2 cycles (this period is sufficient for power systems applications).

The sum of total capacitor voltages, and voltage across top and bottom capacitors (i.e. V_{c1} and V_{c5}) are shown in Figs. 7(e) and 7(f) to show the charge balance on DC capacitors. It is evident from the figures that charges on the capacitors are well balanced and transition from one level to another level is quick.



(a)



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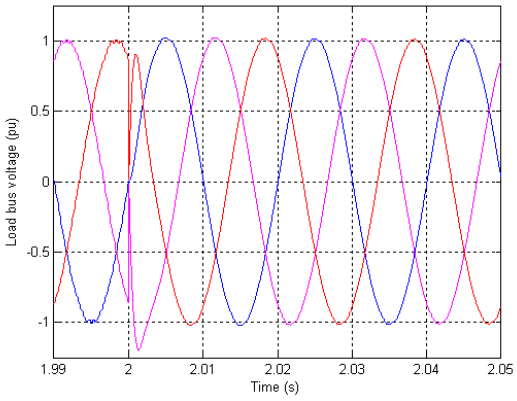
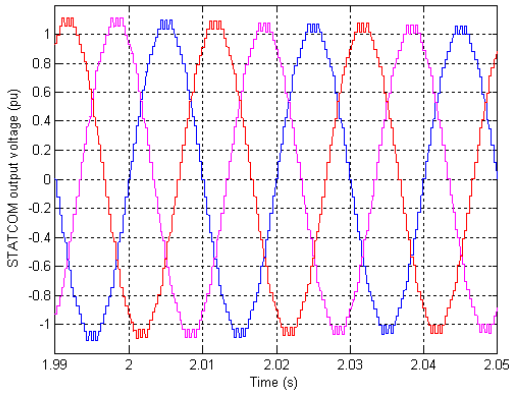
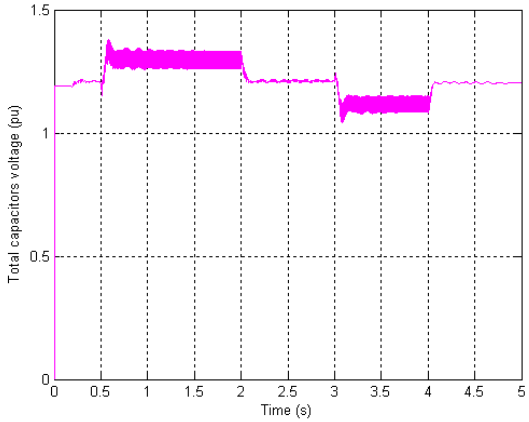


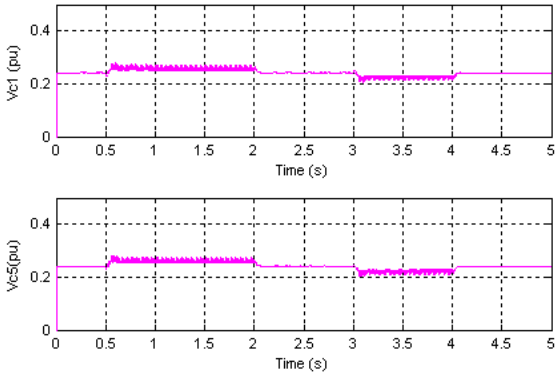
(c)



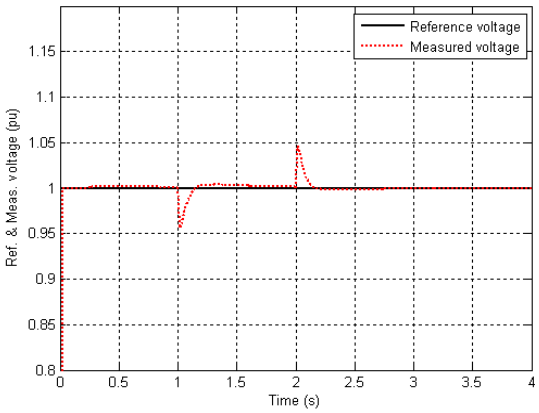
(d)



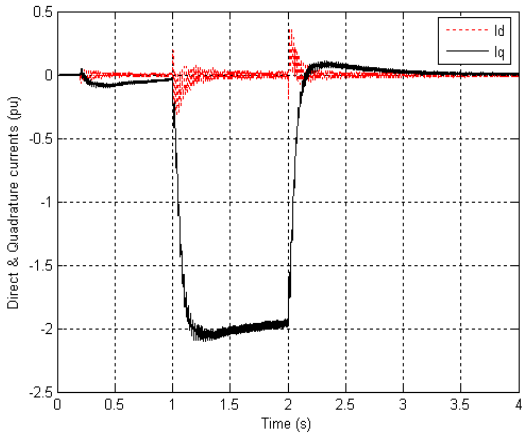
(e)



(f)



(g)



(h)

Fig. 7. Digital simulation results of STATCOM operation: (a)-(f) when inductive load of P = 0.15 (pu), Q = 0.50 (pu) from t = 0.50s to 3s, and capacitive load P = 0.10(pu), Q = 0.50(pu) from t = 2s to 4s is applied at load bus; and (g)-(h) -5% voltage change is applied to source voltage from t = 1s to 2s.

V. CONCLUSION

A simple control scheme has been implemented for a type II cascade multilevel inverter for power systems voltage regulation problems. The proposed scheme is very effective in mitigation of voltage fluctuations caused by generation side as well as load side disturbances. Through series of digital simulations, it has been shown that the response time for voltage restoration is very small; moreover, it has also been shown that there is almost perfect balancing of charge on DC capacitors.

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