NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA
MID - TERM EXAMINATION, 2015
SESSION: 2015 – 2016 (Spring)
MTech 2nd Semester

Subject code: CS 641 **Subject Name: Advanced Computer Architecture** Dept. Code: **CS**
No. of pages: 02 Full Marks: 30 Duration: 2 ***Hours***

Answer ALL questions. Eack question carries equal marks.

1. A computer implemented in single-cycle implementation. When stages are split by functionality, stages do not require exactly the same amount of time. The original machine had a clock cycle of 7 ns. After the stages were split, the measured times were IF, 1 ns; ID, 1.5 ns; EX, 1 ns; MEM, 2 ns; and WB, 1.5 ns. The pipeline register delay is 0.1 ns. What is the clock cycle time of the 5-stage pipelined machine? What is the speedup of the pipelined machine over the single cycle machine, if there is a stall for every 4 instruction?

2. Show the timing of execution of the following code fragment in a 5-stage pipeline with full forwarding and bypassing hardware. Assume that the branch is handeled by predicting it as not taken. If all memory references take 1 cycle, how many cycles does this loop take to execute? Assume the initial value of R3 is R2 + 396.

```
Loop:  LD     R1, 0(R2)
       DAADI  R1, R1, #1
       SD     R1, 0, (R2)
       DADDI  R2, R2, #4
       DSUB   R4, R3, R2
       BNEZ   R4, Loop
```

3. Suppose the branch frequencies (as percentages of all instructions) are as follows: Conditional branches : 15%, Jumps and Calls : 1%, and Taken conditional branches: 60% are taken. Assume a high-performance processor in which we have a 15-deep pipeline where branch is resolved at the end of the fifth cycle for unconditional branches and at the end of the tenth cycle for conditional branches. Assuming that only the first pipe stage can always be done independent of whether the branch goes and ignoring other pipeline stalls, how much faster would the machine be without any branch hazard ?

4. Assume a five-stage pipeline microarchitecture and the code given below. All operations are one cycle except LW and SW, which are 3 cycles, and branches, which are 2 cycles. There is no forwarding. Show the phases of each instruction per clock cycle for one iteration of the loop. How many clock cycles per loop iteration are lost to branch overhead?

```
Loop:  LW     R3, 0(R0)
       LW     R1, 0(R3)
       SUB    R4, R3, R2
       DSUB   R4, R3, R2
       SW     R1,0(R3)
       BNEZ   R4, Loop
```

5. For the loop given below, list the dependences and then rewrite the loop so that it is parallel

```
for (i =1; i<100; i=i+1)
{
        A[i] = B[i] + C[i];          /* S1*/
        B[i] = A[i] + D[i];          /*S2*/
        A[i+1] = A[i] + E[i];        /*S3*/
}
```

6. Three enhancements with the following speedups are proposed for a new architecture: $Speedup_1 = 30$, $Speedup_2 = 20$, and $Speedup_3 = 15$. Only one enhancement is usuable at a time. If enhancement 1 and 2 are each usuable for 25% of time, what fraction of the time must enhancement 3 be used to achieve an overall speedup of 10 ?