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A Comparative Study of 1-Bit Full Adder Cell for Low-Power Applications

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Abstract—The 1-bit full adder circuit is one of the most commonly used extensively in many very large-scale integration circuits such as application- specific digital signal processing systems and microprocessors. An adder is used for the overall analysis of the circuits in most of the systems. This paper describes various types of full adders based on different techniques for low power. All the analysis is depends on some different simulation parameters such as transistor count, delay, power-delay product, power consumption, and the value of power supply. Each full adder used different tool for the simulation purpose. The various type of full adder circuit design are studied and evaluated. This survey paper discussed various technologies for low power. This paper is very useful for the circuit designers to find the full adder as per the requirement of their applications.

Index Terms— Full-adder, MUX, XOR, XNOR, Low-power, PDP, GDI technique, delay, VLSI Circuit.

I. INTRODUCTION

Great attention has been focused on low-power and high-speed circuits due to the rapid change in the development of laptops, portable personal communication systems and cellular networks. Low-power consumption has become a major consideration in the designing of the circuits (Navi et al., 2009; Wang et al., 2009).

Technology trends show that circuit delay is scaling down by 30% performance and transistor density are doubled approximately every two years, and the transistor's threshold voltage is reduced by almost 15% every generation. All of these technology trends lead to higher and higher power consumption in circuits. Higher power consumption raises chip's temperature and directly affects battery life. A higher temperature directly affects circuit operation and reliability; complicated cooling and packing techniques are required. In addition higher current density either shortens battery packs [1].

Designing a circuit of low power has been in challenge from a long time and now it is one of the most useful goals of today's CMOS design. Adders are the core unit of complex arithmetic circuits as they are mostly used in arithmetic logic units (ALU), for adder generation in the case of cache or memory access (Lee et al., 2007; Xia et al., 2009), in the floating-points units, in compressors and in the parity checkers. The 1-bit adder cell is the most important and basic block of all the modules in additions to its main task, which is adding two or more binary numbers. It most of these systems the adder is part of the critical path that determines the overall performance of the system. Obviously, improving its performance directly leads to improving the performance of the whole module.

There are various issues related to the full adders. Some of them are power consumption, area, performance, regularity, noise immunity and best driving ability [2]. Several works have been done in order to decrease number of transistor and consequently decrease power consumption and area [2-5].

In microelectronic circuits, two types of full adder styles are used such as static and dynamic style. Static full adders are simpler reliable and less power than dynamic ones. However, dynamic full adders are faster and some times more compact than static full adders. Dynamic full adders suffer from charge sharing, high power due to high switching activity, clock load and complexity [6].

II. PREVIOUSWORKS SURVEY

The full-adder function can be described as follows: Given the three 1-bit inputs A, B, and C_{in}, it is desired to calculate the two 1-bit outputs SUM and C_{out}, where

$$SUM = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = C_{in} (A \oplus B) + AB \quad (2)$$

These outputs can be expressed in many different logic expressions. Therefore, many full adder circuits can be designed using the different expressions. There are three main components to design a full adder cell [3]. Those are XOR or XNOR, Carry generator and SUM Generator.

1. Complementary Pass Transistor Full Adder (CPLFA)

Another conventional adder use the Complementary Pass Transistor Logic (CPL) [7] with swing restoration is shown in Fig.1. It has Transistor count 32. CPL produces various intermediate nodes with their complement to find the outputs. The basic difference between the pass-transistor logic and the complementary CMOS logic styles is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines. One pass transistor network is enough to implement the logic function therefore; results are generated by smaller number of transistors and smaller input load.

Pass-transistor logic has the problem of threshold voltage drop. So, output inverters are necessary to guarantee the drivability. CPL is not an appropriate choice for low power due its high switching activity of intermediate nodes, its high transistor count, its static inverters and overloading of its inputs. But, CPL is better than CMOS for the studied circuit conditions.

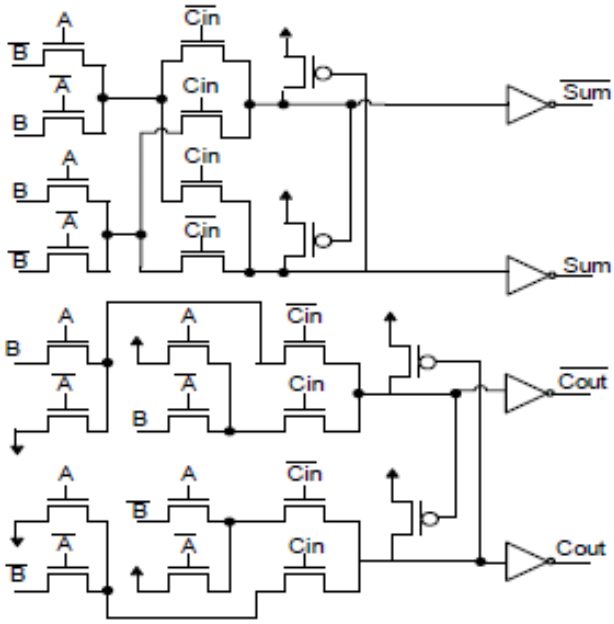

Fig. 1: The Complementary pass transistor logic full adder.

2. Complementary CMOS Full Adder (C-CMOSFA)

The complementary CMOS adder [4] is based on regular CMOS structure with conventional pull-up and pull-down transistors and has 28 transistors is shown in fig.2. Due to high number of transistors, its power consumption is more. The input capacitance of a static CMOS gate is larger because each input is connected to the gate of either NMOS or PMOS transistor. However, using inverters on the output nodes decreases the rise-time and fall-time and increases the driving ability. It functions well at low power supply voltages because it does not have threshold loss problem. The advantage of complementary CMOS style is its robustness against transistor sizing and voltage scaling.

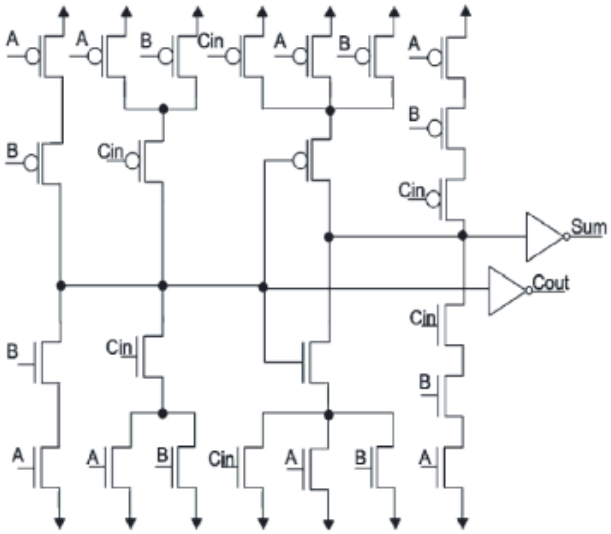

Fig. 2: CCMOS full adder.

3. The Hybrid Full Adder (HFA)

Fig. 3 shows another full adder called Hybrid full adder [4]. In this design the pass logic circuit that cogenerates the intermediate *XOR* and *XNOR* outputs has been improved. This full adder cell uses 26 transistors but has the full swing logic, balanced output and good output drivability.

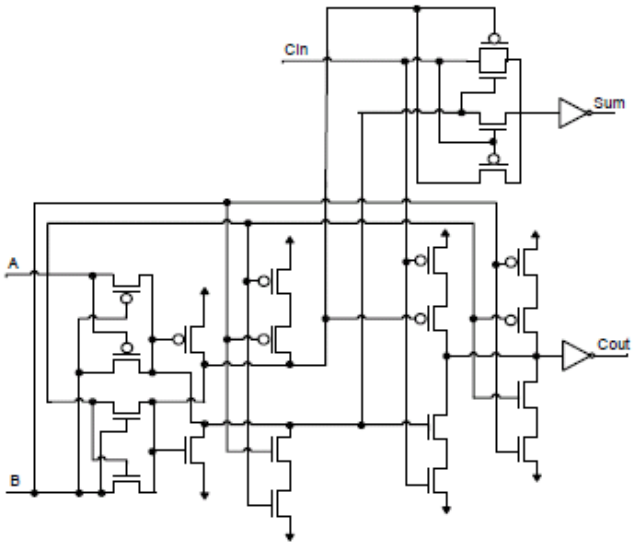

Fig. 3: The Hybrid Full Adder

4. GDI Technique Full Adder (GDIFA)

A. Bazzazi and B. Eskafi says that Full adder cell with the GDI technique is implemented to design a high performance and low power full adder cell. The new adder design with GDI technique [8] is shown in Fig.4. GDI cell contains three inputs – G (common state input of NMOS and PMOS), P (input to the source or drain of PMOS) and N (input to the source or drain of NMOS). In this adder cell 24 transistors are used. Full adder is divided into two stages; GDI technique is used in first cell to generate XOR and XNOR functions. Full swing with low voltages is shown in first stage and complementary outputs with other inputs will be fed to the second stage. Sum and carry is generated in second stage.

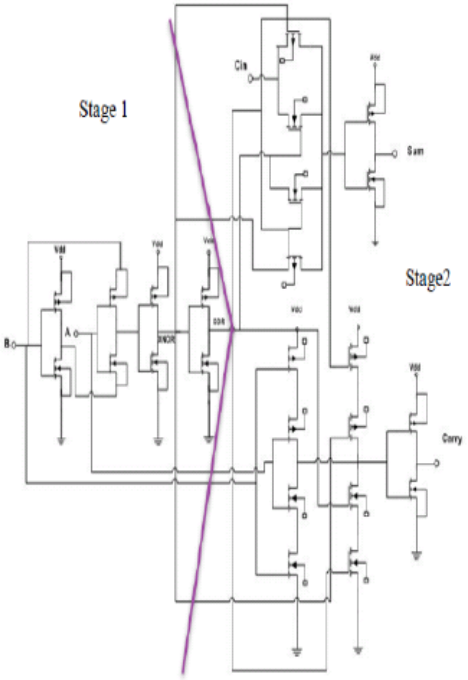

Fig. 4: Full Adder using GDI Technique.

5. Transmission Gate Full Adder (TGA)

Transmission gate full adder consists of 20 transistors, as shown in Fig.5 [9] is based on the concept of transmission gate. TFA consists of a PMOS transistors and an NMOS transistor that are connected in parallel way, which is particular type of pass – transistor logic circuit. This adder cell is required double number of transistors to design the function. It is low power consuming and this is good for designing XOR or XNOR gates. The main disadvantage of this circuit is that it lacks in driving capability, more number of transistors are needed. It also have lower loading of the inputs and intermediate nodes, lower – transistor count and balanced generation of SUM and C_{out} signals.

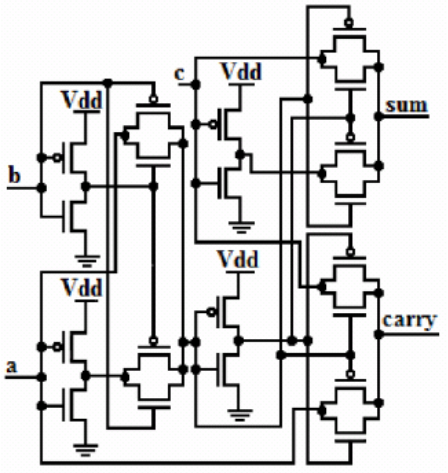

Fig.5 Transimission gate Full Adder

6. Multiplex Based Full Adder (MBFA)

MB12T [10] has been implemented using six multiplexers or 12 transistors. Each multiplexer is implemented by pass-transistor logic with two transistors. As shown in Fig. 6, there is no VDD or GND connection in this circuit and there are some paths containing three serried transistors. It causes to increase delay of producing SUM signal. The size of each transistor in mentioned path should be three times larger to balance the output and optimize the circuit for PDP. Therefore, the area of the circuit is increased.

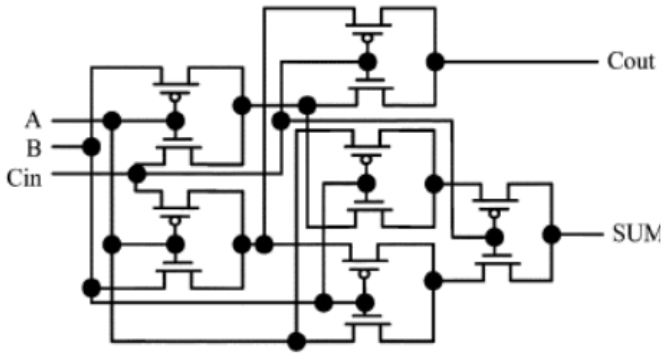

Fig.6. Multiplexer based full adder (MB12T).

7. The 10- Transistors Full Adder (10-T-FA)

H.T. Bui, Y. Wang and Y. Jiang say that the 10 transistor Full adder is use more than one design style for the implementation, so that it is called as Hybrid logic design style. The 10-Transistors full adder (10T) is shown in Fig. 7[3]. A, B and Cin are the inputs. Sum and Cout are the outputs. This full adder generates A⊕B and uses it and its complement as a select signal to generate the outputs. In

full adder 10T small number of transistors count are used and produces the non full swing pass transistor with swing restored transmission gate technique. This full adder cannot work properly when supply voltage is less than 1.8V. Due to its power supply it has smallest delay.

The main disadvantage of 10-transistor adder cell is the producing the high capacitance values for the inputs.

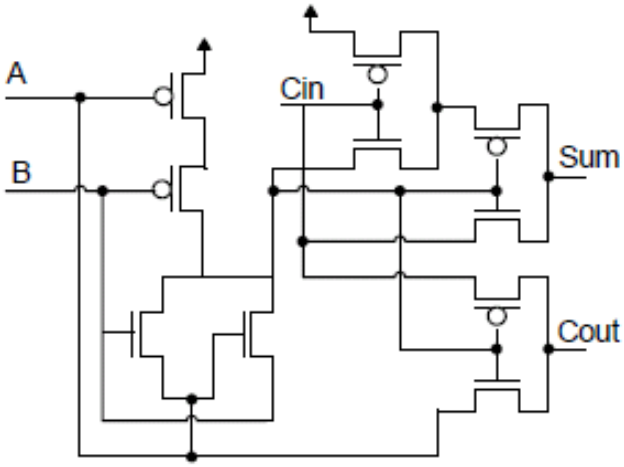

Fig. 7: The 10- transistor full adder.

8. SERF Full Adder

SERF full adder is also implemented by 10 transistors, as shown in Fig.8, uses energy recovery technique to reduce power consumption [2]. SERF use energy recovery technique to decrease the power consumption. Energy recovery logics reuse charge. Therefore, it consumes less energy than the other full adders. There are some problems in this circuit. First SUM is generated from two cascaded XNOR gates (group1) which lead to long delay. Second, it cannot work correctly in low voltage. As shown in Fig. 9 in the worst case, when *A=B='1'* there is *2Vtn* threshold loss in output voltage. Therefore, logic 1 is becomes equal to *VDD-2Vtn* in this case. The suitable operating supply voltage is limited to *VDD> 2Vtn+|Vtp|*. Second, there are five gate capacitances on node X. It causes to long delay in generating of intermediate $A \oplus B$ signal and finally delay in generating SUM and COUT. This problem also increases the power.

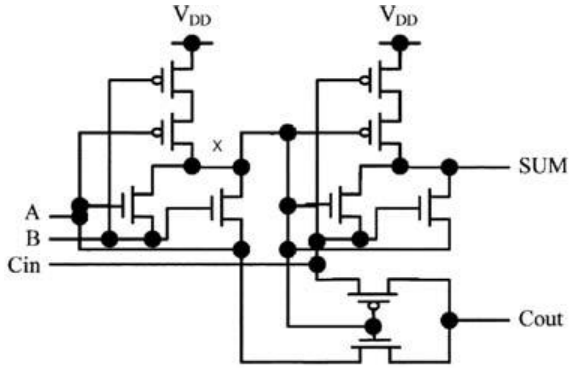

Fig.8: Energy recovery full adder -SERF full adder circuit.

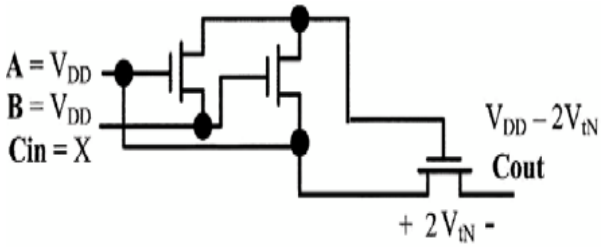

Fig. 9: Worst case of threshold loss problem in SERF full adder.

9. The 8-Transistors full adder (DG-8TFA)

DG-8T [6] has been implemented a full adder is based on three transistor XOR gate and 2-to-1 multiplexer with 8 transistors in total is shown in fig.10. It acquires least silicon area. The heart of the design is based on a modified version of a CMOS inverter and a PMOS pass transistor. The sum output is basically obtained by a cascaded exclusive ORing of the three inputs in accordance with equation (1).The carry output is obtained in accordance with equation (2). The final sum of the products is obtained using a wired OR logic.

For this design, authors were considered that the W/L ratios of transistors M1-M6 are same. The voltage drop due to the threshold drop in transistors M3 and M6 in fig.10 can be minimized by suitably increasing the aspect ratios of the two transistors. However, the threshold voltage drop of |VT,p| provided by the pMOS pass transistor M3 when a=0 and b=0 is used to turn on the nMOS pass transistor M8 and therefore we get an output voltage equal to |VT,p|-VT,n , where VT,p is the threshold voltage of the pMOS transistor and VT,n is the value is very close to 0V. Similarly, the threshold drop of the transistors M7 and M8 can be minimized by suitably increasing the aspect ratios of transistors M7 and M8.

This implementation has been found to operate faithfully at low input 0.17V when using the 0.18 micrometer technology and give less power consumption.

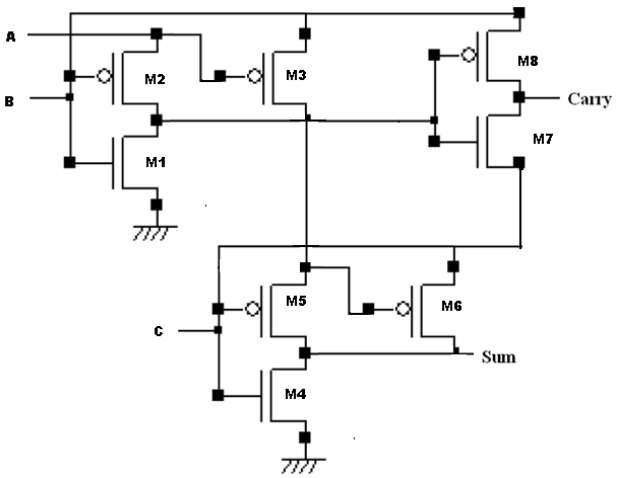

Fig.10. Full-adder cell using 8-Transistor (DG-8T).

10. The 4-Transistors full adder (4-TFA)

Fig. 11shows the 4-Transistors full adder cell. This adder cell is based on the majority function [4, 10] and eliminates time consuming XOR gates. In this adder two static CMOS inverter are used as inverter gate. Due to its less number of transistors, this design works at low supply voltage 0.65V with low and high performance. Carry signal is generated by majority function and at the same time sum signal is generated by majority not function. By considering majority function truth table, the majority function returns logic 1, only if there is more logic 1s than logic 0s given at the input. The main disadvantage is the area due to the uses of capacitors in its design.

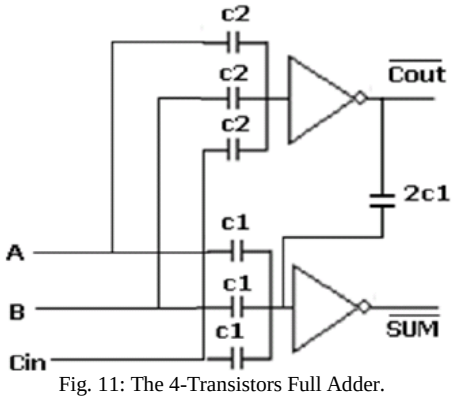

Fig. 11: The 4-Transistors Full Adder.

TABLE I: -COMPARATIVE STUDIES OF POWER-DELAY PRODUCT OF DIFFERENT ADDERS

Adder	Transistor Count	Power Supply(V)	Technology (µm)	Average Power(µW)	Delay(ns)	PDP
Complementary Pass Transistor Full Adder [7]	32	0.8	0.18	0.800	0.681	0.4172fj
Complementary CMOS Full Adder [4]	28	2.3	0.18	4.82	0.048	233.16E-18j
Hybrid Full Adder [11]	26	0.8	0.18	0.5978	0.672	0.4017fj
GDI Technique Full Adder [4]	24	1.8	0.18	0.78	50	39aj
Transmission Gate Full Adder [8,9]	20	1.8	0.18	2.7036	0.102	275.75E-18j
Multiplex Based Full Adder [10]	12	2.3	0.18	5.253	0.029	157.142E-18j
10- Transistors Full Adder [7]	10	0.8	0.18	0.5978	0.672	0.4017fj
SERF Full Adder[2,6]	10	2.3	0.18	1.000	0.039	39.481E-18j
8-Transistors full adder [6]	8	2.3	0.18	1.129	0.012	14.123E-18j

4-Transistors full adder [8]	4	0.8	0.18	0.5451	0.687	0.3745fj

III. CONCLUSION

In this paper, we have studied and compaired various methods of designing 1-bit full adder cell from some recent published research work. First we discussed Complementary Pass Transistor Logic full adder and gradually come across minimum transistor count of 4 in the designing of full adder. It is observe that a optimum number of transistor to be selected to get best combination of power and delay.

A comparative study is shown in table-I, which indicates that the minimum delay, minimum power are two different parameters of interest. Real time applications including embedded & application specific processors are best suited for minimum delay while other general purpose systems can be design for minimum power requirements.

Research may go more directions, each targeting on some specific applications. Enhanced driving capability also facilitates lower voltage of faster operations, which lead to less energy consumption.

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