SVGA060 Series
Low-Power AMOLED Microdisplay

Data Sheet

Pre-Spec V1.0


SVGA060SC


SVGA060SW


SVGA060SG

For Products:

SVGA060SC — Full Color
SVGA060SW — Monochrome White
SVGA060SG — Monochrome Green

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Record of Revision

Version	Revise Date	Page	Content
Pre-spec. V0.1	2011-10-13		Initial release.

Contents

1 FEATURES

1.1 Description

- Si-Base AMOLED Microdisplay
  - 0.18μm CMOS Technology
  - Full Digital Video Core
  - High Efficiency Top Emission Structure
  - Active Driver Technology
  - Low Power Consumption
- 800×600 (SVGA) Resolution
  - View Area: 0.6 inch
  - Pixel Pitch : 15μm
  - Total Pixels : 804 (×3)× 604
- Digital Video Interface
  - Compatible with ITU-R BT.656/601
  - Accept 8/16/24 Bit Digital Video
  - Accept YCbCr/RGB Color or Mono
  - Support SVGA/VGA/PAL/NTSC etc
  - Support Progressive & Interlaced
- Digital Video Signal Enhancement
  - Brightness
  - Contrast
  - R/G/B Offset
- Gamma Correction
  - Piecewise-Linear by 17 Entry Lookup Table
  - Expand 8bit Input to 9bit Output
- Digital 8 Bit Input/9bit Output Gray Level
- Support Binocular Stereovision
- Horizontal/Vertical Mirror
- Shift and Position Control
- Embed Temperature Sensor
- Integrate Vcom DC-DC Module
- Built-in Test Patterns
- 2-Wire Series Interface

1.2 Products Coding

SVGA	050	S	C	V1	R1
①	②	③	④	⑤	⑥

①Type	
SVGA	800x600
SXGA	1280x1024

③Temperature	
S	Standard: -40 ~ +60℃
N	Normal: -10 ~ +40℃

⑤Connector	
V1	Board to Board
V2	FPC to Board

②Size	
050	0.5 Inch
060	0.6 Inch
097	0.97 Inch

④Color	
C	Full Color
W	Mono White
G	Mono Green

⑥Revision	
R1	Revision No.

2 INTRODUCTION

SVGA060 series AMOLED microdisplay fabricated by OLiGHTEK's proprietary top emitting and high luminance efficiency Si-Base AMOLED technology. SVGA060 series microdisplay includes full color, Monochrome white, Monochrome green and other specifications. With the same interface and pin definition, SVGA060 series products have 12.06mm×9.06mm (0.6 inch) display area, and supported less than or equal to SVGA resolutions format. With proper optical magnification devices, the microdisplay can provide high quality, large virtual image.

SVGA060 series microdisplay's silicon substrate is fabricated by 0.18μm CMOS technology, integrated full digital video signal processing, 804×604×3 active driving units, digital logic control, scan distribution, D/A converting, temperature sensor, gamma correction, DC-DC for cathode's negative voltage, two-wire serial communication interface and so on. The input video signal is compatible with ITU-R BT. 656/601 and support 8/16/24 bit digital video. The function of microdisplay such as display mode, scanning direction, display position, brightness, contrast, R/G/B offset and gamma correction can be programmed through the two-wire serial communication interface. The digital interface voltage level is compatible with 1.8~3.3V CMOS standard. The microdisplay can be applied in various near-to-eye display systems that demand compact size, high resolution, low power consumption and wide working temperature range.

2.1 Characteristic Parameters

<table>
<tr><th colspan="2">Model</th><th colspan="3">SVGA060</th></tr>
<tr><th colspan="2">Product Type</th><th>Color</th><th>Monochrome White</th><th>Monochrome Green</th></tr>
<tr><td colspan="2">Resolution</td><td colspan="3">800 (×3) × 600</td></tr>
<tr><td colspan="2">Active pixels</td><td colspan="3">804 (×3) × 604</td></tr>
<tr><td colspan="2">Pixel Aspect Ratio</td><td colspan="3">1:1</td></tr>
<tr><td colspan="2">Color Pixel Arrangement</td><td colspan="3">RGB Vertical Stripe</td></tr>
<tr><td colspan="2">Gray Levels</td><td colspan="3">8bit/256Levels</td></tr>
<tr><td colspan="2">Luminance Uniformity</td><td colspan="3">> 90%</td></tr>
<tr><td colspan="2">Contrast</td><td colspan="3">> 10000:1</td></tr>
<tr><td colspan="2">Digital Video Interface</td><td colspan="3">ITU-R BT.601/656
24bit，4:4:4，RGB/YCbCr
16bit，4:2:2，YCbCr
8bit，4:2:2，YCbCr/Mono</td></tr>
<tr><td rowspan="2">Power Supply</td><td>Kernel</td><td colspan="3">DC 1.8V@Max50mA</td></tr>
<tr><td>OLED Pixels</td><td colspan="3">DC 5.0V@Max200mA</td></tr>
<tr><td rowspan="2">Operating Temperature</td><td>Standard</td><td colspan="3">-40℃ ～ +65℃</td></tr>
<tr><td>Normal</td><td colspan="3">-10℃ ～ +40℃</td></tr>
<tr><td rowspan="3">Chromaticity</td><td>White (Color)</td><td colspan="3">CIEx=0.30±0.05, CIEy=0.35±0.05</td></tr>
<tr><td>White (Mono)</td><td colspan="3">CIEx=0.30±0.05, CIEy=0.33±0.05</td></tr>
<tr><td>Green (Mono)</td><td colspan="3">CIEx=0.30±0.05, CIEy=0.63±0.05</td></tr>
<tr><td colspan="2">Operating Humidity</td><td colspan="3">≤85%RH（Non condensing）</td></tr>
<tr><td colspan="2">Pixel Size(μm²)</td><td colspan="3">15 × 15</td></tr>
<tr><td colspan="2">Viewing Area(mm²)</td><td colspan="3">12.06 × 9.06</td></tr>
<tr><td colspan="2">Mechanical Envelope(mm³)</td><td colspan="3">19.8 × 15.2 × 4.6</td></tr>
<tr><td colspan="2">Typical Luminance(Cd/m²)</td><td>>70</td><td>>100</td><td>>1500</td></tr>
<tr><td colspan="2">Typical Power Consumption(mW)</td><td><250</td><td><250</td><td><450</td></tr>
<tr><td colspan="2">Lifetime(Hours)</td><td>25000</td><td>25000</td><td>20000</td></tr>
<tr><td colspan="2">Weight(g)</td><td colspan="3">≤1.8</td></tr>
</table>

2.2 Product Structure

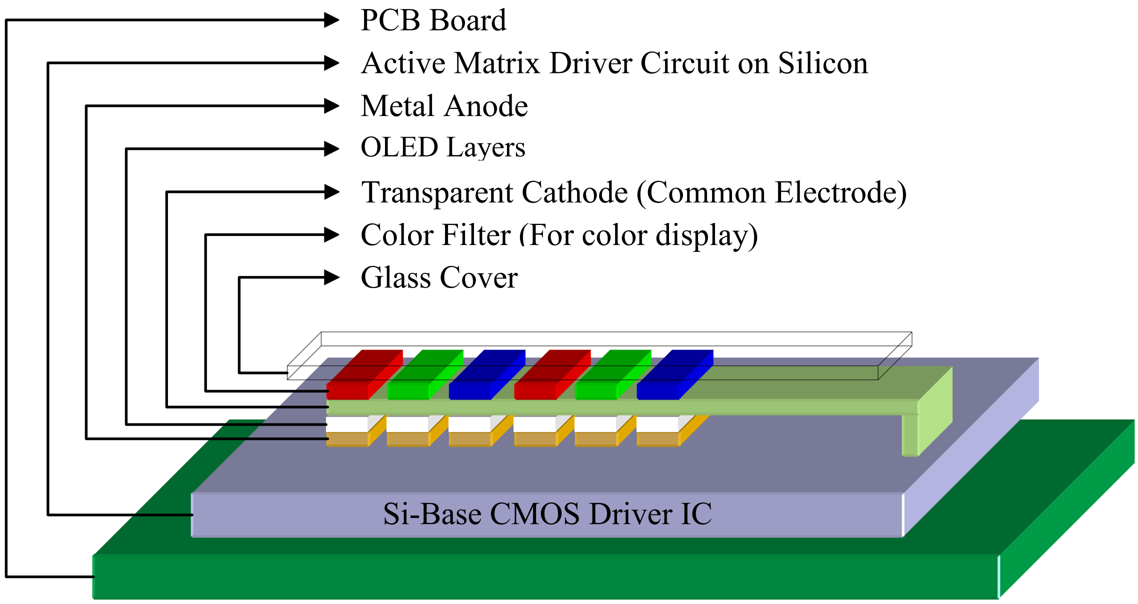


Figure 2-1 SVGA060 series device’s structure

OLiGHTEK’s SVGA060 series AMOLED microdisplay is manufactured on a silicon substrate which is integrated with video signal processing and active driver, then followed by sub-pixel metal anode, multi-layer OLED light-emitting film, transparent cathode(common cathode), compound high density sealing film, RGB color filter layer, etc., after which paste glass cover to protect the microdisplay, and bond with PCB board. Figure 2-1 shows the device’s structure.

2.3 Pixel Array

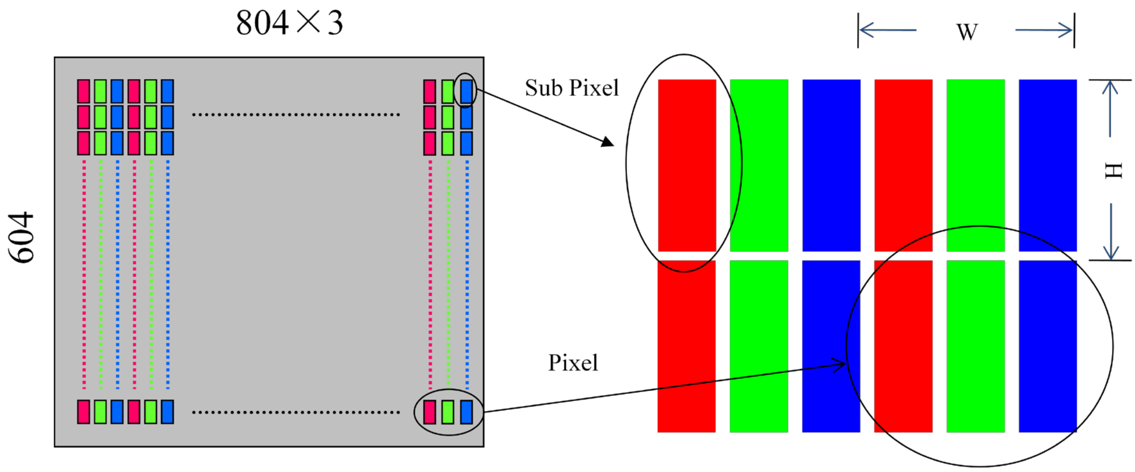


Figure 2-2 Pixel and Sub-Pixel Array

Each pixel of OLiGHTEK’s SVGA060 series AMOLED microdisplay is formed by three sub-pixels (Figure 2-2). The pixel’s related parameters are shown below:

Model	Pixel Size		Duty Cycle	View Area	
	Width(W)	Height(H)		Width（804×W）	Height（604×H）
SVGA060	15μm	15μm	75%	12.06mm	9.06mm

Each sub-pixel of colorful display emits white light, and full-color display is fulfilled through the RGB color filter. Since there is no color filter, the luminous efficiency of the monochrome display is higher than the color display.

2.4 Function Diagram

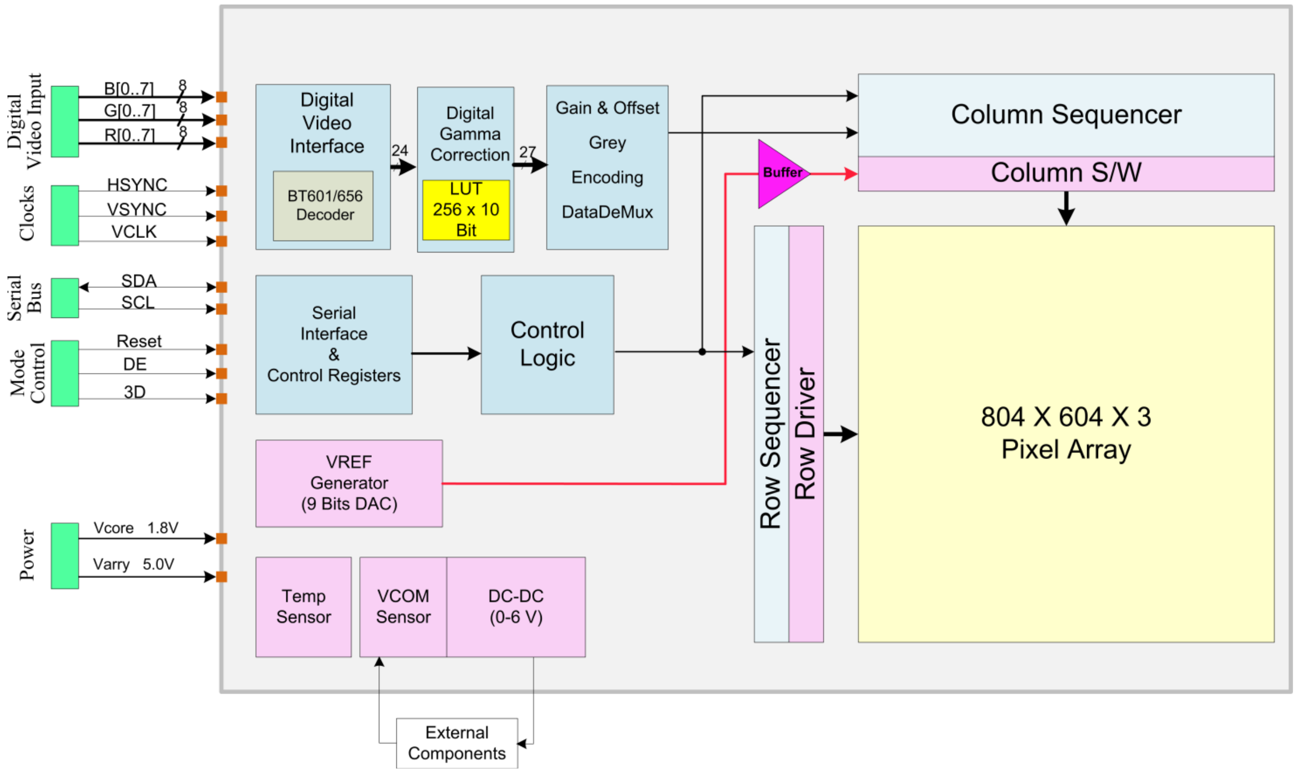


Figure 2-3 SVGA060 Series Architecture & Principle Diagram

Figure 2-3 shows top level block diagram of SVGA060 series microdisplay's driver circuit. The chip is mainly composed of the digital video signal interface and decoder, digital video signal processing, digital Gamma correction, color saturation adjustment, gray mapping, D/A conversion, row & column scanning, pixel driver array, two-wire serial communication interface, programmable control logical unit, temperature sensor, DC/DC converter and other function modules.

Compatible with ITU-R BT.656/601 standards, digital video signal interface has three 8-bit data channels and accepts 8/16/24 bit RGB or YCbCr video signals. According to the different input formats, the internal video decoder outputs 24bit RGB signal. The digital video signal processing circuit receives the 24bit RGB signal, and then adjusts the brightness, contrast respectively. The output signal is still 24bit format and sent to the gamma correction circuit. The gamma correction circuit makes corrections of the 24bit RGB signal by look-up table, and extends it to 27bit RGB signal output. Color saturation adjustment circuit makes adjustment of RGB offset respectively and the output is 9bit in each RGB path. By D/A conversion, the gray mapping circuit converts the three 9 bit R/G/B signals to three R/G/B analog voltage signals. The voltage stands for the R,G,B luminance, Then, the analog signal is stored in sub-pixel driving unit; driving unit circuit applies the RGB analog voltage signal to OLED's anode and holds the voltage on for one frame/field cycle time. With external 5V power supply and external components on PCB backplane, the DC/DC module generates a negative voltage which is applied to all of the OLED sub-pixels' common cathode. Under the bias voltage between the anode and the cathode, OLED keeps emitting light in one whole frame/field cycle.

Through the internal 256 programmable SRAM (register), control logic unit deals with the digital signal, makes the different unit circuits working in harmony with each other, and realizes the binocular 3D display.

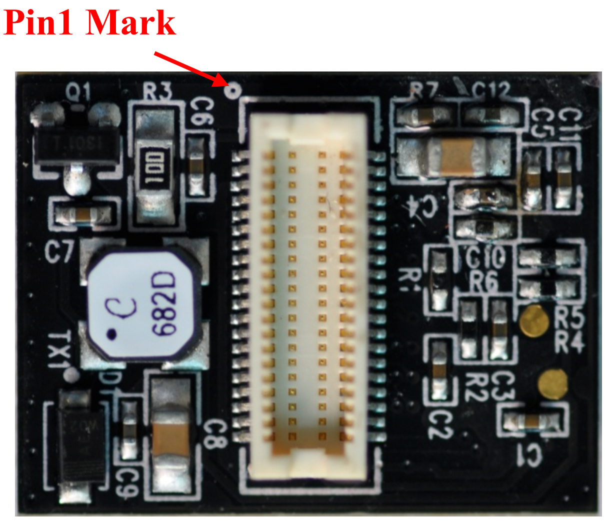
Compatible with I^2C communication standard, the two-wire serial interface is used to realize the read/write operation of the 256 registers, accordingly, make the chip circuit programmable, such as digital video signal decoding and processing, gamma correction, DC/DC conversion and so on.

The internal temperature sensor circuit updates the corresponding register's numeral value which represents the real-time internal working temperature. The numeral value is read by the external control logic unit through the two-wire serial interface. According to the luminance-temperature character, OLED's common cathode's negative voltage can be adjusted by DC/DC converter so as to get proper luminance at different temperatures.

2.5 Interface & Pin Assignment

2.5.1 Connector & Pin Assignment

SVGA060 series microdisplay use a 0.5mm pitch, 40pins connector made by Hirose, part number is DF12D(3.0)-40DP-0.5.



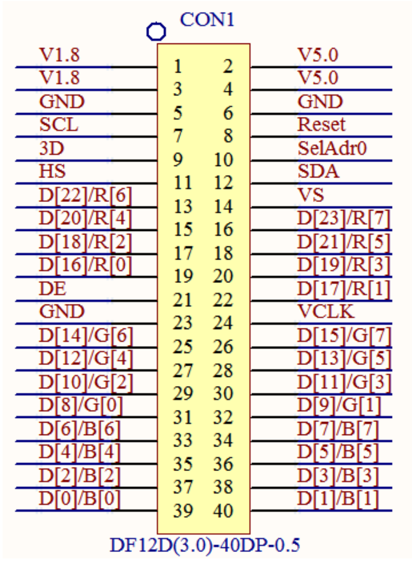


Figure 2-4 SVGA060 series microdisplay connector & pin assignment

2.5.2 Pin Definition

Symbol	Pin No.	Function Description	I/O	Remark
V1.8	1,3	1.8V Power for digital core	P	
V5.0	2,4	5.0V Power for OLED driver	P	
GND	5,6,23	Power Ground	P	
SCL	7	Serial Communication Clock Line	I/O	
Reset	8	Master Reset (Active Low)	I	No Floating
3D	9	3D Left/Right Eye Mode Select	I	
SelAdr0	10	Device Slave Address Select	I	Default Pull-up
HS	11	Hsync Signal Input	I	
SDA	12	Serial Communication Data Line	I/O	
VS	14	Vsync Signal Input	I	
D[16..23]/ R[0]—R[7]	13,22, 15—20	ITU-R Standard, 8 Bit Red Signal	I	
DE	21	Data Enable Signal Input	I	
VCLK	24	Pixel Clock Signal Input	I	
D[8..15]/ G[0]—G[7]	25—32	ITU-R Standard, 8 Bit Green Signal	I	
D[0..7]/ B[0]—B[7]	33—40	ITU-R Standard, 8 Bit Blue Signal	I	

2.6 Recommended Operation Ratings

SYMBOL	DESCRIPTION	MIN	TYP	MAX ①	UNIT
V1.8	1.8V Power Supply	1.62	1.8	2.5	V
V5.0	5.0V Power Supply	4.5	5.0	6.0	V
$V_{I/O}$	Digital Signal Voltage②	—	1.8	3.3	V
Tstorage	Storage Temperature	-55	20	90	°C
Toperate	Operation Temperature	-40	20	65	°C

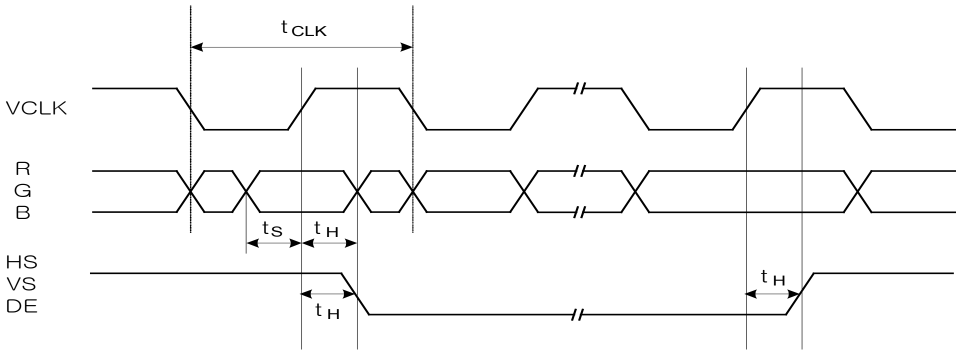
Note ①: The absolute maximum rating values (except $V_{I/O}$) of this product are not allowed to be exceeded at any time. If the product is used with its symbol value exceeding the maximum rating or in an extreme condition, the characteristics of the device maybe recovered and the lifetime of the device will decrease, even the device may be permanently destroyed.
Note ②: All the Digital logic Pins (except the Power Pin) can support 1.8V/3.3V CMOS logic level.

2.7 Electrical Characteristics

2.7.1 DC Characteristics

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNIT
$I_{1.8}$	1.8V Supply Current		9	10	12	mA
$I_{5.0}$	5.0V Supply Current		10	20	250	mA
Vcom	Cathode Voltage		-5	-2	0	V
Typical Power Consumption	Working	Color @ 70Cd/m2	80	120	250	mW
		Monochrome White @ 100Cd/m2	60	100	250	
		Monochrome Green @ 1500Cd/m2	150	280	450	
	Display Off		71	-	75	
	Power Down		0	-	0.4	

2.7.2 AC Characteristics



PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Digital Video Data Setup & Hold	t_S	1	-	-	ns
	t_H	0.5	-	-	ns
Video Clock Period	t_{CLK}	17.8	-	-	ns
Video Clock Duty	q	40	50	60	%

3 DETAILED FUNCTION DESCRIPTION

3.1 Digital Video Interface

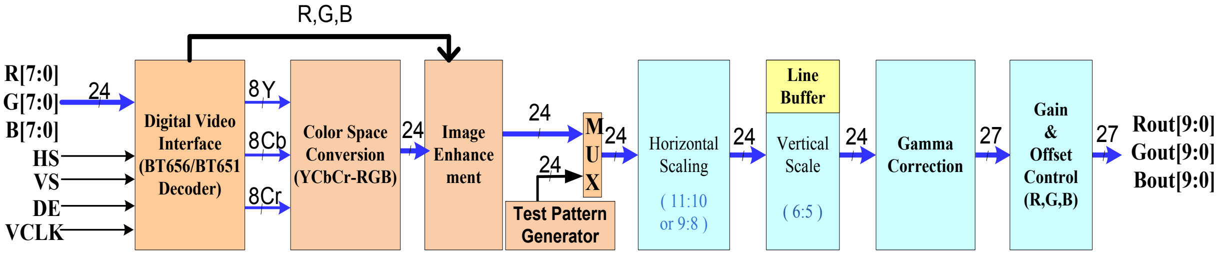


Figure 3-1 Digital Video Processing Flow Diagram

The digital video interface has three 8-bit data channels, and additional horizontal and vertical sync (HS/VS), data enable (DE), pixel clock signals (VCLK). User should select the correct signals to connect according to different Video format. VCLK is always needed in any mode. When use 8bit with embedded sync signal (8bit ITU-R BT.656 YCbCr/Mono 4:2:2), only G[7..0] bus and VCLK is needed.

OLED Display receives data with BT601/656 format, like 8/16/24bit and 4:2:2/4:4:4 format, and transfers to 24bit RGB signal, then sends the signal to Video signal enhancement module, after scaling (only a scaled-down), gamma correction, RGB offset adjustment, finally output 27bit RGB signal.

If the input video format is CVBS, component, VGA (analog RGB), HDMI, DVI video signals, etc., OLED Display requires an external video decoder, such as ADV7180, AD9883, TVP7002 and so on.

3.1.1 Input Video Standard

Table 3-1 Input Signal Standard & Pin Used

Video Standard	Color Space	PIN		
		R[7:0]	G[7:0]	B[7:0]
8-bit, 4:2:2	YCbCr	-	YCbCr[7:0]	-
8-bit, Mono	Y	-	Y[7:0]	-
16-bit, 4:2:2	YCbCr	-	Y[7:0]	CbCr[7:0]
24-bit, 4:4:4	YCbCr	Cr[7:0]	Y[7:0]	Cb[7:0]
24-bit, 4:4:4	RGB	R[7:0]	G[7:0]	B[7:0]

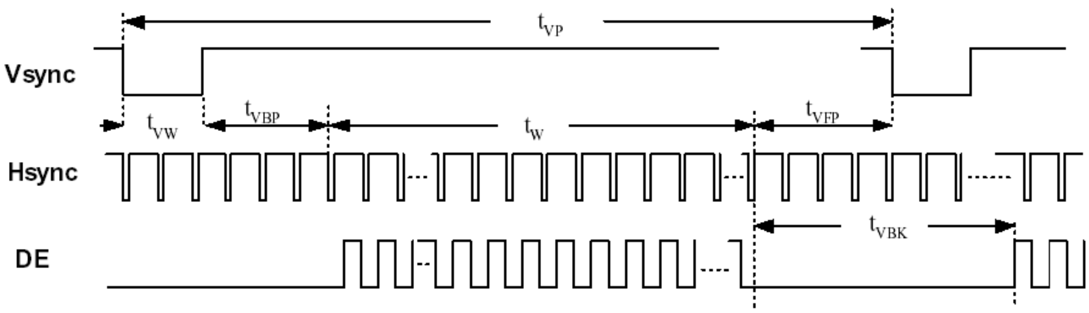


Figure 3-2 Input Sync Signals Timing (For All Formats)

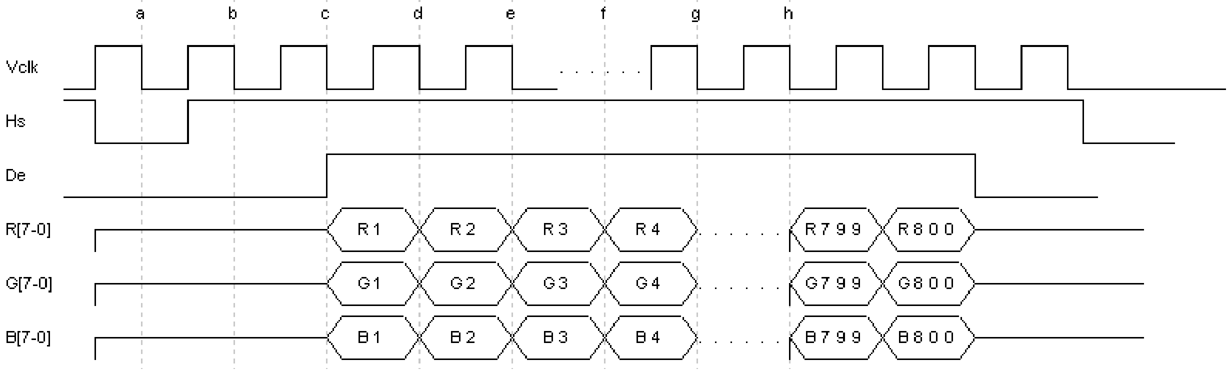


Figure 3-3 24-bit, 4:4:4 RGB Input VideoTiming

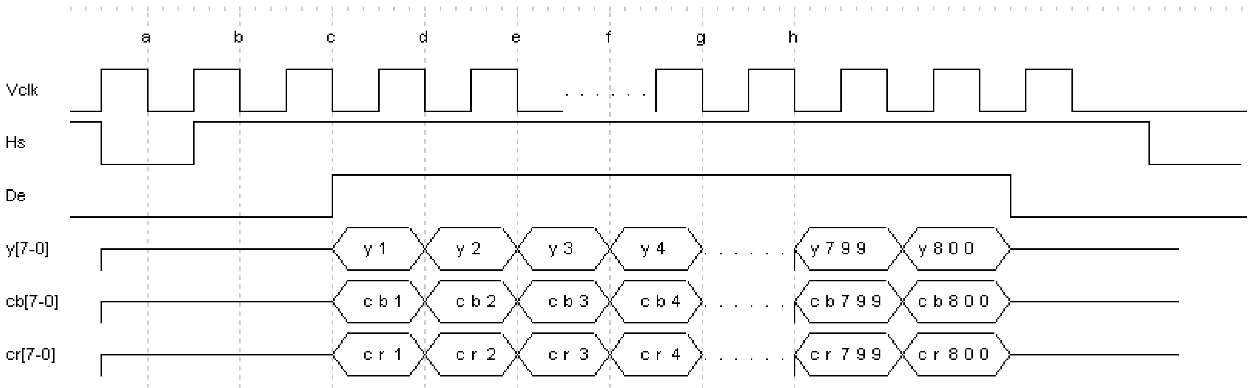


Figure 3-4 24-bit, 4:4:4 YCbCr Input Video Timing

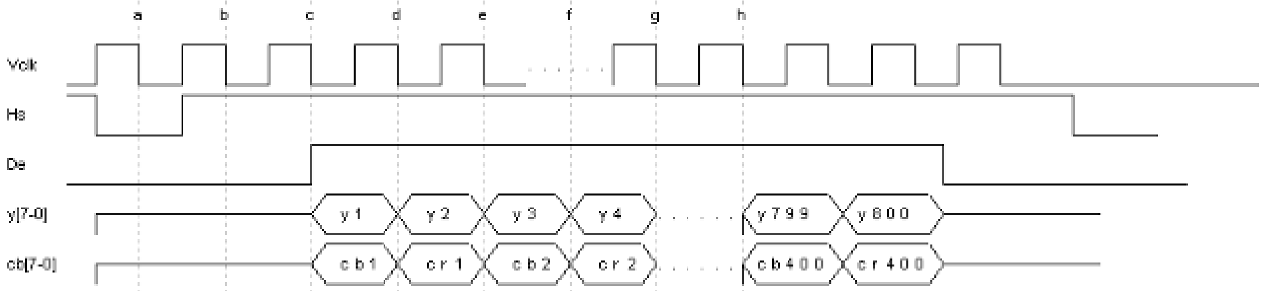


Figure 3-5 16-bit, 4:2:2 YCbCr Input Video Timing

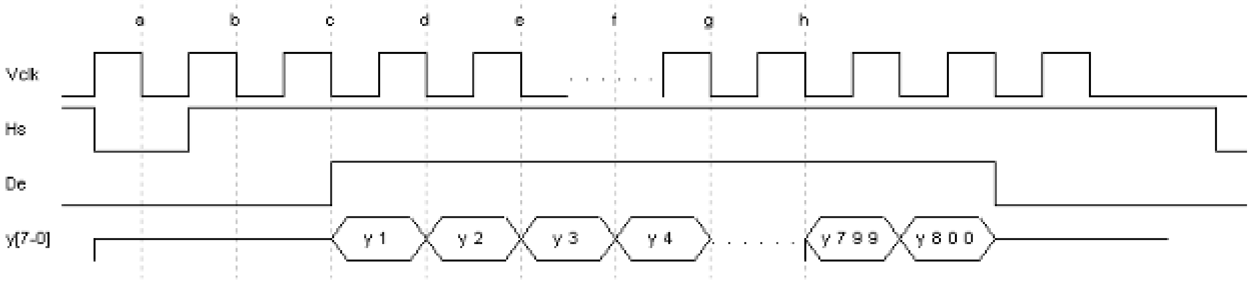


Figure 3-6 8-bit, Mono Input Video Timing

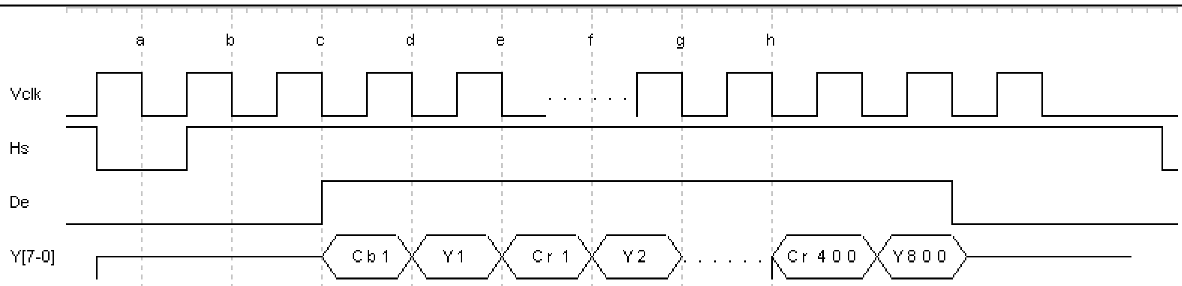


Figure 3-7 8-bit, 4:2:2 YCbCr input Video timing

Table 3-2 VESA Progressive Video Modes

Mode		Frequency	Total	Active	Front Porch + Border	Sync Pulse	Back Porch + Border
SVGA 800X600 85Hz non-interlaced	H	53.674 KHz	1048 pixels	800 pixels	32 pixels	64 pixels	152 pixels
	V	85.061 Hz	631 lines	600 lines	1 line	3 lines	27 lines
	P	56.250 MHz					
SVGA 800X600 75Hz non-interlaced	H	46.875 KHz	1056 pixels	800 pixels	16 pixels	80 pixels	160 pixels
	V	75.000 Hz	625 lines	600 lines	1 line	3 lines	21 lines
	P	49.500 MHz					
SVGA 800X600 72Hz non-interlaced	H	48.077 KHz	1040 pixels	800 pixels	56 pixels	120 pixels	64 pixels
	V	72.188 Hz	666 lines	600 lines	37 line	6 lines	23 lines
	P	50.000 MHz					
SVGA 800X600 60Hz non-interlaced	H	37.879 KHz	1056 pixels	800 pixels	40 pixels	128 pixels	88 pixels
	V	60.317 Hz	628 lines	600 lines	1 line	4 lines	23 lines
	P	40.000 MHz					
VGA 640X480 85Hz non-interlaced	H	43.269 KHz	832 pixels	640 pixels	56 pixels	56 pixels	80 pixels
	V	85.008 Hz	509 lines	480 lines	1 line	3 lines	25 lines
	P	36.000 MHz					
VGA 640X480 75Hz non-interlaced	H	37.500 KHz	840 pixels	640 pixels	16 pixels	64 pixels	120 pixels
	V	75.000 Hz	500 lines	480 lines	1 line	3 lines	16 lines
	P	31.500 MHz					
VGA 640X480 72Hz non-interlaced	H	37.861 KHz	832 pixels	640 pixels	24 pixels	40 pixels	128 pixels
	V	72.809 Hz	520 lines	480 lines	9 line	3 lines	28 lines
	P	31.500 MHz					
VGA 640X480 60Hz non-interlaced	H	31.469 KHz	800 pixels	640 pixels	16 pixels	96 pixels	48 pixels
	V	59.940 Hz	525 lines	480 lines	10 line	2 lines	33 lines
	P	25.175 MHz					

Table 3-3 VESA Interlaced Video Modes

Mode		Frequency	Total	Active
MPTE-170M-1 640X480 Mono 30Hz interlaced	H	15.734 KHz	780 pixels	640 pixels
	V	60 Hz Field	262.5 lines	240 lines
	P	12.27 MHz		
SMPTE-170M-2 800X600 Mono 25Hz interlaced	H	15.625 KHz	1052 pixels	800 pixels
	V	50 Hz Field	312.5 lines	600 lines
	P	16.437 MHz		

Mode		Frequency	Total	Active
NTSC 720X480 Color 30Hz interlaced	H	15.734 KHz	858 pixels	720 pixels
	V	60 Hz Field	262.5 lines	240 lines
	P	13.5 MHz		
PAL 720X576 Color 25Hz interlaced	H	15.625 KHz	864 pixels	720 pixels
	V	50 Hz Field	312.5 lines	288 lines
	P	13.5 MHz		
NTSC (Square) 640X480 Color 30Hz interlaced	H	15.734 KHz	780 pixels	640 pixels
	V	60 Hz Field	262.5 lines	240 lines
	P	12.2727 MHz		
PAL (Square) 768X576 Color 25Hz interlaced	H	15.625 KHz	944 pixels	768 pixels
	V	50 Hz Field	312.5 lines	288 lines
	P	14.75 MHz		

Table 3-4 VGA and SVGA Video Timing

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Clock Frequency	f_{CLK}			56.25	MHz	SVGA 85Hz
HSYNC Period	t_{HP}	660			t_{CLK}	
HSYNC Pulse Width	t_{HW}	10			t_{CLK}	
HSYNC Back Porch	t_{HBP}	10			t_{CLK}	
Horizontal Valid data width	t_{HV}	296		804	t_{CLK}	
HSYNC Front Porch	t_{HFP}	60			t_{CLK}	t_{HV} >= 580
Horizontal Blank	t_{HBK}	80			t_{CLK}	
VSYNC Period	t_{VP}	106			t_{HP}	
VSYNC Pulse Width	t_{VW}	1			t_{HP}	
VSYNC Back Porch	t_{VBP}	7			t_{HP}	
Vertical valid data width	t_{W}	96		604	t_{HP}	
Vertical Front Porch	t_{VFP}	2			t_{HP}	
Vertical Blank	t_{VBK}	10			t_{HP}	

3.1.2 Color Space

If the input data format is YCbCr, the device will change it to RGB format. Color space conversion block converts color space from YCbCr to RGB and uses the following equations. Output signal is 24-bit RGB format, 8-bit in each path.

$$R = 1.164 \times (Y - 16) + 1.596 \times (Cr - 128)$$
$$G = 1.164 \times (Y - 16) + 0.813 \times (Cr - 128) - 0.392 \times (Cb - 128)$$
$$B = 1.164 \times (Y - 16) + 2.017 \times (Cb - 128)$$

3.1.3 Digital Video Signal Enhancement

Digital video signal enhancement can be achieved by adjusting the brightness and the contrast ratio, as is Shown in Figure 3-8.

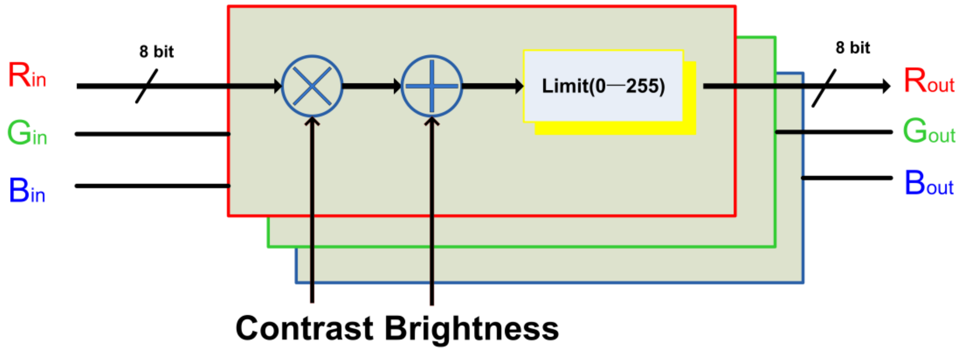


Figure 3-8 Digital Video Signal Enhancement Diagram

Brightness adjustment using addition and subtraction to achieve, the output value is equal to the input value plus the value of register 08H, and then minus 128. When the value of register 08H is greater than 80H, it means increase the brightness, whereas decrease. Brightness adjustment range is ±128.

$$V_{out} = V_{in} + Reg(08H) - 128$$

Contrast adjustment using multiplication and division to achieve, the output value is equal to the input value multiplied by the value of register 09H and then divided by 128. When the value of register 09H is greater than 80H, it means increase the contrast, whereas decrease. The gain of contrast adjustment range is 0 to 2.

$$V_{out} = V_{in} \cdot \frac{Reg(09H)}{128}$$

Note: The algorithms keep only 8bit data, if overflow, automatically discarded high bit.

3.1.4 Video Pattern Generation

Built-in test pattern generator can generate color bars, gray scale, tiles, horizontal stripes, vertical stripes, as well as monochrome red, green, blue, and white test pattern. Line width, line spacing, foreground color, background color, etc. of all test pattern can be set by relevant registers. Register 4AH is pattern mode selection, default value is 0, indicates the test pattern generator is turned off; register 4BH, 4CH, 4DH were used to set line width, line spacing, etc. respectively. Details of setting refer to Table 3-5and Figure 3-9

Table 3-5 Summary of Test Pattern Setting

Test Pattern Name	Patterns (4AH)	LineWidth (4BH)	LineSpace (4CH)	BGMASK (4DH)	FGMASK (4DH)
Color Bar	001	-	-	-	-
Gray Scale	010	-	-	-	-
Checker Board	011	-	-	-	-
Alternating Column	100	LineWide	Line Space	000	111
Alternating Row	101	LineWide	Line Space	000	111
Alternating Row & Column	110	LineWide	Line Space	000	111
All Black	100	-	-	000	000
All White	100	-	-	111	111
All Red	100	-	-	100	100
All Green	100	-	-	010	010
All Blue	100	-	-	001	001

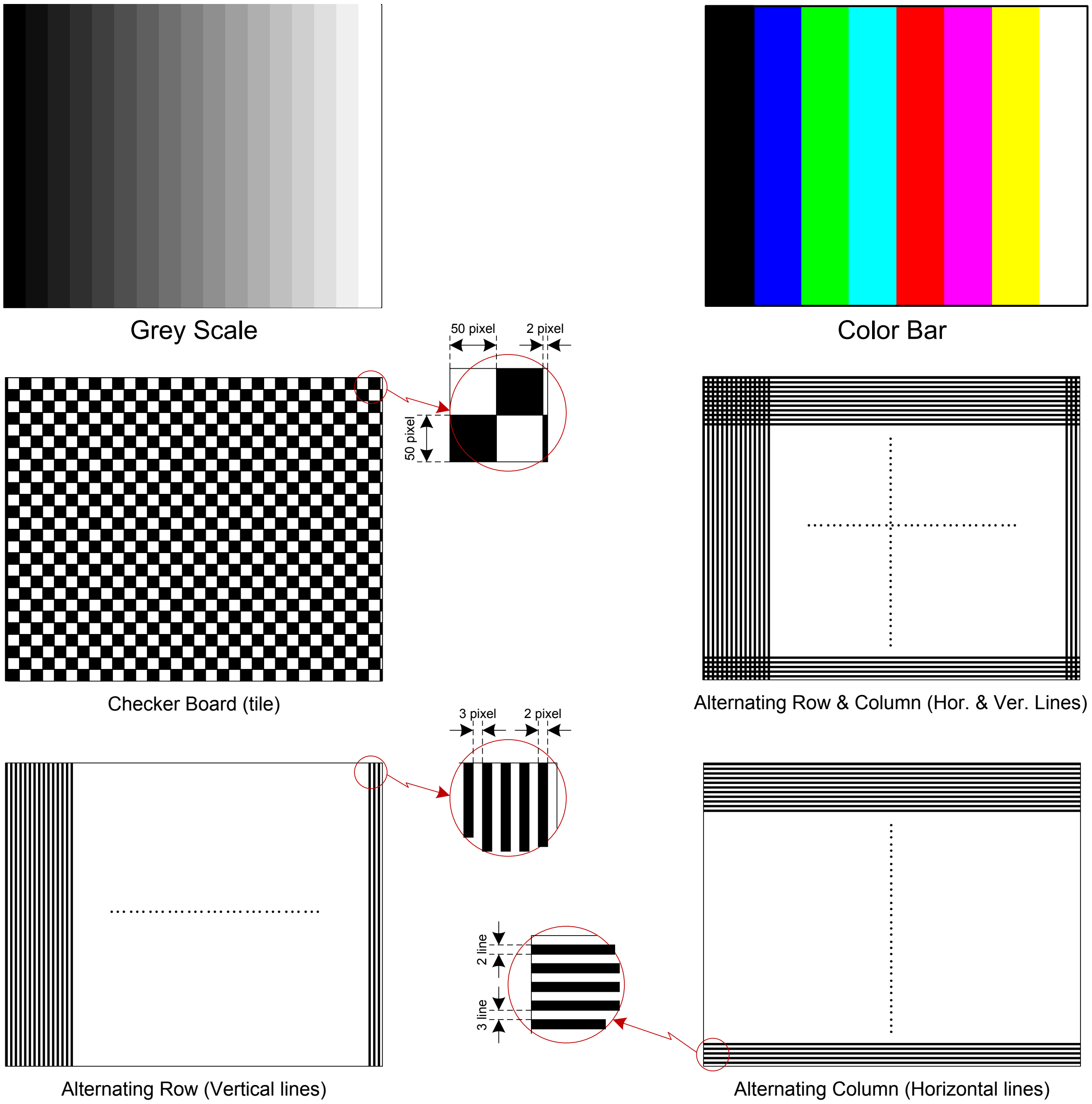


Figure 3-9 Test Video Patterns

3.1.5 Scaling

In order to maintain the aspect ratio of input image, some video format in need of scaling. Scaling could be achieved by set register 07H, the algorithm is shown in Figure 3-10 and Figure 3-11, applicable video format is shown in Table 3-6.

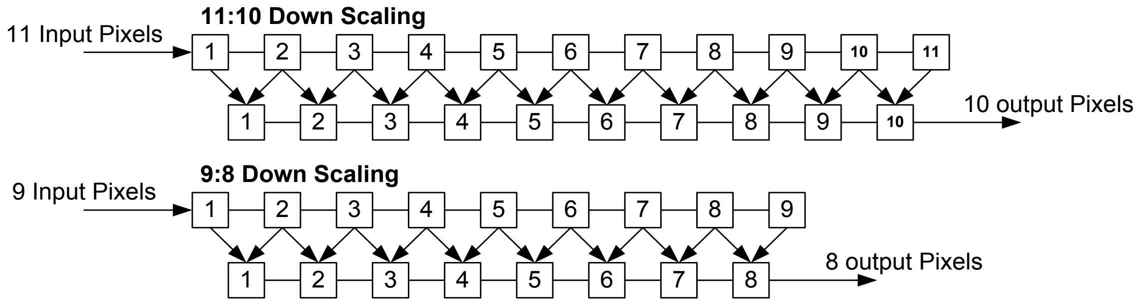


Figure 3-10 Diagram of the Horizontal Scaling Algorithm

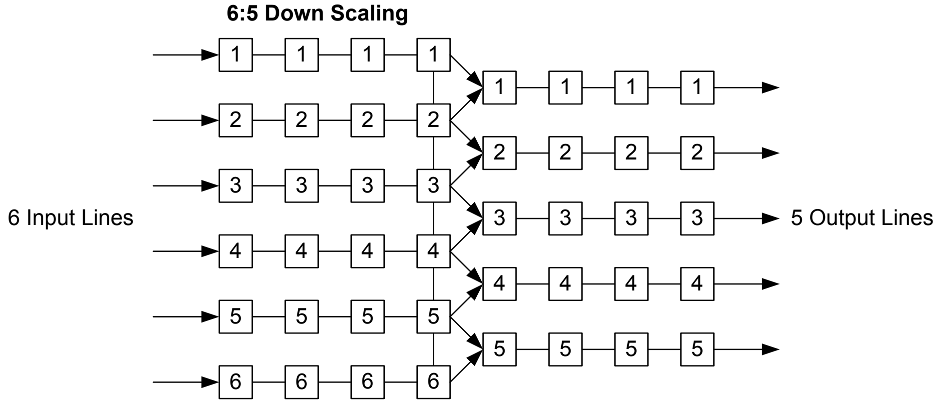


Figure 3-11 Diagram of the Vertical Scaling Algorithm

Table 3-6 Scaling format applied

Video Format Name	Input Resolution	Scan Mode	Hor. Scaling	Ver. Scaling	Display Resolution
SVGA	800 × 600	Progressive	1:1	1:1	800 × 600
VGA	640 × 480	Progressive	1:1	1:1	640 × 480
SMPTE-170M-2	800 × 600 Mono	Interlaced	1:1	1:1	800 × 600
SMPTE-170M-1	640 × 480 Mono	Interlaced	1:1	1:1	640 × 480
NTSC	720 × 480	Interlaced	11:10/9:8	1:1	640 × 480
NTSC (Square)	640 × 480	Interlaced	1:1	1:1	640 × 480
PAL (Square)	768 × 576	Interlaced	1:1	1:1	768 × 576
PAL	720 × 576	Interlaced	11:10/9:8	6:5	640 × 480

3.1.6 Gamma Correction

Gamma correction is performed using piecewise-linear function by a 17-entry lookup table. Gamma correction expends 8 bit input to 9 bit output by Look-Up Table (LUT). Intermediate values are computed by interpolating between the two nearest LUT entries. In C notation:

$$\mathbf{V_{out} = LUT[V_{in}/16] + V_{in}\%16 * (LUT[V_{in}/16+1] - LUT[V_{in}/16])\,/16}$$

Note:

- '/' denotes integer division truncating the remainder, '*' denotes multiplication, '%' denotes integer division taking remainder
- LUT[0~15] is 9 bit register to support the full 0-511 range without missing codes.
- LUT[16] is 10 bit register to support 201H~3FEH range, set to "200H" as maximum value (512) and "3FFH" as minimum value (-1).

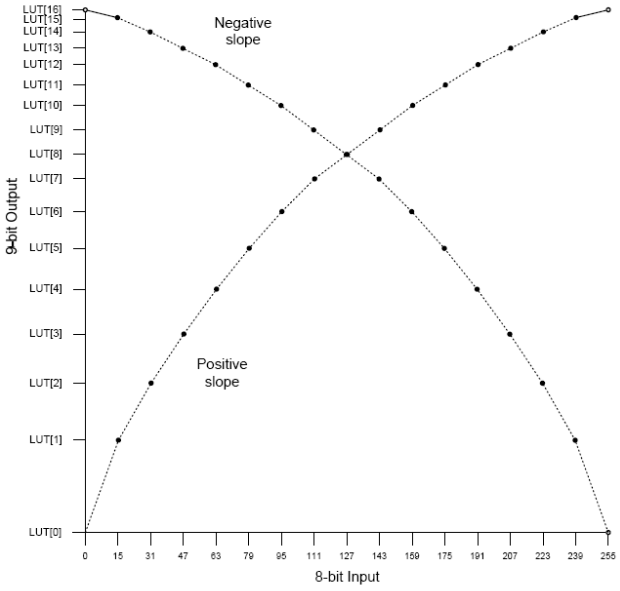


Figure 3-12 Gamma Correction LUT and Curve

3.1.7 RGB offset

After gamma correction process, the corrected R/G/B value can be shifted separately by Roffset, Goffset, Boffset configuration registers, color offset control registers 44H-49H are used to adjust separate R/G/B signal's offset. Gamma correction output 9bit data each channel, color offset adjustment range is 0~511.

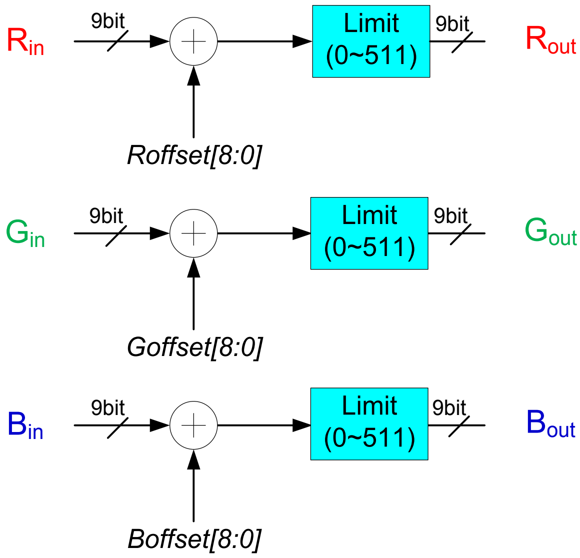


Figure 3-13 Color Offset Control

3.2 3D Video Display

Stereo register(02H) and 3DMODE pin can set 3D video display. If 3DMODE pin state is the same as the ST_mode bit (02H) value, the screen display is updated, whereas not. 3DMODE pin signal is latched at Vsync falling edge. 3D video display timing is shown below.

In progressive mode, 3D video signal using frame timing mode, such as the odd frame is updated left display, and the even frame is updated right display.

In interlaced mode, 3D video signal using field timing mode, such as the odd field is updated left display, and the even field is updated right display. At this point, the vertical resolution of each field is lower compare with the source, the last two bit of register 01H should be set to “11”, display will repeat to display each line in next line automatically, to ensure that the image aspect ratio and display.

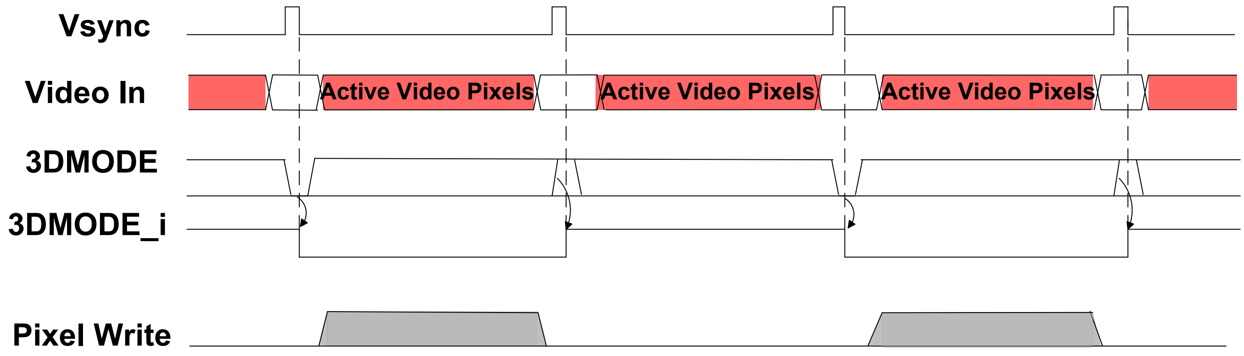


Figure 3-14 3D Video Display Timing

3.3 Power Supply & Reset

SVGA060 series microdisplay need 1.8V and 5V external power supply to operate, 1.8V is used for digital core include decoder, video signal enhancement, gamma correction, communication, etc.; 5V is used for drive circuit, D/A converter, and so on. To ensure the display image quality, please note that ripple and interference rejection of 5V power supply.

3.3.1 Power UP/Down Sequence

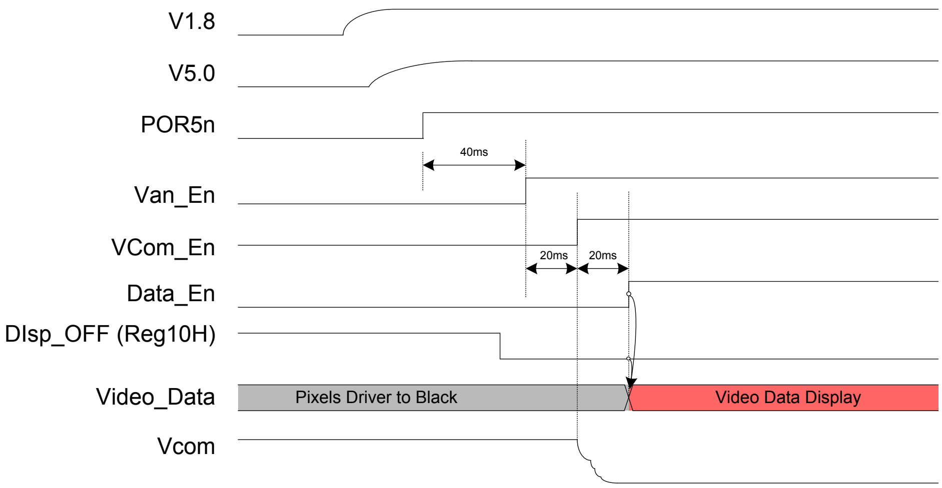


Figure 3-15 Power-up Sequence (1.8V power-up, threshold voltage = 1.2V)

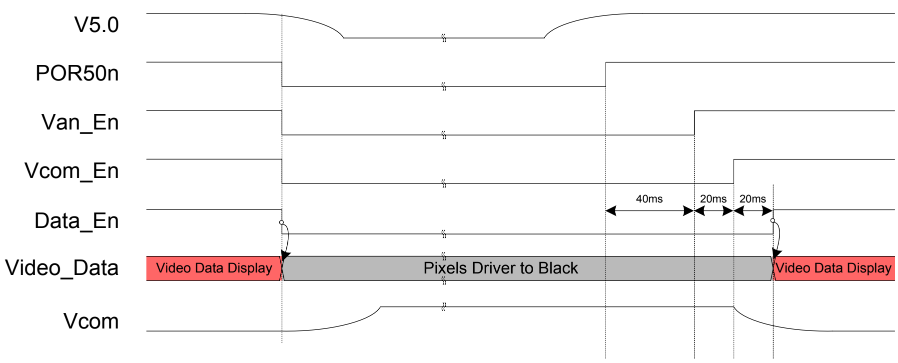


Figure 3-16 V5.0 Power Down & Up (POR5n threshold Voltage = 4V)

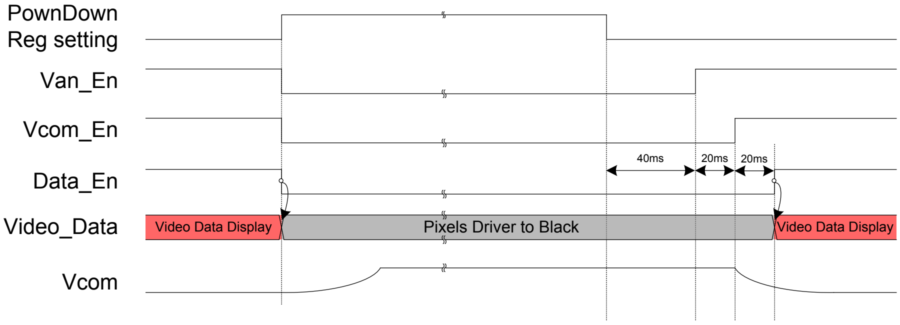


Figure 3-17 Register Control Power Down & Up

3.3.2 Reset Sequence

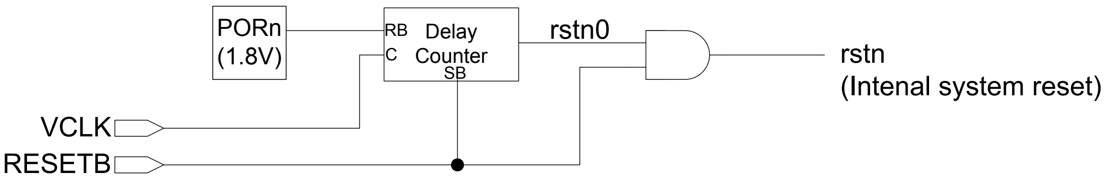


Figure 3-18 Reset Block Diagram

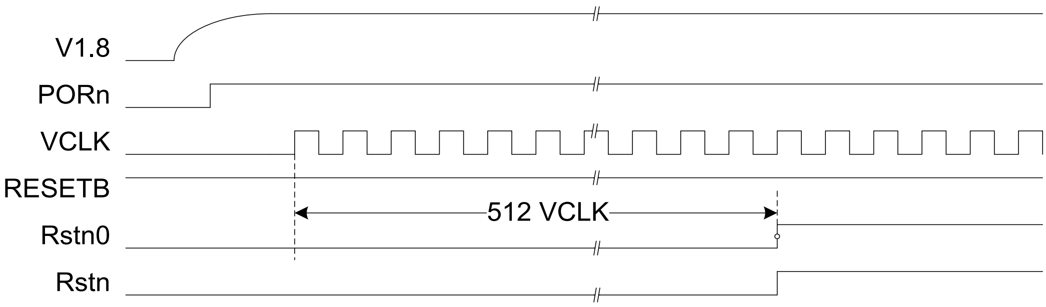


Figure 3-19 Reset Timing Case 1 – No external reset pin used (RESETB=1)

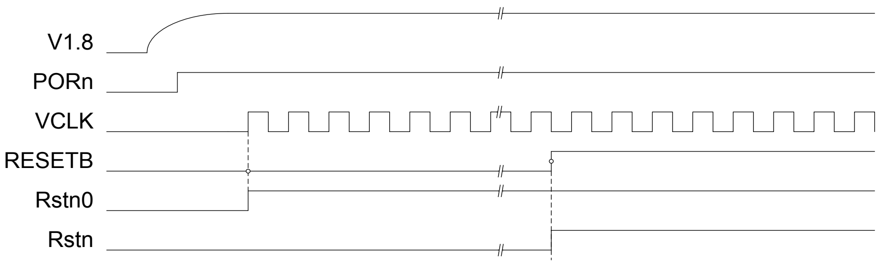


Figure 3-20 Reset Timing Case 2 – External reset pin depend on VCLK

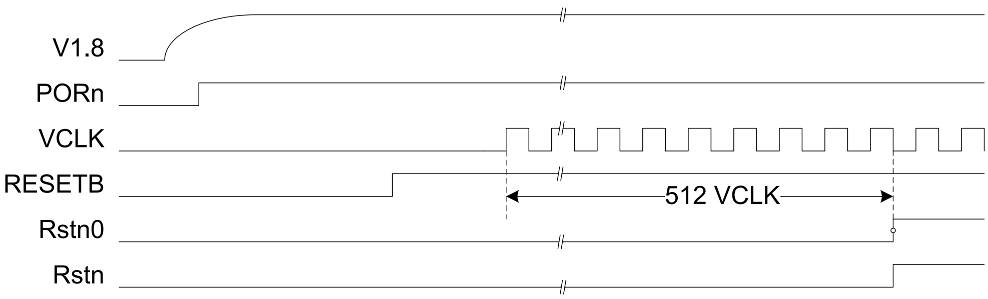


Figure 3-21 Reset Timing Case 3 – External reset pin applied

3.4 Unit Drive Circuit

SVGA060 series AMOLED pixel drive circuit as shown in Figure 3-22. Each OLED light-emitting diodes use voltage-driven approach, the typical photo electric properties as shown in Figure 3-23.

When scan signals ROWSEL and ROWSWL_B are valid at the same time, signal Video_In charges the capacitance C through MOS transistors P1&N1, and controls the output of N2. The capacitance C can be guaranteed to maintain the output of N2 in a frame/field cycle.

N2 is used in Source-Follower structure to control 5V(Van) power supply, the current flowed through the protection resistor R is applied to the OLED anode.

All pixels cathode of OLED is connected to negative voltage Vcom(common cathode structure), Vcom can be adjusted by set register 19H in order to achieve the display brightness adjustment.

N3 is used for discharge of parasitic capacitance of the OLED rapidly, thereby improving dynamic contrast of the display. The discharge current can be selected by register 17H and controlled by register 18H.

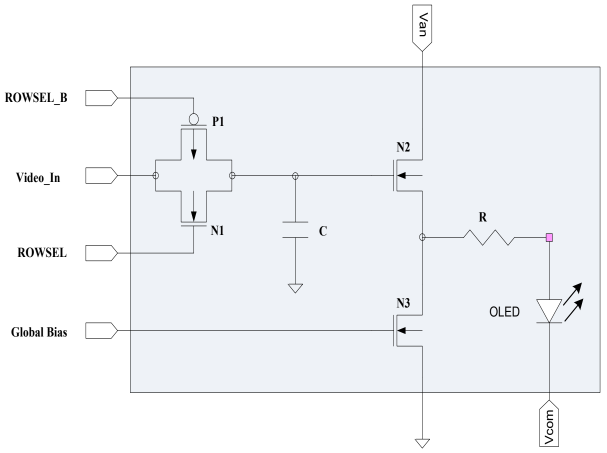


Figure 3-22 Unit Drive Circuit

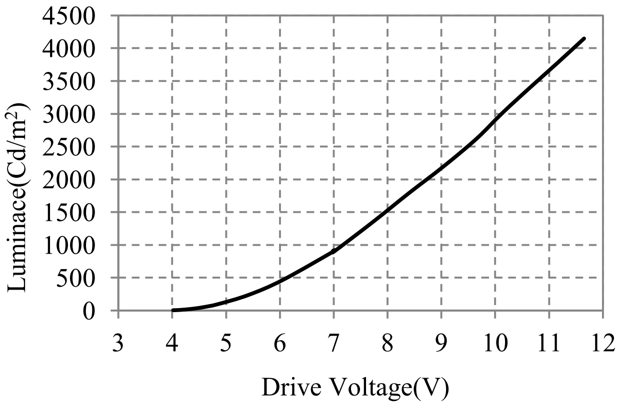


Figure 3-23 OLED photo electricity properties

3.5 DC/DC Converter

OLED emitting light needs to be applied positive bias voltage between the anode and cathode, the anode voltage from 5V power supply is controlled by drive transistor, all pixel's common cathode voltage Vcom supplied by DC/DC converter on the PCB backplane. The driving pulse of DC/DC converter is generated by the internal programmable pulse generator, the circuit shown in Figure 3-24. Vcom adjustment range is 0 ~-3V, corresponding to register 19H, the typical working curve is shown in Figure 3-25

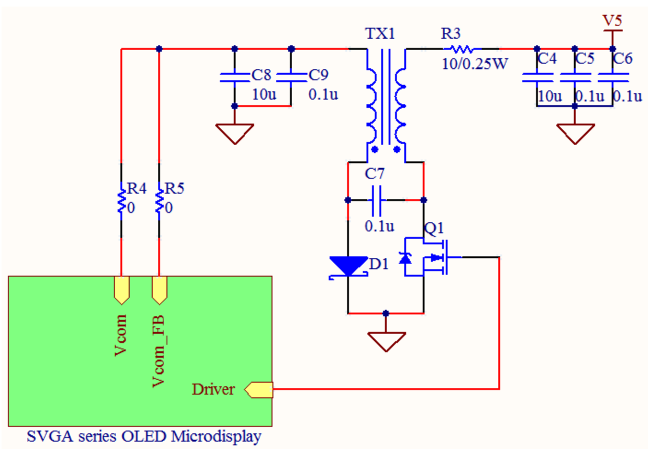


Figure 3-24 DC/DC Principal Diagram

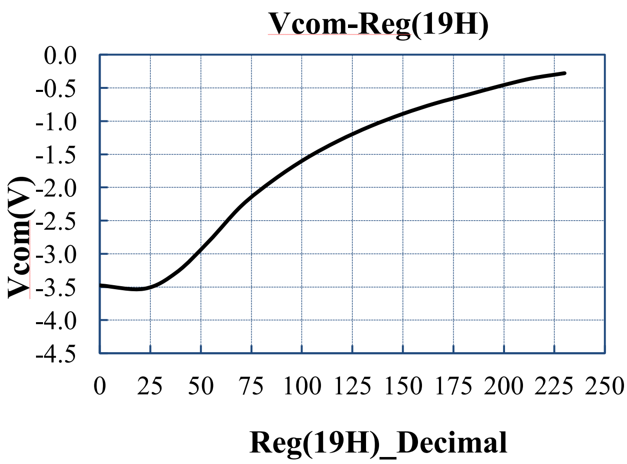


Figure 3-25 Vcom Programmable Working Curve

3.6 Temperature Sensor

The value of register 1DH is the internal temperature sensor's measured value. So the real-time internal working temperature can be read out through the two-wire serial interface. The temperature and the readout conversion relation is: $T = 0.47 \times Reg\,(1DH) - 40$

The temperature sensor response curve and the calibration curve are shown as Figure 3-26 and Figure 3-27.

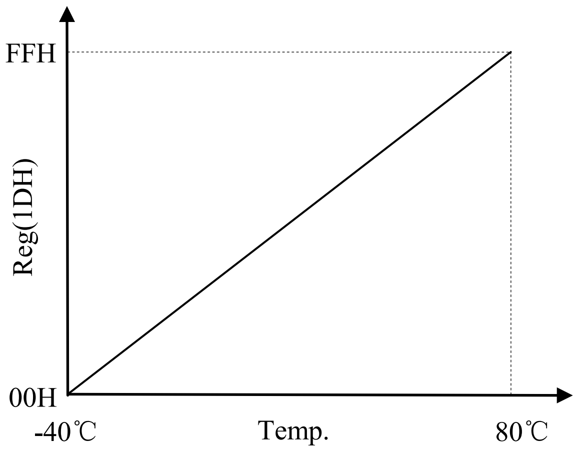


Figure 3-26 Temp. Sensor Readout

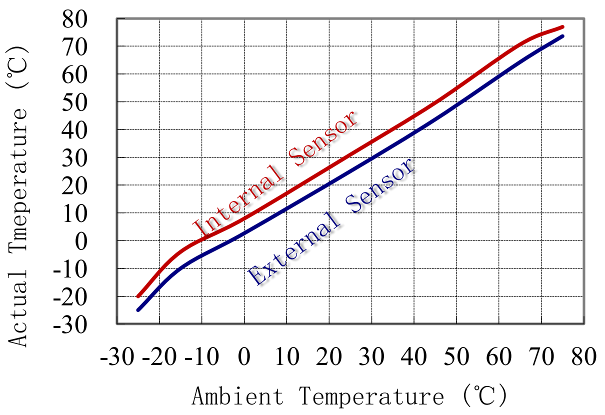


Figure 3-27 Temp. Sensor calibration curve

3.7 Two-wire Serial Interface

Compatible with I^2C communication standard, the two-wire serial interface is used to read/write the registers to realize the display programmable control, such as digital video signal decoding and processing, gamma correction, Vcom adjustment and so on.

SVGA060 series microdisplay acts as a slave for receiving and transmitting data, all read/write operations must be launched by the master. The SDA and SCL line must be pull-up to1.8v or 3.3v power via a resistance by the outside communication controller.

Key Features and tag:

- Communication speed (SCL) support from 100K to 1MHz;
- 8-bits Slave Address consists of 7-bits device address and 1-bit read/write flag;
- Start/Re-Start: SDA change from HIGH to LOW while SCL is HIGH, See Figure 3-28;
- Stop: SDA change from LOW to HIGH while SCL is HIGH, see Figure 3-28;
- ACK: SDA is LOW during the acknowledge clock pulse;
- NAK: SDA is HIGH during the acknowledge clock pulse;
- One transmission includes 8bit data and an acknowledge bit, total nine clock of SCL;
- Except Start and Stop condition:
  - HIGH or LOW state of SDA can only being changed while SCL is LOW
  - Data on the SDA line must be stable during the HIGH period of the SCL

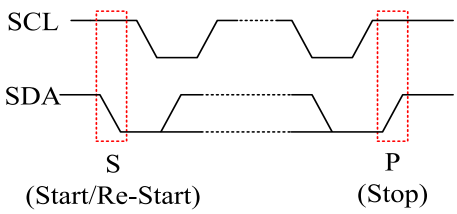


Figure 3-28 Start & Stop Timing

3.7.1 Communication Operating

- Write data (Figure 3-29) :
  1) Master sends Start condition (S)
  2) Master sends 7bit Slave Address and 1bit write flag ($\overline{W}$) represents as low
  3) Slave sends 1bit ACK (A) response
  4) Master sends 8bit register address (Register)
  5) Slave sends 1bit ACK (A) response
  6) Master sends 8bit data (Data)
  7) Slave sends 1bit ACK (A) response
  8) Master sends stop condition(P)

S	Slave Addr	$\overline{W}$	A	Register	A	Data	A	P

Figure 3-29 Write Data format

- Read Data (Figure 3-30)
  1) Master sends Start condition (S)
  2) Master sends 7bit Slave Address and 1bit Write flag ($\overline{W}$) represents as low
  3) Slave sends ACK (A) response
  4) Master sends 8bit Register Address (Register)
  5) Slave sends 1bit ACK (A) response
  6) Master sends 1bit Re-Start condition (Sr)
  7) Master sends 7bit Slave Address and 1bit Read flag (R) represents as high
  8) Slave sends 1bit ACK (A) response
  9) Slave sends 8bit Data (Data)
  10) Master sends 1bit NAK ($\overline{A}$) response
  11) Master sends Stop condition (P)

S	Slave Addr	$\overline{W}$	A	Register	A	Sr	Slave Addr	R	A	Data	$\overline{A}$	P

Figure 3-30 Data format(Master reads from Slave)

3.7.2 Serial Interface Bus Address Selection

Two salve address of SVGA060 series microdisplay can be selected by an externally SelAdr0 pin. The SelAdr0 pin has an internal pull up resistor (10K) to pull up to 1.8V power. One of microdisplay's SelAdr0 pin must be connected to GND when used in binocular stereovision application. Microdisplay's corresponding read/write address is shown as Table 3-7.

Table 3-7 Slave Address list

A7 (MSB)	A6	A5	A4	A3	A2	A1 (SelAdr0)	A0 (R/$\overline{W}$)	Slave Address (R/$\overline{W}$)
0	0	0	1	1	1	1(Default)	1/0	1FH/1EH
0	0	0	1	1	1	0	1/0	1DH/1CH

4 REGISTER DESCRIPTION

4.1 Summary of Registers

Table 4-1 Summary of Registers

Address	Bytes	Description	Default Value
00H	1	Chip's Drive Circuit Revision	00H
01H	1	Input Video Type Set	34H
02H	1	Sync signal Polarity Set & 3D functions	00H
03H	1	Vertical Blank Lines	00H
04H	1	Horizontal Blank Pixels	00H
05H	1	Adjust Start Active Video Position	01H
06H	1	Field Start Line Position Adjustment For Interlaced Video	00H
07H	1	Down Scaling for NTSC & PAL Video	00H
08H	1	Brightness Control (Video Signal Brightness)	80H
09H	1	Contrast Control (Video Signal Contrast)	80H
0AH	1	Reserved	4AH
0BH	1	Reserved	5AH
0CH	1	Reserved	00H
0DH	1	Reserved	00H
0EH	1	Reserved	00H
0FH	1	Power Down Mode Control	00H
10H	1	Display ON/Off & Scan Directions	04H
11H	1	Display Left Margin	02H
12H	1	Display Right Margin	02H
13H	1	Display Top Margin	02H
14H	1	Display Bottom Margin	02H
15H	1	Reserved	44H
16H	1	D/A Offset Setting	80H
17H	1	Discharge Current Setting	01H
18H	1	Discharge Enabled Control	00H
19H	1	Vcom Level Setting (Display's Brightness)	FFH
1AH	1	Reserved	1DH
1BH	1	Reserved	74H
1CH	1	Reserved	FFH
1DH	1	Temperature Sensor Readout	-
1E~1FH	2	Reserved	-
[21,20H]	2	9 Bit Gamma Correction LUT0	000H
[23,22H]	2	9 Bit Gamma Correction LUT1	020H
[25,24H]	2	9 Bit Gamma Correction LUT2	040H
[27,26H]	2	9 Bit Gamma Correction LUT3	060H
[29,28H]	2	9 Bit Gamma Correction LUT4	080H
[2B,2AH]	2	9 Bit Gamma Correction LUT5	0A0H
[2D,2CH]	2	9 Bit Gamma Correction LUT6	0C0H
[2F,2EH]	2	9 Bit Gamma Correction LUT7	0E0H
[31,30H]	2	9 Bit Gamma Correction LUT8	100H
[33,32H]	2	9 Bit Gamma Correction LUT9	120H

Address	Bytes	Description	Default Value
[35,34H]	2	9 Bit Gamma Correction LUT10	140H
[37,36H]	2	9 Bit Gamma Correction LUT11	160H
[39,38H]	2	9 Bit Gamma Correction LUT12	180H
[3B,3AH]	2	9 Bit Gamma Correction LUT13	1A0H
[3D,3CH]	2	9 Bit Gamma Correction LUT14	1C0H
[3F,3EH]	2	9 Bit Gamma Correction LUT15	1E0H
[41,40H]	2	10 Bit Gamma Correction LUT16	200H
42H	1	Reserved	-
43H	1	Reserved	-
[45,44H]	2	9 Bit Red Signal Offset	100H
[47,46H]	2	9 Bit Green Signal Offset	100H
[49,48H]	2	9 Bit Blue Signal Offset	100H
4AH	1	Test Pattern Mode Selection	00H
4BH	1	Test Pattern Line Width Setting	02H
4CH	1	Test Pattern Line Space Setting	03H
4DH	1	Test Pattern Foreground & Background Color Setting	07H
4E~FFH	178	Reserved	-

4.2 Detailed Information of Register

1) Revision information (Read Only)

Register Address	7	6	5	4	3	2	1	0
00H	N.A.					Revision		
Default	-					0	0	0

4.2.1 Video Related Registers

2) Input video type set

Register Address	7	6	5	4	3	2	1	0
01H	N.A.	Data Mode			Sync signal		Scan mode	
Default	-	0	1	1	0	1	0	0

- Signal Mode: Select input data format

Data Mode	Input Video Format
000	16-bit 422, YCbCr
001	24-bit 444, YcbCr
010	8-bit MONO
011	24-bit 444, RGB
100	8-bit 422, YcbCr

- Sync Signal: Select sync mode

Sync signal	Sync Mode
00	Embedded Sync
01	Embedded Sync
10	External Sync with DE
11	External Sync without DE

- Scan mode : Select scan mode

Interlaced	Interlaced mode
00	Non-interlaced
01	Interlaced
10	Do not use
11	Pseudo-Interlaced

3) V sync/H sync Polarity& 3D function Setting

Register Address	7	6	5	4	3	2	1	0
02H	Reserved		3D Enable	N.A		3D Refresh	V_Pol	H_Pol
Default	0	0	0	0	0	0	0	0

- 3D function control:

3D Enable	3D Refresh	3D Pin	Display Mode	Operating
0	X	X	Normal Mode	Refresh every Frame/Filed
1	0	0	3D Mode	Refresh
		1		Keep last data
	1	0		Keep last data
		1		Refresh

- V_Pol/H_Pol setting: Select Vsync & Hsync polarity

V_Pol/H_Pol	Polarity Choice
0	Active High
1	Active Low

4) Input video vertical blank lines

Register Address	7	6	5	4	3	2	1	0
03H	V Blank							
Default	0	0	0	0	0	0	0	0

5) Input video horizontal blank pixels

Register Address	7	6	5	4	3	2	1	0
04H	H Blank							
Default	0	0	0	0	0	0	0	0

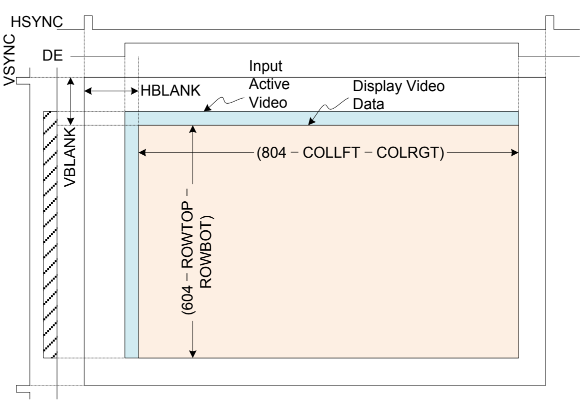


Figure 4-1 Vertical Blank Lines with DE

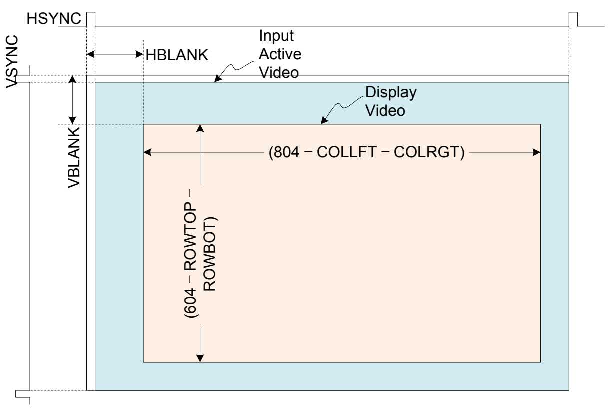


Figure 4-2 Vertical Blank Lines without DE

6) Adjust Start Active Video position

Register Address	7	6	5	4	3	2	1	0
05H	N.A.						SAV Offset	
Default	-						0	1

- SAV Offset : Adjust start active video (SAV) position

SAV Offset	Hsync position
00	1 pixel before input SAV
01	Same as input SAV
10	1 pixel after input SAV
11	2 pixel after input SAV

7) Field start line position adjust for Interlaced video

Register Address	7	6	5	4	3	2	1	0
06H	N.A.						V_offset	
Default	-						0	0

- V Offset : Adjust odd field active video start position when interlaced video mode

V Offset	Odd field start position
00	Same as Even field
01	1 line after Even field
10	Do not use
11	1 line before Even field

8) Down scaling for NTSC & PAL video

Register Address	7	6	5	4	3	2	1	0
07H	N.A.					V_Scale	H_Scale	
Default	-					0	0	0

- V Scale : Vertical 4/3downscale for PAL

V_Scale	Down scaling (In : Out)
0	1:1
1	6:5

- H Scale : Horizontal 4/3downscale for PAL/NTSC

H_Scale	Down scaling (In : Out)
00	1:1
01	11:10
10	9:8
11	Do not use

9) Brightness control

Register Address	7	6	5	4	3	2	1	0
08H	Video Signal Brightness							
Default	1	0	0	0	0	0	0	0

- $V_{out} = V_{in} + Reg(08H) - 128$ (Limit Low 8Bit Data)

Brightness	Brightness adjustment effect
00H	Darkest setting
80H	No change
FFH	Brightest setting

10) Contrast Enhance control

Register Address	7	6	5	4	3	2	1	0
09H	Video Signal Contrast							
Default	1	0	0	0	0	0	0	0

- $V_{out} = V_{in} \times Reg(09H) \div 128$ (Limit Low 8Bit Data)

Contrast	Contrast adjustment effect
00H	Gain =0 (Black Screen)
80H	Gain =1 (Normal)
FFH	Gain =2 (Contrast Double)

11) Reserved

Register Address	7	6	5	4	3	2	1	0
0AH	N.A.	Reserved						
Default	-	1	0	0	1	0	1	0

12) Reserved

Register Address	7	6	5	4	3	2	1	0
0BH	N.A.	Reserved						
Default	-	1	0	1	1	0	1	0

13) Power down

Register Address	7	6	5	4	3	2	1	0
0FH	PDOWN	N.A.		BSGENPD	RDACPD	RAMPPD	VCOMPD	TSENPD
Default	0	-		0	0	0	0	0

- PDOWN: All system power off
- BSGENPD: Discharge current generator power off
- RDACPD: DAC module power off
- RAMPPD: DAC Buffer module power off
- VCOMPD: Vcom power off
- TSENPD: Temperature sensor power off

4.2.2 Video Display Control Registers

14) Display off & Scan directions

Register Address	7	6	5	4	3	2	1	0
10H	N.A.					DispOff	VSCAN	HSCAN
Default	-					1	0	0

• DispOff	
0	Display ON
1	Display OFF

• VSCAN	
0	Top → Bottom
1	Bottom → Top

• HSCAN	
0	Left → Right
1	Right → Left

15) Display Left Margin

Register Address	7	6	5	4	3	2	1	0
11H	COLLFT							
Default	0	0	0	0	0	0	1	0

16) Display Right Margin

Register Address	7	6	5	4	3	2	1	0
12H	COLRGT							
Default	0	0	0	0	0	0	1	0

17) Display Top Margin

Register Address	7	6	5	4	3	2	1	0
13H	ROWTOP							
Default	0	0	0	0	0	0	1	0

18) Display Bottom Margin

Register Address	7	6	5	4	3	2	1	0
14H	ROWBOT							
Default	0	0	0	0	0	0	1	0

19) Reserved

Register Address	7	6	5	4	3	2	1	0
15H	Reserved							
Default	0	1	0	0	0	1	0	0

20) D/A Conversion Offset control

Register Address	7	6	5	4	3	2	1	0
16H	DAOFFSET							
Default	1	0	0	0	0	0	0	0

- DAOFFSET: Adjust D/A output offset

00H	Offset = -40%
80H	Offset = 0
FFH	Offset = +40%

Note: The Register setting affect the gamma correction curve, not recommended to change

21) Discharge Current Setting

Register Address	7	6	5	4	3	2	1	0
17H	NA		Reserved		NA		BIAS	
Default	-	-	0	0	-	-	0	1

- BIAS: OLED pixel discharge current setting. Can enhance the display dynamic contrast ratio, may result in reduced display brightness

BIAS	BIAS Current
00	0 nA (OFF)
01	0.5 nA
10	1nA
11	DO not use

22) Discharge Enable Control

Register Address	7	6	5	4	3	2	1	0
18H	N.A.							BIAS_En
Default	-							0

- BIAS_En: OLED pixel discharge function enable switch, "0" is Disable, "1" is Enable.

23) Vcom Level Setting(can't change)

Register Address	7	6	5	4	3	2	1	0
19H	Vcom							
Default	1	1	1	1	1	1	1	1

- *The valid range of Vcom setting is 20H ~ FFH, and the corresponding cathode voltage is about-3V ~ 0V. The lower cathode voltage makes the display brighter. The curve of Vcom and cathode voltage sees section 3.5 (DC / DC converter).*
- *Low Vcom settings will cause the display too bright, may damage the eyes of the user, and continues use may cause display overheating and damage.*

4.2.3 Temperature Sensor Register

24) Reserved

Register Address	7	6	5	4	3	2	1	0
1AH	Do not use		Reserved					
Default	-	-	0	1	1	1	0	1

25) Reserved

Register Address	7	6	5	4	3	2	1	0
1BH	Reserved							
Default	0	1	1	1	0	1	0	0

26) Reserved

Register Address	7	6	5	4	3	2	1	0
1CH	Reserved							
Default	1	1	1	1	1	1	1	1

27) Temperature Sensor Readout (Read Only)

Register Address	7	6	5	4	3	2	1	0
1DH	TEMP_OUT							
Default	-							

- Temperature conversion formula is : $T = 0.47 \times Reg\ (19H) - 40$

4.2.4 Gamma Look-Up Table Registers

28) 9 Bit Gamma Correction LUT0

Register Address	7	6	5	4	3	2	1	0
21H	N.A.							LUT0[8]
Default	-							0
20H	LUT0[7:0]							
Default	0	0	0	0	0	0	0	0

29) 9 Bit Gamma Correction LUT1

Register Address	7	6	5	4	3	2	1	0
23H	N.A.							LUT1[8]
Default	-							0
22H	LUT1[7:0]							
Default	0	0	1	0	0	0	0	0

30) 9 Bit Gamma Correction LUT2

Register Address	7	6	5	4	3	2	1	0
25H	N.A.							LUT2[8]
Default	-							0
24H	LUT2[7:0]							
Default	0	1	0	0	0	0	0	0

31) 9 Bit Gamma Correction LUT3

Register Address	7	6	5	4	3	2	1	0
27H	N.A.							LUT3[8]
Default	-							0
26H	LUT3[7:0]							
Default	0	1	1	0	0	0	0	0

32) 9 Bit Gamma Correction LUT4

Register Address	7	6	5	4	3	2	1	0
29H	N.A.							LUT4[8]
Default	-							0
28H	LUT4[7:0]							
Default	1	0	0	0	0	0	0	0

33) 9 Bit Gamma Correction LUT5

Register Address	7	6	5	4	3	2	1	0
2BH	N.A.							LUT5[8]
Default	-							0
2AH	LUT5[7:0]							
Default	1	0	1	0	0	0	0	0

34) 9 Bit Gamma Correction LUT6

Register Address	7	6	5	4	3	2	1	0
2DH	N.A.							LUT6[8]
Default	-							0
2CH	LUT6[7:0]							
Default	1	1	0	0	0	0	0	0

35) 9 Bit Gamma Correction LUT7

Register Address	7	6	5	4	3	2	1	0
2FH	N.A.							LUT7[8]
Default	-							0
2EH	LUT7[7:0]							
Default	1	1	1	0	0	0	0	0

36) 9 Bit Gamma Correction LUT8

Register Address	7	6	5	4	3	2	1	0
31H	N.A.							LUT8[8]
Default	-							1
30H	LUT8[7:0]							
Default	0	0	0	0	0	0	0	0

37) 9 Bit Gamma Correction LUT9

Register Address	7	6	5	4	3	2	1	0
33H	N.A.							LUT9[8]
Default	-							1
32H	LUT9[7:0]							
Default	0	0	1	0	0	0	0	0

38) 9 Bit Gamma Correction LUT10

Register Address	7	6	5	4	3	2	1	0
35H	N.A.							LUT10[8]
Default	-							1
34H	LUT10[7:0]							
Default	0	1	0	0	0	0	0	0

39) 9 Bit Gamma Correction LUT11

Register Address	7	6	5	4	3	2	1	0
37H	N.A.							LUT11[8]
Default	-							1
36H	LUT11[7:0]							
Default	0	1	1	0	0	0	0	0

40) 9 Bit Gamma Correction LUT12

Register Address	7	6	5	4	3	2	1	0
39H	N.A.							LUT12[8]
Default	-							1
38H	LUT12[7:0]							
Default	1	0	0	0	0	0	0	0

41) 9 Bit Gamma Correction LUT13

Register Address	7	6	5	4	3	2	1	0
3BH	N.A.							LUT13[8]
Default	-							1
3AH	LUT13[7:0]							
Default	1	0	1	0	0	0	0	0

42) 9 Bit Gamma Correction LUT14

Register Address	7	6	5	4	3	2	1	0
3DH	N.A.							LUT14[8]
Default	-							1
3CH	LUT14[7:0]							
Default	1	1	0	0	0	0	0	0

43) 9 Bit Gamma Correction LUT15

Register Address	7	6	5	4	3	2	1	0
3FH	N.A.							LUT15[8]
Default	-							1
3EH	LUT15[7:0]							
Default	1	1	1	0	0	0	0	0

44) 10 Bit Gamma Correction LUT16

Register Address	7	6	5	4	3	2	1	0
41H	N.A.						LUT16[9:8]	
Default	-						1	0
40H	LUT16[7:0]							
Default	0	0	0	0	0	0	0	0

4.2.5 Color Offset Control Registers

45) 9 Bit R offset control

Register Address	7	6	5	4	3	2	1	0
45H	N.A.							Roffset[8]
Default	-							1
44H	Roffset[7:0]							
Default	0	0	0	0	0	0	0	0

46) 9 Bit G offset control

Register Address	7	6	5	4	3	2	1	0
47H	N.A.							Goffset[8]
Default	-							1
46H	Goffset[7:0]							
Default	0	0	0	0	0	0	0	0

47) B offset control

Register Address	7	6	5	4	3	2	1	0
49H	N.A.							Boffset[8]
Default	-							1
48H	Boffset[7:0]							
Default	0	0	0	0	0	0	0	0

4.2.6 Test Pattern Generator Control Register

48) Select Test Pattern

Register Address	7	6	5	4	3	2	1	0
4AH	N.A.					PatternMode		
Default	-					0	0	0

- PatternMode: Select Test Pattern

Patterns	Test Pattern
000	Pattern Generator Off (Normal)
001	Color Bar
010	Gray Scale
011	Tile
100	Vertical Lines
101	Horizontal Lines
110	Ver. & Hor. Lines
111	Do not use

49) Set line width for lines pattern (Patterns = 100 ~110)

Register Address	7	6	5	4	3	2	1	0
4BH	LineWidth							
Default	0	0	0	0	0	0	1	0

50) Set line space for line pattern (Patterns = 100 ~ 110)

Register Address	7	6	5	4	3	2	1	0
4CH	LineSpace							
Default	0	0	0	0	0	0	1	1

51) Set Foreground & Background RGB color for lines pattern (Patterns = 100 ~ 110)

Register Address	7	6	5	4	3	2	1	0
4BH	N.A.	BGCOLOR			N.A.	FGCOLOR		
Default	-	0	0	0	-	1	1	1

- BGCOLOR : Background color

BGCOLOR	Color
000	Black
001	Blue
010	Green
100	Red
111	White

- FGCOLOR : Foreground color

FGCOLOR	Color
000	Black
001	Blue
010	Green
100	Red
111	White

4.3 Register Setting Example

Table 4-2 Register Setting Example

Video Mode				Register Setting					
Mode	**Scan**	**Input**	**Display**	**Reg(01H)**	**Reg(07H)**	**Reg(11h)**	**Reg(12H)**	**Reg(13H)**	**Reg(14H)**
SVGA	Progressive	800×600	800×600	3CH	00H	02H	02H	02H	02H
VGA	Progressive	640×480	640×480	3CH	00H	52H	52H	52H	3EH
SMPTE-170M-1	Interlaced	640×480	640×480	21H	00H	52H	52H	52H	3EH
SMPTE-170M-2	Interlaced	800×600	800×600	3DH	00H	02H	02H	02H	02H
NTSC	Interlaced	720×480	640×480	41H	04H	52H	52H	52H	3EH
PAL	Interlaced	720×480	640×480	41H	05H	52H	52H	52H	3EH
NTSC (SQ)	Interlaced	640×480	640×480	41H	00H	52H	52H	52H	3EH
PAL (SQ)	Interlaced	768×676	768×576	41H	00H	12H	12H	14H	0EH

5 PHOTOELECTRONIC PROPERTIES

5.1 Test Conditions

In this Datasheet, unless special notes, the test circuit is shown in Figure 5-1. The display is working on the built-in test pattern mode, and typical test conditions and test pattern mode is shown as follows:

- Temperature: 23℃±2℃
- Humidity: (40±10)%RH
- Power: V5.0=5.0V, V1.8=1.8V
- VCLK: 40MHz
- Display Resolution: 804×604
- Display ON: Reg(10H) = 0
- Typical Vcom: Reg(19H) = 80H
- White or Green Test Pattern for Monochrome Display:
  Reg(4AH) = 04H, Reg(4DH) = 77H
- W/R/G/B Test Pattern for Monochrome Display:
  Reg(4AH)=04, Reg(4DH) = 77H/44H/22H/11H
- Black Test Pattern:
  Reg(4AH) = 04H, Reg(4DH) = 00H
- Other Registers Setting: Default value

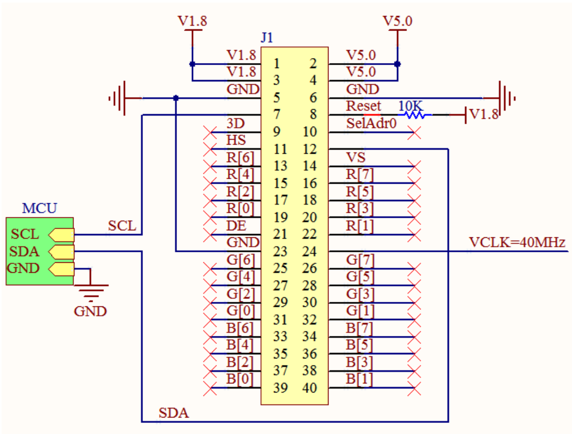


Figure 5-1 Test Circuit Schematic

5.1.1 Luminance & Chromaticity Test Conditions

Use photometer to measure the center of display's luminance (Cd/m^2) and chromatic coordinates (CIEx, CIEy). The test diagram shown in Figure 5-2.

5.1.2 Uniformity Test Conditions

All pixels fully on and adjust register 19H to make the luminance is about $100Cd/m^2$, acquire the actually luminance of P0 to P4 shown in Figure 5-3, and then calculate the uniformity by the follow formula:

$$\text{Uniformity} = 1 - \frac{L_{max} - L_{min}}{L_{average}} \times 100\%$$

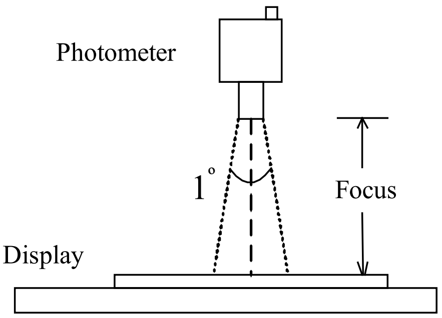


Figure 5-2 Photometer Test Diagram

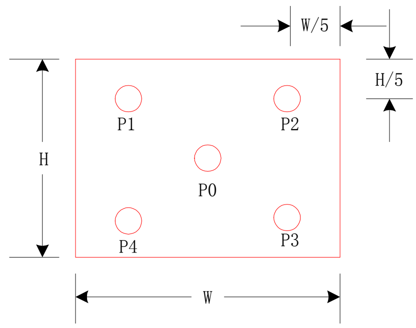


Figure 5-3 Uniformity Test Diagram

5.1.3 Contrast Test Conditions

All pixels fully on and adjust register 19H to make the luminance is about $100Cd/m^2$ as L_{255}, then change the display working on the all pixels full off (black mode), acquire the luminance as L_0. Calculate the contrast by the follow formula:

$$\text{Contrast} = \frac{L_{255}}{L_0}$$

5.1.4 Power Consumption Test Conditions

All pixels fully on and adjust register 19H to make the luminance respectively 70Cd/m^2, 100 Cd/m^2 and 1500 Cd/m^2 for color, Monochrome white, Monochrome green display, acquired the voltage and current for each power supply, then calculate the power consumption by the follow formula:

$$P = V_{5.0} \times I_{5.0} + V_{1.8} \times I_{1.8}$$

5.2 Photics Properties

Table 5-1 Photics Properties

<table>
<tr><th colspan="4">Item</th><th colspan="2">Remark</th><th>Minimum Value</th><th>Typical Value</th><th>Maximum value</th></tr>
<tr><td colspan="4">Contrast Ratio</td><td colspan="2">Highest gray: Minimum gray</td><td>10000:1</td><td>-</td><td>-</td></tr>
<tr><td colspan="2" rowspan="3">Luminance</td><td colspan="2">Full Color</td><td colspan="2" rowspan="3">Using Built-in test pattern under typical test conditions and all pixels are fully on</td><td>0</td><td>70</td><td>800</td></tr>
<tr><td colspan="2">Monochrome White</td><td>0</td><td>100</td><td>2600</td></tr>
<tr><td colspan="2">Monochrome Green</td><td>0</td><td>1500</td><td>9000</td></tr>
<tr><td colspan="4">luminance uniformity</td><td colspan="2">The average of five test points</td><td>90</td><td>95</td><td>100</td></tr>
<tr><td rowspan="12">Chromaticity</td><td rowspan="8">Full Color</td><td rowspan="2">White</td><td>CIEX</td><td rowspan="2">all pixels are fully on</td><td rowspan="12">Using Built-in test pattern under typical test conditions and all pixels are fully on.</td><td>0.25</td><td>0.30</td><td>0.35</td></tr>
<tr><td>CIEY</td><td>0.30</td><td>0.35</td><td>0.40</td></tr>
<tr><td rowspan="2">Red</td><td>CIEX</td><td rowspan="2">all red are sub-pixels fully on</td><td>0.48</td><td>0.61</td><td>0.66</td></tr>
<tr><td>CIEY</td><td>0.32</td><td>0.34</td><td>0.37</td></tr>
<tr><td rowspan="2">Green</td><td>CIEX</td><td rowspan="2">all green are sub-pixels fully on</td><td>0.15</td><td>0.25</td><td>0.30</td></tr>
<tr><td>CIEY</td><td>0.48</td><td>0.53</td><td>0.58</td></tr>
<tr><td rowspan="2">Blue</td><td>CIEX</td><td rowspan="2">all blue are sub-pixels are on</td><td>0.10</td><td>0.13</td><td>0.18</td></tr>
<tr><td>CIEY</td><td>0.13</td><td>0.16</td><td>0.19</td></tr>
<tr><td rowspan="2">Monochrome White</td><td rowspan="2">White</td><td>CIEX</td><td rowspan="2">all pixels are fully on</td><td>0.25</td><td>0.30</td><td>0.35</td></tr>
<tr><td>CIEY</td><td>0.28</td><td>0.33</td><td>0.38</td></tr>
<tr><td rowspan="2">Monochrome Green</td><td rowspan="2">Green</td><td>CIEX</td><td rowspan="2">all pixels are fully on</td><td>0.25</td><td>0.30</td><td>0.35</td></tr>
<tr><td>CIEY</td><td>0.58</td><td>0.63</td><td>0.68</td></tr>
</table>

5.3 Brightness and Contrast Properties

5.3.1 Brightness

The OLED's luminance is depending on the bias voltage and current, increasing the bias voltage can obtain the higher brightness. With OLiGHTEK's proprietary active matrix driver technology, SVGA060 series microdisplay has two kinds of method for brightness adjustment.

1) Through the input video signal control the anode voltage, realizing each pixel brightness control. The video signal can enhancement by change the value of register 08H and 09H.

2) Adjusting the common cathode voltage, while achieving all pixel brightness adjustment. The cathode negative voltage adjustments by change the value of register 19H.

5.3.2 Contrast

OLED's quickly response and self-emitting characteristics make it has excellent contrast features. But the leakage current will causing the contrast decreased when using a higher bias voltage. The SVGA060 series display's contrast property is shown in Figure 5-4, Figure 5-5 and Figure 5-6.

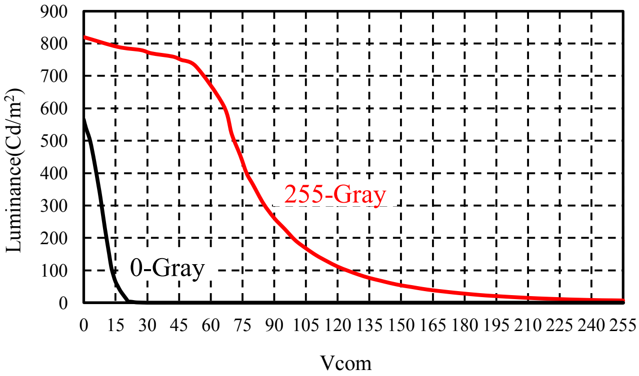


Figure 5-4 Full Color Display

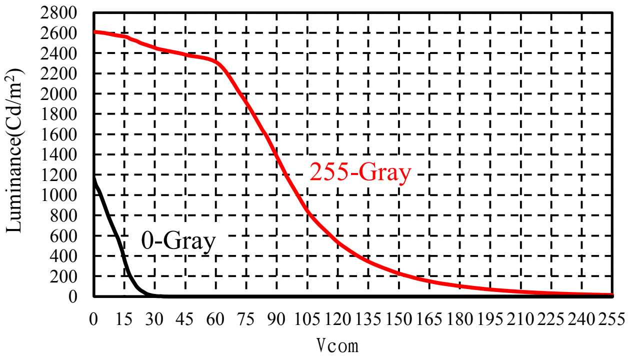


Figure 5-5 Monochrome White Display

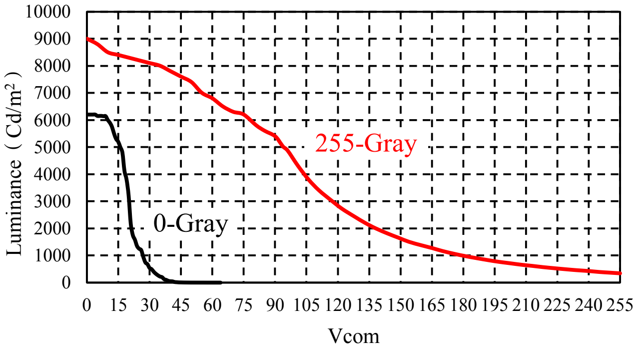
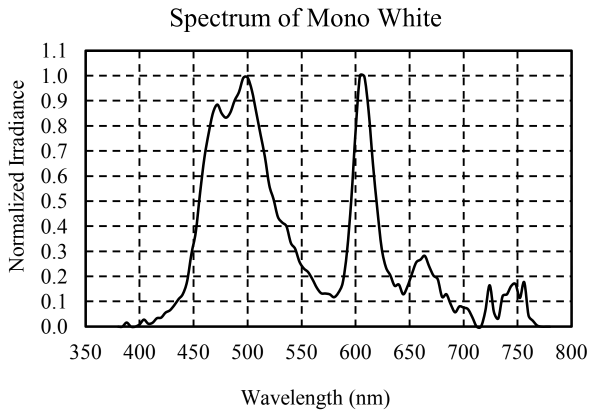
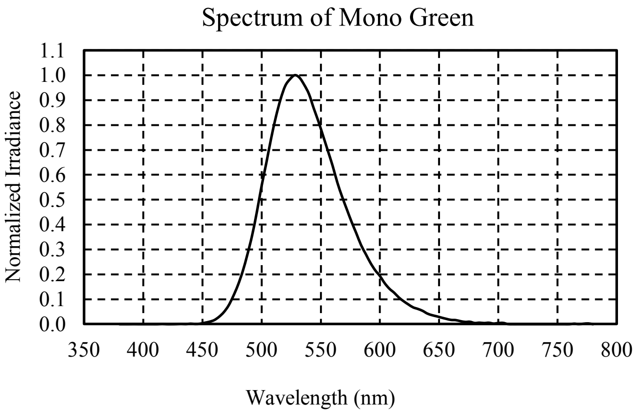
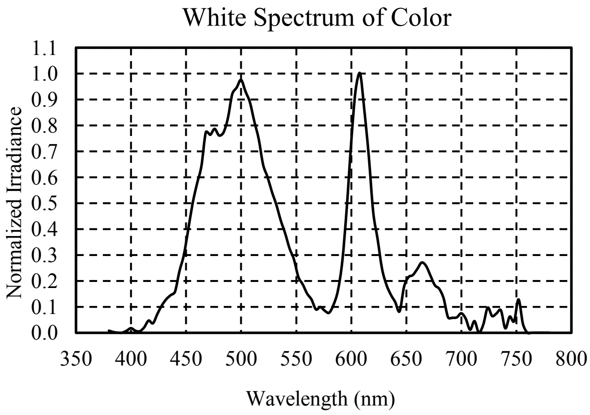


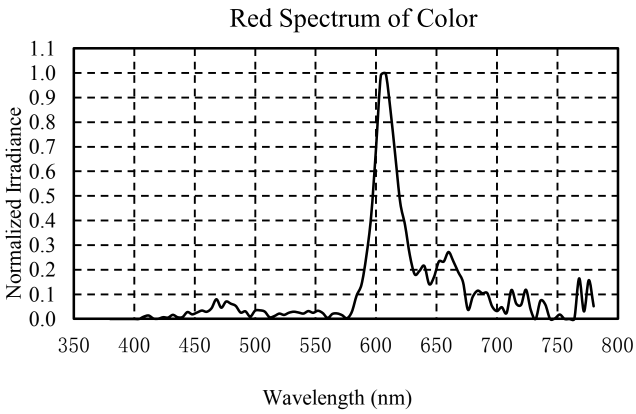
Figure 5-6 Monochrome Green Display

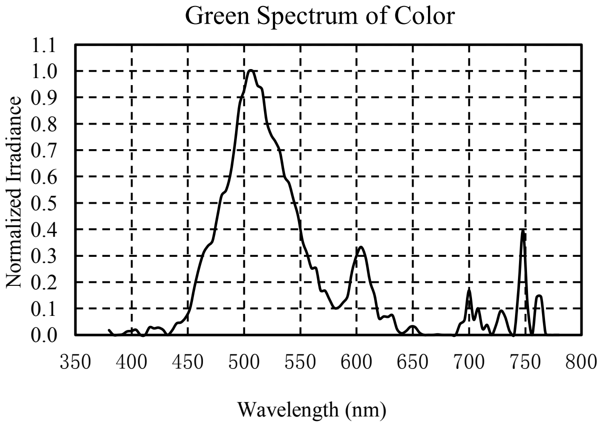
5.4 Spectrum Properties

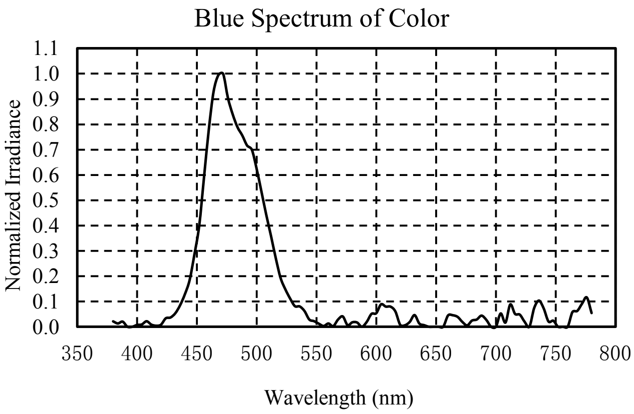












5.5 Luminance Characteristic with Temperature

Test conditions: V5=5.0V, V1.8=1.8V, All White Pattern, Reg(19H)=80H, VCLK=40MHz

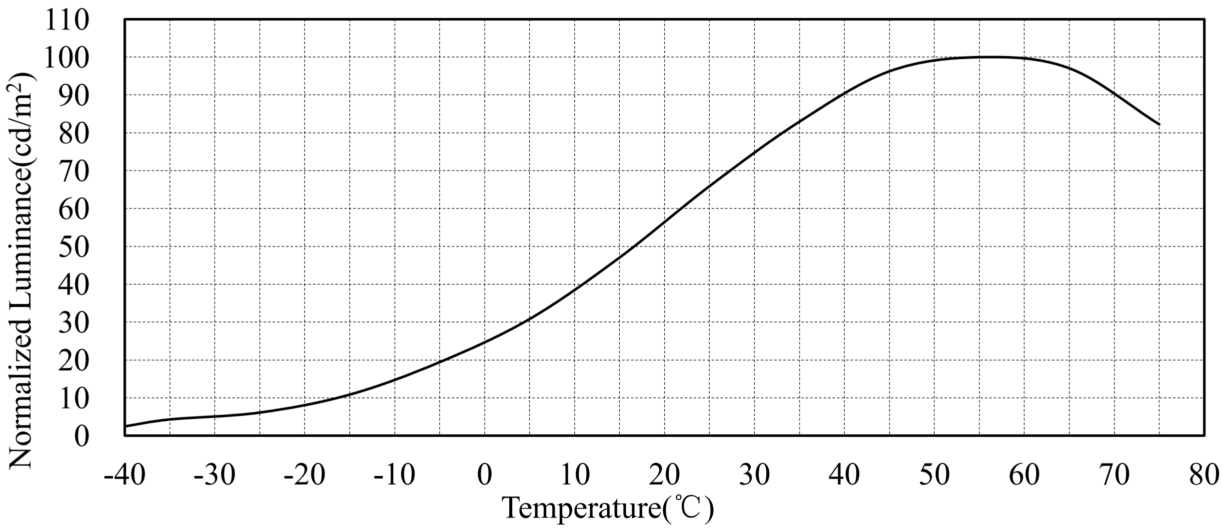


Figure 5-7 SVGA060 Luminance characteristic curve with temperature

5.6 Power Consumption Characteristic with Luminance

Test conditions: T=23℃±2℃, V5=5.0V, V1.8=1.8V, All White Pattern, VCLK=40MHz

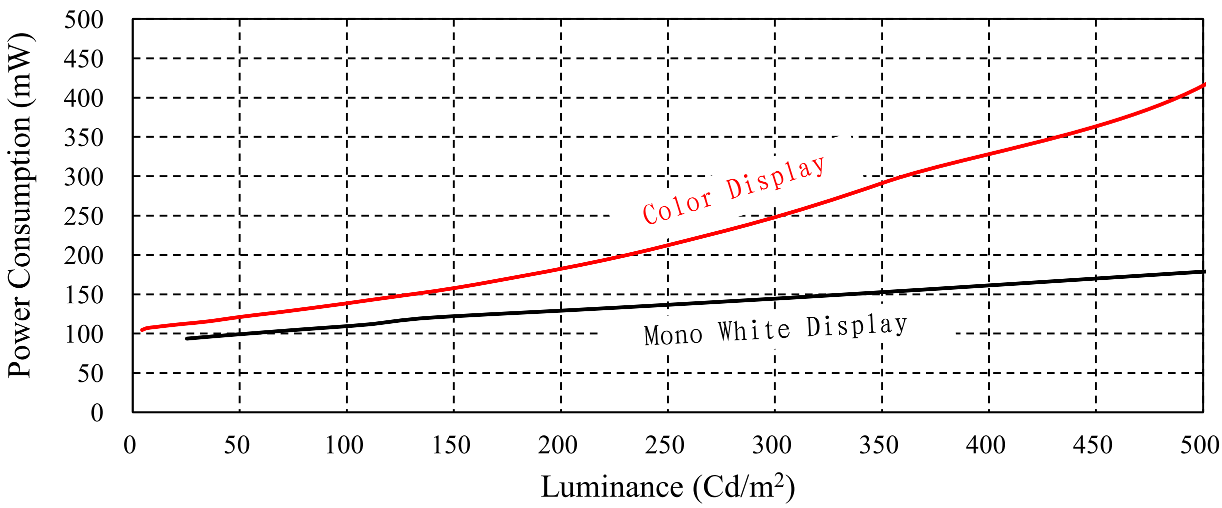
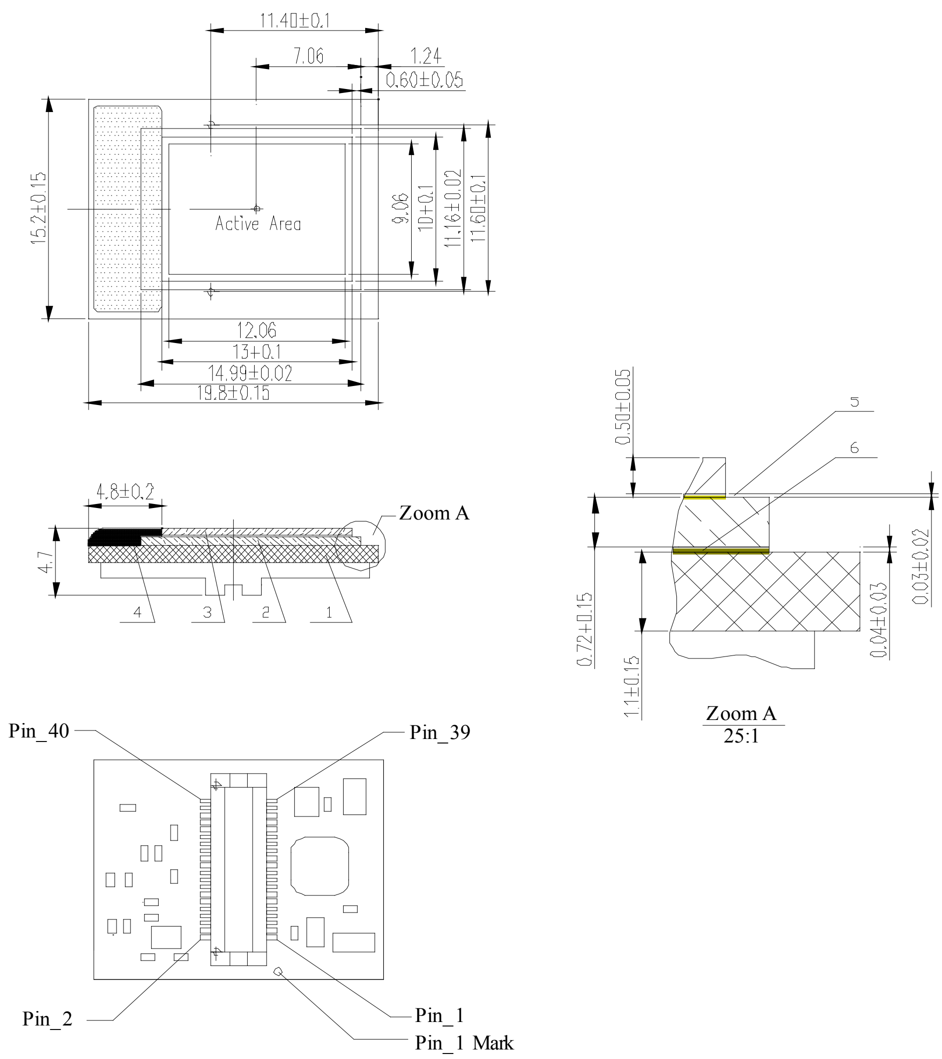


Figure 5-8 SVGA060 Power consumption characteristic with luminance

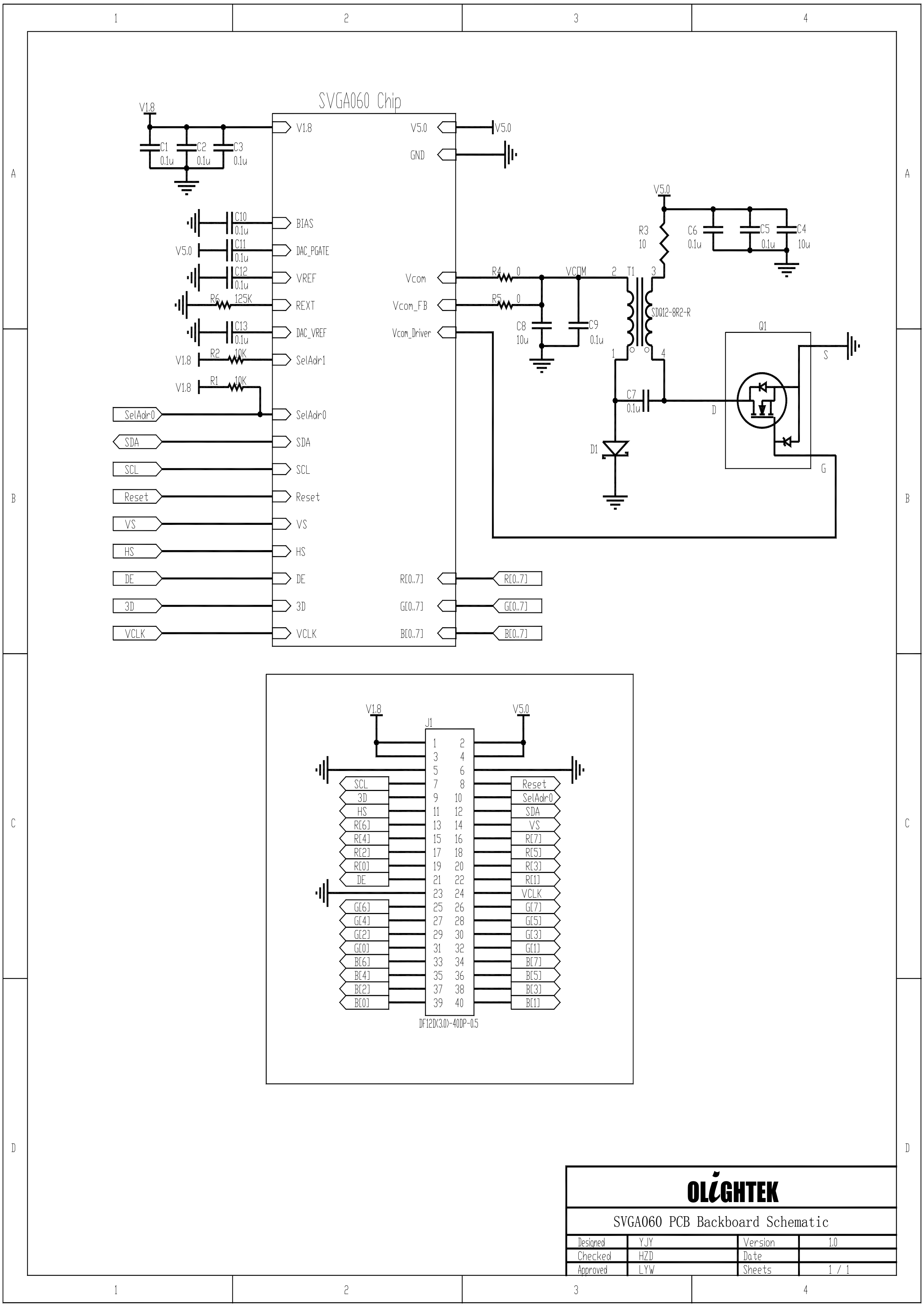
6 MECHANICAL CHARACTERISTICS

6.1 Mechanical Drawing

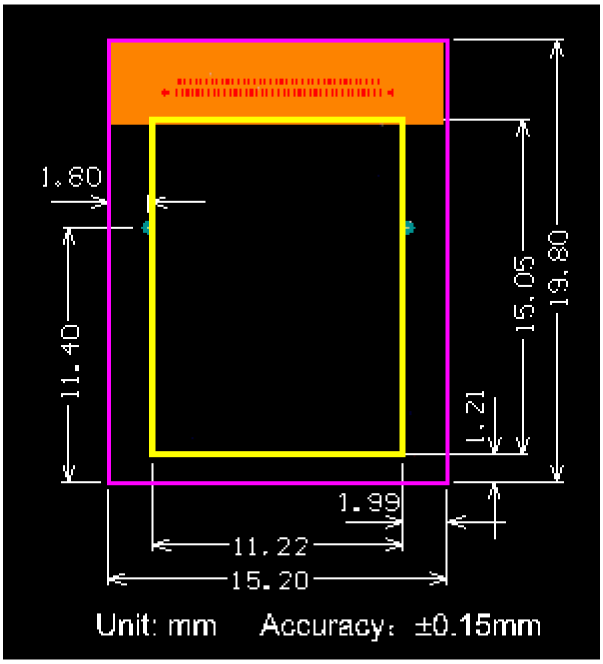


6	Adhesive	Scale	OLiGHTEK			
5	OLED Layer & Adhesive	2.5:1				
4	Wirebond Encapsulant		Title	SVGA060 Assembly Drawing		
3	Glass Cover					
2	Si Substrate		Designed	ZHQ	Version	V1.0
1	PCB Backboard		Checked	YXH	Date	
Item	Name		Approved	LYW	Sheets	1 / 1

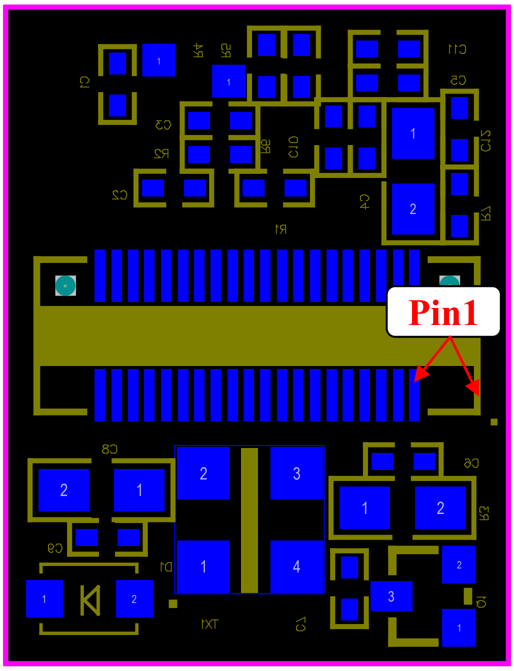
6.2 PCB Backboard Schematic



6.3 PCB Backboard Layout



PCB Top Layer



Bottom Layer (Perspective)

6.4 Assembly Bill of Materials

Item	Name	Reference	Qty	Description	Coding	Manufacturer
1	CAP	C1,C2,C3,C5,C6,C7 C9,C10,C11,C12,R7	11	Cap, 0.1μF/25V,X5R,10%,0402	TMK105BJ104KV-T	TAIYO YUDEN
2	CAP	C4,C8	2	Cap, 10μF/16V,X5R,10%,0805	EMK212BJ106KG-T	TAIYO YUDEN
3	Diode	D1	1	Diode, Schottky, 30V, 1.5A, SOD123F	PMEG3015EH	PHILIPS
4	Connector	Con1	1	Con, 40Pin, 0.5mm, Header	DF12D(3.0)-40DP-0.5(81)	Hirose
5	nFET	Q1	1	nFET, 25V/0.22A, SOT-23	FDV301N	Fairchild
6	Resistance	R2,R1	2	Resistor,10K,5%,1/16W,0402	RC0402JR-0710KL	YAGEO
7	Resistance	R3	1	Resistor,10Ω,5%,1/4W,0805	RC0805JR-0710RL	YAGEO
8	Resistance	R4,R5	2	Resistor,0Ω,5%,1/16W,0402	RC0402JR-070RL	YAGEO
9	Resistance	R6	1	Resistor,127K,1%,1/16W,0402	RC0402FR-07127KL	YAGEO
10	Transformer	TX1	1	Transformer, 6.8μH/0.6A, 1:1	LPD4012-682ML	Coilcraft

7 PRODUCTS CLEANING, HANDLING AND STORAGE

7.1 Cleaning

- Avoid using any acid, alkali and organic solvent to clean or contact to the display
- Using the lens paper or clean cloth to clean the surface is recommend

7.2 General Handling Considerations

- Do not expose the display to strong acids, alkalis, or solvents.
- Do not expose the display surface to UV or other strong ionizing radiation.
- Do not using sharp objects to contact the glass and silicon regions of display.
- Avoid applying force to the any region except the PCB backplane, especially apply the force to the region of sealing, silicon edge and cover glass is not allowed.
- Avoid immersion of the display in any liquid.
- Handing with PVC clean gloves is recommended.

7.3 Static Charge Prevention

The microdisplay is sensitive to electro-static discharge due to integrated CMOS circuit in the display. The following measures are recommended to minimize ESD occurrences:

- Operate on a region which is equipped with electro-static eliminator, such as ionizing air blowers.
- Wear the anti-static wrist strap
- wear the non-chargeable clothes
- Keep away from charged region.

Figure 7-1 Handing the Display

7.4 Storage

7.4.1 Short Term Storage

The display should be stored in a dry environment with temperature range from -50℃ to 90℃ for a short period(≤100hrs).

7.4.2 Long Term Storage

If the display is stored in such an environment with excessive heat or cold or moisture, the lifetime of display will be shorten, even the environment can cause permanent damage to the display. Recommended long-term storage condition as follows:

- Room temperature: 25℃±5℃
- Dry environment: dry nitrogen or vacuum sealing cabinet
- Static placing: avoid violent vibration

8 APPLICATIONS

8.1 Status test

SVGA060 series microdisplay need the following condition before it can work:

1) 5V and 1.8Vpower supply
2) VCLK signal (more than 25MHz is recommended)
3) The input of reset pin pull up to V1.8 via 10K resistance
4) Set DispOff bit of register 10H to 0
5) Set the value of register 19H is close to 128

At any time, after make sure the above conditions, set the value of register 4AH to 01H/02H/03H, the built-in pattern can be displayed without any video input. Through this way, the product status can be verified. The test circuit schematic is shown in Figure 5-1.

8.2 Temperature Compensation

8.2.1 Compensation Principle

The OLED's emitting relies on the mobility and recombination of charge carrier, but the mobility of charge carrier is affected by temperature, so the luminance of OLED microdisplay is also affected by temperature. As shown in Figure 8-1 the luminance of OLED microdisplay increased with the temperature increasing, and the luminance begin to decrease after the temperature hotter than 60℃. In order to achieve stable luminance within a wide temperature range, OLED drive voltage compensation is required.

SVGA060 series microdisplay uses a common cathode structure and the cathode voltage is programmable, besides it also integrated a readable temperature sensor. So the closed-loop control of automatic luminance compensation can be achieved by an external Microcontroller (MCU). The software flow chart is shown in Figure 8-2.

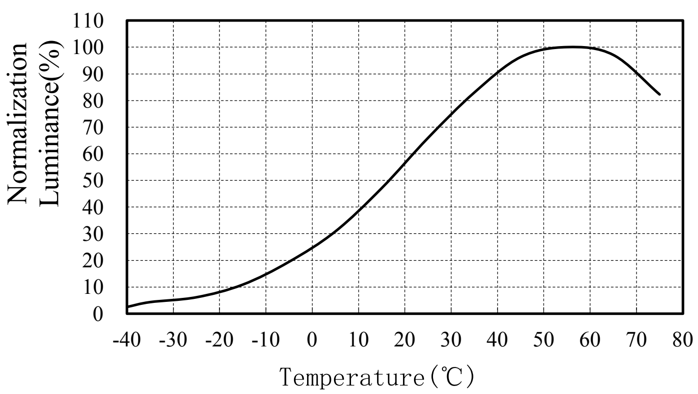


Figure 8-1 Typical Luminance-Temp. Curve

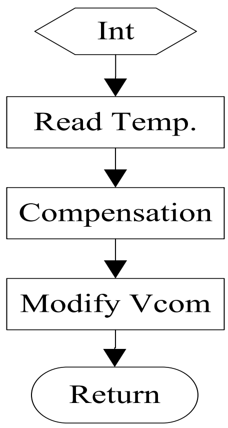


Figure 8-2 Compensation flow chart

8.2.2 Compensation Look-Up Table

In the Table 8-1, for the convenience of 8-bit MCU calculation, the coefficient is changed from 0.47 to 0.5 and the formula is simplified as follows:

$$T = 0.5 \times \mathrm{Reg(1DH)} - 40$$

Table_Index can be calculated by the temperature T+40, i.e.

$$\mathrm{Table\_Index} = 0.5 \times \mathrm{Reg(1DH)}$$

The new value after compensation is equal to the △Reg(19H) which from the look up table plus the default value of register 19H at room temperature.

$$\mathrm{Reg\ (19H)\_New} = \mathrm{Reg(19H)\_Default} + \Delta\mathrm{Reg(19H)}$$

Notice: ● ***Limit the minimum value of register 19H not less than 20H***

- ***The compensation value is corrected based on the luminance of default value (Reg(19H)_Default) at room temperature (20~25 ℃)***
- ***Auto luminance compensation is in conflict with manual adjust luminance (modify the Vcom value), so, avoid Vcom adjusted by the other way is required.***

Table 8-1 Luminance-Temperature compensation Look-up Table

Temp.	Index	ΔReg(19H)	Temp.	Index	ΔReg(19H)	Temp.	Index	ΔReg(19H)
-40	0	-87	1	41	-44	41	81	6
-39	1	-86	2	42	-43	42	82	8
-38	2	-85	3	43	-42	43	83	9
-37	3	-84	4	44	-41	44	84	10
-36	4	-83	5	45	-40	45	85	11
-35	5	-82	6	46	-39	46	86	12
-34	6	-82	7	47	-38	47	87	13
-33	7	-81	8	48	-37	48	88	14
-32	8	-80	9	49	-35	49	89	15
-31	9	-79	10	50	-34	50	90	16
-30	10	-78	11	51	-32	51	91	17
-29	11	-77	12	52	-30	52	92	18
-28	12	-76	13	53	-28	53	93	19
-27	13	-75	14	54	-27	54	94	20
-26	14	-74	15	55	-26	55	95	21
-25	15	-73	16	56	-25	56	96	22
-24	16	-72	17	57	-24	57	97	23
-23	17	-71	18	58	-23	58	98	24
-22	18	-69	19	59	-21	59	99	26
-21	19	-68	20	60	-20	60	100	27
-20	20	-67	21	61	-19	61	101	28
-19	21	-66	22	62	-18	62	102	29
-18	22	-65	23	63	-17	63	103	30
-17	23	-64	24	64	-16	64	104	31
-16	24	-62	25	65	-15	65	105	32
-15	25	-61	26	66	-14	66	106	33
-14	26	-60	27	67	-13	67	107	34
-13	27	-59	28	68	-11	68	108	35
-12	28	-58	29	69	-10	69	109	35
-11	29	-57	30	70	-8	70	110	36
-10	30	-56	31	71	-6	71	111	37
-9	31	-55	32	72	-5	72	112	38
-8	32	-54	33	73	-4	73	113	39
-7	33	-53	34	74	-3	74	114	40
-6	34	-52	35	75	-2	75	115	40
-5	35	-51	36	76	-1	76	116	41
-4	36	-51	37	77	0	77	117	41
-3	37	-50	38	78	0	78	118	42
-2	38	-49	39	79	2	79	119	43
-1	39	-47	40	80	4	80	120	44
0	40	-46						

8.3 Gamma Correction

8.3.1 Gamma Correction Principle

The typical luminance gamma curves at γ=1 and γ=2.2 are shown in Figure 8-3, and the theory of gamma correction is base on the following formula

$$L_i = (\frac{i}{255})^{\gamma} \cdot L_{max}$$

i: is the grey level number (0-255)
L_{max}: is the luminance of the maximum grey level (255)
L_i: is the output luminance of the *i* gray level after gamma correction
γ: is gamma correction coefficient.

SVGA060 use voltage drive architecture and the luminance with drive voltage of OLED are non-linear. For this reason, the default gamma correction LUT setting is not good for display. Figure 8-4 shows the default gamma properties of SVGA060.

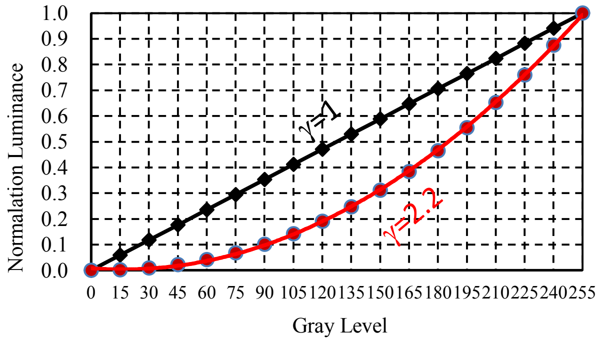


Figure 8-3 Typical Gamma Correction Curve

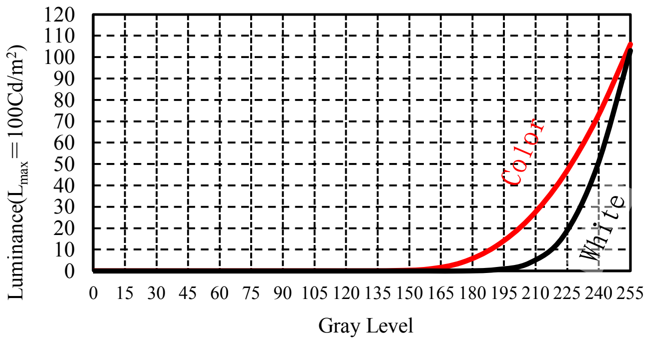


Figure 8-4 Default Gamma Properties of SVGA060

8.3.2 Gamma Correction process

For SVGA060 series microdisplay, the method for gamma correction is shown as below.

1) Adjust the luminance of display and fix the setting of register 19H when the luminance meets the using requirements, then acquired the luminance as L_{max} by using photometer.
2) Set LUT[16] = 200H (default).
3) Divide the Gray level 0-255 into 16 sections: Gn=16n (n=0 to 15)
4) Confirm the gamma coefficient γ, and calculate the values of Ln: $L_n = (\frac{G_n}{256})^{\gamma} \cdot L_{max}$
5) From n=0 to 15, input the video signal with gray level is Gn, then adjust the value of LUT[n] to make the luminance to reach or equal L_n.

The reference gamma LUT setting of γ=2.2 is shown in Table 8-2 and the gray scale display effect after correction shown in Figure 8-5.

Table 8-2 Reference Gamma LUT Setting with γ=2.2 and L_{max}=100Cd/m^2

Gamma LUT	Monochrome Display		Color Display	
	Dec Value	Hex Value	Dec Value	Hex Value
LUT[0]	0	0H	0	0H
LUT[1]	391	187H	320	140H
LUT[2]	394	18AH	328	148H
LUT[3]	403	193H	343	157H
LUT[4]	414	19EH	359	167H
LUT[5]	424	1A8H	372	174H
LUT[6]	433	1B1H	385	181H
LUT[7]	441	1B9H	399	18FH
LUT[8]	448	1C0H	410	19AH
LUT[9]	456	1C8H	423	1A7H
LUT[10]	462	1CEH	435	1B3H
LUT[11]	469	1D5H	447	1BFH
LUT[12]	475	1DBH	459	1CBH
LUT[13]	482	1E2H	470	1D6H
LUT[14]	488	1E8H	480	1E0H
LUT[15]	494	1EEH	490	1EAH
LUT[16]	512	200H	512	200H

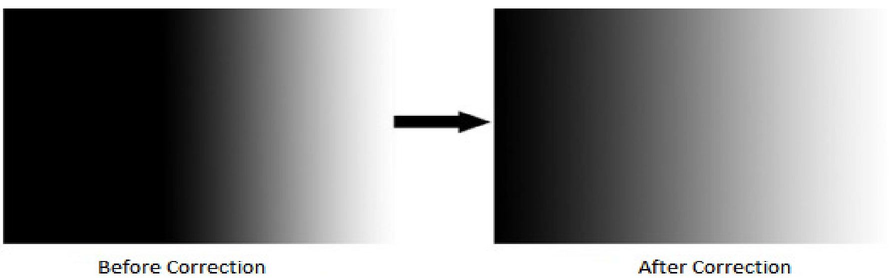


Figure 8-5 Gray Scale Display Effect with Gamma Correction

8.4 Ghost Effect

Just like other emitting device, lifetime degradation is also a problem for the OLED display. The high-brightness pixels lifetime decay faster than the low-brightness pixels. When display a static image with high-brightness and high-contrast for long time, the high-brightness area become darkness compare with the low-brightness area when display an image with same brightness. That's called negative ghost effect and shown in Figure 8-6.

Under the typical status: maximum luminance less than 200Cd/m^2, continually display a static image for 30-60 minutes, SVGA060 series microdisplay will appear the slight ghost effect. Longer time continually display will cause serious ghost effect.

Figure 8-6 Ghost Effect Demo

8.4.1 Avoid Ghost

- Avoid displaying static image for a long time; limit display less than 10 minutes if necessary
- Avoid displaying the characters or menu with high gray level in a fix position for a long time or repeatedly. If necessary, using the half gray level and auto fadeout technology.
- Avoid display operation under high luminance condition.

8.4.2 Clear Ghost

Serious ghost will causing the unrecoverable trace to display, such as burns.

After the slight ghost generated, using the built-in test pattern to make the display operating under full white mode, then, increase luminance properly, after a few minutes, the ghost will be eliminated.

8.5 Application Examples

8.5.1 Digital System Application

SVGA060 series microdisplay use full digital video process architecture, for simplifying system structure and increasing system flexibility, the application system use digital system in the front-end is recommended, such as FPGA, DSP, and SOC etc. So the A/D and D/A unit can take out and transferring the digital video signal to the display directly. Application system diagram is shown in Figure 8-8.

8.5.2 Composite Video

SVGA060 series microdisplay use square pixel layout and the screen's aspect ratio is 4:3. The decoders which support square mode are recommended when using the composite video input. For instance, ADV7180, it supports 768×576 output of PAL format, so it can be taken full advantage of full screen display resolution of 804×604. Application system diagram is shown in Figure 8-8.

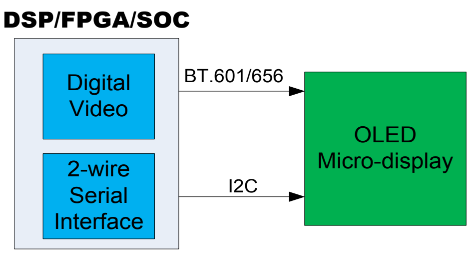


Figure 8-7 Digital System Application

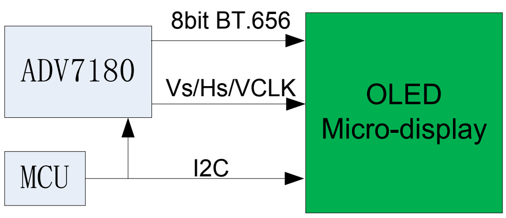


Figure 8-8 Composite Video Application

8.5.3 Analog RGB (VGA)

AD9883/9985 decoder chips can be used for VGA video input (analog RGB signal) and 800×600/85Hz resolution is recommended. The application system diagram is shown in Figure 8-9 .

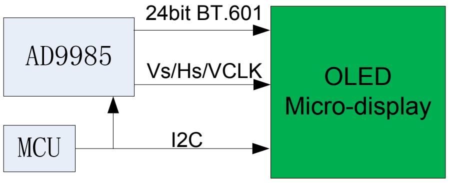


Figure 8-9 VGA Input Application

9 APPENDIX

9.1 List of Figures

9.2 List of Tables