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MICROIR™

ELECTRICAL INTERFACE CONTROL DOCUMENT

TWV640
UNCOOLED 12 µm (MICRON) THERMAL IMAGER

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Revision History

REV	DATE	COMMENT
-	10/27/2015	Initial release per ECO EOB57783
A	06/08/2016	Revised IAW ECO EOB67860
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Abbreviations and Acronyms

Abbreviation	Description	Abbreviation	Description
A	Amp(s)	NA	Not applicable
ADC	Analog to Digital Converter	NETD	Noise equivalent temperature difference
°C	Celsius	NTSC	National Television System Committee
DAC	Digital to Analog Converter	O	Output
DC	Direct current	OEM	Original equipment manufacturer
FFE	Focal plane front end board	PAL	Phase alternating line
FPA	Focal plane array	PWR	Power
GND	Ground	ROI	Region of interest
GPIO	General purpose input and output	UART	Universal asynchronous receiver/transmit.
DGND	Digital ground return path	A_GND	Analog ground return path
HSYNC	Horizontal sync	USB	Universal serial bus
I	Input	USB HS	Universal Serial Bus 2.0 “High-speed"
I/O	Input and output	V	Volt(s)
ICD	Interface control document	VSYNC	Vertical sync
IR	Infrared	W	Watt(s)
LWIR	Long wave infrared	SFE	Smart Front End

Reference Documentation

This document describes the electrical and timing interfaces only; the following documents further describe the camera cores and all other information needed to use the camera in a system.

Document No: 8507493 MicroIR™ Mechanical ICD: Camera Core

Document No: 8498820 MicroIR™ Software ICD

External documents and references listed below.

S600458002-00	Nanomotion RS08™ rotary shutter
ITU-R BT.601-7	Recommendation ITU-R BT.601-7
ITU-R BT.656-5	Recommendation ITU-R BT.656-5
D01-500649-05	VGA 640 X 480 LOW POWER COLOR XL AMOLED MICRODISPLAY

1. Product description

The MicroIR™ family of uncooled thermal cameras provide advanced imaging capabilities in the 7.5µm - 13.5µm, long wave infrared (LWIR) spectral band while remaining affordable, compact and low power. The TWV640 features a 640x480 pixel array with a 12µm pixel. The BAE Systems fabricated array enables superior sensitivity to dynamic scenes at all frame rates. The TWV640 is available in four configurations: the Base configuration, the Core configuration, the Smart Front End configuration and the Product Evaluation Kit. An overview of each configuration is described in this document. A standalone sensor configuration is also available, but does not fall into the scope of this document. For more information regarding a sensor only solution please contact BAE Systems directly. Figure 1-1 shows an example of an IR image using a thermal sensor.

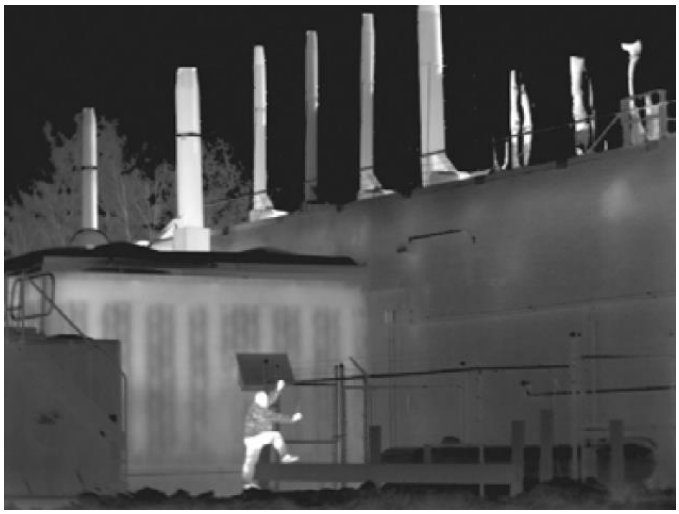

Figure 1-1: An example IR image

The Output Peripheral Summary shown in Table 1-1 presents the four different configurations with a summary of available video outputs. Additional functionality and technical details are discussed in later sections of this document.

Table 1-1: Configuration video format summary

Output Peripheral Summary						
Peripheral	NTSC/PAL	eMagin 10-bit Mono	8-BIT YCbCr	8-BIT YCbCr (BT.656)	USB video	16-Bit Parallel Digital Video
Smart Front End		x	x	x	x	x
Base Configuration		x	x	x	x	x
Core Configuration	x	x	x	x	x	x
Product Evaluation Kit	x				x	

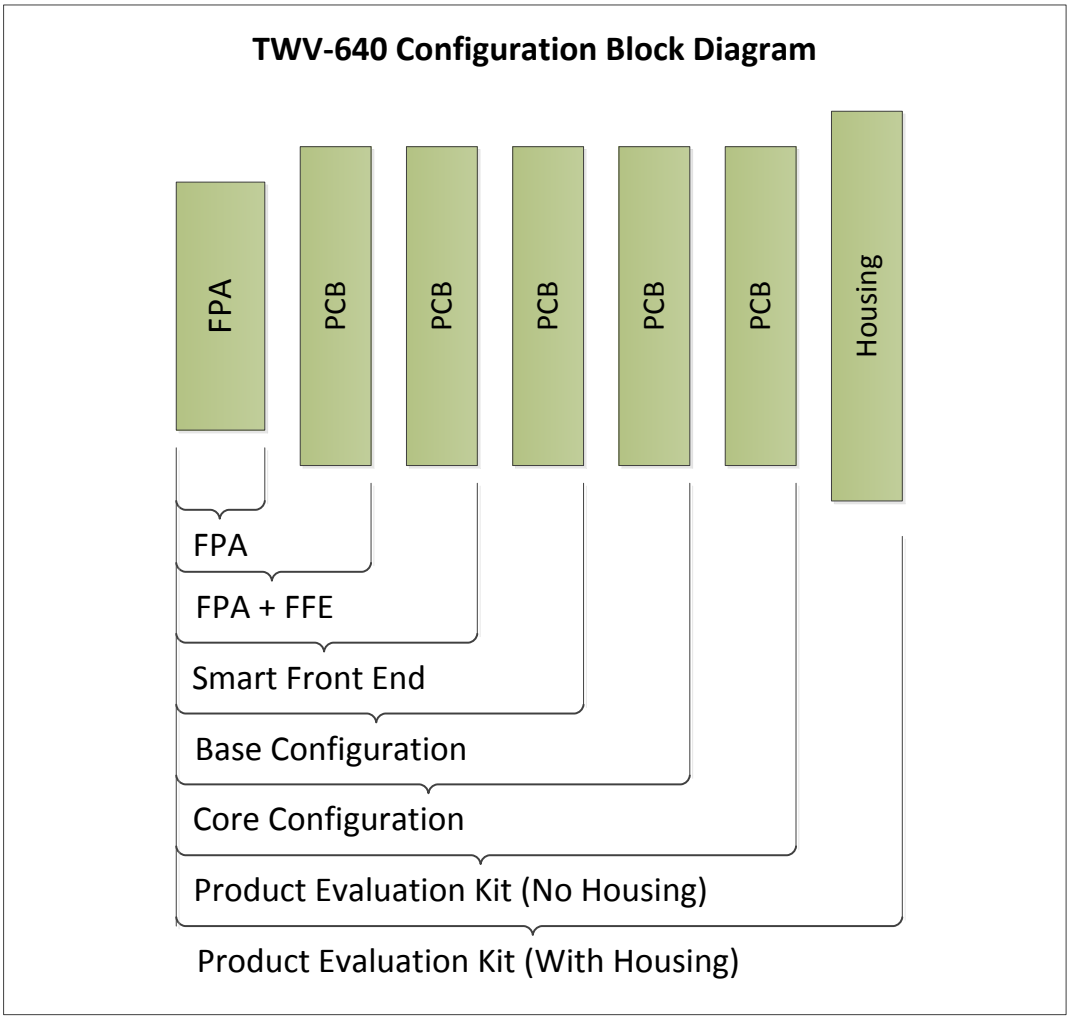

Figure 1-2: TWV640 configuration block diagram

1.1 Supported Frame rates

The TWV640 camera supports 30Hz and 60Hz frame rates. The 30Hz and 60Hz mode can be offered as a switchable operating mode where the user can switch between the two frame rates. The TWV640I is a subset of the TWV640 product. The TWV640I only supports 7.5Hz content.

1.2 Document Scope

This Electrical Interface and Control Document (ICD) provide details on the available hardware configurations and associated electrical interfaces of the TWV640. Information on the mechanical layout, tolerances and dimensions can be obtained in the Mechanical ICD for the camera core electronics. Software commands for controlling camera functionality are located in the Software ICD.

2. Electrical Interfaces

The TWV640 is designed to support a range of applications by providing a configurable electrical interface to meet user needs. Each configuration offers a variety of video formats while providing flexibility for user integration. This section provides an overview of what each configuration offers and focuses on the electrical interfaces of each configuration. The contained information can be used to select which configuration best meets the user's needs.

3. Smart Front End configuration

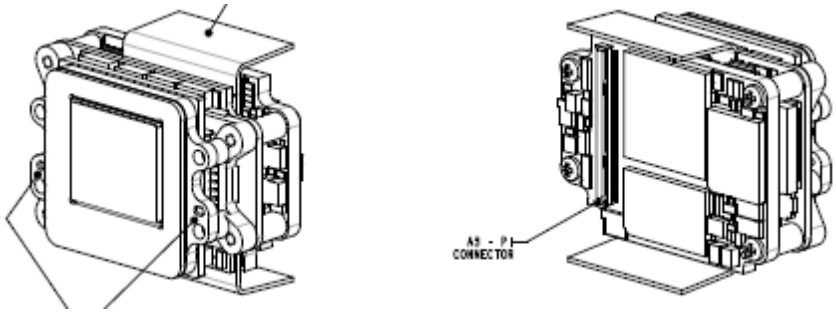

Figure 3-1: Smart Front End

For applications with extreme space constraints or large embedded systems, the Smart Front End configuration can be utilized. The Smart Front End offers a two board stack solution as seen in Figure 3-1 and supports a variety of pre or post processed video modes, however NTSC/PAL is not available in this mode. The SFE is ideal for systems with significant electrical infrastructure that require preprocessed video formats. The highlighted row in Table 3-1 lists the video outputs available in the SFE configuration.

Table 3-1: SFE Configuration video format summary

Output Peripheral Summary						
Peripheral	NTSC/PAL	eMagin 10-bit Mono	8-BIT YCbCr	8-BIT YCbCr (BT.656)	USB video	16-Bit Parallel Digital Video
Smart Front End		x	x	x	x	x
Base Configuration		x	x	x	x	x
Core Configuration	x	x	x	x	x	x
Product Evaluation Kit	x				x	

3.1 Power supply electrical characteristics

The Smart Front End requires five regulated DC power rails to operate, with the power requirements listed in Table 3-2. It is highly recommended that a DC to DC regulator is used to support each power parameters with respect to the specifications included in Table 3-2. The power supply ripple specification is measured in milli volts, peak to peak and applies to each power parameter.

Table 3-2: Smart Front End configuration power supplies

Parameter	Description	Min	Typ.	Max	Units
PLS_3_3V	Input voltage	3.23	3.3	3.44	V
	Current	-	-	15	mA
PLS_1_2V	Input voltage	1.18	1.2	1.21	V
	Current	-	-	350	mA
PLS_1_8V	Input voltage	1.78	1.8	1.83	V
	Current	-	-	115	mA
PLS_2_5V	Input voltage	2.43	2.5	2.58	V
	Current	-	-	45	mA
PLS_5_5V	Input voltage	5.42	5.5	5.64	V
	Current	-	-	45	mA
Power supply ripple		-	+/-10	+/-15	mV P-P

3.2 Power supply sequencing

The SFE configuration requires a specific power supply startup sequence in order to operate correctly. Figure 3-2 shows the supply sequencing in detail. The timing documented in Figure 3-2 are minimum values tha should be observed.

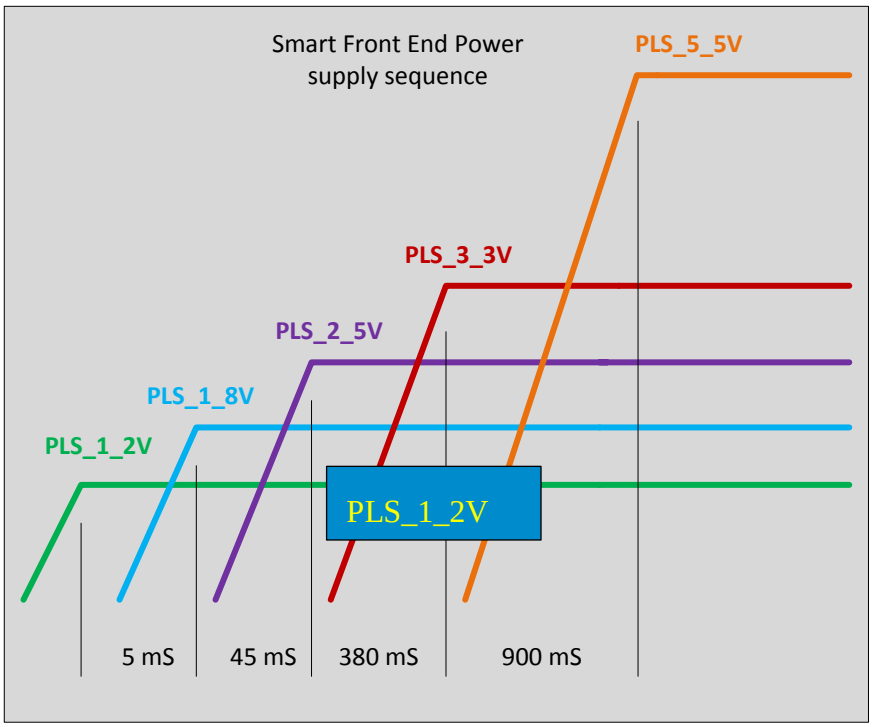

Figure 3-2: Smart Front End power supply sequence

3.3 Smart Front End connector description

The following section describes details with the P1 90-pin connector. Figure 3-3 shows the orientation of P1 using a horseshoe pin numbering scheme. Table 3-4 and Table 3-5 provide additional details on P1 including connector component details and electrical signal descriptions.

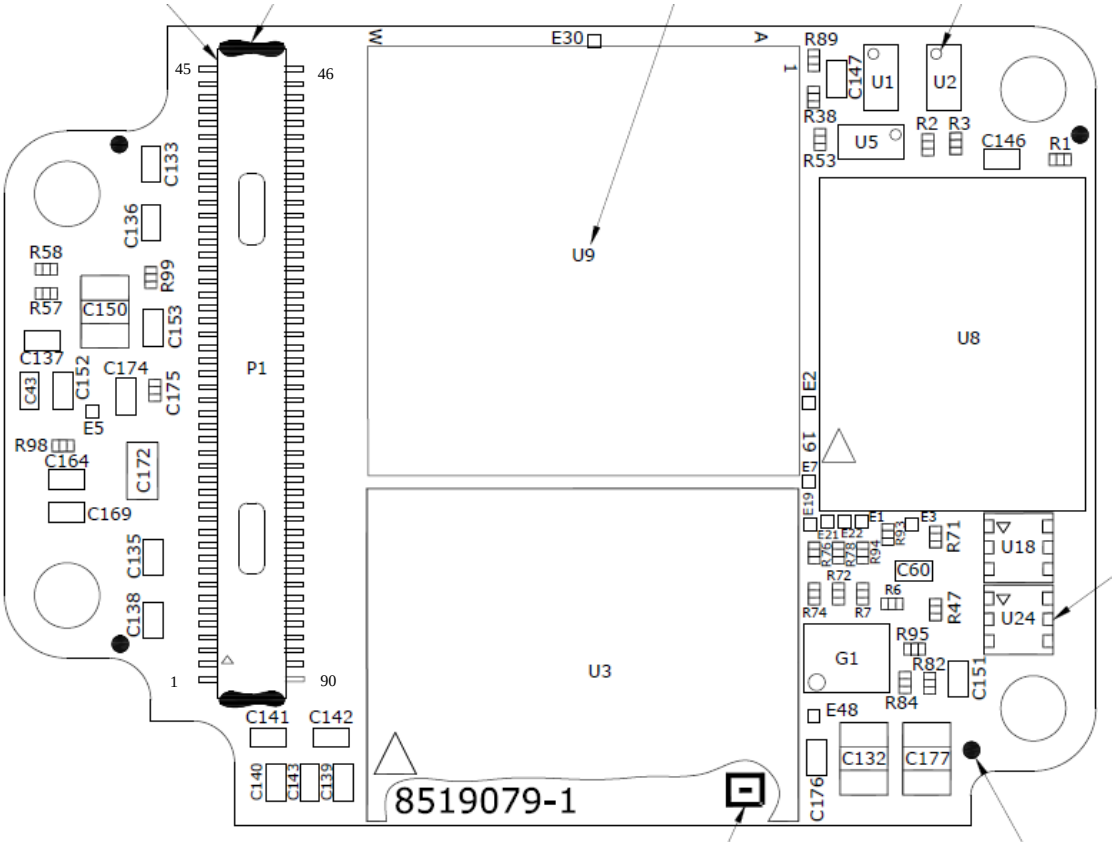

Figure 3-3: Smart Front End P1 orientation

Table 3-3: Connector Details

Ref. Des.	Function	Manufacturer	Part Number	Mating Connector
P1	System Interface	Hirose	DF40C-90DP-0.4V(51)	DF40HC(4.0)-90DS-0.4V(51)

Table 3-4: Electrical Interface

Pin	Net Name	Function	Value	Description
1	PLS_1_2V	N/A	1.2V	+1.2 V digital power supply
2	PLS_1_2V	N/A	1.2V	+1.2 V digital power supply
3	PLS_1_2V	N/A	1.2V	+1.2 V digital power supply
4	DGND	GND		Digital power return
5	DGND	GND		Digital power return
6	DGND	GND		Digital power return
7	DGND	GND		Digital power return
8	RESERVED	N/A		Do not connect

Pin	Net Name	Function	Value	Description
9	DGND	GND		Digital power return
10	DGND	GND		Digital power return
11	DGND	GND		Digital power return
12	PLS_5_5V	PWR	5.5V	+5.5 V digital power supply
13	DGND	GND		Digital power return
14	PLS_1_8V	PWR	1.8V	+1.8 V digital power supply
15	DGND	GND		Digital power return
16	PLS_3_3V	PWR	3.3V	+3.3 V digital power supply
17	PLS_3_3V	PWR	3.3V	+3.3 V digital power supply
18	DGND	GND		Digital power return
19	DGND	GND		Digital power return
20	PLS_3_3V_SW	PWR	3.3V	+3.3 V Digital switch
21	DGND	GND		Digital power return
22	PLS_2_5V_FPGA	PWR	2.5V	+2.5 V digital power supply
23	DGND	GND		Digital power return
24	PLS_2_5V_EMGN	PWR	2.5V	+2.5 V digital power supply eMagin
25	DGND	GND		Digital power return
26	RESERVED	N/A		Do not connect
27	RESERVED	N/A		Do not connect
28	RESERVED	N/A		Do not connect
29	RESERVED	N/A		Do not connect
30	DGND	GND		Digital power return
31	RESERVED	N/A		Do not connect
32	RESERVED	N/A		Do not connect
33	SHUTTER_RESET	O	3.3V	Shutter reset control signal
34	RESERVED	N/A		Do not connect
35	RESERVED	N/A		Do not connect
36	DGND	GND		Digital power return
37	UP_BAE_TX	O	3.3V	UART Transmit (User RX)
38	UP_BAE_RX	I	3.3V	UART Receive (User TX)
39	RESERVED	N/A		Do not connect
40	RESERVED	N/A		Do not connect
41	UP_I2C_SCL_0	O	3.3V	I^2C SDA digital clock from µP bus 0
42	UP_I2C_SDA_0	O	3.3V	I^2C SCL digital data from µP bus 0
43	DISPLAY_BL2	O	2.5V	Video data bus
44	DISPLAY _GN1	O	2.5V	Video data bus
45	DISPLAY _BL4	O	2.5V	Video data bus

Pin	Net Name	Function	Value	Description
46	DISPLAY _GN2	O	2.5V	Video data bus
47	DISPLAY _RD9	O	2.5V	Video data bus
48	DISPLAY _RD7	O	2.5V	Video data bus
49	DISPLAY _RD1	O	2.5V	Video data bus
50	DISPLAY _RD3	O	2.5V	Video data bus
51	DISPLAY _GN3	O	2.5V	Video data bus
52	DISPLAY _RD8	O	2.5V	Video data bus
53	DISPLAY _RD4	O	2.5V	Video data bus
54	DISPLAY _BL1	O	2.5V	Video data bus
55	DISPLAY _RD0	O	2.5V	Video data bus
56	DISPLAY _VSYNC	O	2.5V	Video data bus
57	DISPLAY _BL3	O	2.5V	Video data bus
58	DISPLAY _RD6	O	2.5V	Video data bus
59	RESERVED	N/A		Do not connect
60	RESERVED	N/A		Do not connect
61	RESERVED	N/A		Do not connect
62	DISPLAY _BL6	O	2.5V	Display blue video data bus bit 6
63	DISPLAY _VGN	O	2.5V	eMagin display Gamma feedback control
64	DISPLAY _DATA_ENABLE	O	2.5V	eMagin display data enable
65	DGND	GND		Digital power return
66	DISPLAY _BL5	O	2.5V	Video data bus
67	DISPLAY _BL8	O	2.5V	Video data bus
68	DISPLAY _GN6	O	2.5V	Video data bus
69	DISPLAY _GN0	O	2.5V	Video data bus
70	DISPLAY _BL0	O	2.5V	Video data bus
71	DISPLAY _BL7	O	2.5V	Video data bus
72	DISPLAY _BL9	O	2.5V	Video data bus
73	DISPLAY _RD5	O	2.5V	Video data bus
74	DISPLAY _GN5	O	2.5V	Video data bus
75	DISPLAY _HSYNC	O	2.5V	eMagin Display horizontal sync
76	DISPLAY _GN7	O	2.5V	Video data bus
77	DISPLAY _GN9	O	2.5V	Video data bus
78	DISPLAY _SRCCLK	O	2.5V	eMagin Display source clock
79	DISPLAY _RD2	O	2.5V	Video data bus
80	DISPLAY _GN4	O	2.5V	Video data bus

Pin	Net Name	Function	Value	Description
81	DISPLAY _RESET_N	O	2.5V	eMagin Display reset control
82	DISPLAY _GN8	O	2.5V	Video data bus
83	RESERVED	N/A		Do not connect
84	RESERVED	N/A		Do not connect
85	RESERVED	N/A		Do not connect
86	DISPLAY _ENABLE	O	2.5V	eMagin Display enable
87	RESERVED	N/A		Do not connect
88	UP_USB0_DP	I/O	5.0V	USB positive data
89	UP_USB0_VBUS	I		USB 5.0V VBUS
90	UP_USB0_DM	I/O	5.0V	USB negative data

3.4 Video output formats

The SFE configuration features an abbreviated set of outputs that are suited for further formatting. Pins may be shared between the different formats and are repurposed depending on the setting of the SFE. For more information on how to setup the unit for different video or operating modes see the MicroIR™ Software ICD. Table 3-6 lists connector pins and signal names for each video output supported in this mode.

Table 3-5: Video outputs

Pin	eMagin 10-bit Monochrome	8-bit YCbCr	8-bit YCbCr (BT.656)	USB Raw	16-bit Parallel Digital Video
55	DISPLAY_RD0	DISPLAY_RD0			DISPLAY_RD0
49	DISPLAY_RD1	DISPLAY_RD1			DISPLAY_RD1
79	DISPLAY_RD2	DISPLAY_RD2			DISPLAY_RD2
50	DISPLAY_RD3	DISPLAY_RD3			DISPLAY_RD3
53	DISPLAY_RD4	DISPLAY_RD4			DISPLAY_RD4
73	DISPLAY_RD5	DISPLAY_RD5			DISPLAY_RD5
58	DISPLAY_RD6	DISPLAY_RD6			DISPLAY_RD6
48	DISPLAY_RD7	DISPLAY_RD7			DISPLAY_RD7
52	DISPLAY_RD8				DISPLAY_RD8
47	DISPLAY_RD9				DISPLAY_RD9
69			DISPLAY_GN0		
44			DISPLAY_GN1		
46			DISPLAY_GN2		

Pin	eMagin 10-bit Monochrome	8-bit YCbCr	8-bit YCbCr (BT.656)	USB Raw	16-bit Parallel Digital Video
51			DISPLAY_GN3		
80			DISPLAY_GN4		
74			DISPLAY_GN5		
68			DISPLAY_GN6		
76			DISPLAY_GN7		
82			DISPLAY_GN8		
54					DISPLAY_BL1
43					DISPLAY_BL2
57					DISPLAY_BL3
45					DISPLAY_BL4
66					DISPLAY_BL5
62					DISPLAY_BL6
78	DISPLAY_SRCCLK	DISPLAY_SRCCLK			DISPLAY_SRCCLK
63	DISPLAY_VGN				
64	DISPLAY_DATA_EN				
86	DISPLAY_ENABLE				
81	DISPLAY_RESET_N				
56	DISPLAY_VSYNC				DISPLAY_VSYNC
75	DISPLAY_HSYNC				DISPLAY_HSYNC
88				UP_USB0_DP	
90				UP_USB0_DM	

3.5 Serial communications

To communicate to the Smart Front End configuration, both UART and USB options are available. The three USB pins represent an industry standard USB 2.0 HS port, with the fourth and ground pin connected to all digital power return pins. The camera can be controlled via ASCII commands through serial interfaces through either the USB or UART ports. The UART and the USB ASCII interface are considered the same from a system's point of view, and all ASCII output is output through both ports. A signal summary for serial communications signals can be found in Table 3-7.

Table 3-6: Serial Communications

Pin	Net Name	USB Pin	Description
88	UP_USB0_DP	Data+	USB Data I/O positive
90	UP_USB0_DM	Data-	USB Data I/O negative
89	UP_USB0_VBUS	V_{CC} (+5 V)	External USB power input, bus 0
37	UP_BAE_TX	3.3V	UART Transmit (User RX)
38	UP_BAE_RX	3.3V	UART Receive (User TX)

3.6 Shutter Drive Interface

The camera features commands and an I2C interface that can control a Nanomotion RS08™ Rotary Shutter. For more information on the particular shutter refer to documentation provided by the manufacturer, referenced in this document. In this configuration the 3.3V Shutter power rail must be provided by the user. Table 3-8 lists the shutter related signals provided by the SFE.

Table 3-7: Shutter drive interface ports

Pin	Net Name	Function	Value	Description
40	UP_I2C_SDA_0	I/O	3.3V	I^2C SDA digital data from µP bus
41	UP_I2C_SCL_0	O	3.3V	I^2C SCL digital clock from µP bus
33	SHUTTER_RESET	O	3.3V	Shutter reset signal

4. Base Configuration

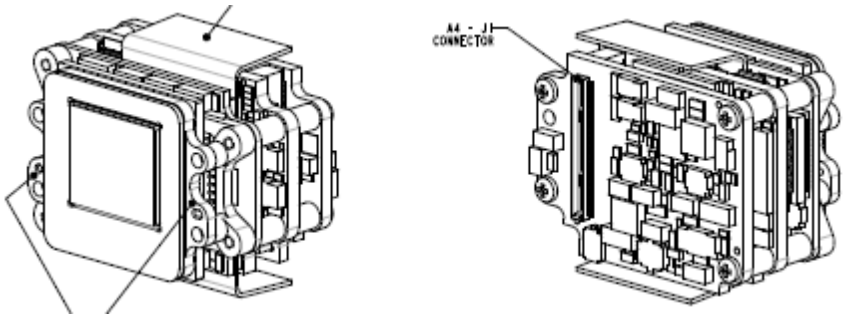

Figure 4-1: Base Module Configuration

The base configuration is a three board solution that is best suited for applications requiring a user designed backend board. Supported video modes for the Base configuration are highlighted in Table 4-1. In this configuration NTSC/PAL video is not available.

Table 4-1: Configuration video format summary

Output Peripheral Summary						
Peripheral	NTSC/PAL	eMagin 10-bit Mono	8-BIT YCbCr	8-BIT YCbCr (BT.656)	USB video	16-Bit Parallel Digital Video
Smart Front End		x	x	x	x	x
Base Configuration		x	x	x	x	x
Core Configuration	x	x	x	x	x	x
Product Evaluation Kit	x				x	

4.1 Power Supply Electrical Characteristics

The Base configuration requires two power supplies to operate. The current consumption of the V_BATT power supply will vary with voltage. Additional power requirements are listed in Table 4-2. The power supply ripple specification is measured in milli volts, peak to peak and applies to PLS_3_3V as well as V_BATT when it is not driven by a battery. Inrush current in Table 4-2 applies to power up conditions in which PLS_3_3V and V_BATT are connected together and driven at 3.3V.

Table 4-2: Base configuration power supplies

Parameter	**Description**	**Min**	**Typ.**	**Max**	**Units**
PLS_3_3V	Input voltage	3.23	3.3	3.44	V
	Current	-	95	105	mA
V_BATT	Input voltage	2.0	3.0	3.8	V
	Current	-	280	430	mA
Inrush current		-	-	1800	mA
Steady state power		0.95	1.1	1.2	W
Power supply ripple		-	+/-10	+/-15	mV P-P

4.2 Power supply sequencing

The necessary power sequencing to operate the Base configuration is shown below in Figure 4-2. For best power performance the sequence below should be observed. For simplicity both supplies can be tied together and sequenced simultaneously at 3.3 volts, doing so will incur an overall power increase.

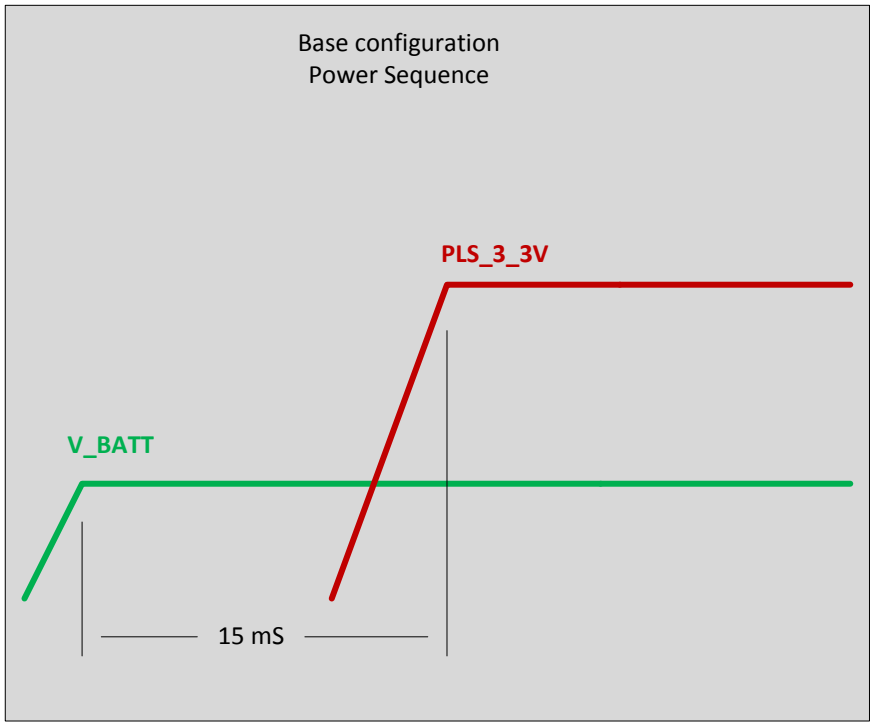

Figure 4-2: Base Module Configuration power supply sequence

4.3 Base configuration connector description

The following section describes details with the J1 80-pin connector. Figure 4-3 shows the orientation of J1 using a horseshoe pin numbering scheme. Table 4-3 and Table 4-4 provide additional details on J1 including connector component details and electrical signal descriptions.

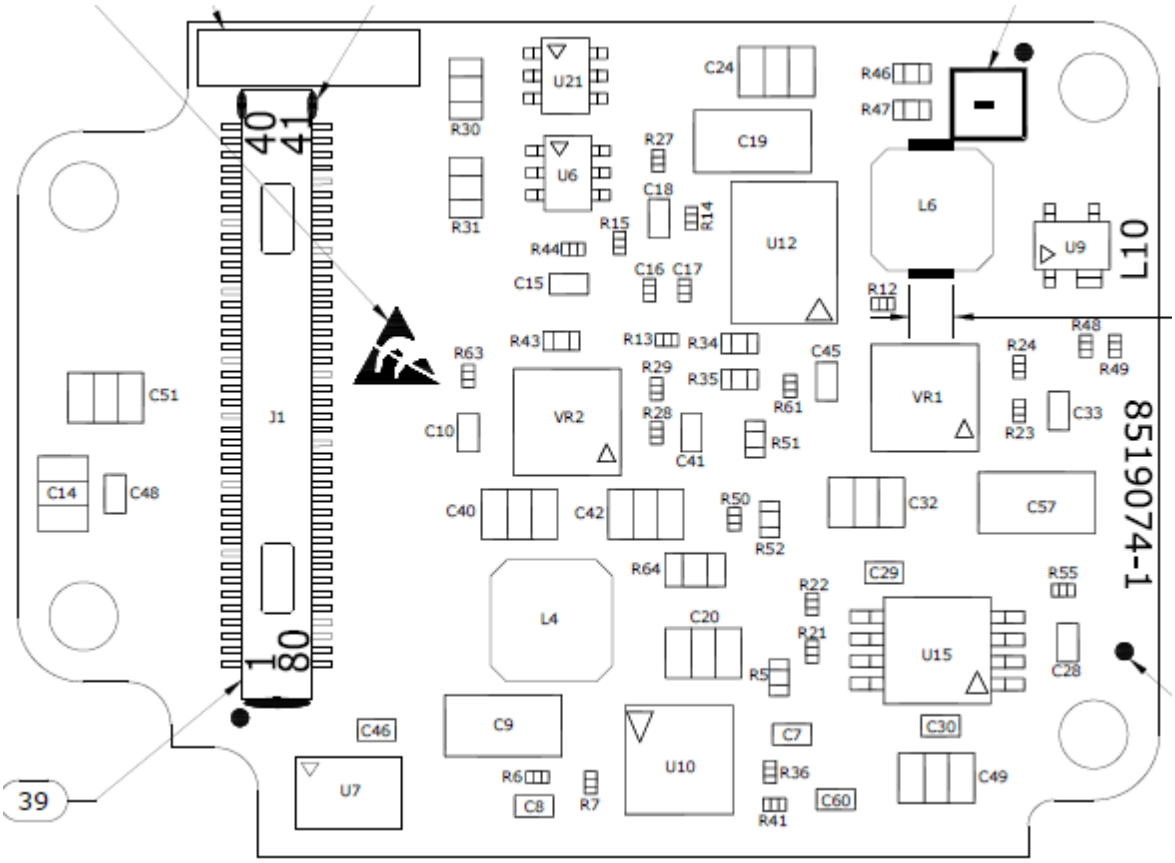

Figure 4-3: Base configuration J1 orientation

Table 4-3: J1 Part Details

Ref. Des.	Function	Manufacturer	Part Number	Mating Connector
J1	System Interface	Hirose	DF40C-80DP-0.4V(51)	DF40HC(3.5)-80DS-0.4V(51)

Table 4-4: J1 pin-out

Pin	Net Name	Function	Value	Description
1	RESERVED	N/A		Do not connect
2	RESERVED	N/A		Do not connect

3	RESERVED	N/A		Do not connect
4	RESERVED	N/A		Do not connect
5	RESERVED	N/A		Do not connect
6	DGND	GND		Digital power return
7	MNS_1_5V	PWR	1.5V	Display 1.5 V bias power supply
8	DGND	GND		Digital power return
9	DISPLAY_VSYNC	O	2.5V	Display vertical sync output
10	DISPLAY_HSYNC	O	2.5V	Display horizontal sync output
11	PLS_2_5V	PWR	2.5V	Display +2.5 V digital power supply
12	PLS_2_5V	PWR	2.5V	Display +2.5 V digital power supply
13	PLS_5_0V	PWR	5.0V	Display +5.0 V analog power supply
14	DGND	GND		Digital power return
15	RESERVED	N/A		Do not connect
16	RESERVED	N/A		Do not connect
17	UP_I2C_SCL_0	I/O	3.3V	I^2C SDA digital data from µP bus 0
18	UP_I2C_SDA_0	O	3.3V	I^2C SCL digital clock from µP bus 0
19	DGND	GND		Digital power return
20	UP_USB0_DP	I/O	5.0	USB Data I/O positive
21	UP_USB0_DM	I/O	5.0	USB Data I/O negative
22	UP_USB0_VBUS	PWR	5.0V	External USB power input, bus 0
23	DGND	GND		Digital power return
24	DISPLAY_RD0	O	2.5V	Display red video data bus bit 0
25	DISPLAY_RD1	O	2.5V	Display red video data bus bit 1
26	DISPLAY_RD2	O	2.5V	Display red video data bus bit 2
27	DISPLAY_RD3	O	2.5V	Display red video data bus bit 3
28	DISPLAY_RD4	O	2.5V	Display red video data bus bit 4
29	DISPLAY_RD5	O	2.5V	Display red video data bus bit 5
30	DISPLAY_RD6	O	2.5V	Display red video data bus bit 6
31	DISPLAY_RD7	O	2.5V	Display red video data bus bit 7
32	DISPLAY_RD8	O	2.5V	Display red video data bus bit 8
33	DISPLAY_RD9	O	2.5V	Display red video data bus bit 9
34	DISPLAY_BL0	O	2.5V	Display blue video data bus bit 0
35	DISPLAY_BL1	O	2.5V	Display blue video data bus bit 1
36	DISPLAY_BL2	O	2.5V	Display blue video data bus bit 2
37	DISPLAY_BL3	O	2.5V	Display blue video data bus bit 3
38	GND	GND		Digital power return
39	GND	GND		Digital power return
40	GND	GND		Digital power return

41	GND	GND		Digital power return
42	PLS_1_8V	PWR		1.8V power supply
43	PLS_1_8V	PWR		1.8V power supply
44	UP_BAE_TX	O	3.3V	UART Transmit (User RX)
45	UP_BAE_RX	I	3.3V	UART Receive (User TX)
46	RESERVED	N/A		Do not connect
47	DISPLAY_SRCCLK	O	2.5V	Display pixel clock
48	DISPLAY_GN0	O	2.5V	Display green video data bus bit 0
49	DISPLAY_GN1	O	2.5V	Display green video data bus bit 1
50	DISPLAY_GN2	O	2.5V	Display green video data bus bit 2
51	DISPLAY_GN3	O	2.5V	Display green video data bus bit 3
52	DISPLAY_GN4	O	2.5V	Display green video data bus bit 4
53	DISPLAY_GN5	O	2.5V	Display green video data bus bit 5
54	DISPLAY_GN6	O	2.5V	Display green video data bus bit 6
55	DISPLAY_GN7	O	2.5V	Display green video data bus bit 7
56	DISPLAY_DATA_EN	O	2.5V	Display data enable control
57	DISPLAY_ENABLE	O	2.5V	Display enable control
58	DISPLAY_VGN	I	2.5V	Display gamma analog feedback control
59	DGND	GND		Digital power return
60	DISPLAY_RESET_N	O	2.5V	Display reset control
61	DGND	GND		Digital power return
62	DISPLAY_BL4	O	2.5V	Display blue video data bus bit 4
63	DISPLAY_BL5	O	2.5V	Display blue video data bus bit 5
64	DISPLAY_BL6	O	2.5V	Display blue video data bus bit 6
65	DISPLAY_BL7	O	2.5V	Display blue video data bus bit 7
66	DISPLAY_BL8	O	2.5V	Display blue video data bus bit 8
67	DISPLAY_BL9	O	2.5V	Display blue video data bus bit 9
68	DISPLAY_GN8	O	2.5V	Display green video data bus bit 8
69	DISPLAY_GN9	O	2.5V	Display green video data bus bit 9
70	DGND	GND		Digital power return
71	DGND	GND		Digital power return
72	DGND	GND		Digital power return
73	DGND	GND		Digital power return
74	DGND	GND		Digital power return
75	PLS_3_3V	PWR	3.3V	Power input
76	PLS_3_3V	PWR	3.3V	Power input
77	V_BATT	PWR		Power/Battery Input, +3 V nominal
78	V_BATT	PWR		Power/Battery Input, +3 V nominal

79	RESERVED	N/A		Do not connect
80	SHUTTER_RESET	O	3.3V	Shutter reset control signal

4.4 Video output formats

The Base configuration features a variety of outputs that are suited for pre or post formatting applications. Some signals may be shared between the different formats and are repurposed depending on the setting of the camera core. For more information on how to setup the unit for different video or operating modes see the MicroIR™ Software ICD. Table 4-5 lists connector pins and signal names for each video output supported in this mode.

Table 4-5: Video Outputs

Pin	eMagin 10-bit Monochrome	8-bit YCbCr	8-bit YCbCr (BT.656)	USB Raw	16-bit parallel digital video
24	DISPLAY_RD0	DISPLAY_RD0			DISPLAY_RD0
25	DISPLAY_RD1	DISPLAY_RD1			DISPLAY_RD1
26	DISPLAY_RD2	DISPLAY_RD2			DISPLAY_RD2
27	DISPLAY_RD3	DISPLAY_RD3			DISPLAY_RD3
28	DISPLAY_RD4	DISPLAY_RD4			DISPLAY_RD4
29	DISPLAY_RD5	DISPLAY_RD5			DISPLAY_RD5
30	DISPLAY_RD6	DISPLAY_RD6			DISPLAY_RD6
31	DISPLAY_RD7	DISPLAY_RD7			DISPLAY_RD7
32	DISPLAY_RD8				DISPLAY_RD8
33	DISPLAY_RD9				DISPLAY_RD9
48			DISPLAY_GN0		
49			DISPLAY_GN1		
50			DISPLAY_GN2		
51			DISPLAY_GN3		
52			DISPLAY_GN4		
53			DISPLAY_GN5		
54			DISPLAY_GN6		
55			DISPLAY_GN7		
68			DISPLAY_GN8		
35					DISPLAY_BL1
36					DISPLAY_BL2
37					DISPLAY_BL3

Pin	eMagin 10-bit Monochrome	8-bit YCbCr	8-bit YCbCr (BT.656)	USB Raw	16-bit parallel digital video
62					DISPLAY_BL4
63					DISPLAY_BL5
64					DISPLAY_BL6
9	DISPLAY_VSYNC				DISPLAY_VSYNC
10	DISPLAY_HSYNC				DISPLAY_HSYNC
47	DISPLAY_SRCCLK	DISPLAY_SRCCLK			DISPLAY_SRCCLK
56	DISPLAY_DATA_EN				
57	DISPLAY_ENABLE				
58	DISPLAY_VGN				
60	DISPLAY_RESET_N				
20				UP_USB0_DP	
21				UP_USB0_DM	

4.5 Serial communications

Refer to Table 4-6 for details on how to communicate to the Base configuration, both UART and USB options are available. The three USB pins represent an industry standard USB 2.0 HS port, with the fourth and ground pin connected to all digital power return pins. The camera can be controlled via ASCII commands through serial interfaces through either the USB or UART ports. The UART and the USB ASCII interface are considered the same from a system's point of view, and all ASCII output is output through both ports. A signal summary for serial communications signals can be found in Table 4-7.

Table 4-6: Serial communications

Pin	Net Name	USB Pin	Description
20	UP_USB0_DP	Data+	USB Data I/O positive
21	UP_USB0_DM	Data-	USB Data I/O negative
22	UP_USB0_VBUS	V_{CC} (+5 V)	External USB power input, bus 0
44	UP_RS232_TX	3.3V	UART Transmit
45	UP_RS232_RX	3.3V	UART Receive

4.6 Shutter Drive Interface

The camera features commands and an I2C interface that can control a Nanomotion RS08™ Rotary Shutter. For more information on the particular shutter refer to documentation provided by the manufacturer. The clock, data and reset signals for the I2C interface are listed in. Table 4-7 lists the shutter related signals provided by the Base configuration.

Table 4-7: Shutter drive interface ports

Pin	Net Name	Function	Value	Description
17	UP_I2C_SDA_0	I/O	3.3V	I^2C SDA digital data from µP bus
18	UP_I2C_SCL_0	O	3.3V	I^2C SCL digital clock from µP bus
75	PLS_3_3V	PWR	3.3V	Power input
80	SHUTTER_RESET	O	3.3V	Shutter reset signal

5. Core configuration

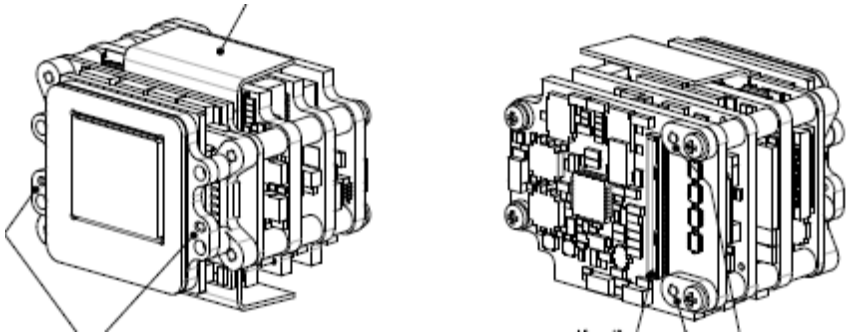

Figure 5-1: Core configuration

The Core configuration offers all advertised outputs including NTSC/PAL. All video formats are available via a single 80 pin connector. The 80 pin connector allows the user flexibility to use either a Flex or PCB board solution to interface to the electronics.

Table 5-1: Configuration video format summary

Output Peripheral Summary						
Peripheral	NTSC/PAL	eMagin 10-bit Mono	8-BIT YCbCr	8-BIT YCbCr (BT.656)	USB video	16-Bit Parallel Digital Video
Smart Front End		x	x	x	x	x
Base Configuration		x	x	x	x	x
Core Configuration	x	x	x	x	x	x
Product Evaluation Kit	x				x	

5.1 Power Supply Electrical Characteristics

This configuration can be powered via the input power or the VBUS input. When VBUS is connected in this configuration the Input power port will be disabled. On the fly switching between both inputs is supported, however VBUS has priority. Additional power requirements are listed in Table 5-2. The power supply ripple specification is measured in milli volts, peak to peak and applies to input power when it is not driven by a battery. Inrush current in Table 5-2 applies to power up conditions where either input power or VBUS power is applied. Table 5-2 lists the maximum power dissipated by NTSC/PAL video, this power figure is not included within the steady state power measurement also found in Table 5-2.

Table 5-2: Electrical Characteristics

Parameter	**Description**	**Min**	**Typ.**	**Max**	**Units**
Input power	Input voltage	2.0	3.0	3.8	V
	Current	-	420	460	mA
VBUS	Input voltage	4.75	5.0	5.25	V
	Current	-	310	350	mA
NTSC/PAL power		-	-	200	mw
Inrush current		-	-	1800	mA
Steady state power		0.95	1.1	1.2	W
Power supply ripple		-	+/- 10	+/-15	mV P-P

5.2 Core configuration connector description

The following section describes details with the J2 80-pin connector. Figure 5-2 shows the orientation of J2 using a horseshoe pin numbering scheme. Table 5-3 and Table 5-4 provide additional details on J2 including connector component details and electrical signal descriptions.

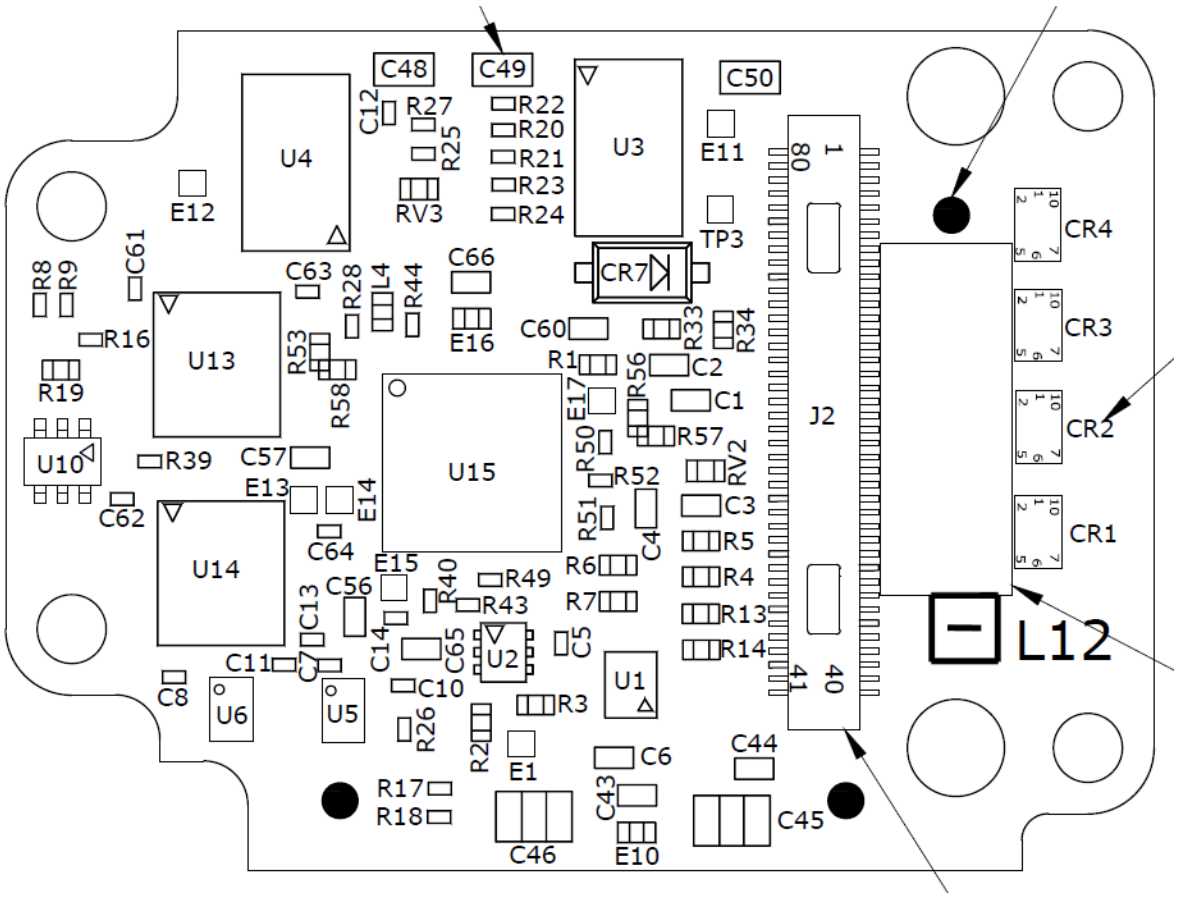

Figure 5-2: Base configuration J1 orientation

Table 5-3: J2 Part Details

Ref. Des.	Function	Manufacturer	Part Number	Mating Connector
J2	System Interface	Hirose	DF40C-80DP-0.4V(51)	DF40HC(3.5)-80DS-0.4V(51)

Table 5-4: Electrical interface

Pin	Net Name	Function	Value	Description
1	INPUT_PWR	PWR		Input power
2	INPUT_PWR	PWR		Input power
3	INPUT_PWR	PWR		Input power
4	INPUT_PWR	PWR		Input power
5	DGND	GND		Digital power return
6	DGND	GND		Digital power return
7	DGND	GND		Digital power return
8	DGND	GND		Digital power return
9	DISPLAY_RD0	O	2.5V	Display red video data bus bit 0
10	DISPLAY_RD1	O	2.5V	Display red video data bus bit 1
11	DISPLAY_RD2	O	2.5V	Display red video data bus bit 2
12	DISPLAY_RD3	O	2.5V	Display red video data bus bit 3
13	DISPLAY_RD4	O	2.5V	Display red video data bus bit 4
14	DISPLAY_RD5	O	2.5V	Display red video data bus bit 5
15	DISPLAY_RD6	O	2.5V	Display red video data bus bit 6
16	DISPLAY_RD7	O	2.5V	Display red video data bus bit 7
17	DISPLAY_RD8	O	2.5V	Display red video data bus bit 8
18	DISPLAY_RD9	O	2.5V	Display red video data bus bit 9
19	DGND	GND		Digital power return
20	DISPLAY_VGN	O	2.5V	Display Gamma analog feedback control
21	DGND	GND		Digital power return
22	DISPLAY_RESET_N	O	2.5V	Display reset control
23	DISPLAY_DATA_EN	O	2.5V	Display data enable control
24	DISPLAY_SRCCLK	O	2.5V	Display pixel clock
25	DISPLAY_ENABLE	O	2.5V	Display enable control
26	DISPLAY_GN0	O	2.5V	Display green video data bus bit 0
27	DISPLAY_GN1	O	2.5V	Display green video data bus bit 1
28	DISPLAY_GN2	O	2.5V	Display green video data bus bit 2
29	DISPLAY_GN3	O	2.5V	Display green video data bus bit 3
30	DISPLAY_GN4	O	2.5V	Display green video data bus bit 4
31	DISPLAY_GN5	O	2.5V	Display green video data bus bit 5
32	DISPLAY_GN6	O	2.5V	Display green video data bus bit 6
33	DISPLAY_GN7	O	2.5V	Display green video data bus bit 7
34	DISPLAY_GN8	O	2.5V	Display green video data bus bit 8
35	DISPLAY_GN9	O	2.5V	Display green video data bus bit 9

Pin	Net Name	Function	Value	Description
36	DISPLAY_BL7	O	2.5V	Display blue video data bus bit 7
37	DISPLAY_BL8	O	2.5V	Display blue video data bus bit 8
38	DISPLAY_BL9	O	2.5V	Display blue video data bus bit 9
39	VIDOUT	O		75 Ohm analog output
40	A_GND	GND		Analog power return
41	DISPLAY_BL6	O	2.5V	Display blue video data bus bit 6
42	DISPLAY_BL5	O	2.5V	Display blue video data bus bit 5
43	DISPLAY_BL4	O	2.5V	Display blue video data bus bit 4
44	DISPLAY_BL3	O	2.5V	Display blue video data bus bit 3
45	DISPLAY_BL2	O	2.5V	Display blue video data bus bit 2
46	DISPLAY_BL1	O	2.5V	Display blue video data bus bit 1
47	DISPLAY_BL0	O	2.5V	Display blue video data bus bit 0
48	DGND	GND		Digital power return
49	DGND	GND		Digital power return
50	DGND	GND		Digital power return
51	DGND	GND		Digital power return
52	RESERVED	N/A		Do not connect
53	RESERVED	N/A		Do not connect
54	DGND	GND		Digital power return
55	3_3V_SHUTTER	PWR		3.3V DC regulated shutter power rail
56	3_3V_SHUTTER	PWR		3.3V DC regulated shutter power rail
57	LVDS-	O	3.3V	LVDS negative data
58	DGND	GND		Digital power return
59	LVDS+	O	3.3V	LVDS positive data
60	DGND	GND		Digital power return
61	SHUTTER_RESET	O	3.3V	Shutter reset control
62	DGND	GND		Digital power return
63	DGND	GND		Digital power return
64	VBUS	PWR		5.0V VBUS power input
65	VBUS	PWR		5.0V VBUS power input
66	UP_USB_DM	I/O		USB negative differential data
67	UP_USB_DP	I/O		USB Positive differential data
68	UP_BAE_TX	O	3.3V	UART Transmit (User RX)
69	DGND	GND		Digital power return
70	UP_BAE_RX	I	3.3V	UART Receive (User TX)
71	UP_I2C_SDA_0	I/O	3.3V	I2C SDA digital data from up bus 0
72	UP_I2C_SCL_0	O	3.3V	I2C SCL digital clock from up bus 0

Pin	Net Name	Function	Value	Description
73	DGND	GND		Digital power return
74	PLS_5V	PWR		5.0V power supply for eMagin display
75	PLS_2_5V_EMGN	PWR		2.5V power supply for eMagin display
76	PLS_2_5V_EMGN	PWR		2.5V power supply for eMagin display
77	FPGA_EMAGIN_HSYNC	O	2.5V	Display Horizontal sync
78	FPGA_EMAGIN_VSYNC	O	2.5V	Display Vertical sync
79	DGND	GND		Digital power return
80	MNS_1_5V	PWR		-1.5V power supply for eMagin display

5.3 Video output formats

The Core configuration supports multiple standard video outputs suited for post processing applications. Pins may be shared between the different formats and are repurposed depending on the setting of the camera core. For more information on how to setup the unit for different video or operating modes see the MicroIR™ Software ICD. Table 5-5 lists connector pins and signal names for each video output supported in this mode.

Table 5-5: Video outputs

Pin	eMagin 10-bit Monochrome	8-bit YCbCr	NTSC/PAL	8-bit YCbCr (BT.656)	USB Raw	16-bit parallel digital video
9	DISPLAY_RD0	DISPLAY_RD0				DISPLAY_RD0
10	DISPLAY_RD1	DISPLAY_RD1				DISPLAY_RD1
11	DISPLAY_RD2	DISPLAY_RD2				DISPLAY_RD2
12	DISPLAY_RD3	DISPLAY_RD3				DISPLAY_RD3
13	DISPLAY_RD4	DISPLAY_RD4				DISPLAY_RD4
14	DISPLAY_RD5	DISPLAY_RD5				DISPLAY_RD5
15	DISPLAY_RD6	DISPLAY_RD6				DISPLAY_RD6
16	DISPLAY_RD7	DISPLAY_RD7				DISPLAY_RD7
17	DISPLAY_RD8					DISPLAY_RD8
18	DISPLAY_RD9					DISPLAY_RD9
26				DISPLAY_GN0		
27				DISPLAY_GN1		
28				DISPLAY_GN2		
29				DISPLAY_GN3		
30				DISPLAY_GN4		
31				DISPLAY_GN5		
32				DISPLAY_GN6		
33				DISPLAY_GN7		

Pin	eMagin 10-bit Monochrome	8-bit YCbCr	NTSC/PAL	8-bit YCbCr (BT.656)	USB Raw	16-bit parallel digital video
34				DISPLAY_GN8		
46						DISPLAY_BL1
45						DISPLAY_BL2
44						DISPLAY_BL3
43						DISPLAY_BL4
42						DISPLAY_BL5
41						DISPLAY_BL6
78	DISPLAY_VSYNC					DISPLAY_VSYNC
77	DISPLAY_HSYNC					DISPLAY_HSYNC
24	DISPLAY_SRCCLK	DISPLAY_SRCCLK				DISPLAY_SRCCLK
23	DISPLAY_DATA_EN					
25	DISPLAY_ENABLE					
22	DISPLAY_RESET_N					
39			VIDOUT			
40			ANALOG_RTN			
66					UP_USB_DM	
67					UP_USB_DP	

5.4 Serial communications

To communicate to the base configuration, both UART and USB options are available. The three USB pins represent an industry standard USB 2.0 HS port, with the fourth and ground pin connected to all digital power return pins. The camera can be controlled via ASCII commands through serial interfaces through either the USB or UART ports. The UART and the USB ASCII interface are considered the same from a system's point of view, and all ASCII output is output through both ports. A signal summary for serial communications signals can be found in Table 5-6.

Table 5-6: Serial communications

Pin	Net Name	USB Pin	Description
67	UP_USB0_DP	Data+	USB Data I/O positive
66	UP_USB0_DM	Data-	USB Data I/O negative
65	UP_USB0_VBUS	V_{CC} (+5 V)	External USB power input, bus 0
64	UP_USB0_VBUS	V_{CC} (+5 V)	External USB power input, bus 0
68	UP_RS232_TX	3.3V	UART Transmit
70	UP_RS232_RX	3.3V	UART Receive

5.5 Shutter Drive Interface

The camera features commands and an I2C interface that can control a Nanomotion RS08™ Rotary Shutter. For more information on the particular shutter refer to documentation provided by the manufacturer. The clock, data and reset signals for the I2C interface are listed in. Table 5-7 lists the shutter related signals provided by the Core configuration.

Table 5-7: Shutter drive interface ports

Pin	Net Name	Function	Value	Description
71	UP_I2C_SDA_0	I/O	3.3V	I^2C SDA digital data from µP bus
72	UP_I2C_SCL_0	O	3.3V	I^2C SCL digital clock from µP bus
61	SHUTTER_RESET	O	3.3V	Shutter reset control
55	3_3V_SHUTTER	PWR	-	3.3V regulated shutter power rail

6. Product Evaluation Kit (PEK)

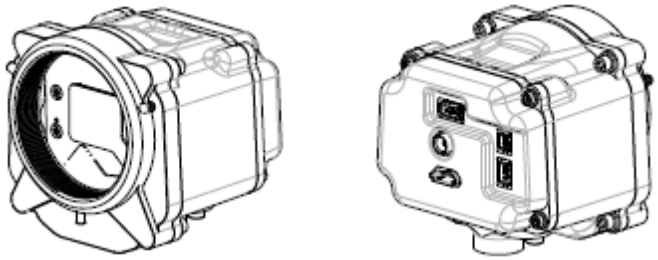

Figure 6-1: Product Evaluation Kit

The PEK offers everything necessary to evaluate the camera performance using raw USB video or NTSC/PAL. This configuration is a standalone camera that is offered with or without camera housing. A variety of lenses are available in order for the user to select a lens to best match their system.

Table 6-1: Configuration video format summary

Output Peripheral Summary						
Peripheral	NTSC/PAL	eMagin 10-bit Mono	8-BIT YCbCr	8-BIT YCbCr (BT.656)	USB video	16-Bit Parallel Digital Video
Smart Front End		x	x	x	x	x
Base Configuration		x	x	x	x	x
Core Configuration	x	x	x	x	x	x

Product Evaluation Kit	x				x	

6.1 Power Supply Electrical Characteristics

The PEK configuration can be powered via the input power or the VBUS input. When VBUS is connected in this configuration the Input power port will be disabled. Hot swap switching between both inputs is supported, however VBUS has priority. Additional power requirements are listed in Table 6-2. The power supply ripple specification is measured in milli volts, peak to peak and applies to input power when it is not driven by a battery. Inrush current in Table 6-2 applies to power up conditions where either input power or VBUS power is applied. Table 6-2 lists the maximum power dissipated by NTSC/PAL video, this power figure is not included within the steady state power measurement also found in Table 6-2.

Table 6-2: PEK configuration power supplies

Parameter	**Description**	**Min**	**Typ.**	**Max**	**Units**
Input power	Input voltage	2.0	3.0	3.8	V
	Current	-	420	460	mA
VBUS	Input voltage	4.75	5.0	5.25	V
	Current	-	310	350	mA
NTSC/PAL power		-	-	200	mw
Inrush current		-	-	1800	mA
Steady state power		0.95	1.1	1.2	W
Power supply ripple		-	+/-10	+/-15	mV P-P

6.2 PEK connector descriptions

The following section describes details of J2 - J7 connectors. Figure 5-2 shows the orientation of the connectors J2 - J7. Table 6-3 and Table 6-4 provide additional details on the connectors including connector component details and electrical signal descriptions.

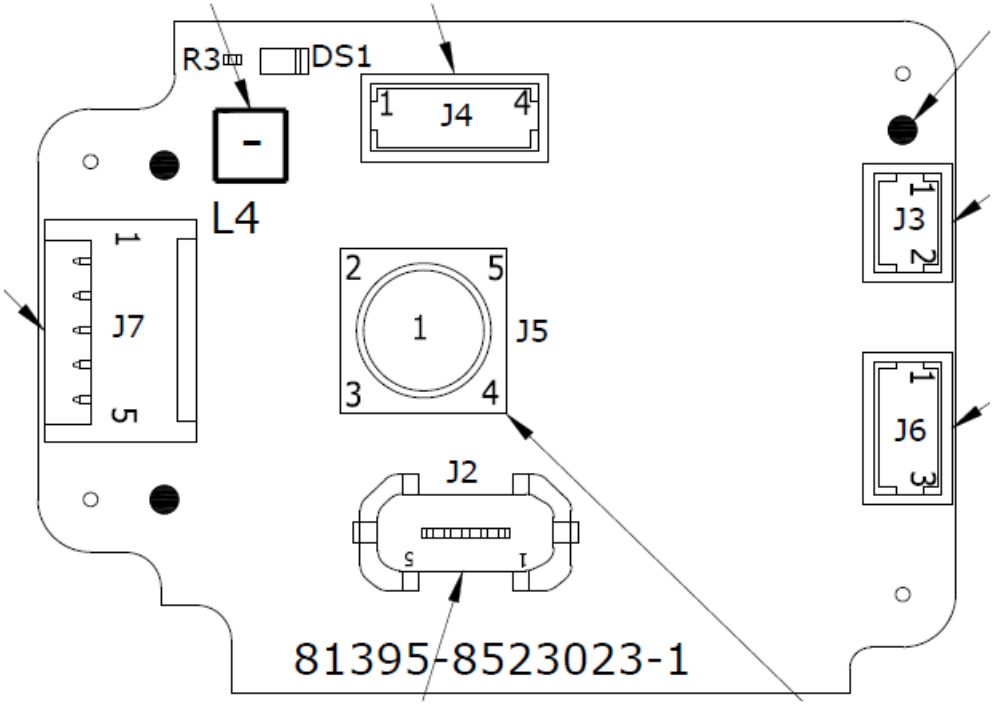

Figure 6-2: Evaluation Board

Table 6-3 Evaluation board connector information

Ref Des	Function	Manufacturer	MFR part number
J2	USB	Hirose	ZX80-B-5P(01)
J3	Input power	Molex	53047-0210
J4	UART	Molex	53047-0410
J5	NTSC/PAL	Cinch Connectivity	133-8701-211
J7	Shutter	Molex	53048-0510

Table 6-4 Evaluation board electrical Interface

J2 USB Interface				
Pin	**Net Name**	**Function**	Value	**Description**
1	VBUS	PWR	-	5.0V input DC power rail
2	UP_USB_DM	I/O	5.0V	USB negative differential data
3	UP_USB_DP	I/O	5.0V	USB Positive differential data
4	Reserved	N/A	-	No connect
5	GND	GND	-	Digital power return
J3 External power Interface				
Pin	**Net Name**	**Function**	**Type**	**Description**
1	INPUT_POWER	PWR	-	DC Input power
2	DGND	GND	-	Digital power return
J4 UART Interface				
Pin	**Net Name**	**Function**	**Type**	**Description**
1	UART_RX	I	3.3V	UART receiver
2	UART_TX	O	3.3V	UART transmitter
3	3_3V	PWR	-	3_3V DC power rail
4	GND	GND	-	Digital power return
J5 NTSC/PAL Interface				
Pin	**Net Name**	**Function**	**Type**	**Description**
1	VIDOUT	O	-	75 ohm analog video
2	A_GND	A_GND	-	Analog power return
3	A_GND	A_GND	-	Analog power return
4	A_GND	A_GND	-	Analog power return
5	A_GND	A_GND	-	Analog power return
J7 NanoMotion Shutter Interface				
Pin	**Net Name**	**Function**	**Type**	**Description**
1	UP_I2C_SCL_0	O	3.3V	I2C digital I2C clock

2	UP_I2C_SDA_1	I/O	3.3V	I2C digital I2C data
3	SHUTTER_RESET	O	3.3V	Shutter reset control
4	DGND	GND		Digital power return
5	3_3V	PWR		3_3V DC power rail

6.3 Serial communications

The PEK can be controlled via ASCII commands through serial interfaces through either the USB or UART ports. If communication via USB is desired, connect the micro USB cable to J2 and plug the other end of the cable into the desired device. The UART and the USB ASCII interface are considered the same from a system's point of view, and all ASCII output is output through both ports.

7. Video Formats

This section contains the technical details of the video formats supported by all the TWV640 configurations.

7.1 eMagin VGA 10-bit Monochrome

The TWV640 supports an eMagin VGA 10-bit Monochrome display. The DISPLAY_RD bus provides 10-bits of data to the eMagin display with DISPLAY_RD0 as the LSB and DISPLAY_RD9 as the MSB. The TWV640 also provides multiple control signals to the eMagin in order for the display to operate correctly. While operating within the Smart Front End configuration, the users system must provide all necessary power supplies to the eMagin. For additional information regarding the eMagin display see the referenced documentation D01-500649-05.

7.2 8-Bit YCbCr

This video format provides 8 digital data signals that contain 8-bit YCbCr encoded data progressively; these signals are described in Table 7-1. A dedicated clock signal is also provided that varies in frequency depending on the operation mode of the camera, specifications of the clock can be found in Table 7-2. In this video mode the horizontal and vertical sync signals are embedded within data bits. Additional details of the horizontal and vertical sync codes and timing information can be found in Figure 7-1 and Figure 7-2. For design details and additional information on the YCbCr compression method please review the ITU-R BT.601-7 document.

Table 7-1 8-bit YCbCr signal descriptions

8-bit YCbCr	Description
DISPLAY_RD0	Data bit 0 (LSB)
DISPLAY_RD1	Data bit 1
DISPLAY_RD2	Data bit 2
DISPLAY_RD3	Data bit 3
DISPLAY_RD4	Data bit 4
DISPLAY_RD5	Data bit 5
DISPLAY_RD6	Data bit 6
DISPLAY_RD7	Data bit 7 (MSB)
DISPLAY_SRCCLK	Clock

Table 7-2 8-bit YCbCr signal descriptions

Timing Parameter	30 Hz			60 Hz			Unit
	Min	typ	Max	min	typ	max	
T_{clock}	-	40.741	-	-	20.370		ns
Clock duty cycle	45	50	55	45	50	55	%
Max clock jitter	-	-	650	-	-	650	ps
$T_{co\ (delay\ until\ data\ is\ valid)}$	-4	-	+4	-4	-	+4	ns
T_{line_active}	-	52.148	-	-	26.074	-	us
T_{line_blank}	-	11.407	-	-	5.704	-	us
T_{line_total}	-	63.556	-	-	31.778	-	us
T_{frame_active}	-	30.507	-	-	15.253	-	ms
T_{frame_blank}	-	2.860	-	-	1.430	-	ms
T_{frame_total}	-	33.367	-	-	16.683	-	ms

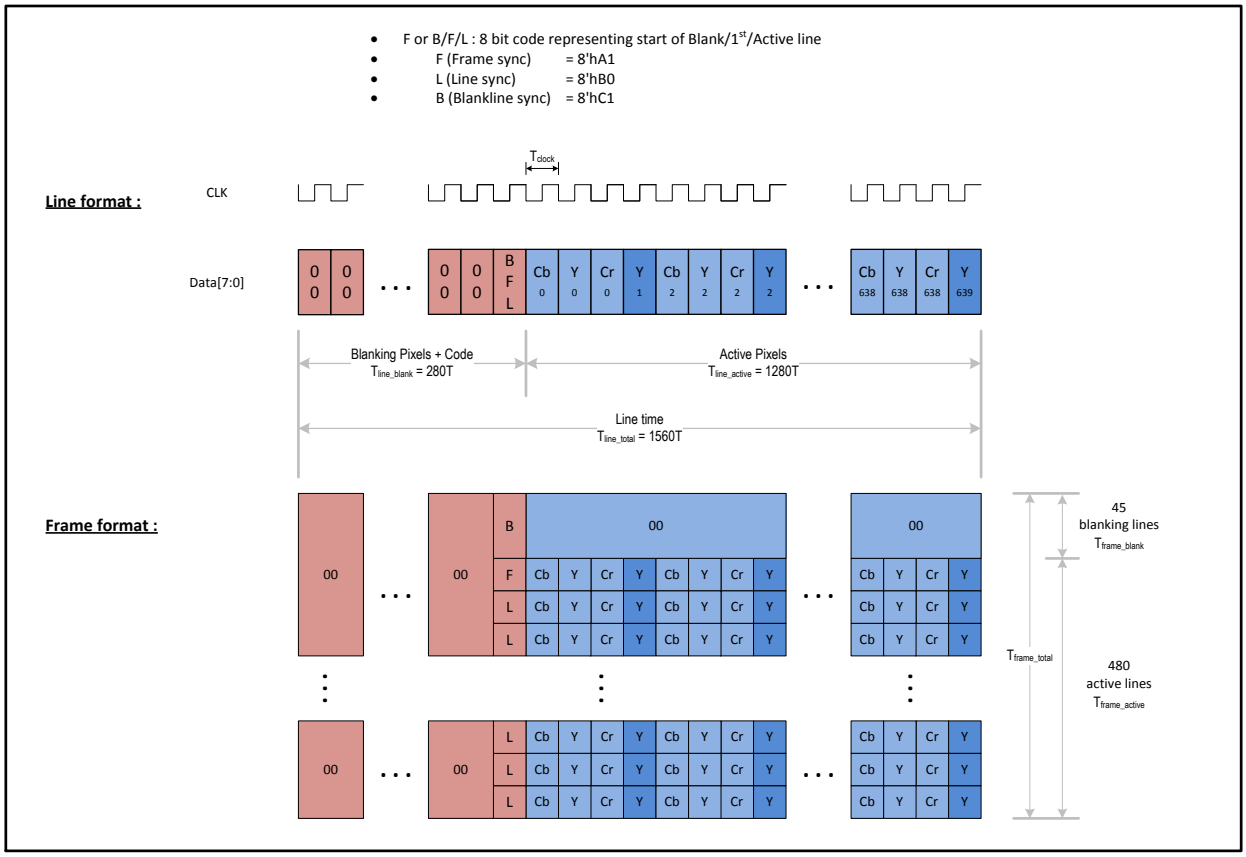

Figure 7-1 - YCbCr timing diagram

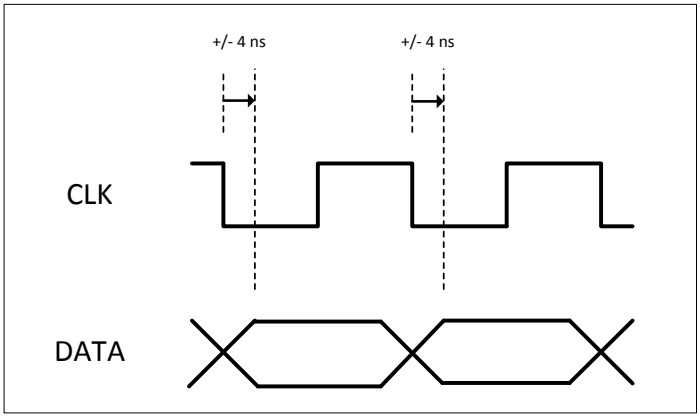

Figure 7-2: 8-bit YCbCr Clock to data

7.3 8-bit YCbCr (BT.656)

This video format provides 8 digital data signals that contain 8-bit YCbCr encoded data in an interlaced format; these signals are described in Table 7-3. A dedicated 27 MHz clock signal is also provided and its specifications can be found in Table 7-4. In this video mode the horizontal and vertical sync signals are embedded within the EAV/SAV codes. Additional information can be found on the EAV/SAV codes as well as timing information can be found in Figure 7-4 and Figure 7-4. For design details and additional information on the YCbCr or BT.656 compression method please review the ITU-R BT.601-7 document. This video format is intended to drive an Analog devices AD7391 analog video encoder IC for systems that require a user designed interface board, but also require an NTSC/PAL output.

Table 7-3 8-bit YCbCr signal descriptions

8-bit YCbCr	Description
DISPLAY_GN0	Data bit 0 (LSB)
DISPLAY_GN1	Data bit 1
DISPLAY_GN2	Data bit 2
DISPLAY_GN3	Data bit 3
DISPLAY_GN4	Data bit 4
DISPLAY_GN5	Data bit 5
DISPLAY_GN6	Data bit 6
DISPLAY_GN7	Data bit 7 (MSB)
DISPLAY_GN8	Clock

Table 7-4: 8-bit YCbCr signal descriptions

Timing Parameter	NTSC			PAL			Unit
	min	typ	max	min	typ	max	
T_{clock}	-	37.037	-	-	37.037	-	ns
Clock duty cycle	45	50	55	45	50	55	%
Max clock jitter	-650	-	650	-650	-	650	ps
T_{co} (delay until data is valid)	-4	-	+4	-4	-	+4	ns
T_{line_active}	-	53.333	-	-	53.333	-	us
T_{line_blank}	-	10.222	-	-	10.667	-	us
T_{line_total}	-	63.556	-	-	64.000	-	us
T_{frame_total}	-	33.367	-	-	40.000	-	ms

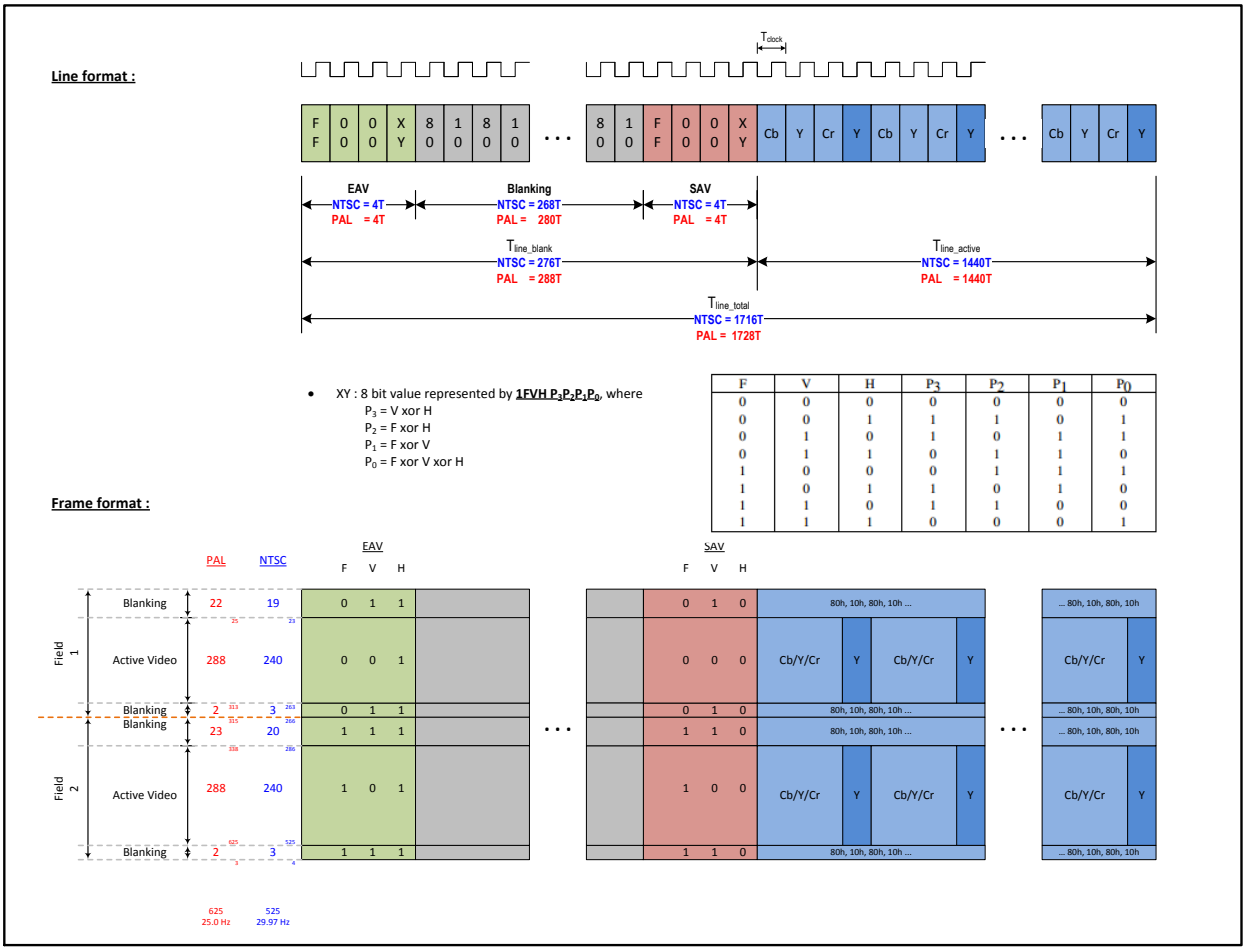

Figure 7-3: YCbCr Clock to data

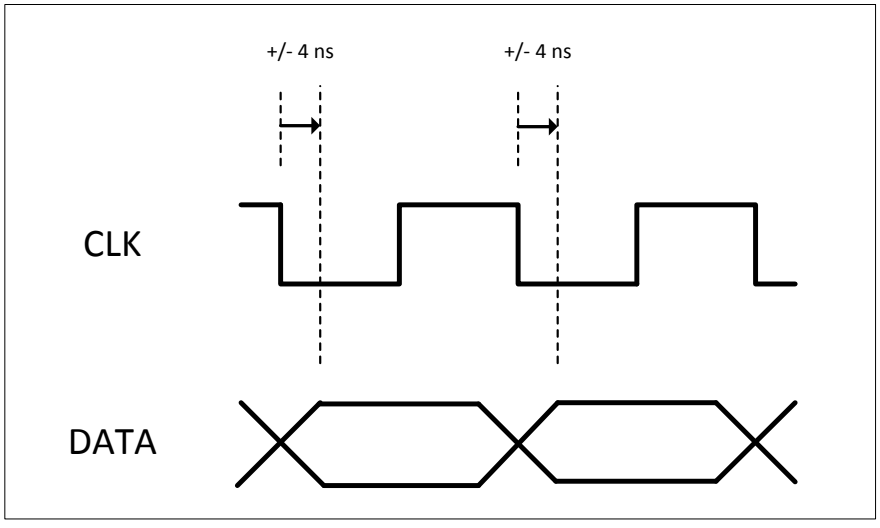

Figure 7-4: YCbCr (BT.656) Clock to data

7.4 USB Raw

USB raw video is provided via the 2-wire USB port and is offered in 16-bit and 24-bit color modes. USB video may be sub 30/60Hz depending on bit depth and color information being used and may not provide consecutive frames in some formats. USB must be used with the BAE commercial GUI. Please see the referenced software ICD for more details regarding USB video and the commercial GUI.

7.5 NTSC/PAL video

NTSC / PAL video formats are available via an SMB style connector. The NTSC / PAL output intended to drive a NTSC / PAL compatible device with a 75 ohm impedance BNC cable. This video format offers a cable detection mode that will disable the NTSC / PAL output if the cable is disconnected from the camera.

7.6 16-bit Parallel Digital video

The TWV640 family of products supports three different modes of 16-bit Parallel Digital video output referred to auto, manual and raw in the Table 7-7. Auto and manual provide 640x480 video in the 16-bit data format post and pre contrast enhanced respectively while the raw output provides coarse offset corrected 664x520 video. The output consists of 16 data signals, a frame valid, a data valid and a clock signal. The 16 data signals provide 16-bit video in parallel with respect to the line valid, data valid and a 24.5454 MHz clock signal, all signals associated with 16-bit video are described within Table 7-5. The necessary digital timing specifications and clock to out timing can be found in the Table 7-6. The 16-bit parallel digital video does not support vertical flip, color, frame capture or frame review functionality. 16-bit parallel digital video is only supported in 60Hz operation.

Table 7-5: 16-bit parallel digital signal description

16-bit Parallel Digital video	Description
DISPLAY_RD0	Data bit 0 (LSB)
DISPLAY_RD1	Data bit 1
DISPLAY_RD2	Data bit 2
DISPLAY_RD3	Data bit 3
DISPLAY_RD4	Data bit 4
DISPLAY_RD5	Data bit 5
DISPLAY_RD6	Data bit 6
DISPLAY_RD7	Data bit 7
DISPLAY_RD8	Data bit 8
DISPLAY_RD9	Data bit 9
DISPLAY_BL1	Data bit 10
DISPLAY_BL2	Data bit 11

16-bit Parallel Digital video	Description
DISPLAY_BL3	Data bit 12
DISPLAY_BL4	Data bit 13
DISPLAY_BL5	Data bit 14
DISPLAY_BL6	Data bit 15 (MSB)
DISPLAY_BL7	Data valid
DISPLAY_VSYNC	Frame valid
DISPLAY_HSYNC	Line valid
DISPLAY_SRCCLK	24.5454 MHz CLK

Table 7-6: 16-bit parallel digital clock to data timing

Timing Parameter	min	typ	max	Unit	Notes
T_{clock}	-	40.741	-	ns	24.5454 MHz, Typ
Pixel Clock duty cycle	45	50	55	%	
Max clock jitter T_{clock}	-650	-	650	ps	
T_{co}	-4	-	+4	ns	
T_{line_active}	-	26.074	-	us	video_16bit auto video_16bit manual
	-	27.052	-	us	video_16bit raw
T_{line_blank}	-	5.704	-	us	video_16bit auto video_16bit manual
	-	4.726	-	us	video_16bit raw
T_{frame_active}	-	15.25	-	ms	video_16bit auto video_16bit manual
	-	16.52	-	ms	video_16bit auto video_16bit manual
T_{frame_blank}	-	1.43	-	ms	video_16bit auto video_16bit manual
	-	0.16	-	ms	video_16bit raw
T_{frame_total}	-	16.68	-	ms	video_16bit auto video_16bit manual video_16bit raw

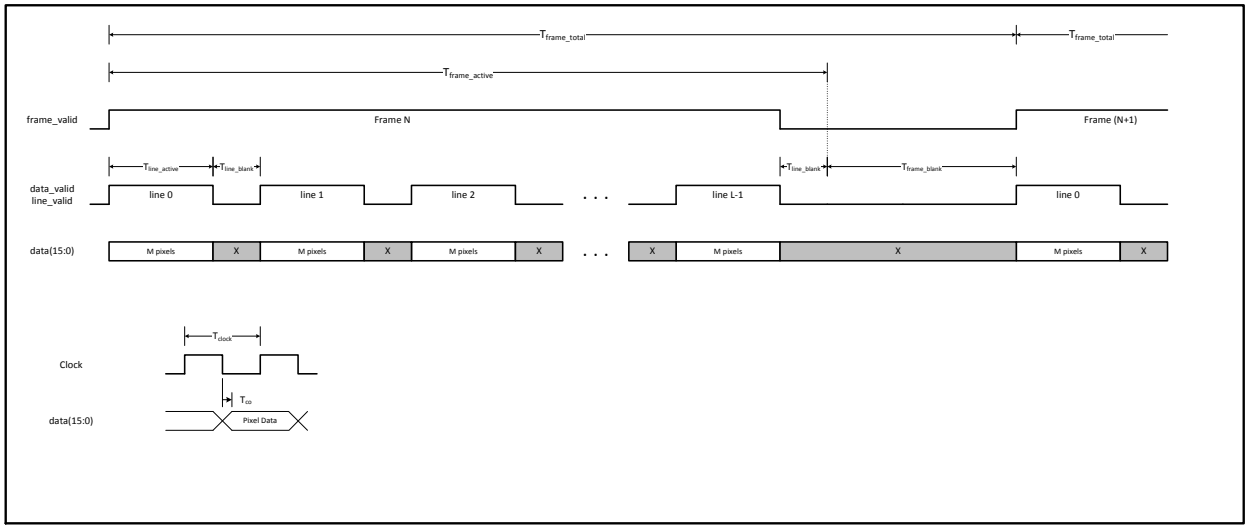

Figure 7-5: 16-bit parallel digital clock to data diagram

Table 7-7: 16-bit parallel digital clock to data timing

command	# of pixels/line M	# of lines/frame L
video_16bit auto	640	480
video_16bit manual	640	480
video_16bit raw	664	520

Review the software ICD for additional information

7.7 Simultaneous video outputs

This section will identify the video formats that can be utilized at the same time, due to pin constraints. It is important to note that USB video is intended as a standalone video format and therefore it cannot operate with any other output.

Table 7-8: 8-bit YCbCr signal descriptions

	eMagin 10-bit Monochrome	8-bit YCbCr	NTSC/PAL	8-bit YCbCr (BT.656)	16-bit parallel digital video
Video mode 1					
Video mode 2					
Video mode 3					
Video mode 4					
Video mode 5					