SVGA050 Series
Low-Power AMOLED Microdisplay

Datasheet

V1.2

SVGA050SC

SVGA050SW

SVGA050SG

For Products:

SVGA050SCV1R1	—	Full Color
SVGA050SWV1R1	—	Monochrome White
SVGA050SGV1R1	—	Monochrome Green

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April 14, 2020

Record of Revision

Version	Revise Date	Page	Content
Pre-spec. V0.1	2011-10-13		Initial release.
V1.0	2013-05-21		Update to official version
V1.1	2014-01-27		Added19H register description，added temperature sensor description
V1.2	2020-04-14		Revise some description.

Contents

1. FEATURES

- Si-Base AMOLED Microdisplay
  - 0.18μm CMOS Technology
  - Full Digital Video Core
  - High Efficiency Top Emission Structure
  - Active Driver Technology
  - Low Power Consumption
- 800×600 (SVGA) Resolution
  - View Area: 0.5 inch
  - Pixel Pitch : 12.6μm
  - Total Pixels : 804 (×3)× 604
- Digital Video Interface
  - Compatible with ITU-R BT.656/601
  - Accept 8/16/24 Bit Digital Video
  - Accept YCbCr/RGB Color or Mono
  - Support Progressive & Interlaced
- Digital Video Signal Enhancement
  - Brightness
  - Contrast
  - R/G/B Offset
- Gamma Correction
  - Piecewise Linear by 17 Entry LUTs
  - Expand 8bit Input to 9bit Output
- Digital 8 Bit Input/9bit Output Gray Level
- Support Binocular Stereovision
- Horizontal/Vertical Mirror
- Shift and Position Control
- Embed Temperature Sensor
- Integrate Vcom DC-DC Module
- Built-in Test Patterns
- 2-Wire Series Interface

SVGA	050	S	C	V1	R1
①	②	③	④	⑤	⑥

①Type	
SVGA	800×600
SXGA	1280×1024

③Temperature	
S	Standard：-40℃～+60℃
N	Normal：-10℃～+40℃

⑤Connector	
V1	Board to board
V2	FPC

②Size	
050	0.5 inch
060	0.6 inch

④Color	
C	Full Color
W	Mono White
G	Mono Green

⑥Revision	
R1	Revision No.

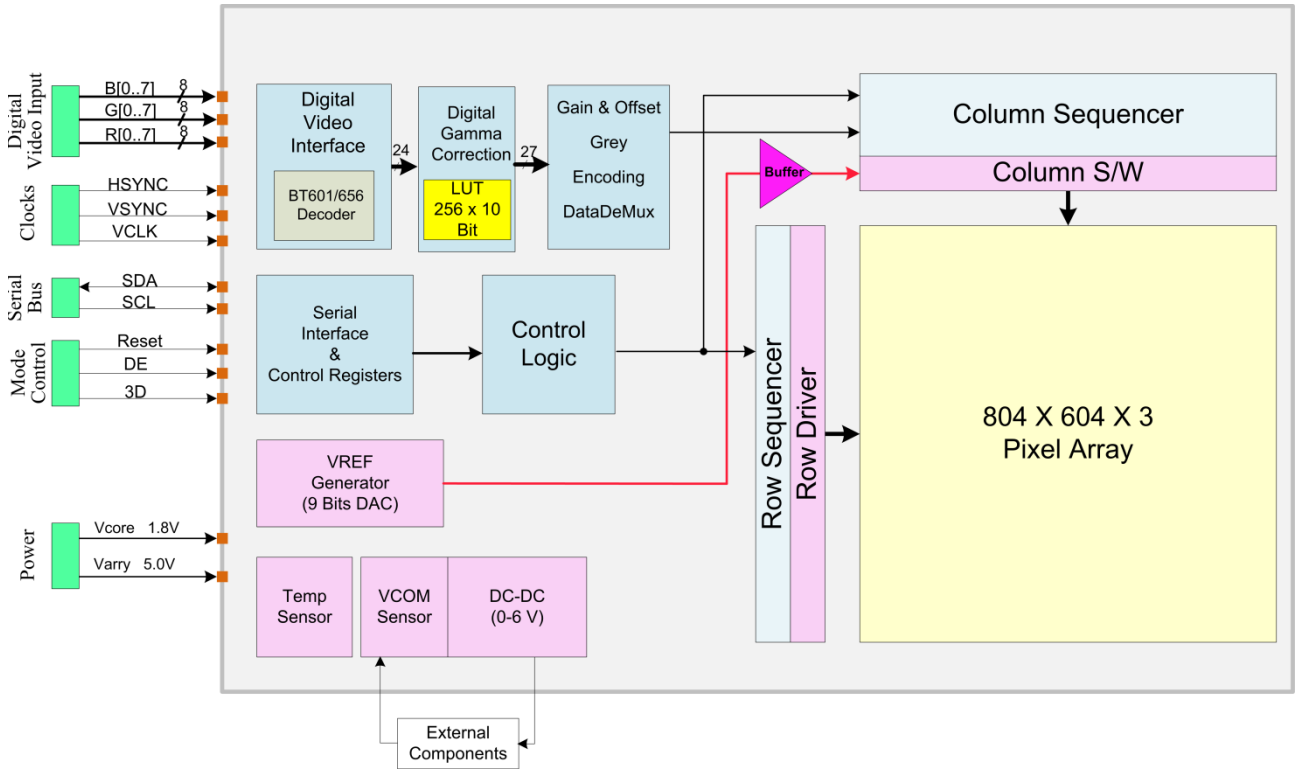
2. GENERAL DESCRIPTION

2.1. SVGA050SV1R1 Microdisplay

Product Type		SVGA050SCV1R1	SVGA050SWV1R1	SVGA050SGV1R1
Resolution		804 (×3) × 604		
Active pixels		804 (×3) × 604		
Pixel Aspect Ratio		1:1		
Color Pixel Arrangement		RGB Vertical Stripe		
Gray Levels		8bits/256Levels		
Luminance Uniformity		> 90%		
Contrast		> 10000:1		
Digital Video Interface		ITU-R BT.601/656 24-bit 4:4:4 RGB/YCbCr 16-bit 4:2:2 YCbCr 8-bit 4:2:2 YCbCr/Mono		
Operating Temperature	Standard	-40℃ ～ +65℃		
	Normal	-10℃ ～ +40℃		
Chromaticity	White	CIEx=0.30±0.05, CIEy=0.35±0.05		
	Green	CIEx=0.30±0.05, CIEy=0.63±0.05		
Operating Humidity		≤85%RH (Non condensing)		
Pixel Size(μm²)		12.6 × 12.6		
Viewing Area(mm²)		10.13 × 7.61		
Mechanical Envelope(mm³)		22 × 17 × 4.6		
Typical Luminance(Cd/m²)		70	100	500
Typical Power Consumption(mW) ①		120	100	200
Power Supply	Digital core	DC 1.8V @ Max50mA		
	OLED array	DC 5.0V@Max200mA		
Weight(g)		≤ 2		

Note①: Measuring method refer to section 2.6.2

2.2. Functional Overview



2.3. Pixel Array

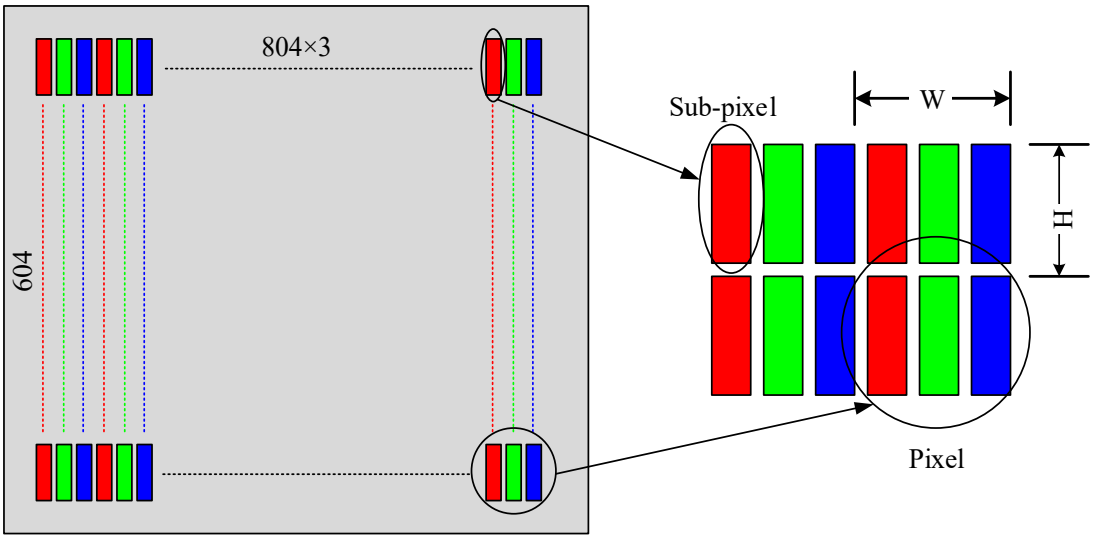


Figure 2-1 Pixel and Sub-Pixel Array

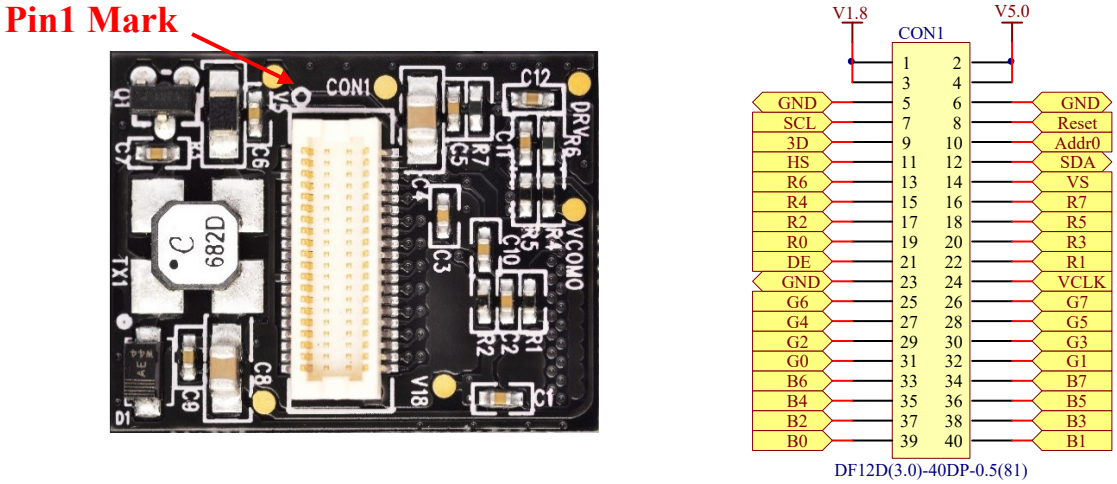
Each pixel of OLiGHTEK's SVGA050 series AMOLED microdisplay is formed by three sub-pixels (Figure 2-1). The pixel's related parameters are shown below:

Model	Pixel Size		Duty Cycle	View Area	
	Width(W)	Height(H)		Width（804×W）	Height（604×H）
SVGA050	12.6μm	12.6μm	70%	10.13mm	7.61mm

2.4. Interface

2.4.1. Pin Assignment

Part number of the connector: Hirose DF12D(3.0)-40DP-0.5 (0.5mm pitch 40 ways).



2.4.2. Pin Definition

Pin	Symbol	I/O	Function	Remark
1	V1.8	P	1.8V Power Supply	
3	V1.8	P	1.8V Power Supply	
5	GND	P	Power groung	
7	SCL	I	Serial port clock line	Pull-up to 1.8V
9	3D	I	3D L/R Signal input	
11	Hs	I	Hsync Signal input	
13	R6	I	Video Data Input R[6]	
15	R4	I	Video Data Input R[4]	
17	R2	I	Video Data Input R[2]	
19	R0	I	Video Data Input R[0]_LSB	
21	DE	I	Data enable signal input	
23	GND	P	Power groung	
25	G6	I	Video Data Input G[6]	
27	G4	I	Video Data Input G[4]	
29	G2	I	Video Data Input G[2]	
31	G0	I	Video Data Input G[0]_LSB	
33	B6	I	Video Data Input B[6]	
35	B4	I	Video Data Input B[4]	
37	B2	I	Video Data Input B[2]	
39	B0	I	Video Data Input B[0]_LSB	

Pin	Symbol	I/O	Function	Remark
2	V5.0	P	5V Power Supply	
4	V5.0	P	5V Power Supply	
6	GND	P	Power groung	
8	Reset	I	Master reset, active low	Can not float
10	Addr0	I	Seiral port Address A0	Pull-up to 1.8V
12	SDA	I/O	Serial port data line	Pull-up to 1.8V
14	Vs	I	Hsync Signal input	
16	R7	I	Video Data Input R[7]_MSB	
18	R5	I	Video Data Input R[5]	
20	R3	I	Video Data Input R[3]	
22	R1	I	Video Data Input R[1]	
24	VCLK	I	Pixel clock input	
26	G7	I	Video Data Input G[7]_MSB	
28	G5	I	Video Data Input G[5]	
30	G3	I	Video Data Input G[3]	
32	G1	I	Video Data Input G[1]	
34	B7	I	Video Data Input B[7]_MSB	
36	B5	I	Video Data Input B[5]	
38	B3	I	Video Data Input B[3]	
40	B1	I	Video Data Input B[1]	

2.4.3. Video Formats

Video Data Formate	Color Space	R[7:0]	G[7:0]	B[7:0]
8-bit, 4:2:2	YCbCr	--	YCbCr[7:0]	--
8-bit, Mono	Y	--	Y[7:0]	--
16-bit, 4:2:2	YCbCr	--	Y[7:0]	CbCr[7:0]
24-bit, 4:4:4	YCbCr	Cr[7:0]	Y[7:0]	Cb[7:0]
24-bit, 4:4:4	RGB	R[7:0]	G[7:0]	B[7:0]

2.5. Timing Characteristics

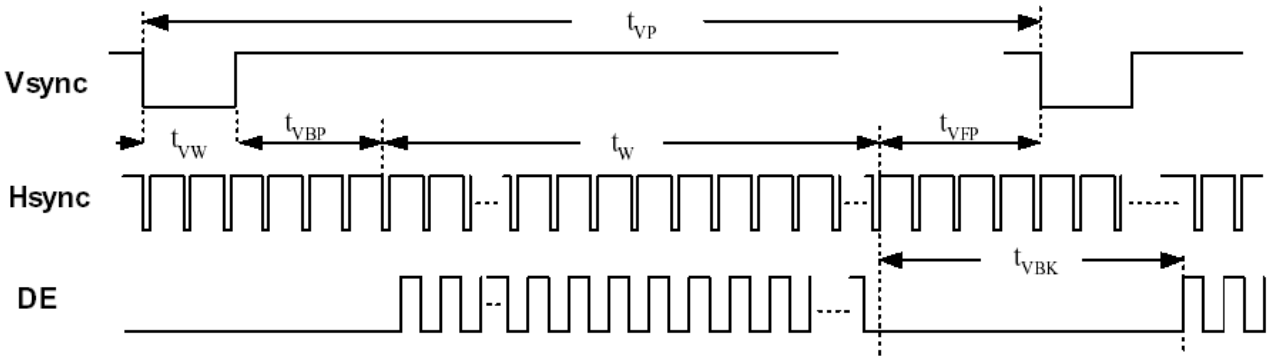


Figure 2-2 Input Sync Signals Timing (For All Formats)

Table 2-1 SVGA Video Timing Characateristics

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Clock Frequency	f_{CLK}		40		MHz	SVGA@60Hz frame rate
HSYNC Period	t_{HP}	660			t_{CLK}	
HSYNC Pulse Width	t_{HW}	10			t_{CLK}	
HSYNC Back Porch	t_{HBP}	10			t_{CLK}	
Horizontal Valid data width	t_{HV}	296		804	t_{CLK}	
HSYNC Front Porch	t_{HFP}	60			t_{CLK}	t_{HV} >= 580
Horizontal Blank	t_{HBK}	80			t_{CLK}	
VSYNC Period	t_{VP}	106			t_{HP}	
VSYNC Pulse Width	t_{VW}	1			t_{HP}	
VSYNC Back Porch	t_{VBP}	7			t_{HP}	
Vertical valid data width	t_W	96		604	t_{HP}	
Vertical Front Porch	t_{VFP}	2			t_{HP}	
Vertical Blank	t_{VBK}	10			t_{HP}	

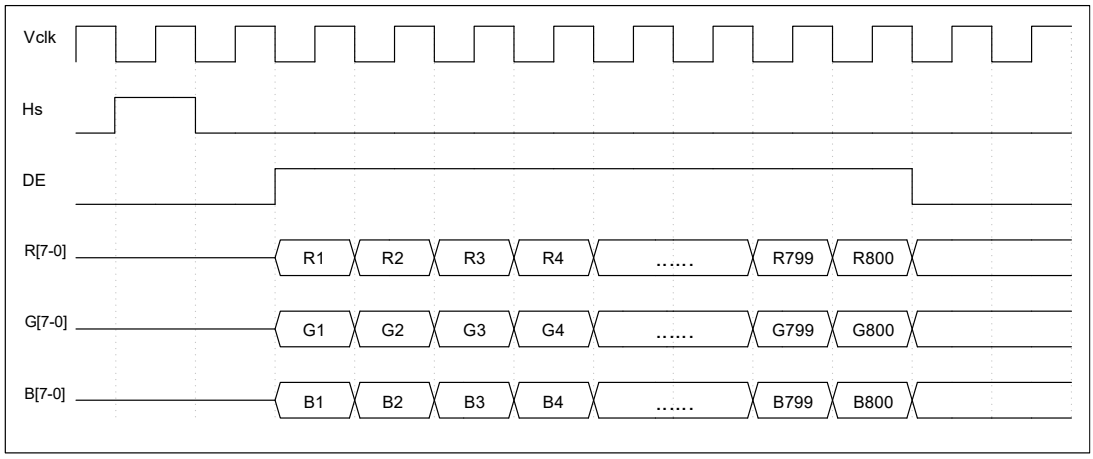


Figure 2-3 24-bit 4:4:4 RGB Input VideoTiming

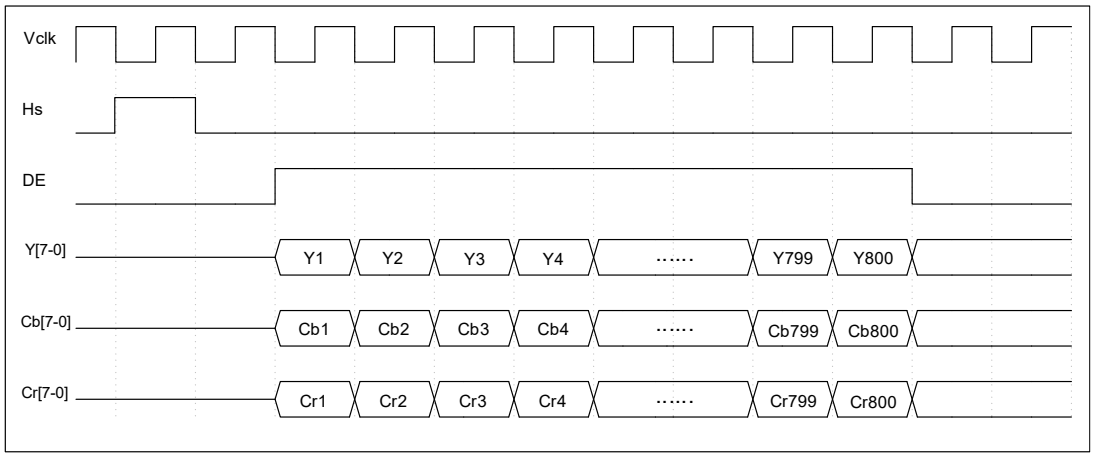


Figure 2-4 24-bit 4:4:4 YCbCr Input Video Timing

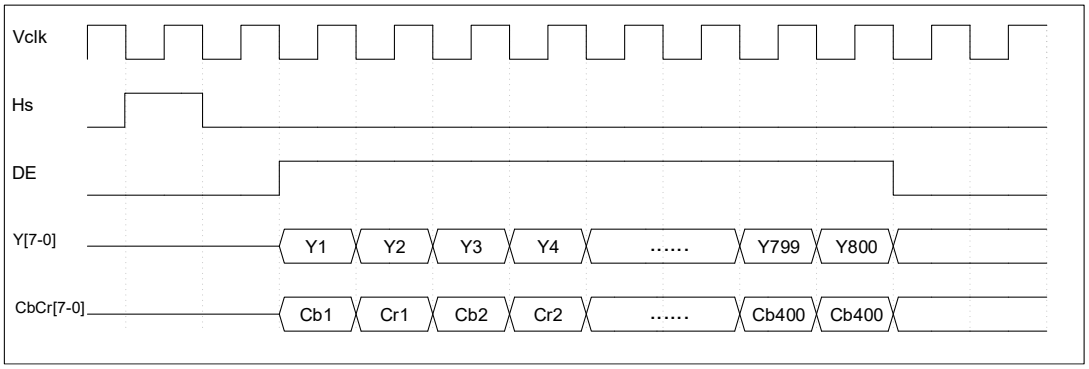


Figure 2-5 16-bit 4:2:2 YCbCr Input Video Timing

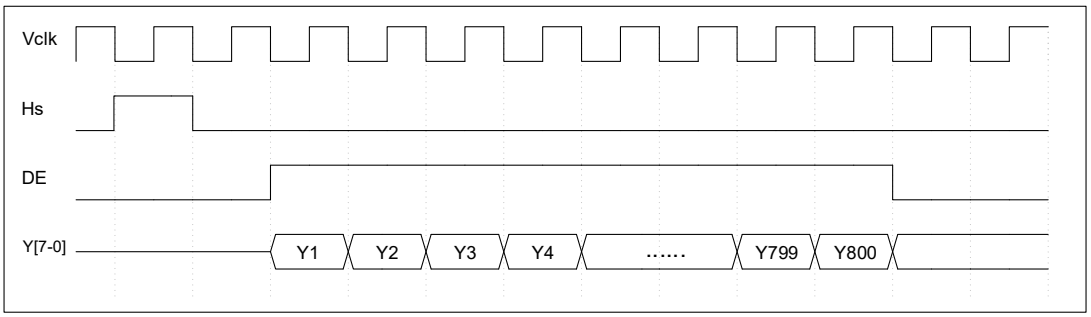


Figure 2-6 8-bit Mono Input Video Timing

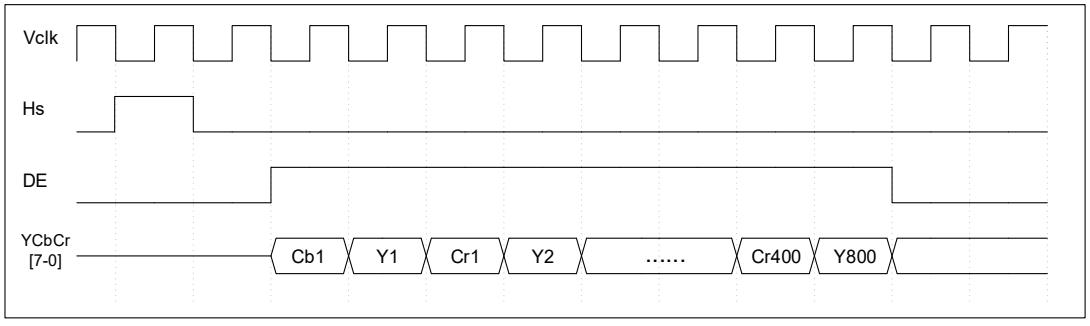


Figure 2-7 8-bit 4:2:2 YCbCr input Video timing

Table 2-2 VESA Progressive Video Timing Specifications

Mode		Frequency	Total	Active	Front Porch + Border	Sync Pulse	Back Porch + Border
SVGA 800X600 85Hz non-interlaced	H	53.674 KHz	1048 pixels	800 pixels	32 pixels	64 pixels	152 pixels
	V	85.061 Hz	631 lines	600 lines	1 line	3 lines	27 lines
	P	56.250 MHz					
SVGA 800X600 75Hz non-interlaced	H	46.875 KHz	1056 pixels	800 pixels	16 pixels	80 pixels	160 pixels
	V	75.000 Hz	625 lines	600 lines	1 line	3 lines	21 lines
	P	49.500 MHz					
SVGA 800X600 72Hz non-interlaced	H	48.077 KHz	1040 pixels	800 pixels	56 pixels	120 pixels	64 pixels
	V	72.188 Hz	666 lines	600 lines	37 line	6 lines	23 lines
	P	50.000 MHz					
SVGA 800X600 60Hz non-interlaced	H	37.879 KHz	1056 pixels	800 pixels	40 pixels	128 pixels	88 pixels
	V	60.317 Hz	628 lines	600 lines	1 line	4 lines	23 lines
	P	40.000 MHz					
VGA 640X480 85Hz non-interlaced	H	43.269 KHz	832 pixels	640 pixels	56 pixels	56 pixels	80 pixels
	V	85.008 Hz	509 lines	480 lines	1 line	3 lines	25 lines
	P	36.000 MHz					
VGA 640X480 75Hz non-interlaced	H	37.500 KHz	840 pixels	640 pixels	16 pixels	64 pixels	120 pixels
	V	75.000 Hz	500 lines	480 lines	1 line	3 lines	16 lines
	P	31.500 MHz					
VGA 640X480 72Hz non-interlaced	H	37.861 KHz	832 pixels	640 pixels	24 pixels	40 pixels	128 pixels
	V	72.809 Hz	520 lines	480 lines	9 line	3 lines	28 lines
	P	31.500 MHz					
VGA 640X480 60Hz non-interlaced	H	31.469 KHz	800 pixels	640 pixels	16 pixels	96 pixels	48 pixels
	V	59.940 Hz	525 lines	480 lines	10 line	2 lines	33 lines
	P	25.175 MHz					

Note: For more details please refer to the VESA Monitor Timing Standard

Table 2-3 VESA interlaced Video Timing Specifications

Mode		Frequency	Total	Active
MPTE-170M-1 640X480 Mono 30Hz interlaced	H	15.734 KHz	780 pixels	640 pixels
	V	60 Hz Field	262.5 lines	240 lines
	P	12.27 MHz		
SMPTE-170M-2 800X600 Mono 25Hz interlaced	H	15.625 KHz	1052 pixels	800 pixels
	V	50 Hz Field	312.5 lines	600 lines
	P	16.437 MHz		
NTSC 720X480 Color 30Hz interlaced	H	15.734 KHz	858 pixels	720 pixels
	V	60 Hz Field	262.5 lines	240 lines
	P	13.5 MHz		
PAL 720X576 Color 25Hz interlaced	H	15.625 KHz	864 pixels	720 pixels
	V	50 Hz Field	312.5 lines	288 lines
	P	13.5 MHz		
NTSC (Square) 640X480 Color 30Hz interlaced	H	15.734 KHz	780 pixels	640 pixels
	V	60 Hz Field	262.5 lines	240 lines
	P	12.2727 MHz		
PAL (Square) 768X576 Color 25Hz interlaced	H	15.625 KHz	944 pixels	768 pixels
	V	50 Hz Field	312.5 lines	288 lines
	P	14.75 MHz		

2.6. Electrical Characteristics

2.6.1. Recommended Operation Ratings

SYMBOL	DESCRIPTION	MIN	TYP	MAX①	UNIT
V1.8	1.8V Power Supply	1.62	1.8	2.5	V
V5.0	5.0V Power Supply	4.5	5.0	6.0	V
$V_{I/O}$	Digital Signal Voltage	—	1.8	3.3	V
Tstorage	Storage Temperature	-55	20	90	℃
Toperate	Operation Temperature	-40	20	65	℃

Note①:The absolute maximum rating values (except $V_{I/O}$) of this product are not allowed to be exceeded at any time. If the product is used with its symbol value exceeding the maximum rating or in an extreme condition, the characteristics of the device maybe recovered and the lifetime of the device will decrease, even the device may be permanently destroyed.

2.6.2. DC Characteristics

Table 2-4 SVGA050V1R1 DC Characteristics

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNIT
$I_{1.8}$	1.8V Supply Current		9	10	12	mA
$I_{5.0}$	5.0V Supply Current		10	20	250	mA
Vcom	Cathode Voltage		-5	-2	0	V
Typical Power Consumption①	Working	Color @ 70Cd/m2	-	120	-	mW
		Monochrome White @ 100Cd/m2	-	100	-	
		Monochrome Green @ 500Cd/m2	-	200	-	
	Display Off		-	-	75	
	Power Down		0	-	0.4	

Note ①:Power consumption measured at 60Hz refresh rate, room ambient temperature and with a full white test pattern(all pixels on) see

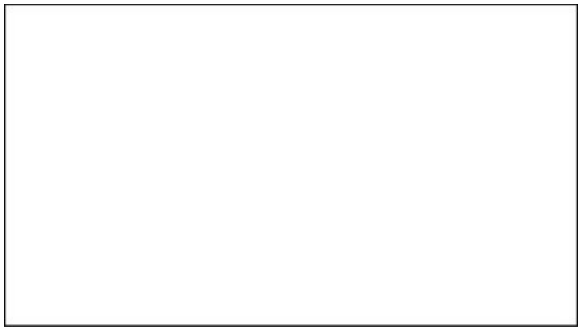
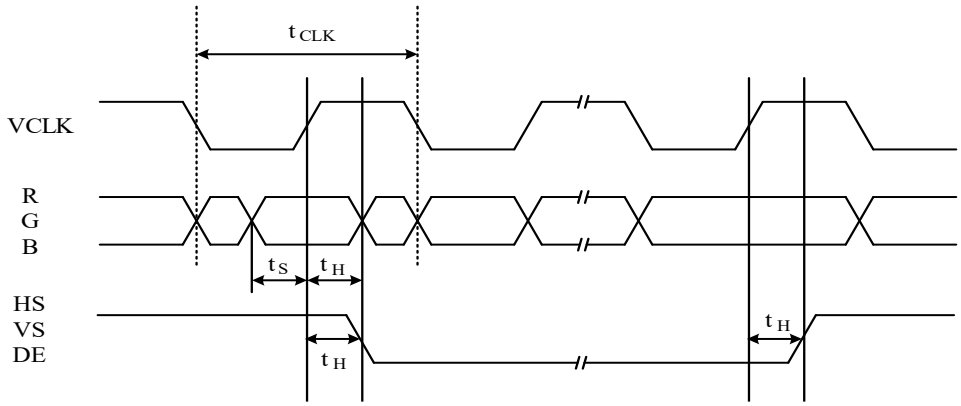


Figure 2-8 Full white test pattern

2.6.3. AC Characteristics



PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Digital Video Data Setup & Hold	t_S	1	-	-	ns
	t_H	0.5	-	-	ns
Video Clock Period	t_{CLK}	17.8	-	-	ns
Video Clock Duty	q	40	50	60	%

3. DETAILED FUNCTION DESCRIPTION

3.1. Digital Video Interface

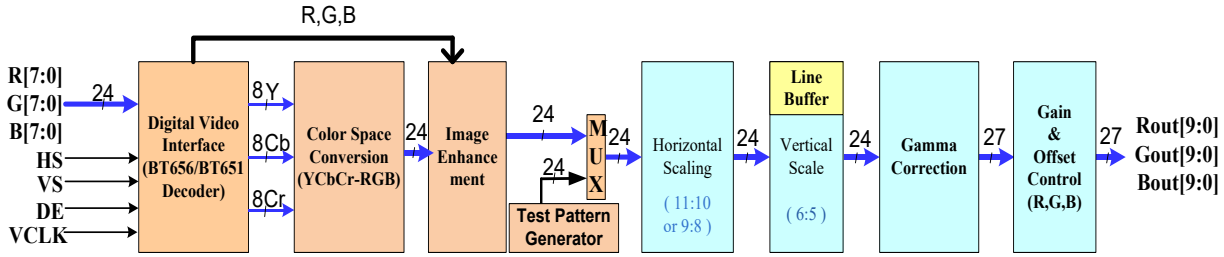


Figure 3-1 Digital Video Processing Flow Diagram

The digital video interface has three 8-bit data channels, and additional horizontal and vertical sync (HS/VS), data enable (DE), pixel clock signals (VCLK). User should select the correct signals to connect according to different Video format. VCLK is always needed in any mode. When use 8bit with embedded sync signal (8bit ITU-R BT.656 YCbCr/Mono 4:2:2), only G[7..0] bus and VCLK is needed.

OLED Display receives data with BT601/656 format, like 8/16/24bit and 4:2:2/4:4:4 format, and transfers to 24bit RGB signal, then sends the signal to Video signal enhancement module, after scaling (only a scaled-down), gamma correction, RGB offset adjustment, finally output 27bit RGB signal.

3.1.1. Color Space

If the input data format is YCbCr, the device will change it to RGB format. Color space conversion block converts color space from YCbCr to RGB and uses the following equations. Output signal is

24-bit RGB format, 8-bit in each path.

$$R = 1.164 \times (Y - 16) + 1.596 \times (Cr - 128)$$
$$G = 1.164 \times (Y - 16) - 0.813 \times (Cr - 128) - 0.392 \times (Cb - 128)$$
$$B = 1.164 \times (Y - 16) + 2.017 \times (Cb - 128)$$

3.1.2. Digital Video Signal Enhancement

Digital video signal enhancement can be achieved by adjusting the brightness and the contrast ratio, as is Shown in Figure 3-2.

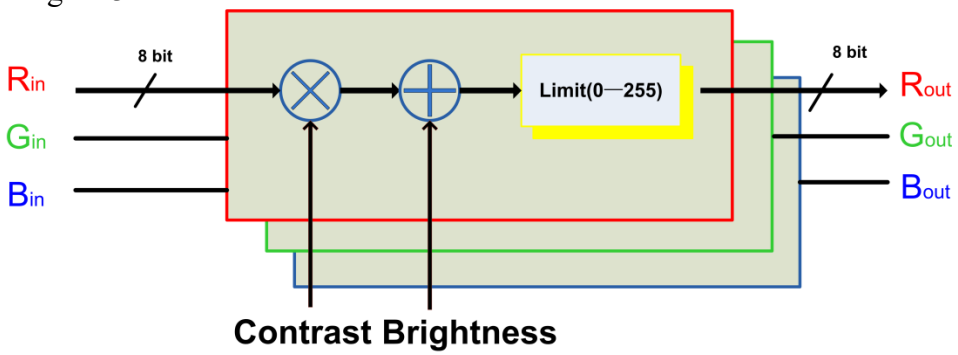


Figure 3-2 Digital Video Signal Enhancement Diagram

Brightness adjustment using addition and subtraction to achieve, the output value is equal to the input value plus the value of register 08H, and then minus 128. When the value of register 08H is greater than 80H, it means increase the brightness, whereas decrease. Brightness adjustment range is ±128.

$$V_{out} = V_{in} + Reg(08H) - 128$$

Contrast adjustment using multiplication and division to achieve, the output value is equal to the input value multiplied by the value of register 09H and then divided by 128. When the value of register 09H is greater than 80H, it means increase the contrast, whereas decrease. The gain of contrast adjustment range is 0 to 2.

$$V_{out} = V_{in} \cdot \frac{Reg(09H)}{128}$$

Note: The algorithms keep only 8bit data, if overflow, automatically discarded high bit.

3.1.3. Video Pattern Generation

Built-in test pattern generator can generate color bars, gray scale, tiles, horizontal stripes, vertical stripes, as well as monochrome red, green, blue, and white test pattern. Line width, line spacing, foreground color, background color, etc. of all test pattern can be set by relevant registers. Register 4AH is pattern mode selection, default value is 0, indicates the test pattern generator is turned off; register 4BH, 4CH, 4DH were used to set line width, line spacing, etc. respectively. Details of setting refer to Table 3-1 and Figure 3-3

Table 3-1 Summary of Test Pattern Setting

Test Pattern Name	Patterns (4AH)	LineWidth (4BH)	LineSpace (4CH)	BGMASK (4DH)	FGMASK (4DH)
Color Bar	001	-	-	-	-
Gray Scale	010	-	-	-	-
Checker Board	011	-	-	-	-
Alternating Column	100	LineWide	Line Space	000	111
Alternating Row	101	LineWide	Line Space	000	111
Alternating Row & Column	110	LineWide	Line Space	000	111
All Black	100	-	-	000	000
All White	100	-	-	111	111
All Red	100	-	-	100	100
All Green	100	-	-	010	010
All Blue	100	-	-	001	001

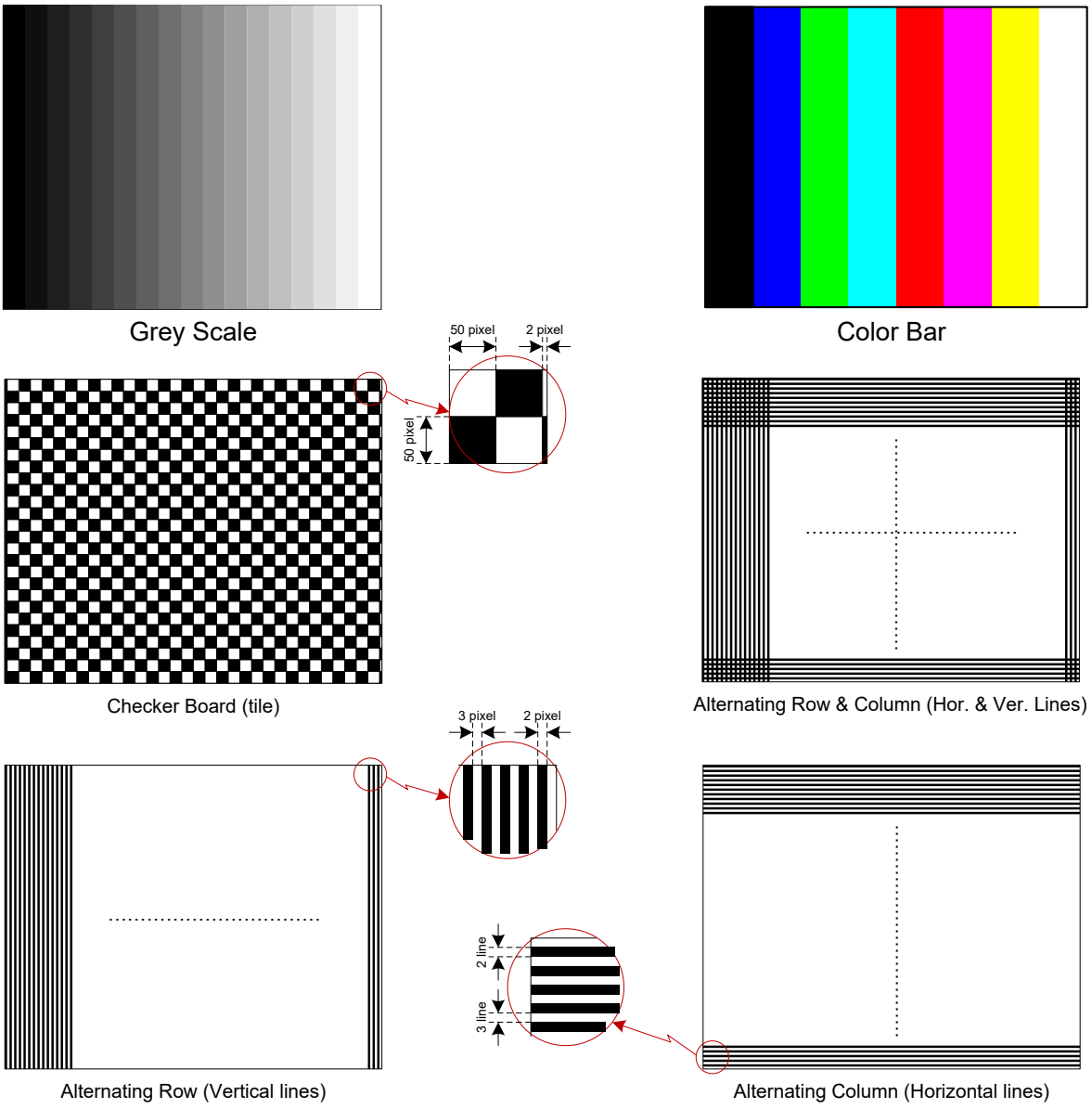


Figure 3-3 Test Video Patterns

3.1.4. Scaling

In order to maintain the aspect ratio of input image, some video format in need of scaling. Scaling could be achieved by set register 07H, the algorithm is shown in Figure 3-4 and Figure 3-5, applicable video format is shown in Table 3-2.

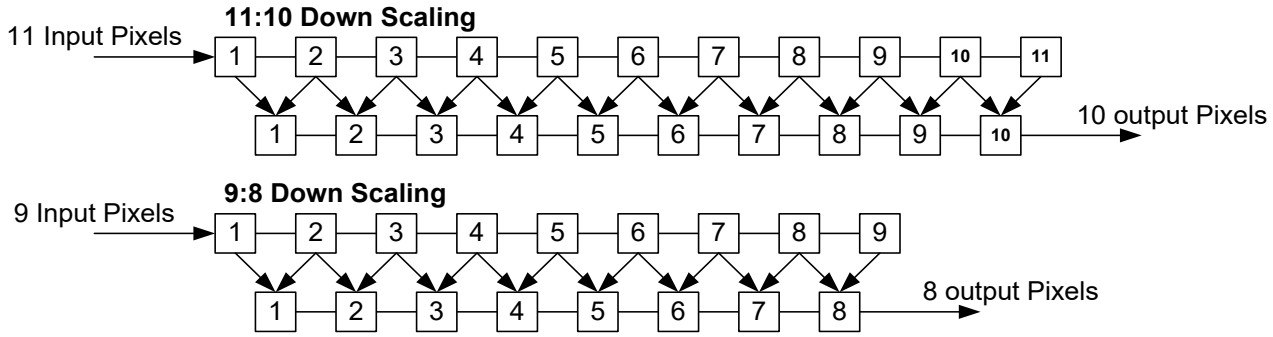


Figure 3-4 Diagram of the Horizontal Scaling Algorithm

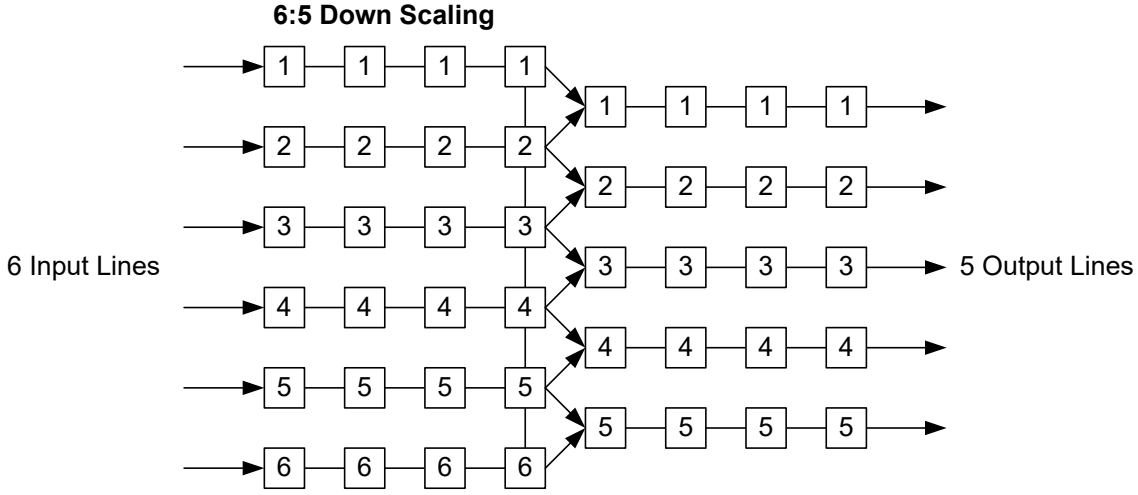


Figure 3-5 Diagram of the Vertical Scaling Algorithm

Table 3-2 Scaling format applied

Video Format Name	Input Resolution	Scan Mode	Hor. Scaling	Ver. Scaling	Display Resolution
SVGA	800 × 600	Progressive	1:1	1:1	800 × 600
VGA	640 × 480	Progressive	1:1	1:1	640 × 480
SMPTE-170M-2	800 × 600 Mono	Interlaced	1:1	1:1	800 × 600
SMPTE-170M-1	640 × 480 Mono	Interlaced	1:1	1:1	640 × 480
NTSC	720 × 480	Interlaced	11:10/9:8	1:1	640 × 480
NTSC (Square)	640 × 480	Interlaced	1:1	1:1	640 × 480
PAL (Square)	768 × 576 Color	Interlaced	1:1	1:1	768 × 576
PAL	720 × 576	Interlaced	11:10/9:8	6:5	640 × 480

3.1.5. Gamma Correction

Gamma correction is performed using piecewise-linear function by a 17-entry lookup table. Gamma correction expends 8 bit input to 9 bit output by Look-Up Table (LUT). Intermediate values are computed by interpolating between the two nearest LUT entries. In C notation:

$$\mathbf{V_{out} = LUT[V_{in}/16] + V_{in}\%16 * (LUT[V_{in}/16 + 1] - LUT[V_{in}/16])/16}$$

Note:

- *'/' denotes integer division truncating the remainder, '*' denotes multiplication, '%' denotes integer division taking remainder*
- *LUT[0~15] is 9 bit register to support the full 0-511 range without missing codes.*
- *LUT[16] is 10 bit register to support 201H~3FEH range, set to "200H" as maximum value (512) and "3FFH" as minimum value (-1).*

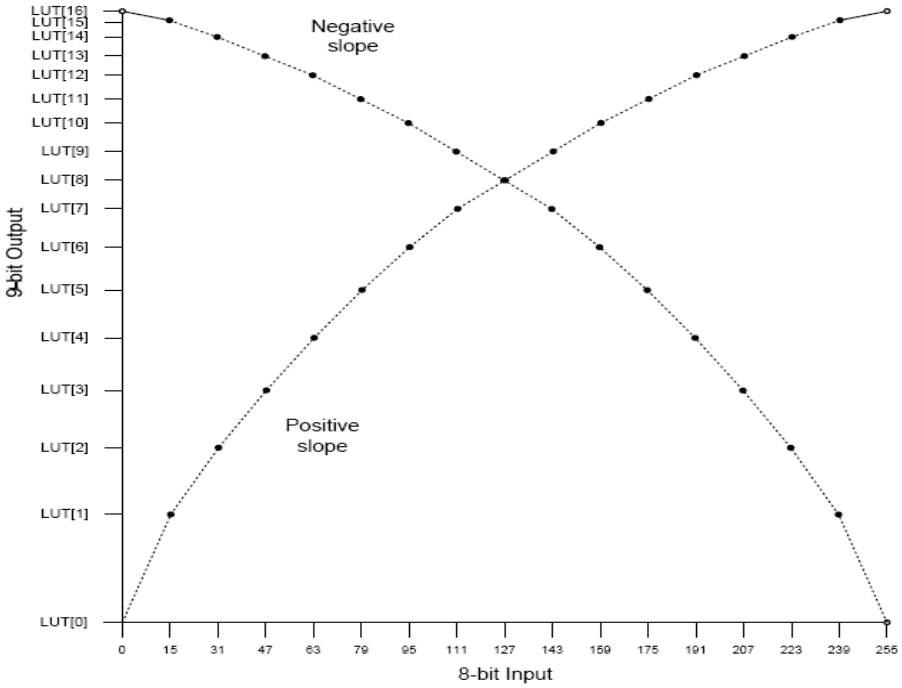


Figure 3-6 Gamma Correction LUT and Curve

3.1.6. RGB offset

After gamma correction process, the corrected R/G/B value can be shifted separately by Roffset, Goffset, Boffset configuration registers, color offset control registers 44H-49H are used to adjust separate R/G/B signal's offset. Gamma correction output 9bit data each channel, color offset adjustment range is 0~511.

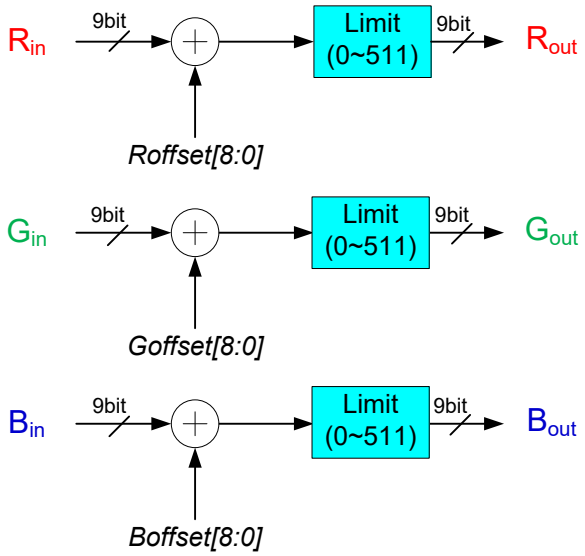


Figure 3-7 Color Offset Control

3.2. 3D Video Display

Stereo register(02H) and 3DMODE pin can set 3D video display. If 3DMODE pin state is the same as the ST_mode bit (02H) value, the screen display is updated, whereas not. 3DMODE pin signal is latched at Vsync falling edge. 3D video display timing is shown below.

In progressive mode, 3D video signal using frame timing mode, such as the odd frame is updated left display, and the even frame is updated right display.

In interlaced mode, 3D video signal using field timing mode, such as the odd field is updated left display, and the even field is updated right display. At this point, the vertical resolution of each field is lower compare with the source, the last two bit of register 01H should be set to “11”, display will repeat to display each line in next line automatically, to ensure that the image aspect ratio and display.

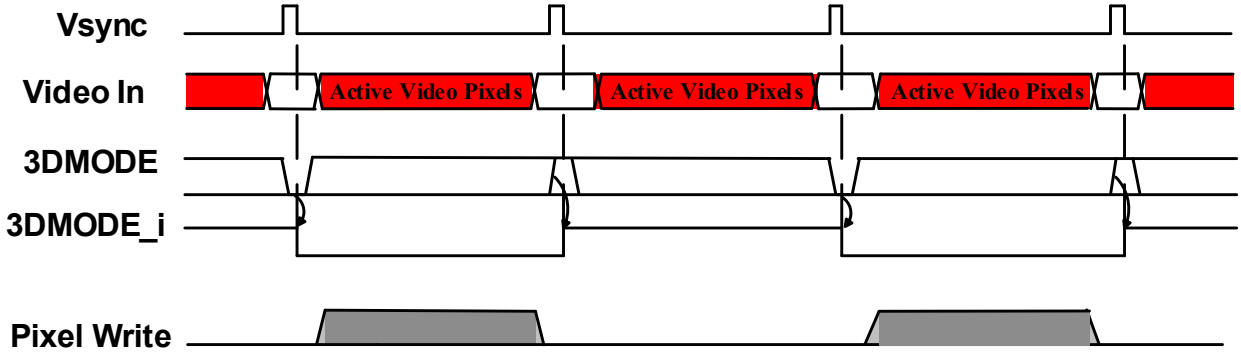


Figure 3-8 3D Video Display Timing

3.3. Power Supply & Reset

SVGA050 series microdisplay need 1.8V and 5V external power supply to operate, 1.8V is used for digital core include decoder, video signal enhancement, gamma correction, communication, etc.; 5V is used for drive circuit, D/A converter, and so on. To ensure the display image quality, please note that ripple and interference rejection of 5V power supply.

3.3.1. Power UP/Down Sequence

The system power-up mechanism relies on the clock single(VCLK), so the power supply and VCLK input sequence is very important. SVGA050 repquires first provide VCLK, followed is 1.8v, and last is 5V. The working principle is shown by following figure and section 3.3.2.

If the power-up sequence can not meet requirements, SVGA050's working state may abnormal. In that case, after the reset and initialization operations, user can set the PDOWN(Register 0FH_Bit7) to 1 firt, and wait 20ms , then set PDOWN to 0.

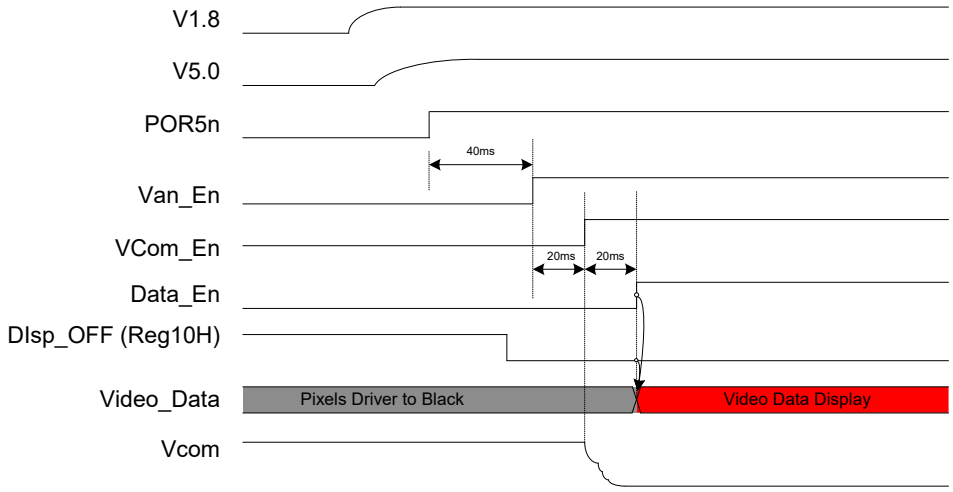


Figure 3-9 Power-up Sequence (1.8V power-up, threshold voltage = 1.2V)

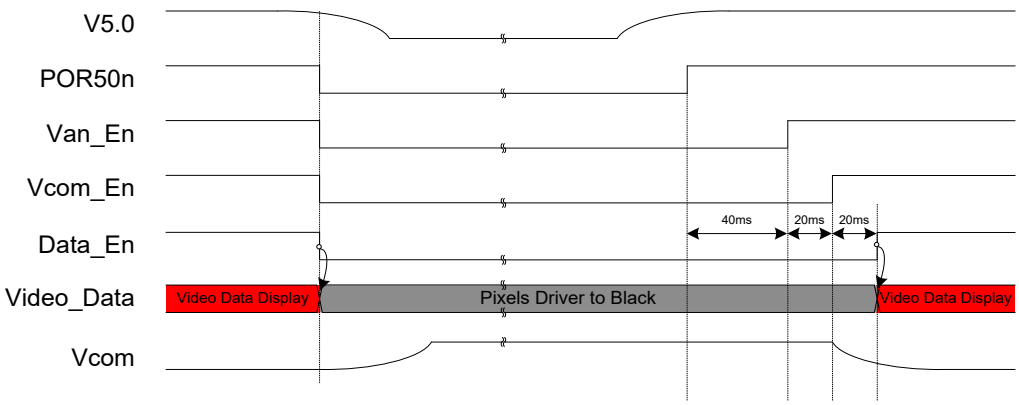


Figure 3-10 V5.0 Power Down & Up (POR5n threshold Voltage = 4V)

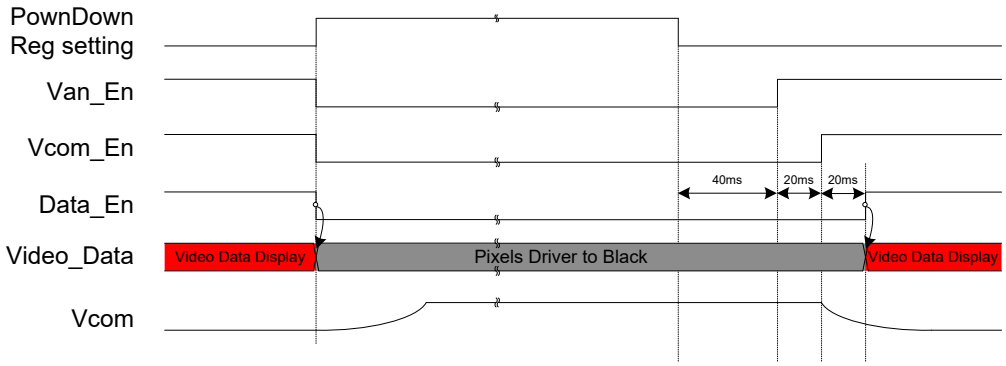


Figure 3-11 Register Control Power Down & Up

3.3.2. Reset Sequence

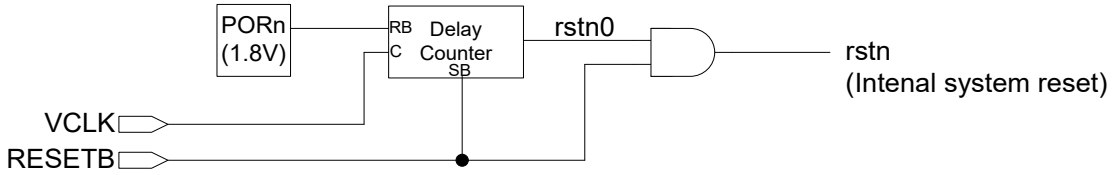


Figure 3-12 Reset Block Diagram

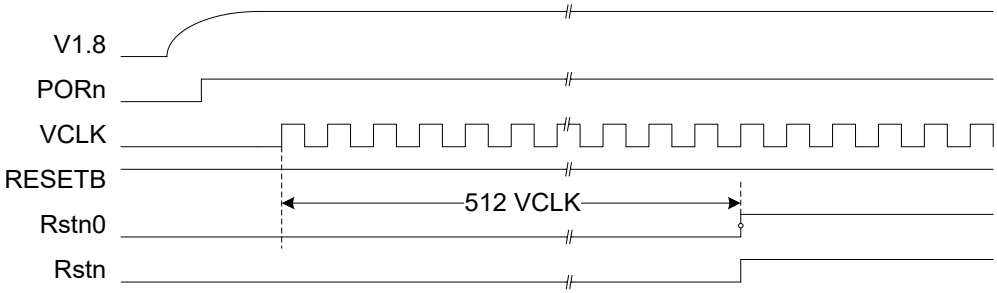


Figure 3-13 Reset Timing Case 1 – No external reset pin used (RESETB=1)

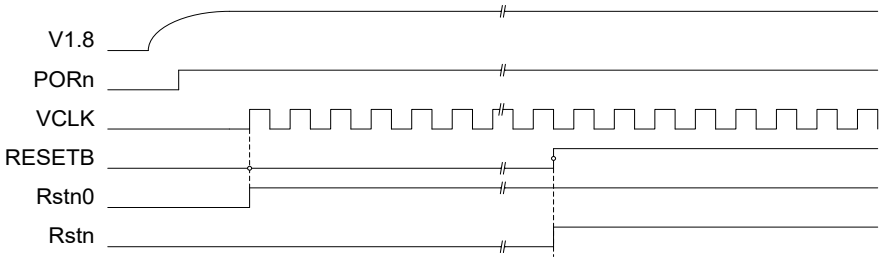


Figure 3-14 Reset Timing Case 2 – External reset pin depend on VCLK

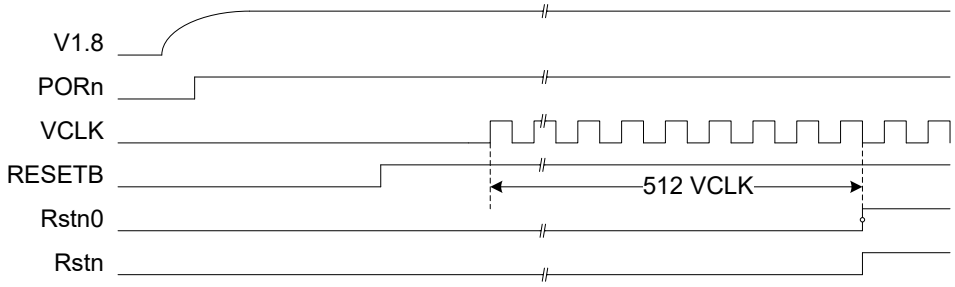


Figure 3-15 Reset Timing Case 3 – External reset pin applied

3.4. DC/DC Converter

OLED emitting light needs to be applied positive bias voltage between the anode and cathode, the anode voltage from 5V power supply is controlled by drive transistor, all pixel's common cathode voltage Vcom supplied by DC/DC converter on the PCB backplane. The driving pulse of DC/DC converter is generated by the internal programmable pulse generator, the circuit shown in Figure 3-16. Vcom adjustment range is 0 ~-3V, corresponding to register 19H, the typical working curve is shown in Figure 3-17

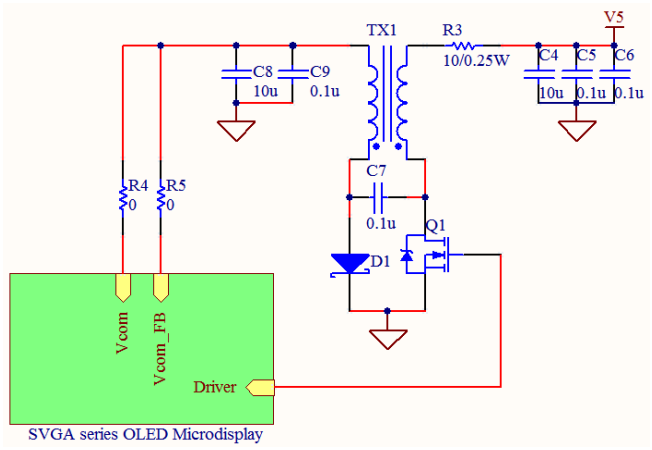


Figure 3-16 DC/DC Principal Diagram

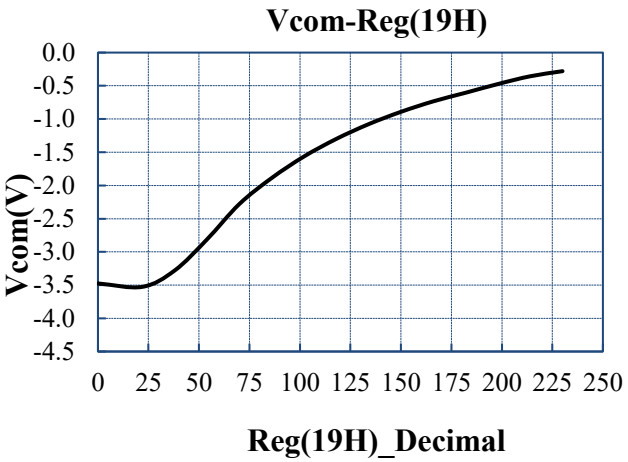


Figure 3-17 Vcom Programmable Working Curve

3.5. Temperature Sensor

The value of register 1DH is the internal temperature sensor's measured value. So the real-time internal working temperature can be read out through the two-wire serial interface. The temperature and the readout conversion relation is:

$$T = 0.47 \times \text{Reg}\ (1DH) - 40$$

The temperature sensor response curve and the calibration curve are shown as Figure 3-18 and Figure 3-19.

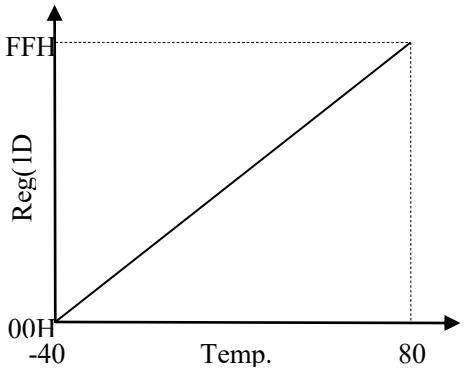


Figure 3-18 Temp. Sensor Readout

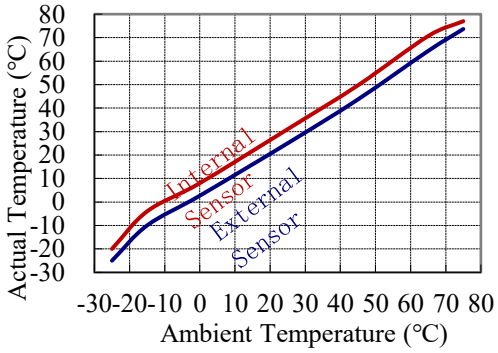


Figure 3-19 Temp. Sensor calibration curve

Note: Temperature sensor in SVGA050 series display updates readings (1DH register value) depending on field sync signal (VS)。 External VS must be provided to ensure the inner temperature sensor working properly in 8-bit BT.656 format application embedded sync signal.

3.6. Two-wire Serial Interface

Compatible with I^2C communication standard, the two-wire serial interface is used to read/write the registers to realize the display programmable control, such as digital video signal decoding and processing, gamma correction, Vcom adjustment and so on.

SVGA050 series microdisplay acts as a slave for receiving and transmitting data, all read/write operations must be launched by the master. The SDA and SCL line must be pull-up to1.8v or 3.3v power via a resistance by the outside communication controller.

Key Features and tag:

- Communication speed (SCL) support from 100K to 1MHz;
- 8-bits Slave Address consists of 7-bits device address and 1-bit read/write flag;
- Start/Re-Start: SDA change from HIGH to LOW while SCL is HIGH, See Figure 3-20;
- Stop: SDA change from LOW to HIGH while SCL is HIGH, see Figure 3-20;
- ACK: SDA is LOW during the acknowledge clock pulse;
- NAK: SDA is HIGH during the acknowledge clock pulse;
- One transmission includes 8bit data and an acknowledge bit, total nine clock of SCL;
- Except Start and Stop condition:
  - HIGH or LOW state of SDA can only being changed while SCL is LOW
  - Data on the SDA line must be stable during the HIGH period of the SCL

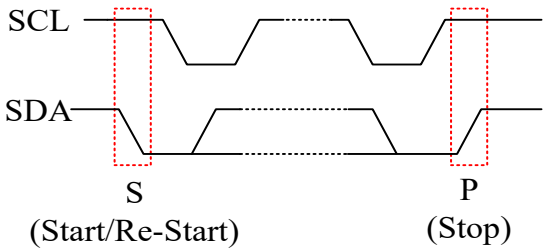


Figure 3-20 Start & Stop Timing

3.6.1. Communication Operating

- Write data (Figure 3-21) :
  1) Master sends Start condition (S)
  2) Master sends 7bit Slave Address and 1bit write flag ($\overline{W}$) represents as low
  3) Slave sends 1bit ACK (A) response
  4) Master sends 8bit register address (Register)
  5) Slave sends 1bit ACK (A) response
  6) Master sends 8bit data (Data)
  7) Slave sends 1bit ACK (A) response
  8) Master sends stop condition(P)

S	Slave Addr	$\overline{W}$	A	Register	A	Data	A	P

Figure 3-21 Write Data format

- Read Data (Figure 3-22)
  1) Master sends Start condition (S)
  2) Master sends 7bit Slave Address and 1bit Write flag ($\overline{W}$) represents as low
  3) Slave sends ACK (A) response
  4) Master sends 8bit Register Address (Register)
  5) Slave sends 1bit ACK (A) response
  6) Master sends 1bit Re-Start condition (Sr)
  7) Master sends 7bit Slave Address and 1bit Read flag (R) represents as high
  8) Slave sends 1bit ACK (A) response
  9) Slave sends 8bit Data (Data)
  10) Master sends 1bit NAK ($\overline{A}$) response
  11) Master sends Stop condition (P)

S	Slave Addr	$\overline{W}$	A	Register	A	Sr	Slave Addr	R	A	Data	$\overline{A}$	P

Figure 3-22 Data format(Master reads from Slave)

3.6.2. Serial Interface Bus Address Selection

Two salve address of SVGA050 series microdisplay can be selected by an externally SelAdr0 pin. The SelAdr0 pin has an internal pull up resistor (10K) to pull up to 1.8V power. One of microdisplay's SelAdr0 pin must be connected to GND when used in binocular stereovision application. Microdisplay's corresponding read/write address is shown as Table 3-3.

Table 3-3 Slave Address list

A7 (MSB)	A6	A5	A4	A3	A2	A1 (SelAdr0)	A0 (R/$\overline{W}$)	Slave Address (R/$\overline{W}$)
0	0	0	1	1	1	1(Default)	1/0	1FH/1EH
0	0	0	1	1	1	0	1/0	1DH/1CH

4. REGISTER DESCRIPTION

4.1. Summary of Registers

Table 4-1 Summary of Registers

Address	Bytes	Description	Default Value
00H	1	Chip's Drive Circuit Revision	00H
01H	1	Input Video Type Set	34H
02H	1	Sync signal Polarity Set & 3D functions	00H
03H	1	Vertical Blank Lines	00H
04H	1	Horizontal Blank Pixels	00H
05H	1	Adjust Start Active Video Position	01H
06H	1	Field Start Line Position Adjustment For Interlaced Video	00H
07H	1	Down Scaling for NTSC & PAL Video	00H
08H	1	Brightness Control (Video Signal Brightness)	80H
09H	1	Contrast Control (Video Signal Contrast)	80H
0AH	1	Reserved	4AH
0BH	1	Reserved	5AH
0CH	1	Reserved	00H
0DH	1	Reserved	00H
0EH	1	Reserved	00H
0FH	1	Power Down Mode Control	00H
10H	1	Display ON/Off & Scan Directions	04H
11H	1	Display Left Margin	02H
12H	1	Display Right Margin	02H
13H	1	Display Top Margin	02H
14H	1	Display Bottom Margin	02H
15H	1	Reserved	44H
16H	1	D/A Offset Setting	0CH
17H	1	Discharge Current Setting	01H
18H	1	Discharge Enabled Control	00H
19H	1	Vcom Level Setting (Display's Brightness)	FFH
1AH	1	Reserved	1DH
1BH	1	Reserved	74H
1CH	1	Reserved	FFH
1DH	1	Temperature Sensor Readout	-
1E~1FH	2	Reserved	-
[21,20H]	2	9 Bit Gamma Correction LUT0	000H
[23,22H]	2	9 Bit Gamma Correction LUT1	020H
[25,24H]	2	9 Bit Gamma Correction LUT2	040H
[27,26H]	2	9 Bit Gamma Correction LUT3	060H
[29,28H]	2	9 Bit Gamma Correction LUT4	080H
[2B,2AH]	2	9 Bit Gamma Correction LUT5	0A0H
[2D,2CH]	2	9 Bit Gamma Correction LUT6	0C0H
[2F,2EH]	2	9 Bit Gamma Correction LUT7	0E0H

Address	Bytes	Description	Default Value
[31,30H]	2	9 Bit Gamma Correction LUT8	100H
[33,32H]	2	9 Bit Gamma Correction LUT9	120H
[35,34H]	2	9 Bit Gamma Correction LUT10	140H
[37,36H]	2	9 Bit Gamma Correction LUT11	160H
[39,38H]	2	9 Bit Gamma Correction LUT12	180H
[3B,3AH]	2	9 Bit Gamma Correction LUT13	1A0H
[3D,3CH]	2	9 Bit Gamma Correction LUT14	1C0H
[3F,3EH]	2	9 Bit Gamma Correction LUT15	1E0H
[41,40H]	2	10 Bit Gamma Correction LUT16	200H
42H	1	Reserved	-
43H	1	Reserved	-
[45,44H]	2	9 Bit Red Signal Offset	100H
[47,46H]	2	9 Bit Green Signal Offset	100H
[49,48H]	2	9 Bit Blue Signal Offset	100H
4AH	1	Test Pattern Mode Selection	00H
4BH	1	Test Pattern Line Width Setting	02H
4CH	1	Test Pattern Line Space Setting	03H
4DH	1	Test Pattern Foreground & Background Color Setting	07H
4E~FFH	178	Reserved	-

4.2. Detailed Information of Register

1) Revision information (Read Only)

Register Address	7	6	5	4	3	2	1	0
00H	N.A.					Revision		
Default	-					0	0	0

4.2.1. Video Related Registers

2) Input video type set

Register Address	7	6	5	4	3	2	1	0
01H	N.A.	Data Mode			Sync signal		Scan mode	
Default	-	0	1	1	0	1	0	0

- Signal Mode: Select input data format

Data Mode	Input Video Format
000	16-bit 422, YCbCr
001	24-bit 444, YcbCr
010	8-bit MONO
011	24-bit 444, RGB
100	8-bit 422, YcbCr

- Sync Signal: Select sync mode

Sync signal	Sync Mode
00	Embedded Sync
01	External Sync with DE
10	Do not use
11	External Sync without DE

- Scan mode : Select scan mode

Interlaced	Interlaced mode
00	Non-interlaced
01	Interlaced
10	Do not use
11	Pseudo-Interlaced

3) V sync/H sync Polarity& 3D function Setting

Register Address	7	6	5	4	3	2	1	0
02H	Reserved		3D Enable	N.A		3D Refresh	V_Pol	H_Pol
Default	0	0	0	0	0	0	0	0

- 3D function control:

3D Enable	3D Refresh	3D Pin	Display Mode	Operating
0	X	X	Normal Mode	Refresh every Frame/Filed
1	0	0	3D Mode	Refresh
		1		Keep last data
	1	0		Keep last data
		1		Refresh

- V_Pol/H_Pol setting: Select Vsync & Hsync polarity

V_Pol/H_Pol	Polarity Choice
0	Active High
1	Active Low

4) Input video vertical blank lines

Register Address	7	6	5	4	3	2	1	0
03H	V_Blank							
Default	0	0	0	0	0	0	0	0

5) Input video horizontal blank pixels

Register Address	7	6	5	4	3	2	1	0
04H	H_Blank							
Default	0	0	0	0	0	0	0	0

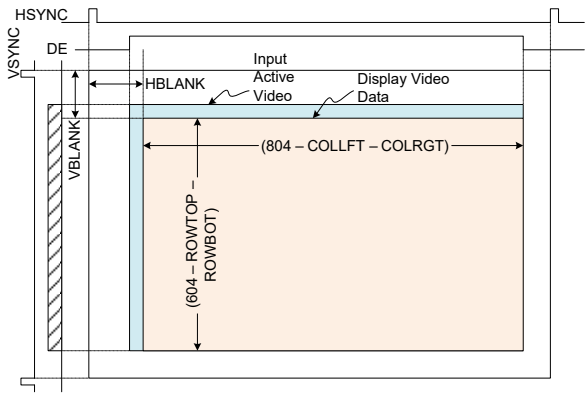


Figure 4-1 Vertical Blank Lines with DE

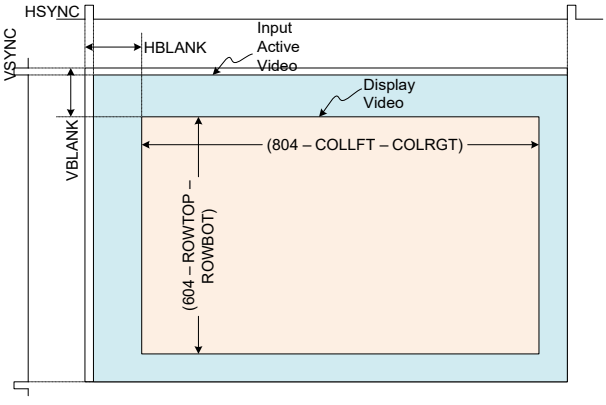


Figure 4-2 Vertical Blank Lines without DE

6) Adjust Start Active Video position

Register Address	7	6	5	4	3	2	1	0
05H	N.A.						SAV Offset	
Default	-						0	1

- SAV Offset : Adjust start active video (SAV) position

SAV Offset	Hsync position
00	1 pixel before input SAV
01	Same as input SAV
10	1 pixel after input SAV
11	2 pixel after input SAV

7) Field start line position adjust for Interlaced video

Register Address	7	6	5	4	3	2	1	0
06H	N.A.						V_offset	
Default	-						0	0

- V Offset : Adjust odd field active video start position when interlaced video mode

V Offset	Odd field start position
00	Same as Even field
01	1 line after Even field
10	Do not use
11	1 line before Even field

8) Down scaling for NTSC & PAL video

Register Address	7	6	5	4	3	2	1	0
07H	N.A.					V_Scale	H_Scale	
Default	-					0	0	0

- V Scale : Vertical 4/3downscale for PAL

V_Scale	Down scaling (In : Out)
0	1:1
1	6:5

- H Scale : Horizontal 4/3downscale for PAL/NTSC

H_Scale	Down scaling (In : Out)
00	1:1
01	11:10
10	9:8
11	Do not use

9) Brightness control

Register Address	7	6	5	4	3	2	1	0
08H	Video Signal Brightness							
Default	1	0	0	0	0	0	0	0

- $V_{out} = V_{in} + Reg(08H) - 128$ (Limit Low 8Bit Data)

Brightness	Brightness adjustment effect
00H	Darkest setting
80H	No change
FFH	Brightest setting

10) Contrast enhance control

Register Address	7	6	5	4	3	2	1	0
09H	Video Signal Contrast							
Default	1	0	0	0	0	0	0	0

- $V_{out} = V_{in} \times Reg(09H) \div 128$ (Limit Low 8Bit Data)

Contrast	Contrast adjustment effect
00H	Gain =0 (Black Screen)
80H	Gain =1 (Normal)
FFH	Gain =2 (Contrast Double)

11) Reserved

Register Address	7	6	5	4	3	2	1	0
0AH	N.A.	Reserved						
Default	-	1	0	0	1	0	1	0

12) Reserved

Register Address	7	6	5	4	3	2	1	0
0BH	N.A.	Reserved						
Default	-	1	0	1	1	0	1	0

13) Power down

Register Address	7	6	5	4	3	2	1	0
0FH	PDOWN	N.A.		BSGENPD	RDACPD	RAMPPD	VCOMPD	TSENPD
Default	0	-		0	0	0	0	0

- PDOWN: All system power off
- BSGENPD: Discharge current generator power off
- RDACPD: DAC module power off
- RAMPPD: DAC Buffer module power off
- VCOMPD: Vcom power off
- TSENPD: Temperature sensor power off

4.2.2. Video Display Control Registers

14) Display off & Scan directions

Register Address	7	6	5	4	3	2	1	0
10H	N.A.					DispOff	VSCAN	HSCAN
Default	-					1	0	0

• DispOff	
0	Display ON
1	Display OFF

• VSCAN	
0	Top → Bottom
1	Bottom → Top

• HSCAN	
0	Left → Right
1	Right → Left

15) Display Left Margin

Register Address	7	6	5	4	3	2	1	0
11H	COLLFT							
Default	0	0	0	0	0	0	1	0

16) Display Right Margin

Register Address	7	6	5	4	3	2	1	0
12H	COLRGT							
Default	0	0	0	0	0	0	1	0

17) Display Top Margin

Register Address	7	6	5	4	3	2	1	0
13H	ROWTOP							
Default	0	0	0	0	0	0	1	0

18) Display Bottom Margin

Register Address	7	6	5	4	3	2	1	0
14H	ROWBOT							
Default	0	0	0	0	0	0	1	0

19) Reserved

Register Address	7	6	5	4	3	2	1	0
15H	Reserved							
Default	0	1	0	0	0	1	0	0

20) D/A Conversion Offset control

Register Address	7	6	5	4	3	2	1	0
16H	DAOFFSET							
Default	0	0	0	0	1	1	0	0

- DAOFFSET: Adjust D/A output offset

00H	Offset = -40%
80H	Offset = 0
FFH	Offset = +40%

Note: The Register setting affect the gamma correction curve, not recommended to change

21) Discharge Current Setting

Register Address	7	6	5	4	3	2	1	0
17H	NA		Reserved		NA		BIAS	
Default	-	-	0	0	-	-	0	1

- BIAS: OLED pixel discharge current setting. Can enhance the display dynamic contrast ratio, may result in reduced display brightness

BIAS	BIAS Current
00	0 nA (OFF)
01	0.5 nA
10	1nA
11	DO not use

22) Discharge Enable Control

Register Address	7	6	5	4	3	2	1	0
18H	N.A.							BIAS_En
Default	-							0

- BIAS_En: OLED pixel discharge function enable switch, "0" is Disable, "1" is Enable.

23) Vcom Level Setting

Register Address	7	6	5	4	3	2	1	0
19H	Vcom							
Default	1	1	1	1	1	1	1	1

- *The valid range of Vcom setting is 20H ~ FFH, and the corresponding cathode voltage is about-3V ~ 0V. 20H is the brightest, FFH is the darkest*

The lower cathode voltage makes the display brighter. The curve of Vcom and cathode voltage sees section 3.4 (DC / DC converter).

- *Low Vcom settings will cause the display too bright, may damage the eyes of the user, and continues use may cause display overheating and damage.*

4.2.3. Temperature Sensor Register

24) Reserved

Register Address	7	6	5	4	3	2	1	0
1AH	Do not use		Reserved					
Default	-	-	0	1	1	1	0	1

25) Reserved

Register Address	7	6	5	4	3	2	1	0
1BH	Reserved							
Default	0	1	1	1	0	1	0	0

26) Reserved

Register Address	7	6	5	4	3	2	1	0
1CH	Reserved							
Default	1	1	1	1	1	1	1	1

27) Temperature Sensor Readout (Read Only)

Register Address	7	6	5	4	3	2	1	0
1DH	TEMP_OUT							
Default	-							

- Temperature conversion formula is : $T = 0.47 \times \text{Reg}\,(1DH) - 40$

4.2.4. Gamma Look-Up Table Registers

28) 9 Bit Gamma Correction LUT0

Register Address	7	6	5	4	3	2	1	0
21H	N.A.							LUT0[8]
Default	-							0
20H	LUT0[7:0]							
Default	0	0	0	0	0	0	0	0

29) 9 Bit Gamma Correction LUT1

Register Address	7	6	5	4	3	2	1	0
23H	N.A.							LUT1[8]
Default	-							0
22H	LUT1[7:0]							
Default	0	0	1	0	0	0	0	0

30) 9 Bit Gamma Correction LUT2

Register Address	7	6	5	4	3	2	1	0
25H	N.A.							LUT2[8]
Default	-							0
24H	LUT2[7:0]							
Default	0	1	0	0	0	0	0	0

31) 9 Bit Gamma Correction LUT3

Register Address	7	6	5	4	3	2	1	0
27H	N.A.							LUT3[8]
Default	-							0
26H	LUT3[7:0]							
Default	0	1	1	0	0	0	0	0

32) 9 Bit Gamma Correction LUT4

Register Address	7	6	5	4	3	2	1	0
29H	N.A.							LUT4[8]
Default	-							0
28H	LUT4[7:0]							
Default	1	0	0	0	0	0	0	0

33) 9 Bit Gamma Correction LUT5

Register Address	7	6	5	4	3	2	1	0
2BH	N.A.							LUT5[8]
Default	-							0
2AH	LUT5[7:0]							
Default	1	0	1	0	0	0	0	0

34) 9 Bit Gamma Correction LUT6

Register Address	7	6	5	4	3	2	1	0
2DH	N.A.							LUT6[8]
Default	-							0
2CH	LUT6[7:0]							
Default	1	1	0	0	0	0	0	0

35) 9 Bit Gamma Correction LUT7

Register Address	7	6	5	4	3	2	1	0
2FH	N.A.							LUT7[8]
Default	-							0
2EH	LUT7[7:0]							
Default	1	1	1	0	0	0	0	0

36) 9 Bit Gamma Correction LUT8

Register Address	7	6	5	4	3	2	1	0
31H	N.A.							LUT8[8]
Default	-							1
30H	LUT8[7:0]							
Default	0	0	0	0	0	0	0	0

37) 9 Bit Gamma Correction LUT9

Register Address	7	6	5	4	3	2	1	0
33H	N.A.							LUT9[8]
Default	-							1
32H	LUT9[7:0]							
Default	0	0	1	0	0	0	0	0

38) 9 Bit Gamma Correction LUT10

Register Address	7	6	5	4	3	2	1	0
35H	N.A.							LUT10[8]
Default	-							1
34H	LUT10[7:0]							
Default	0	1	0	0	0	0	0	0

39) 9 Bit Gamma Correction LUT11

Register Address	7	6	5	4	3	2	1	0
37H	N.A.							LUT11[8]
Default	-							1
36H	LUT11[7:0]							
Default	0	1	1	0	0	0	0	0

40) 9 Bit Gamma Correction LUT12

Register Address	7	6	5	4	3	2	1	0
39H	N.A.							LUT12[8]
Default	-							1
38H	LUT12[7:0]							
Default	1	0	0	0	0	0	0	0

41) 9 Bit Gamma Correction LUT13

Register Address	7	6	5	4	3	2	1	0
3BH	N.A.							LUT13[8]
Default	-							1
3AH	LUT13[7:0]							
Default	1	0	1	0	0	0	0	0

42) 9 Bit Gamma Correction LUT14

Register Address	7	6	5	4	3	2	1	0
3DH	N.A.							LUT14[8]
Default	-							1
3CH	LUT14[7:0]							
Default	1	1	0	0	0	0	0	0

43) 9 Bit Gamma Correction LUT15

Register Address	7	6	5	4	3	2	1	0
3FH	N.A.							LUT15[8]
Default	-							1
3EH	LUT15[7:0]							
Default	1	1	1	0	0	0	0	0

44) 10 Bit Gamma Correction LUT16

Register Address	7	6	5	4	3	2	1	0
41H	N.A.						LUT16[9:8]	
Default	-						1	0
40H	LUT16[7:0]							
Default	0	0	0	0	0	0	0	0

4.2.5. Color Offset Control Registers

45) 9 Bit R offset control

Register Address	7	6	5	4	3	2	1	0
45H	N.A.							Roffset[8]
Default	-							1
44H	Roffset[7:0]							
Default	0	0	0	0	0	0	0	0

46) 9 Bit G offset control

Register Address	7	6	5	4	3	2	1	0
47H	N.A.							Goffset[8]
Default	-							1
46H	Goffset[7:0]							
Default	0	0	0	0	0	0	0	0

47) B offset control

Register Address	7	6	5	4	3	2	1	0
49H	N.A.							Boffset[8]
Default	-							1
48H	Boffset[7:0]							
Default	0	0	0	0	0	0	0	0

4.2.6. Test Pattern Generator Control Register

48) Select Test Pattern

Register Address	7	6	5	4	3	2	1	0
4AH	N.A.					PatternMode		
Default	-					0	0	0

- PatternMode: Select Test Pattern

Patterns	Test Pattern
000	Pattern Generator Off (Normal)
001	Color Bar
010	Gray Scale
011	Tile
100	Vertical Lines
101	Horizontal Lines
110	Ver. & Hor. Lines
111	Do not use

49) Set line width for lines pattern (Patterns = 100 ~110)

Register Address	7	6	5	4	3	2	1	0
4BH	LineWidth							
Default	0	0	0	0	0	0	1	0

50) Set line space for line pattern (Patterns = 100 ~ 110)

Register Address	7	6	5	4	3	2	1	0
4CH	LineSpace							
Default	0	0	0	0	0	0	1	1

51) Set Foreground & Background RGB color for lines pattern (Patterns = 100 ~ 110)

Register Address	7	6	5	4	3	2	1	0
4BH	N.A.	BGCOLOR			N.A.	FGCOLOR		
Default	-	0	0	0	-	1	1	1

- BGCOLOR : Background color

BGCOLOR	Color
000	Black
001	Blue
010	Green
100	Red
111	White

- FGCOLOR : Foreground color

FGCOLOR	Color
000	Black
001	Blue
010	Green
100	Red
111	White

4.3. Register Setting Example

Table 4-2 Register Setting Example

Video Mode				Register Setting					
Mode	**Scan**	**Input**	**Display**	**Reg(01H)**	**Reg(07H)**	**Reg(11h)**	**Reg(12H)**	**Reg(13H)**	**Reg(14H)**
SVGA	Progressive	800×600	800×600	3CH	00H	02H	02H	02H	02H
VGA	Progressive	640×480	640×480	3CH	00H	52H	52H	52H	3EH
SMPTE-170M-1	Interlaced	640×480	640×480	21H	00H	52H	52H	52H	3EH
SMPTE-170M-2	Interlaced	800×600	800×600	3DH	00H	02H	02H	02H	02H
NTSC	Interlaced	720×480	640×480	41H	04H	52H	52H	52H	3EH
PAL	Interlaced	720×480	640×480	41H	05H	52H	52H	52H	3EH
NTSC (SQ)	Interlaced	640×480	640×480	41H	00H	52H	52H	52H	3EH
PAL (SQ)	Interlaced	768×676	768×576	41H	00H	12H	12H	14H	0EH

5. OPTICAL CHARACTERISTICS

Table 5-1 Optical Characteristics table

Item				Remark		Mini	Typical	Max
Contrast Ratio				Highest gray: Minimum gray		10000:1	-	-
Luminance	Full Color			Using Built-in test pattern under typical test conditions and all pixels are fully on			70	
	Monochrome White						100	
	Monochrome Green						500	
luminance uniformity				The average of five test points		90	95	100
Chromaticity	Full Color	White	CIEX	all pixels are fully on	Using Built-in test pattern under typical test conditions and all pixels are fully on.	0.25	0.30	0.35
			CIEY			0.30	0.35	0.40
		Red	CIEX	all red are sub-pixels fully on		0.48	0.61	0.66
			CIEY			0.32	0.34	0.37
		Green	CIEX	all green are sub-pixels fully on		0.18	0.22	0.27
			CIEY			0.40	0.51	0.53
		Blue	CIEX	all blue are sub-pixels are on		0.13	0.15	0.18
			CIEY			0.13	0.18	0.23
	Monochrome White	White	CIEX	all pixels are fully on		0.25	0.30	0.35
			CIEY			0.30	0.35	0.40
	Monochrome Green	Green	CIEX	all pixels are fully on		0.25	0.30	0.35
			CIEY			0.60	0.65	0.70

5.1. Brightness and Contrast Properties

5.1.1. Brightness

The OLED's luminance is depending on the bias voltage and current, increasing the bias voltage can obtain the higher brightness. With OLiGHTEK's proprietary active matrix driver technology, SVGA050 series microdisplay has two kinds of method for brightness adjustment.

1) Through the input video signal control the anode voltage, realizing each pixel brightness control. The video signal can enhancement by change the value of register 08H and 09H.
2) Adjusting the common cathode voltage, while achieving all pixel brightness adjustment. The cathode negative voltage adjustments by change the value of register 19H.

5.1.2. Contrast

OLED's quickly response and self-emitting characteristics make it has excellent contrast features. But the leakage current will causing the contrast decreased when using a higher bias voltage. The SVGA050 series display's contrast property is shown in Figure 5-1, Figure 5-2 and Figure 5-3.

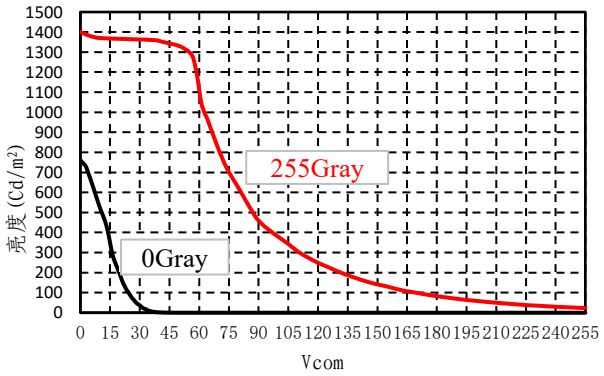


Figure 5-1 Full Color Display

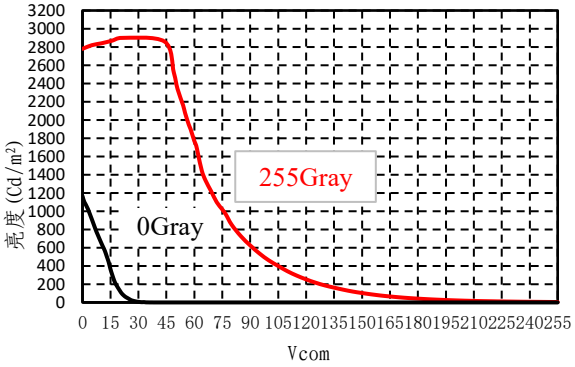


Figure 5-2 Monochrome White Display

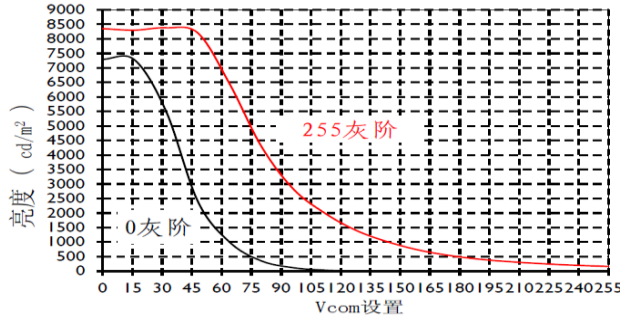
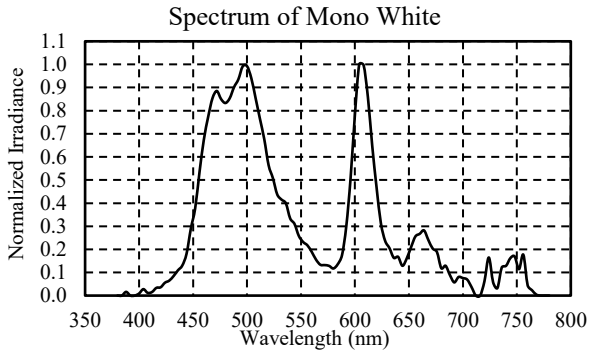
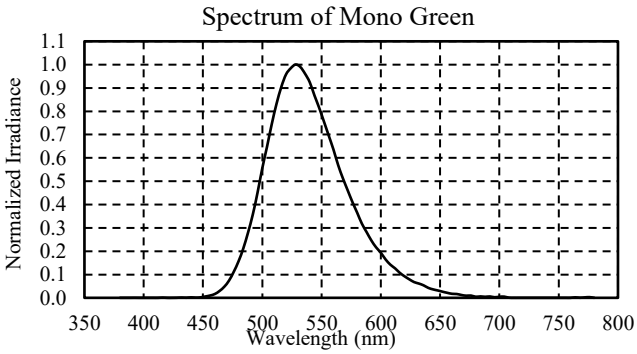
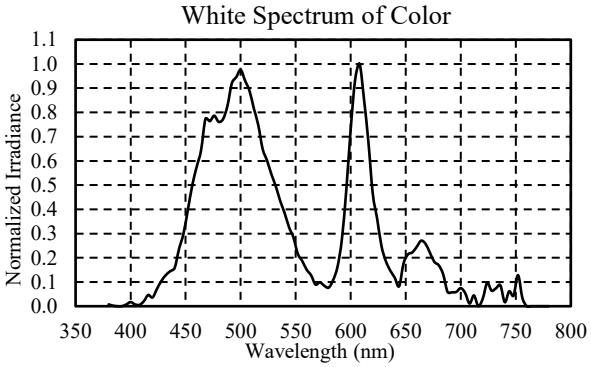


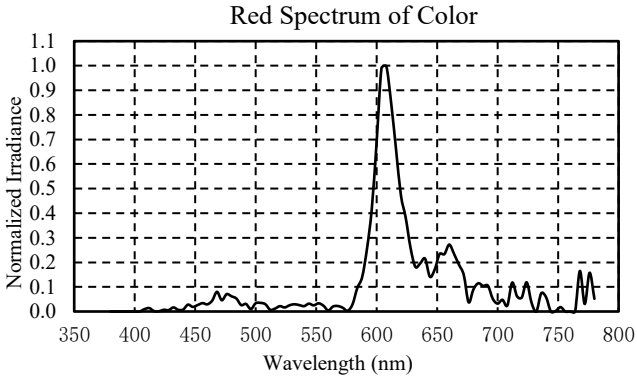
Figure 5-3 Monochrome Green Display

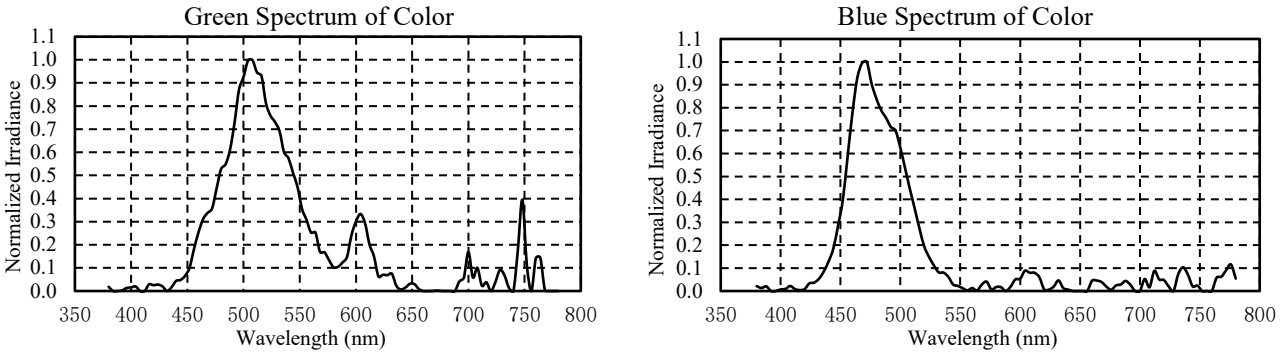
5.2. Spectrum Characteristics











5.3. Luminance Characteristic with Temperature

Test conditions: V5=5.0V, V1.8=1.8V, All White Pattern, Reg(19H)=80H, VCLK=40MHz

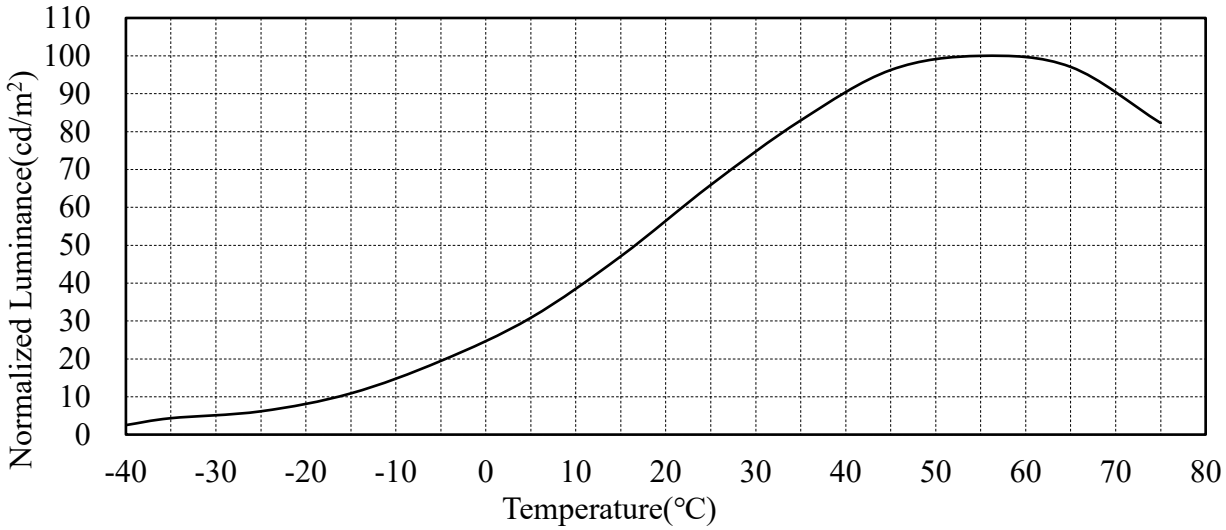


Figure 5-4 SVGA050 Luminance characteristic curve with temperature

5.4. Power Consumption Characteristic with Luminance

Test conditions: T=23℃±2℃, V5=5.0V, V1.8=1.8V, All White Pattern, VCLK=40MHz

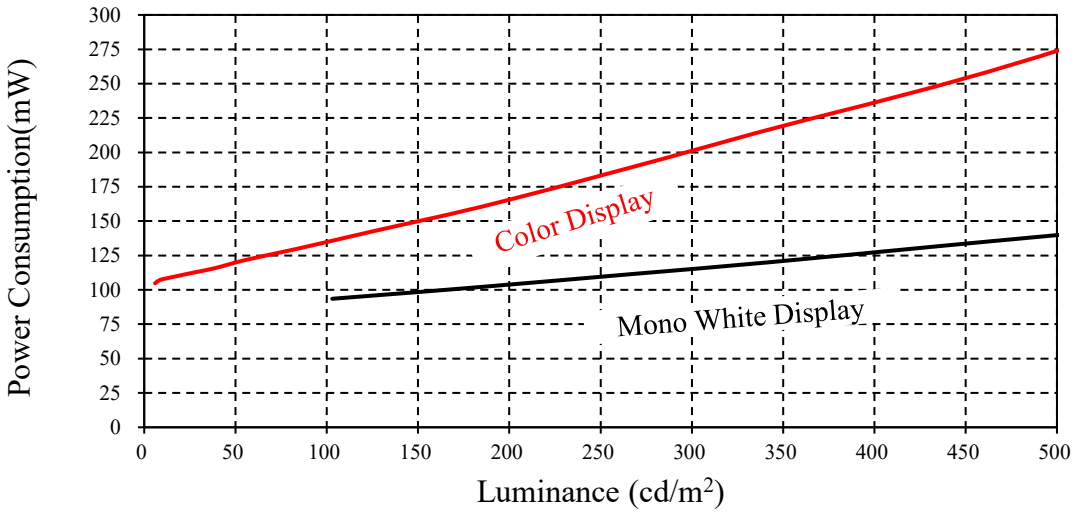
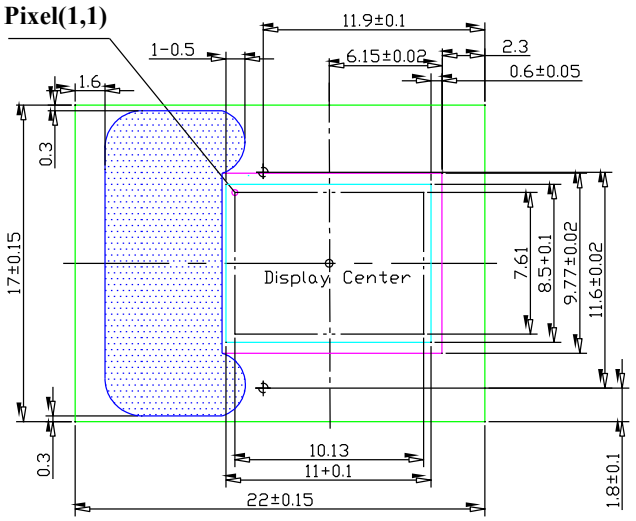
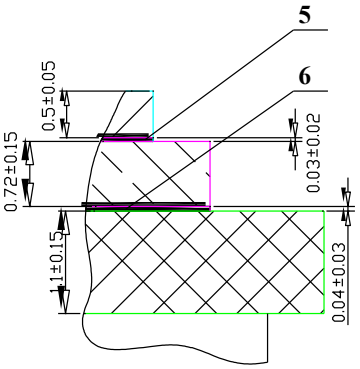


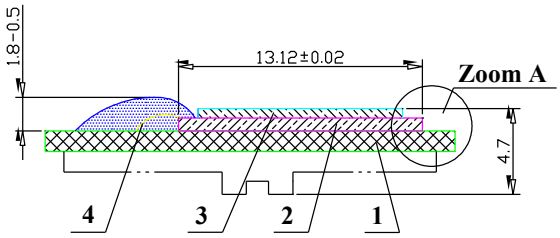
Figure 5-5 SVGA050 Power consumption characteristic with luminance

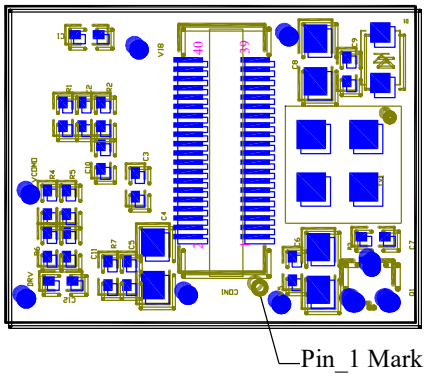
6. MECHANICAL CHARACTERISTICS





Zoom A
25:1





6	Adhesive	Scale	OLiGHTEK Co., Ltd.			
5	OLED Layer & Adhesive	3.2:1				
4	Wirebond Encap		Title	SVGA050 Assembly Drawing		
3	Glass Cover					
2	Si-Base Sub		Designed	ZHQ	Version	V2.0
1	PCB Backboard		Checked	YXH	Date	May 7, 2013
Item	Name		Approved	LYW	Sheets	1/1

7. PRODUCTS CLEANING, HANDLING AND STORAGE

7.1. Cleaning

- Avoid using any acid, alkali and organic solvent to clean or contact to the display
- Using the lens paper or clean cloth to clean the surface is recommend

1.1. General Handling Considerations

- Do not expose the display to strong acids, alkalis, or solvents.
- Do not expose the display surface to UV or other strong ionizing radiation.
- Do not using sharp objects to contact the glass and silicon regions of display.
- Avoid applying force to the any region except the PCB backplane, especially apply the force to the region of sealing, silicon edge and cover glass is not allowed.
- Avoid immersion of the display in any liquid.
- Handing with PVC clean gloves is recommended.

1.2. Static Charge Prevention

The microdisplay is sensitive to electro-static discharge due to integrated CMOS circuit in the display. The following measures are recommended to minimize ESD occurrences:

- Operate on a region which is equipped with electro-static eliminator, such as ionizing air blowers.
- Wear the anti-static wrist strap
- wear the non-chargeable clothes
- Keep away from charged region.

Figure 7-1 Handing the Display

1.3. Storage

1.3.1. Short Term Storage

The display should be stored in a dry environment with temperature range from -50℃ to 90℃ for a short period(≤100hrs).

1.3.2. Long Term Storage

If the display is stored in such an environment with excessive heat or cold or moisture, the lifetime of display will be shorten, even the environment can cause permanent damage to the display. Recommended long-term storage condition as follows:

- Room temperature: 25℃±5℃
- Dry environment: dry nitrogen or vacuum sealing cabinet
- Static placing: avoid violent vibration

APPENDIX

List of Figures

List of Tables