SXGA060 Series
Low-Power AMOLED Microdisplay

Datasheet

V1.2

SXGA060SC

SXGA060SW

SXGA060SG

For Products:

SXGA060SCV1R1/R2	—	Full Color
SXGA060SWV1R1/R2	—	Monochrome White
SXGA060SGV1R1/R3	—	Monochrome Green

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October 12, 2020

Record of Revision

Version	Revise Date	Page	Content
V1.0	2020-06		Official Version.
V1.1	2020-08	P2/P3	Correct the error in version number. Modify the weight range.
V1.2	2020-10	P20	Modify the description of Vs&Hs control register 0: Active Low –> 0: Active High 1: Active High –> 1: Active Low

Contents

1. FEARTURES

- Si-Base AMOLED Microdisplay
  - 0.18μm CMOS Technology
  - Full Digital Video Core
  - High Efficiency Top Emission Structure
  - Low Power Consumption
- 1280×1024 (SXGA) Resolution
  - View Area: 0.6 inch
  - Pixel Pitch : 9.3μm
  - Total Pixels : 1284 (×3)× 1028
- Digital Video Interface
  - Compatible with ITU-R BT.656/601
  - Accept 8/16/24-Bit Digital Video
  - Accept YCbCr/RGB Color or Mono
  - Support SXGA/XGA/SVGA/VGA etc
  - Support DDR/SDR Mode
- Digital Video Signal Enhancement
  - Brightness
  - Contrast
- Gamma Correction
  - RGB Separated 10Bit×256 Gamma LUTs
- Full Scale 10-Bit DAC
- Support Binocular Stereovision
- Horizontal/Vertical Mirror
- Scan and Position Control
- Integrated Temperature Sensor
- Integrated 9-Bit ProgrammableVcom Module
- Built-in Test Patterns
- 2-Wire Series Interface
- Single 5V Power suplly

SXGA 060 S C V1 R1

① ② ③ ④ ⑤ ⑥

①Type	
SVGA	800×600
SXGA	1280×1024

③Temperature	
S	Standard：-40℃～+60℃
N	Normal：-10℃～+40℃

⑤Connector	
V1	Board to board
V2	FPC

②Size	
050	0.5 inch
060	0.6 inch

④Color	
C	Full Color
W	Mono White
G	Mono Green

⑥Revision	
R1	Normal brightness
R2	High brightness
R3	Green High brightness

2. GENERAL DESCRIPTION

2.1. SXGA060SV1R1 Normal-brightness version Microdisplay

Product Type		SXGA060SCV1R1	SXGA060SWV1R1	SXGA060SGV1R1
Resolution		1280 (×3) × 1024		
Active pixels		1284 (×3) × 1028		
Pixel Aspect Ratio		1:1		
Color Pixel Arrangement		RGB Vertical Stripe		
Gray Levels		8bits/256Levels		
Luminance Uniformity		> 90%		
Contrast		> 10000:1		
Digital Video Interface		ITU-R BT.601/656 24-bit 4:4:4 RGB/YCbCr 16-bit 4:2:2 YCbCr 8-bit 4:2:2 YCbCr/Mono		
Operating Temperature	Standard	-40℃ ～ +65℃		
	Normal	-10℃ ～ +40℃		
Chromaticity	White	CIEx=0.30±0.05, CIEy=0.35±0.05		
	Green	CIEx=0.30±0.05, CIEy=0.63±0.05		
Operating Humidity		≤85%RH (Non condensing)		
Pixel Size(μm²)		9.3 × 9.3		
Viewing Area(mm²)		11.941× 9.560		
Mechanical Envelope(mm³)		22 × 17 × 5.2		
Operating Luminance(Cd/m²)		70	100	500
Power Consumption(mW) ①		180	150	250
Power Supply		DC 5.0V@Max250mA		
Weight(g)		< 3		

Note ①: Measuring method refer to section 2.7.2

2.2. SXGA060SV1R2/R3 High-brightness version Microdisplay

Product Type		SXGA060SCV1R2	SXGA060SWV1R2	SXGA060SGV1R3
Resolution		1280 (×3) × 1024		
Active pixels		1284 (×3) × 1028		
Pixel Aspect Ratio		1:1 Square		
Color Pixel Arrangement		RGB Vertical Stripe		
Gray Levels		8bits/256Levels		
Luminance Uniformity		> 90%		
Contrast		> 10000:1		
Digital Video Interface		ITU-R BT.601/656 24-bit 4:4:4 RGB/YCbCr 16-bit 4:2:2 YCbCr 8-bit 4:2:2 YCbCr/Mono		
Operating Temperature	Standard	-40℃ ～ +65℃		
	Normal	-10℃ ～ +40℃		
Chromaticity	White	CIEx=0.30±0.05, CIEy=0.35±0.05		
	Green	CIEx=0.30±0.05, CIEy=0.63±0.05		
Operating Humidity		≤85%RH (Non condensing)		
Pixel Size(μm^2)		9.3 × 9.3		
Viewing Area(mm^2)		11.941× 9.560		
Mechanical Envelope(mm^3)		22 × 17 × 5.2		
Operating Luminance(Cd/m^2)		150	1000	5000
Power Consumption(mW)①		230	300	450
Power Supply		DC 5.0V@Max250mA		
Weight(g)		< 3		

Note ①: Measuring method refer to section 2.7.2

2.3. Functional Overview

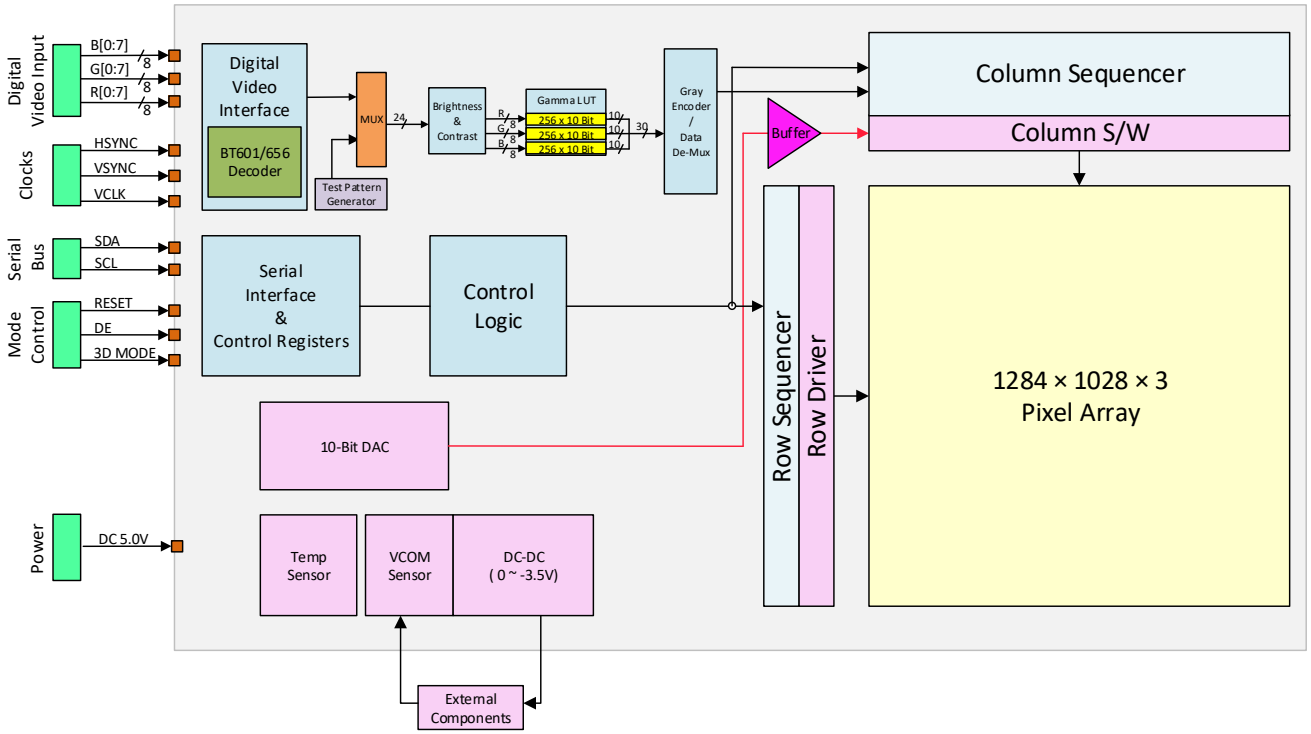


Figure 2-1 SXGA060 Series Architecture & Principle Diagram

2.4. Pixel Array

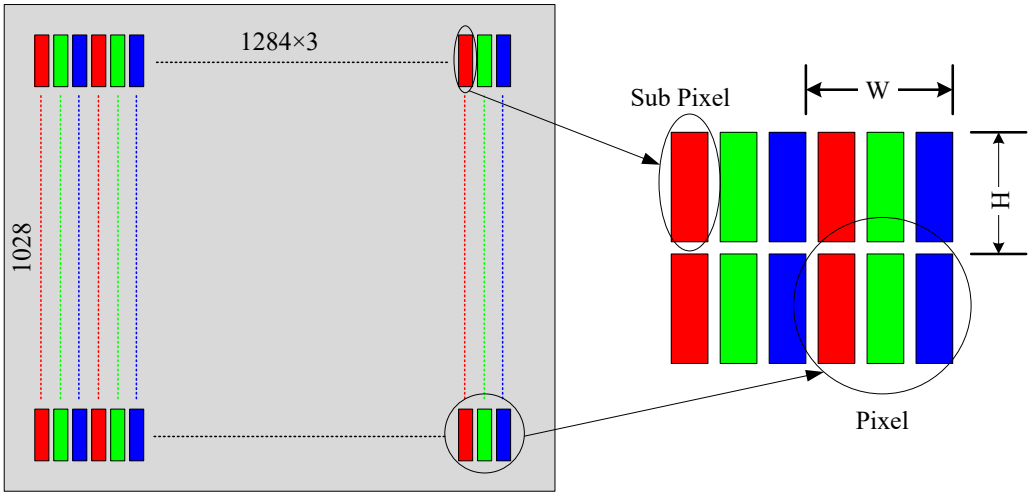


Figure 2-2 Pixel and Sub-Pixel Array

Each pixel of olightek's SXGA060 series AMOLED microdisplay is formed by three sub-pixels (Figure 2-2). The pixel's related parameters are shown below:

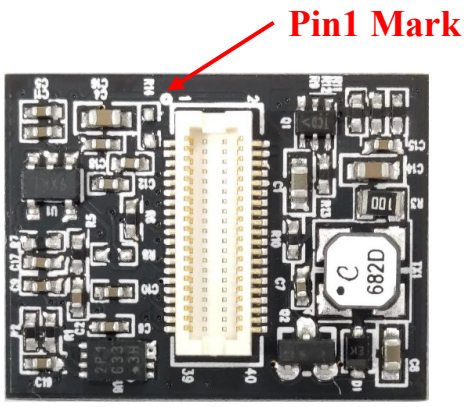
Model	Pixel Size		Duty Cycle	View Area	
	Width(W)	Height(H)		Width（1284×W）	Height（1028×H）
SXGA060	9.3μm	9.3μm	68%	11.941mm	9.560mm

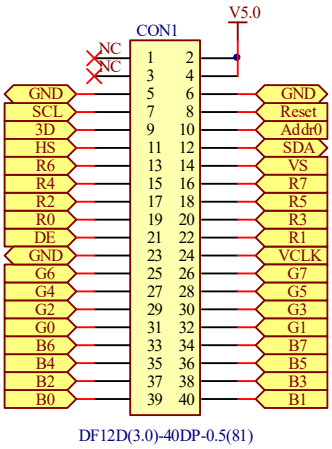
2.5. INTERFACE

2.5.1. Pin Assignment

Part number of the receptacle: *Hirose DF12D(3.0)-40DP-0.5* (0.5mm pitch 40 ways).

Part number of the matched plug: *Hirose DF12D(3.0)-40DS-0.5*





2.5.2. Pin Definition

Pin	Symbol	I/O	Function	Remark
1	NC	-	Not used	
3	NC	-	Not used	
5	GND	P	Power ground	
7	SCL	I	Serial Port Clock Line	Pull-up 1.8V
9	3D	I	3D L/R Signal Input	
11	Hs	I	Hsync Signal Input	
13	R6	I	Video Data Input R[6]	
15	R4	I	Video Data Input R[4]	
17	R2	I	Video Data Input R[2]	
19	R0	I	Video Data Input R[0]_LSB	
21	DE	I	Data Enabl Signal Input	
23	GND	P	Power ground	
25	G6	I	Video Data Input G[6]	
27	G4	I	Video Data Input G[4]	
29	G2	I	Video Data Input G[2]	
31	G0	I	ideo Data Input G[0]_LSB	
33	B6	I	Video Data Input B[6]	
35	B4	I	Video Data Input B[4]	
37	B2	I	Video Data Input B[2]	
39	B0	I	Video Data Input B[0]_LSB	

Pin	Symbol	I/O	Function	Remark
2	V5.0	P	5.0V Power Suppply	
4	V5.0	P	5.0V Power Suppply	
6	GND	P	Power ground	
8	Reset	I	Master Reset, Active Low	Can't Floating
10	Addr0	I	Serial Port Address A0	Pull-up 1.8V
12	SDA	I/O	Serial Port Data Line	Pull-up 1.8V
14	Vs	I	Vsync Signal Input	
16	R7	I	Video Data Input R[7]_MSB	
18	R5	I	Video Data Input R[5]	
20	R3	I	Video Data Input R[3]	
22	R1	I	Video Data Input R[1]	
24	VCLK	I	Pixel Clock Input	
26	G7	I	Video Data Input G[7]_MSB	
28	G5	I	Video Data Input G[5]	
30	G3	I	Video Data Input G[3]	
32	G1	I	Video Data Input G[1]	
34	B7	I	Video Data Input B[7]_MSB	
36	B5	I	Video Data Input B[5]	
38	B3	I	Video Data Input B[3]	
40	B1	I	Video Data Input B[1]	

2.5.3. Video Formats

Video Data Formate	Color Space	R[7:0]	G[7:0]	B[7:0]
8-bit, 4:2:2	YCbCr	N.C.	YCbCr[7:0]	N.C.
8-bit, Mono	Y	N.C.	Y[7:0]	N.C.
16-bit, 4:2:2	YCbCr	N.C.	Y[7:0]	CbCr[7:0]
24-bit, 4:4:4	YCbCr	Cr[7:0]	Y[7:0]	Cb[7:0]
24-bit, 4:4:4	RGB	R[7:0]	G[7:0]	B[7:0]

2.6. Timing Characteristics

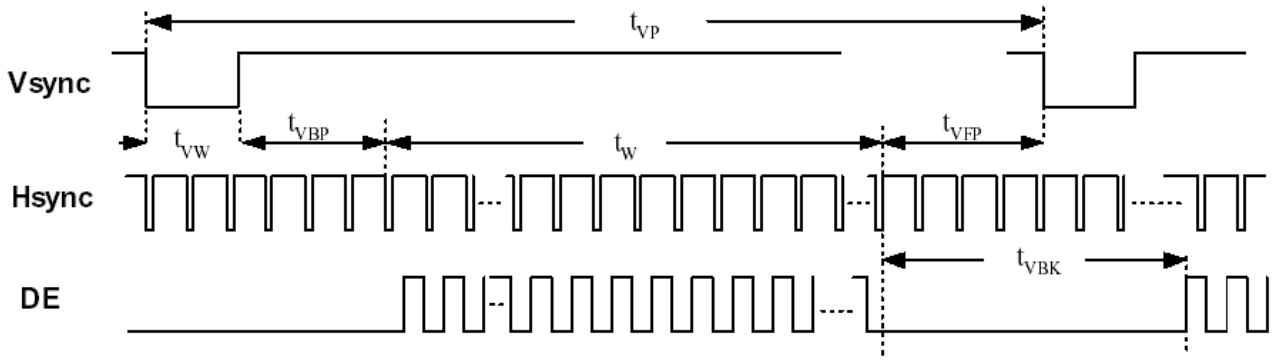


Figure 2-3 Input Sync Signals Timing (For All Formats)

Table 2-1 SXGA Video Timing Characteristics

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Clock Frequency	f_{CLK}		108		MHz	SXGA@60Hz frame rate
HSYNC Period	t_{HP}	670			t_{CLK}	
HSYNC Pulse Width	t_{HW}	10			t_{CLK}	
HSYNC Back Porch	t_{HBP}	10			t_{CLK}	
Horizontal Valid data width	t_{HV}	640		1280	t_{CLK}	
HSYNC Front Porch	t_{HFP}	10			t_{CLK}	
Horizontal Blank	t_{HBK}	30			t_{CLK}	
VSYNC Period	t_{VP}	243			t_{HP}	
VSYNC Pulse Width	t_{VW}	1			t_{HP}	
VSYNC Back Porch	t_{VBP}	1			t_{HP}	
Vertical valid data width	t_W	240		1024	t_{HP}	
Vertical Front Porch	t_{VFP}	1			t_{HP}	
Vertical Blank	t_{VBK}	3			t_{HP}	

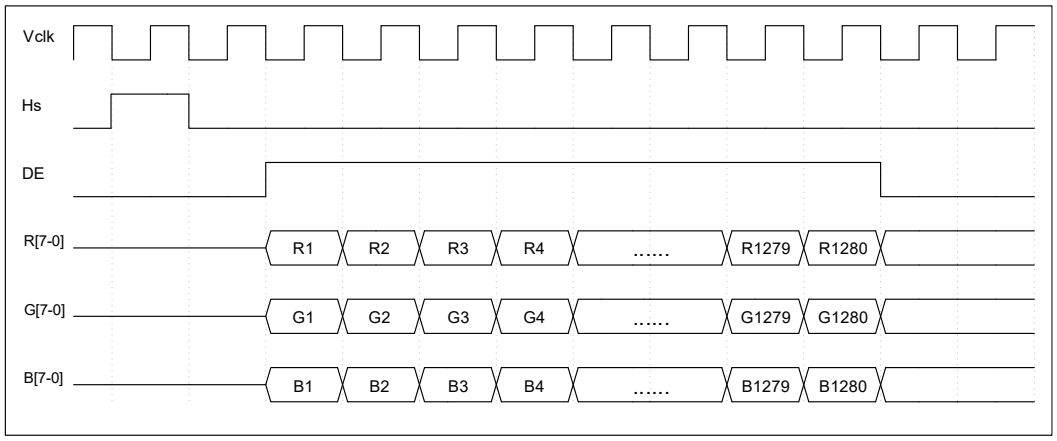


Figure 2-4 24-bit 4:4:4 RGB Input VideoTiming

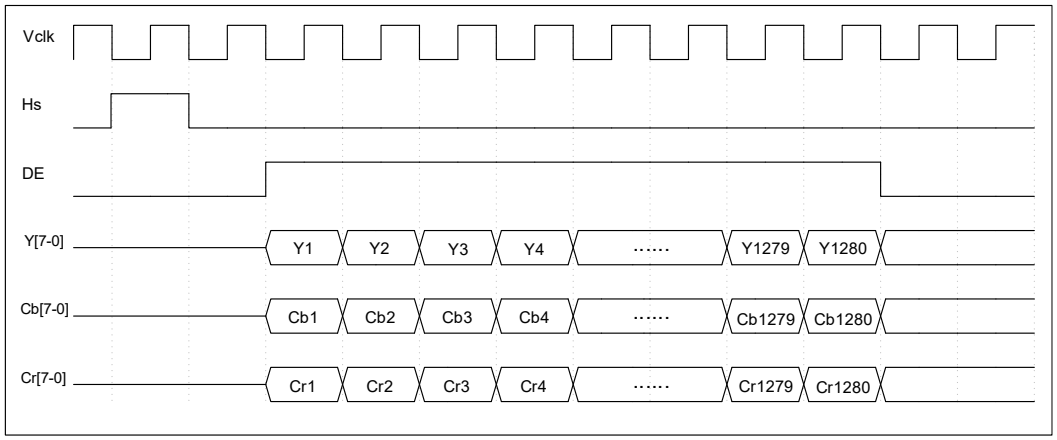


Figure 2-5 24-bit 4:4:4 YCbCr Input Video Timing

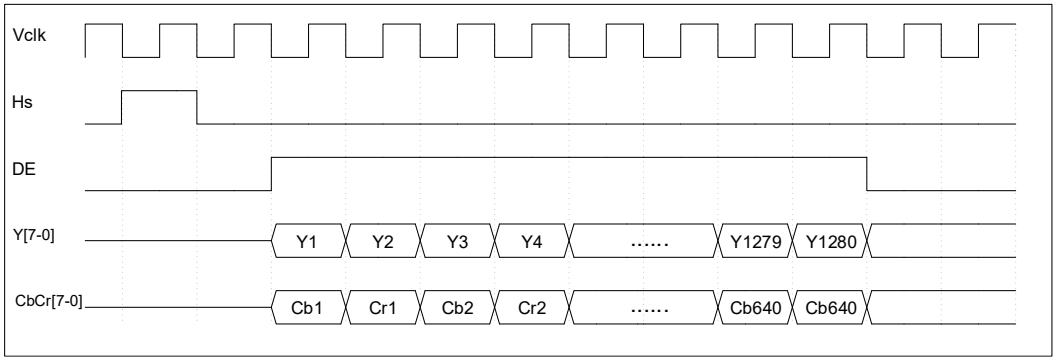


Figure 2-6 16-bit 4:2:2 YCbCr Input Video Timing

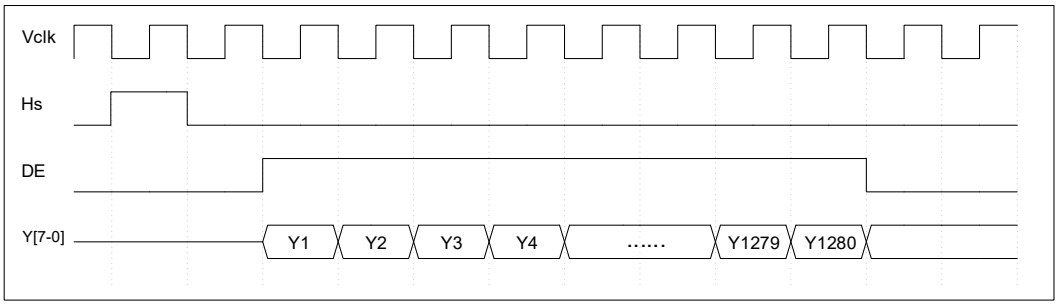


Figure 2-7 8-bit Mono Input Video Timing

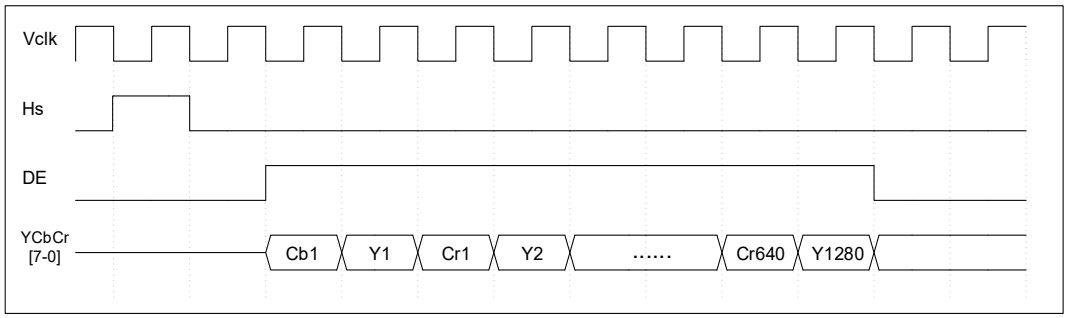


Figure 2-8 8-bit 4:2:2 YCbCr input Video timing

Table 2-2 VESA Video Timing Specifications

Mode		Frequency	Total	Active	Front Porch + Border	Sync Pulse	Back Porch + Border
SXGA 1280X1024 85Hz non-interlaced	H	91.146 KHz	1728 pixels	1280 pixels	64 pixels	160 pixels	224 pixels
	V	85.024 Hz	1072 lines	1024 lines	1 line	3 lines	44 lines
	P	157.500 MHz					
SXGA 1280X1024 75Hz non-interlaced	H	79.976 KHz	1688 pixels	1280 pixels	16 pixels	144 pixels	248 pixels
	V	75.025 Hz	1066 lines	1024 lines	1 line	3 lines	38 lines
	P	135.000 MHz					
SXGA 1280X1024 60Hz non-interlaced	H	63.981 KHz	1688 pixels	1280 pixels	48 pixels	112 pixels	248 pixels
	V	60.020 Hz	1066 lines	1024 lines	1 line	3 lines	38 lines
	P	108.000 MHz					
XGA 1024X768 85Hz non-interlaced	H	68.677 KHz	1376 pixels	1024 pixels	48 pixels	96 pixels	208 pixels
	V	84.997 Hz	808 lines	768 lines	1 line	3 lines	36 lines
	P	94.500 MHz					
XGA 1024X768 75Hz non-interlaced	H	60.023 KHz	1312 pixels	1024 pixels	16 pixels	96 pixels	176 pixels
	V	75.029 Hz	800 lines	768 lines	1 line	3 lines	28 lines
	P	78.750 MHz					
XGA 1024X768 60Hz non-interlaced	H	48.363 KHz	1344 pixels	1024 pixels	24 pixels	136 pixels	160 pixels
	V	60.004 Hz	806 lines	768 lines	3 line	6 lines	29 lines
	P	65.000 MHz					

Note: For more details please refer to the VESA Monitor Timing Standard

2.7. Electrical Characteristics

2.7.1. Recommended Operation Ratings

SYMBOL	DESCRIPTION	MIN	TYP	MAX[1]	UNIT
V5.0	5.0V Power Supply	4.5	5.0	6.0	V
$V_{I/O}$	Digital Signal Voltage	—	1.8	3.3	V
Tstorage	Storage Temperature	-55	20	90	°C
Toperate	Operation Temperature	-40	20	65	°C

Note 1: The absolute maximum rating values (except $V_{I/O}$) are not allowed to be exceeded at any time. If it is used exceeding the maximum rating or in an extreme condition, the characteristics of the device maybe recovered and the lifetime of the device will decrease, even the device may be permanently destroyed.

2.7.2. DC Characteristics

Table 2-3 SXGA060SV1R2(Normal-brightness) DC Characteristics

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNIT
$I_{5.0}$	5.0V Supply Current		10	40	250	mA
Vcom	Cathode Voltage		-3.5	-2	0	V
Typical Power Consumption[1]	Working	Color @ 70Cd/m2	-	180	-	mW
		Monochrome White @ 100Cd/m2	-	150	-	
		Monochrome Green @ 500Cd/m2	-	250	-	
	Display Off		40	-	60	
	Power Down		0.4	-	2	

Table 2-4 SXGA060SV1R3(High-brightness) DC Characteristics

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNIT
$I_{5.0}$	5.0V Supply Current		10	40	250	mA
Vcom	Cathode Voltage		-3.5	-2	0	V
Typical Power Consumption[1]	Working	Color @ 150Cd/m2	-	230	-	mW
		Monochrome White @ 1000Cd/m2	-	200	-	
		Monochrome Green @ 5000Cd/m2	-	450	-	
	Display Off		40	-	60	
	Power Down		0.4	-	2	

Note 1:Power consumption measured at 60Hz refresh rate, room ambient temperature and with a full white test pattern(all pixels on) see Figure 2-9

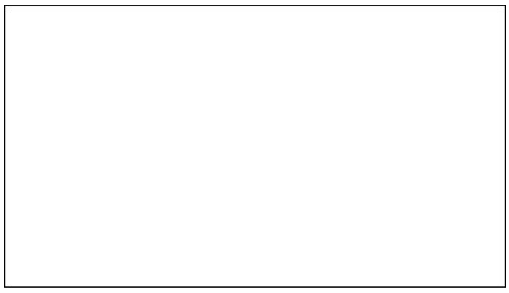
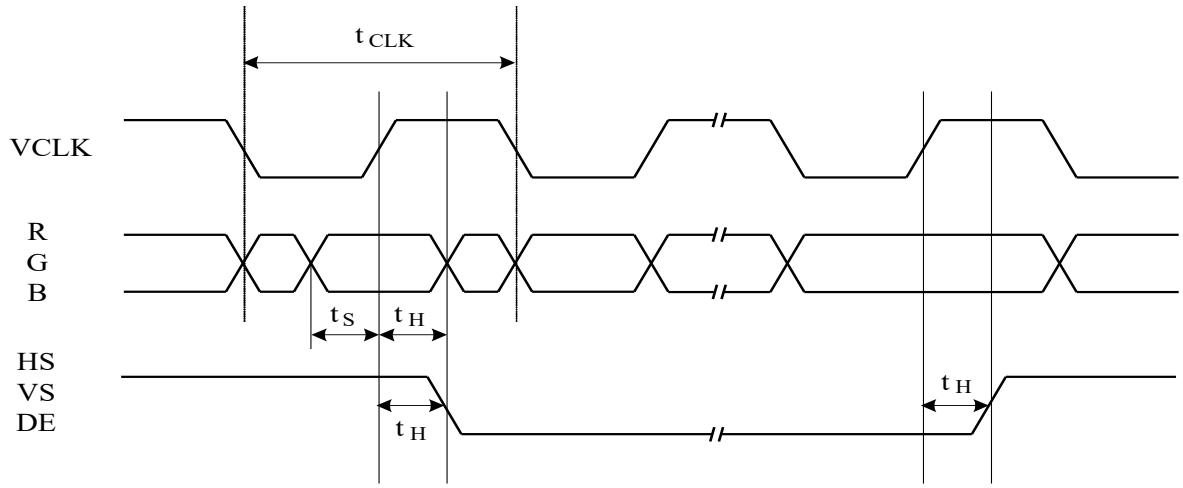


Figure 2-9 Full white test pattern

2.7.3. AC Characteristics



PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Digital Video Data Setup & Hold	t_S	1	-	-	ns
	t_H	1	-	-	ns
Video Clock Period	t_{CLK}	4.6	-	-	ns
Video Clock Duty	q	40	50	60	%

3. DETAILED FUNCTION DESCRIPTION

3.1. Digital Video Interface

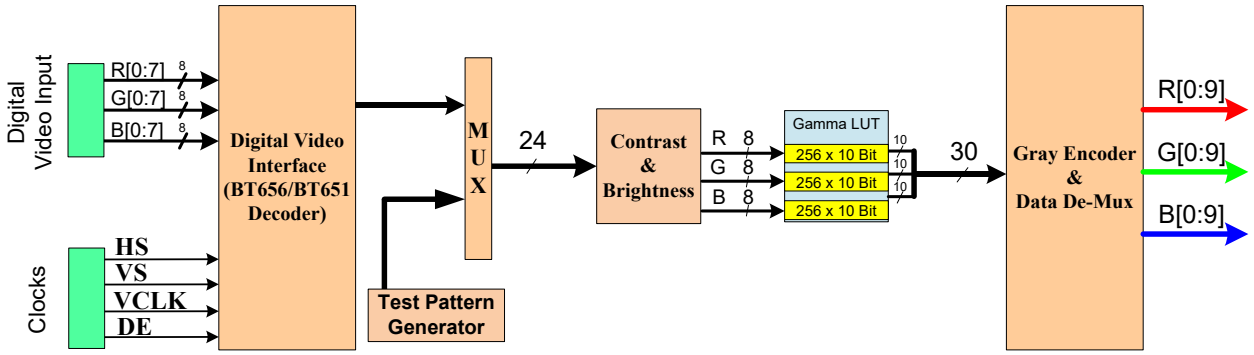


Figure 3-1 Digital Video Processing Flow Diagram

The digital video interface has three 8-bit data channels, and additional horizontal and vertical sync (HS/VS), data enable (DE), pixel clock signals (VCLK). User should select the correct signals to connect according to different Video format. VCLK is always needed in any mode. When use 8bit with embedded sync signal (8bit ITU-R BT.656 YCbCr/Mono 4:2:2), only G[7..0] bus and VCLK are needed.

OLED Display receives data with BT601/656 format, like 8/16/24 bits and 4:2:2/4:4:4 format, and

video decoder outputs 24 bits RGB signal always, then sends the signal to Video signal enhancement module and output keep 24 bits format. The gamma correction circuit makes corrections of the 24 bit RGB signal by separated RGB look-up table, and extends to 30 bits RGB signal output.
If the input video format is CVBS, component, VGA (analog RGB), HDMI, DVI video signals, etc., OLED Display requires an external video decoder, such as ADV7180, AD9985, ADV7611 and so on.

3.1.1. Color Space

If the input data format is YCbCr, the device will change it to RGB format. Color space conversion block converts color space from YCbCr to RGB and uses the following equations. Output signal is 24-bit RGB format, 8-bit in each path.

$$R = 1.164 \times (Y - 16) + 1.596 \times (Cr - 128)$$
$$G = 1.164 \times (Y - 16) - 0.813 \times (Cr - 128) - 0.392 \times (Cb - 128)$$
$$B = 1.164 \times (Y - 16) + 2.017 \times (Cb - 128)$$

3.1.2. Digital Video Signal Enhancement

Digital video signal enhancement can be achieved by adjusting the brightness and the contrast ratio, as is shown in Figure 3-2.

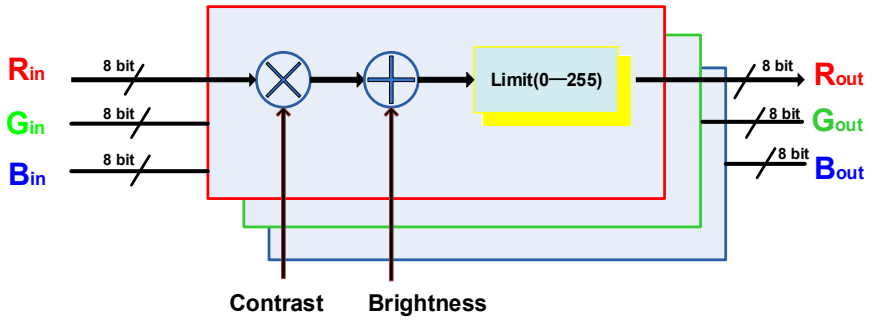


Figure 3-2 Digital Video Signal Enhancement Diagram

Brightness adjustment using addition and subtraction to achieve, the output value is equal to the input value plus the value of register 0EH, and then minus 128. When the value of register 0EH is greater than 80H, it means increase the brightness, whereas decrease. Brightness adjustment range is ±128.

$$V_{out} = V_{in} + Reg(0EH) - 128$$

Contrast adjustment using multiplication and division to achieve, the output value is equal to the input value multiplied by the value of register 0FH and then divided by 128. When the value of register 0FH is greater than 80H, it means increase the contrast, whereas decrease. The gain of contrast adjustment range is 0 to 2.

$$V_{out} = V_{in} \cdot \frac{Reg(0FH)}{128}$$

Note: The algorithms keep only 8bit data, if overflow, automatically discarded high bit.

3.1.3. Video Pattern Generation

Register 06H is pattern mode selection, default value is 0, indicates the test pattern generator is turned

off, details of setting refer to Table 3-1 and Figure 3-3

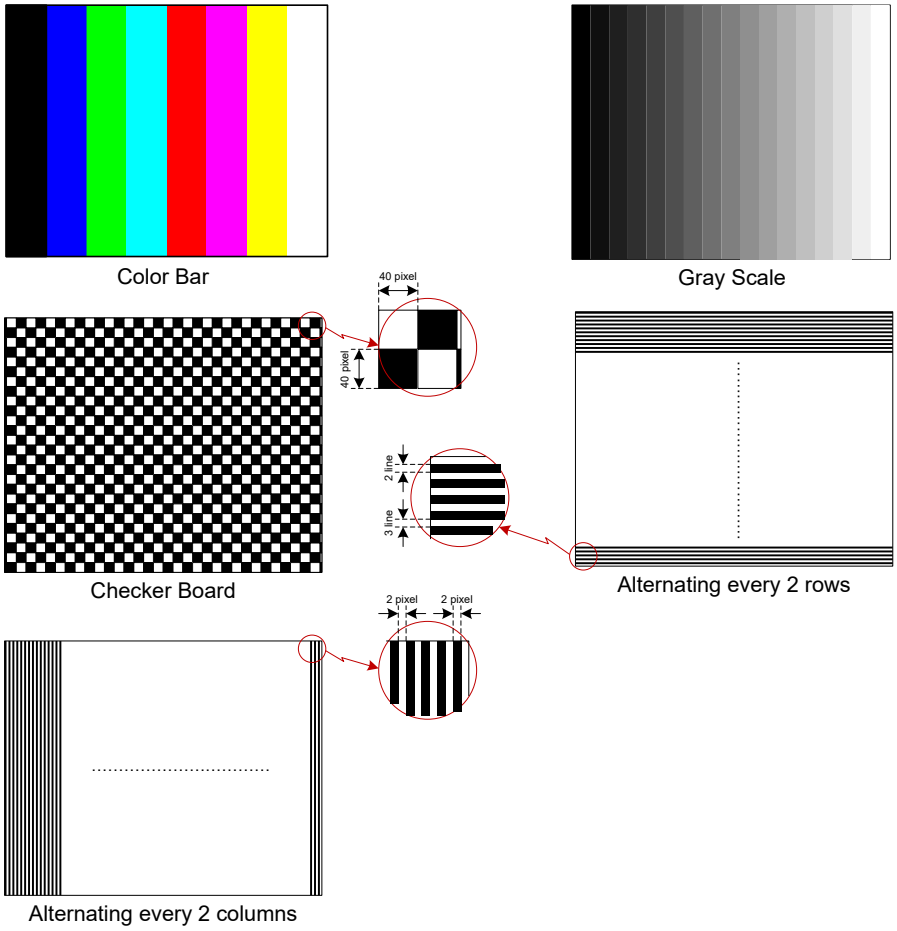


Figure 3-3 Video Test Patterns

Table 3-1 Summary of Test Pattern Setting

Register / Pattern	Mode (06H)	R (07:08H)	G (09:0AH)	B (0B:0CH)
Video input mode	00H	—	—	—
Color Bar	01H	—	—	—
Gray Scale	02H	—	—	—
Checker Board (40×40)	03H	—	—	—
Alternating every 2 rows	04H	—	—	—
Alternating every 2 columns	05H	—	—	—
All black	06H	—	—	—
All white	07H	—	—	—
All Red	08H	—	—	—
All Green	09H	—	—	—
All Blue	0AH	—	—	—
Adjustable RGB Gray[1]	0BH	0~1023	0~1023	0~1023

Note 1：At adjustable RGB gray mode, the gray level range both are 0~1023 (10-bit) of RGB channels. Two 8-bit registers are used to storing the 10-bit data.

3.1.4. Gamma Correction

SXGA series products integrate 3-channel RGB separate lookup table (LUT) to achieve high-precision gamma correction. Each LUT has 256-point, 8-bit input to 10-bit output resolution.

At power-on default state, gamma correction is disabled, the LUTs were filled with random values. 8-bit input video data is directly sent to the MSB of 10-bit output bus, and the low 2-bit is set to 0. User needs to initializes the LUT before enabled the gamma correction, otherwise there might be display irregularly.

The LUT's working is depended on the external input clock signal (VCLK), when the Reset pin is release (set to 1), wait at least 1024 VCLK cycles before to operating the LUT. If no VCLK, the LUT's operating does not have any error response, but the actual operating will not been performed, even to enabled the gamma correction.

The LUT's operating using a register groups and special timing, details refer to section 3.6.3.

3.2. 3D Video Display

Register 20H.bit1 used to enable the 3D function and 20H.bit0 used to set the polarity of 3D input signal, cooperated with 3D pin's input (Pin9), the 3D video display can be achieved. If 3D pin's input level is same as the setting of 20H.bit0, the video input is valid, and the frame/field video will be updated, otherwise, video input is invalid and the display will keep the current frame/field. 3D pin's signal is latched at VS falling edge. 3D video display timing is shown in Figure 3-4.

In progressive mode, 3D video signal using frame timing mode, such as the odd frame is updated left display, and the even frame is updated right display.

In interlaced mode, 3D video signal using field timing mode, such as the odd field is updated left display, and the even field is updated right display. At this point, the vertical resolution of each field is lower compare with the source, the bit5 and bit4 of register(02H) should be set to "11", display will repeat to display each line in next line automatically, to ensure that the image aspect ratio and display.

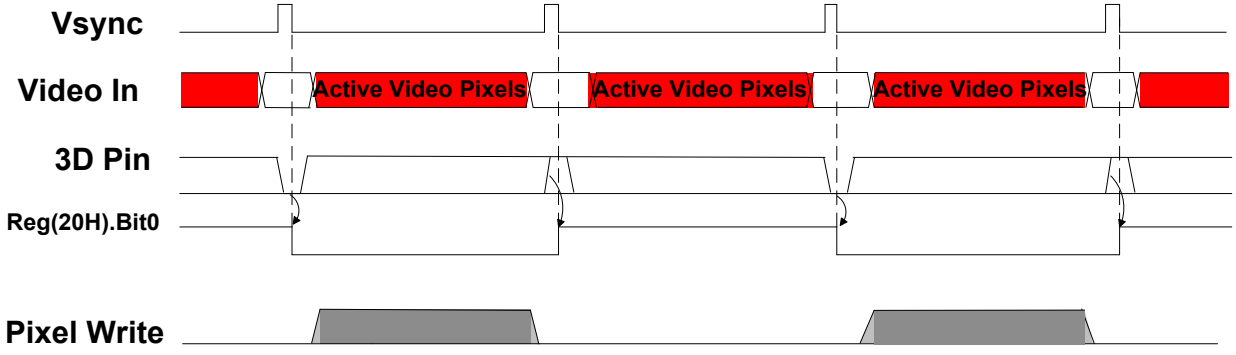


Figure 3-4 3D Video Display Timing

3.3. Power Supply & Reset

SXGA060 need 1.8V and 5V power supply. The 1.8V is used for digital core. 5V is used for OLED pixels driver, D/A converter and DC-DC module. To ensure the display image quality, please note that ripple and noise rejection of 5V power supply.

3.3.1. Power UP/Down Sequence

The system power-up mechanism relies on the clock signal (VCLK), so the power supply and VCLK input sequence is very important. SXGA060 requires first provide VCLK, followed is 1.8v, and last is 5V. The working principle is shown by following figure and section 3.3.2.

If the power-up sequence cannot meet requirements, SXGA060's working state may abnormal. In that case, after the reset and initialization operations, user can set the PDOWN (Register 40H.Bit7) to 1 first, and wait 20ms, then set PDOWN to 0.

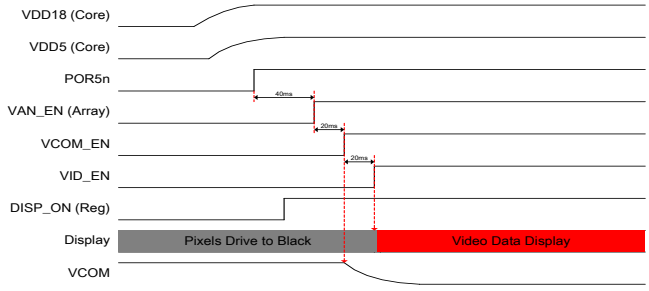


Figure 3-5 Power-up Sequence ($V_{th\_1.8}$=1.2V)

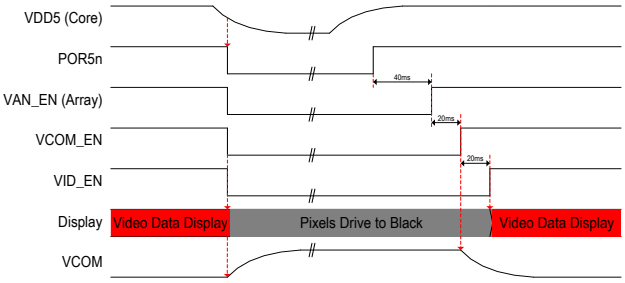


Figure 3-6 V5.0 Power Down & Up (Vth=4V)

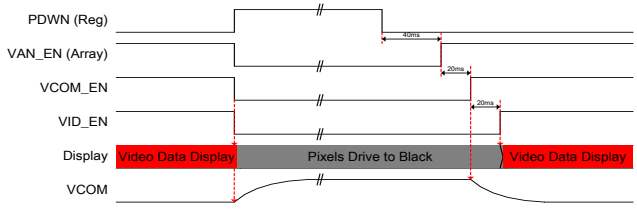


Figure 3-7 Register Control Power Down & Up

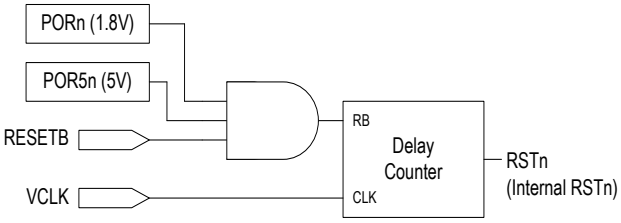


Figure 3-8 Reset Block Diagram

3.3.2. Reset Sequence

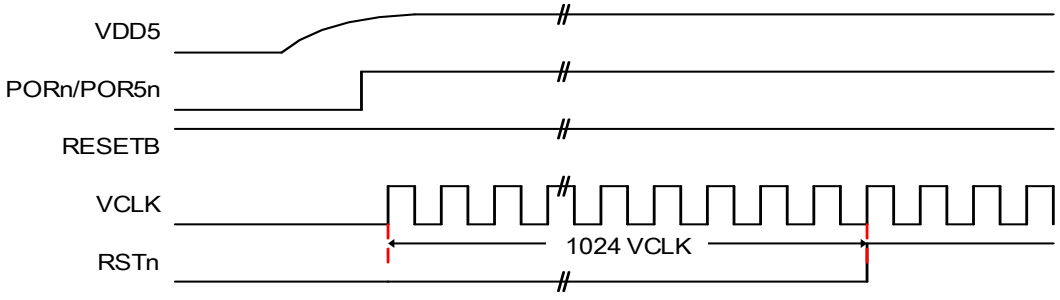


Figure 3-9 Reset Timing Case 1 – No external reset pin used (RESETB=1)

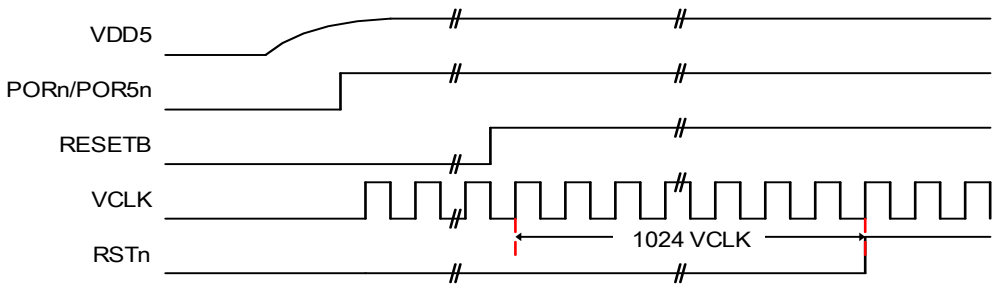


Figure 3-10 Reset Timing Case 2 – External reset pin depend on VCLK

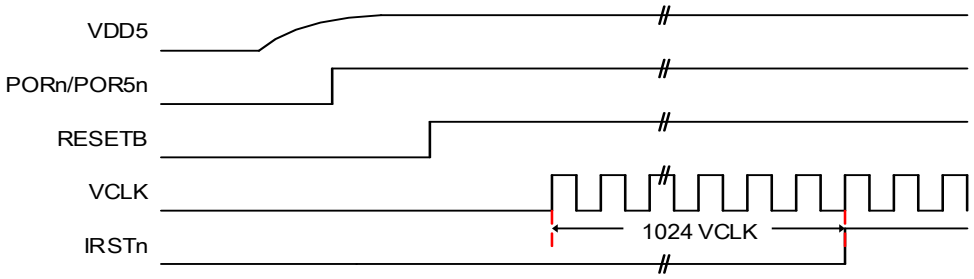


Figure 3-11 Reset Timing Case 3 – External reset pin applied

3.4. DC/DC Converter

OLED emitting light needs to be applied positive bias voltage between the anode and cathode, the anode voltage from 5V power supply is controlled by drive transistor, all pixel's common cathode voltage Vcom supplied by DC/DC converter on the PCB backplane. The driving pulse of DC/DC converter is generated by the internal programmable pulse generator, the circuit shown in Figure 3-12. Vcom adjustment range is 0 ~-3V, corresponding to 9-bit registers 34:35H, the typical working curve is shown in Figure 3-13

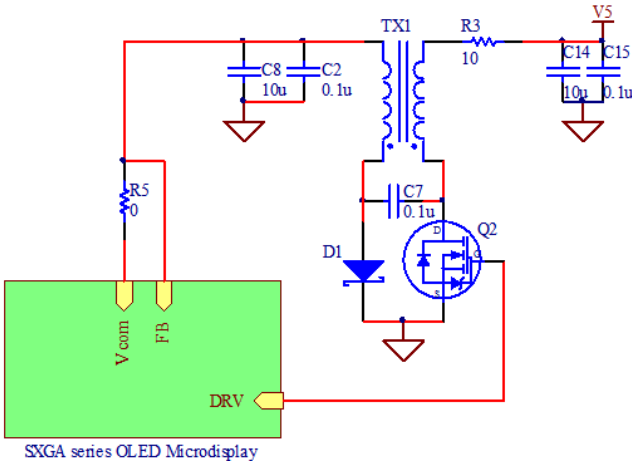


Figure 3-12 DC/DC Principal Diagram

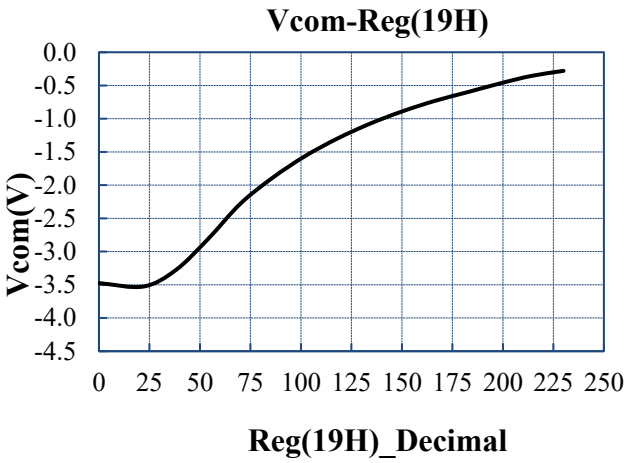


Figure 3-13 Vcom Programmable Working Curve

3.5. Temperature Sensor

The working of SXGA060's temperature sensor depend on external VS signal, and the measured value update period is 256 cycles of VS signal (if VS=60Hz, it's about 4.3s). To use the temperature sensor exactly three registers must be set as follow:

- Reg(32H) = 0xA0
- Reg(36H) = 0x18
- Reg(37H) = 0x32

The value of register 39H is the measured value of internal temperature sensor. So the real-time internal working temperature can be read out through the two-wire serial interface. The temperature value and the readout conversion relation is:

$$T = 0.47 \times \text{Reg}\ (39H) - 40$$

The temperature sensor response curve and the calibration curve are shown as Figure 3-14 and Figure 3-15.

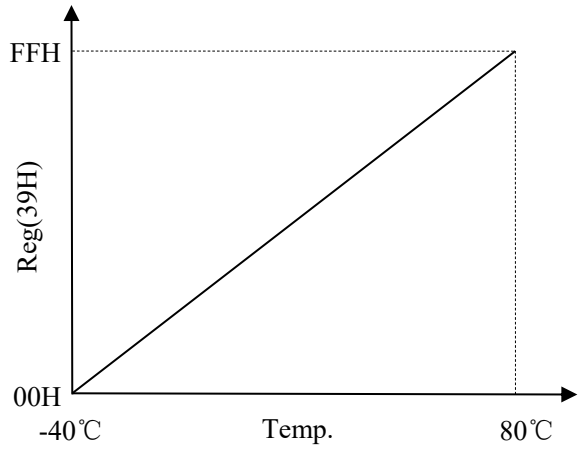


Figure 3-14 Temp. Sensor Readout

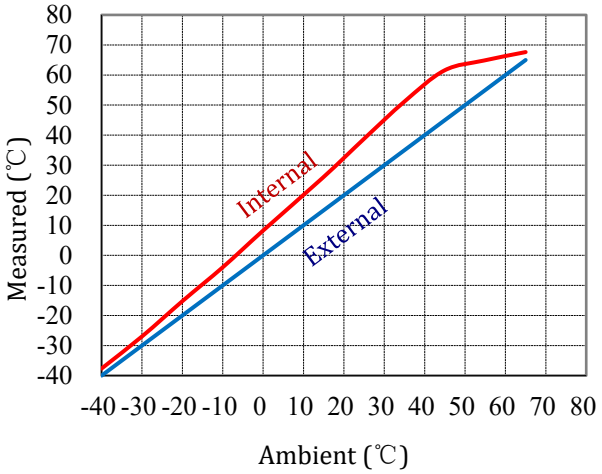


Figure 3-15 Temp. Sensor calibration curve

3.6. Two-wire Serial Interface

SXGA060's two-wire serial interface compatible only with the random address read/write operations of I2C communication standard.

SXGA060 series microdisplay acts as a slave for receiving and transmitting data, all read/write operations must be launched by the master. The SDA and SCL line has been pulled up to internal 1.8v via 10k resistor.

User can realize the display programmable control by use two-wire interface, such as digital video signal decoding and processing, gamma correction, Vcom adjustment and so on. Key Features and tags of the two-wire serial communication:

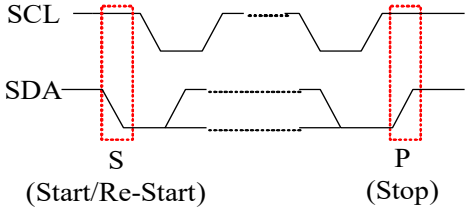


Figure 3-16 Start & Stop Timing

1) Communication speed (SCL) support from 100K to 1MHz;
2) 8-bits Slave Address consists of 7-bits device address and 1-bit read/write flag;

3) Start/Re-Start: SDA change from HIGH to LOW while SCL is HIGH, See Figure 3-16;
4) Stop: SDA change from LOW to HIGH while SCL is HIGH, see Figure 3-16;
5) ACK: SDA is LOW during the acknowledge clock pulse;
6) NAK: SDA is HIGH during the acknowledge clock pulse;
7) One transmission includes 8bit data and an acknowledge bit, total nine clock of SCL;
8) Except Start and Stop condition:
   - HIGH or LOW state of SDA can only being changed while SCL is LOW
   - Data on the SDA line must be stable during the HIGH period of the SCL

3.6.1. Communication Operating

- Write data (Figure 3-17) :
  1) Master sends Start condition (S)
  2) Master sends 7bit Slave Address and 1bit write flag ($\overline{W}$) represents as low
  3) Slave sends 1bit ACK (A) response
  4) Master sends 8bit register address (Register)
  5) Slave sends 1bit ACK (A) response
  6) Master sends 8bit data (Data)
  7) Slave sends 1bit ACK (A) response
  8) Master sends stop condition(P)

S	Slave Addr	$\overline{W}$	A	Register	A	Data	A	P

Figure 3-17 Write Data format

- Read Data (Figure 3-18)
  1) Master sends Start condition (S)
  2) Master sends 7bit Slave Address and 1bit Write flag ($\overline{W}$) represents as low
  3) Slave sends ACK (A) response
  4) Master sends 8bit Register Address (Register)
  5) Slave sends 1bit ACK (A) response
  6) Master sends 1bit Re-Start condition (Sr)
  7) Master sends 7bit Slave Address and 1bit Read flag (R) represents as high
  8) Slave sends 1bit ACK (A) response
  9) Slave sends 8bit Data (Data)
  10) Master sends 1bit NAK ($\overline{A}$) response
  11) Master sends Stop condition (P)

S	Slave Addr	$\overline{W}$	A	Register	A	Sr	Slave Addr	R	A	Data	$\overline{A}$	P

Figure 3-18 Data format (Master reads from Slave)

3.6.2. Serial Interface Bus Address Selection

Two salve address of SXGA060 series microdisplay can be selected by an externally SelAdr0 pin. The SelAdr0 pin has an internal resistor (10K) to pull up to 1.8V power. One of microdisplay's SelAdr0 pin must be connected to GND when used in binocular stereovision application. Microdisplay's corresponding read/write address is shown as Table 3-2.

Table 3-2 Slave Address list

A7 (MSB)	A6	A5	A4	A3	A2	A1 (SelAdr0)	A0 (R/$\overline{W}$)	Slave Address (R/$\overline{W}$)
0	0	0	1	1	1	1(Default)	1/0	1FH/1EH
0	0	0	1	1	1	0	1/0	1DH/1CH

3.6.3. Gamma LUT operation

SXGA060 integrate 3-channel RGB separate lookup table (LUT), each LUT has 256×10-bit data, the LUTs addressing rang beyond 8-bit. SXGA060 use a register groups and special timing to achieve the LUTs operation by indirect addressing mode. The register group definition refers to Table 3-3.

Table 3-3 The register group of Gamma function

Channel	LUT Addressing Register	LUT Data Register		Control Register(10H)		
		MSB_Data[9:8]	LSB_Data[7:0]	En	Read	Update
R	11H	12H	13H	Bit6	Bit5	Bit2
G	14H	15H	16H		Bit4	Bit1
B	17H	18H	19H		Bit3	Bit0

- Write LUT (Example as R channel)
  1) Check 10H.Bit5 = 0;
  2) Initialiation the gamma correction RedData(0~255), Addr=0;
  3) Write the Addr to 11H;
  4) Write RedData(Addr)_[9:8] to 12H;
  5) Write RedData(Addr)_[7:0] to 13H; //means: LUT_Red[Addr] = RedData(Addr)
  6) Addr=Addr+1;
  7) repeat 3~6, until Addr=256;
  8) Set 10H.Bit2=1; //Updating the LUT_Red
- Read LUT (Example as R channel)
  1) Check 10H.Bit5 = 0;
  2) Define arrays ready to receive data; //RData(256)
  3) Addr=0;
  4) Write Addr to 11H
  5) Set 10H.Bit5=1; //Start Reading
  6) wait 10H.Bit5=0; //Data Ready
  7) Read 12H to RData(Addr)_[9:8];
  8) Read 13H to RData(Addr)_[7:0]; // Get RData(Addr)
  9) Addr=Addr+1;
  10) Repeat 4~9, until Addr=256;

4. REGISTER DESCRIPTION

4.1. Summary of Registers

Table 4-1 Summary of Registers

Register	Bytes	Description	Default Value
00H	1	Chip's Revision	10H
01H	1	VCLK and Sync Mode Setting	03H
02H	1	Video Mode Setting	43H
03H	1	Vertical Blank Lines Setting	00H
04H	1	Horizontal Blank Pixels Setting	00H
05H	1	Reserved	-
06H	1	Test Pattern Enable and Mode Setting	00H
07:08H	2	R Channel 10-bit Gray Setting for Pattern Mode(0BH)	000H
09:0AH	2	G Channel 10-bit Gray Setting for Pattern Mode(0BH)	000H
0B:0CH	2	B Channel 10-bit Gray Setting for Pattern Mode(0BH)	000H
0DH	1	Reserved	-
0EH	1	Video Signal Brightness Control	80H
0FH	1	Video Signal Contrast Control	80H
10H	1	Video Coding and Gamma Function Control	40H
11H	1	R Channel LUT Addressing Register	00H
12:13H	2	R Channel 10-bit Correction Data Register	000H
14H	1	G Channel LUT Addressing Register	00H
15:16H	2	G Channel 10-bit Correction Data Register	000H
17H	1	B Channel LUT Addressing Register	00H
18:19H	2	B Channel 10-bit Correction Data Register	000H
1AH~1FH	6	Reserved	-
20H	1	3D Function Control	00H
21H	1	Display On, 2× Zoom and Scanning Direction Control	40H
22:23H	2	Left Margin 9-bit Register	002H
24:25H	2	Right Margin 9-bit Register	002H
26:27H	2	Top Margin 9-bit Register	002H
28:29H	1	Bottom Margin 9-bit Register	002H
30H	1	DAC Offset Control	80H
31H	1	DAC Current Control	44H
32H	1	DAC Function Control	87H
33H	1	DC/DC Function Control	42H
34:35H	2	Vcom 9-bit Setting	1FFH
36H~38H	3	Reserved	-
39H	1	Temperature Output Value	xxH
3AH~3FH	6	Reserved	-
40H	1	Power Down Mode Control	00H

4.2. Detailed Information of Register

Category	Register	R/W	Bit	Function	Default	Description
Revision	00H	R	7:4	Product	0001b	0001b : SXGA
			3:0	Revision	0000b	0000b : Revision Number
Input Video Control	01H	R/W	7	DDRMode	0b	0b : SDR 1b : DDR
			6	DDR Swap	0b	0b : 1st Data Start at VCLK Falling Edge 1b : 1st Data Start at VCLK Rising Edge
			5	Field Swap	0b	0b : Normal Field Sync 1b : Inverted Field Sync
			3	Vsync Polarity	0b	0b : Active High 1b : Active Low
			2	Hsync Polarity	0b	
			1:0	Sync Mode	11b	00b : Embedded Sync 10b : External Sync without DE 11b : External Sync wity DE
Input Video Control	02H	R/W	7:6	SAV Offset	01b	00b : 1 Pixel before Input SAV 01b : Same as Input SAV 10b : 1 Pixel after Input SAV 11b : 2 Pixel after Input SAV
			5:4	Interlace Mode	00b	00b : Progressive 10b : Interlaced 11b : Pseudo-Interlaced (for Field 3D)
			3	DAC CLK Mode	0b	0b : VCLK / 2 1b : Same as VCLK
			2:0	Data Mode	011b	000b : 16-bit 422 YCbCr 001b : 24-bit 444 YCbCr 010b : 8-bit Mono 011b : 24-bit 444 RGB 100b : 8-bit 422 YCbCr
	03H	R/W	7:0	V Blank	00H	Vertical Blank Lines
	04H		7:0	H Blank	00H	Horizontal Blank Pixels
Test Pattern Control	06H	R/W	3:0	Test Pattern Mode	0H	0H : Normal (Test Pattern Closed) 1H : Color Bar 2H : Gray Scale 3H : Checker Board (40×40) 4H : Alternating every 2 Rows 5H : Alternating every 2 Columns 6H : All Black 7H : All White 8H : All Red 9H : All Green AH : All Blue BH : Adjusted R/G/B (Any Gray Level)
RGB Gray for Pattern(0BH)	07H	R/W	1:0	TP Red [9:8]	00b	R Channel 10-bit Gray Value
	08H		7:0	TP Red [7:0]	00H	
	09H		1:0	TP Green [9:8]	00b	G Channel 10-bit Gray Value
	0AH		7:0	TP Green [7:0]	00H	
	0BH		1:0	TP Red [9:8]	00b	B Channel 10-bit Gray Value
	0CH		7:0	TP Red [7:0]	00H	
Video Enhancement	0EH	R/W	7:0	Brightness	80H	00H : Darkest 80H : No Change FFH : Brightest
	0FH	R/W	7:0	Contrast	80H	00H : Black Screen 80H : No Change FFH : Double Contrast
Gamma Function Control	10H	R/W	7	Gray Code	0b	0b : Binary Code 1b : Gray Code
			6	LUTs Bypass	1b	0b : Gamma Control Enable 1b : Gamma Control Disable
			5	R LUTs Read	0b	0b : Read Done 1b : Read Start (Automatic Clear after Read)
			4	G LUTs Read	0b	
			3	B LUTs Read	0b	

Category	Register	R/W	Bit	Function	Default	Description
			2	R LUTs Update	0b	0b : Update Done 1b : Update Start (Automatic Clear after Update)
			1	G LUTs Update	0b	
			0	B LUTs Update	0b	
Gamma LUTs Control	11H	R/W	7:0	R _LUTs_ Address	00H	Read/Write Address for Red Gamma LUTs
	12H		1:0	R_LUTs_Data[9:8]	00b	Read/Write Data[9:0] for Red Gamma LUTs
	13H		7:0	R_LUTs_Data[7:0]	00H	
	14H		7:0	G _LUTs_ Address	00H	Read/Write Address for Green Gamma LUTs
	15H		1:0	G_LUTs_Data[9:8]	00b	Read/Write Data[9:0] for Green Gamma LUTs
	16H		7:0	G_LUTs_Data[7:0]	00H	
	17H		7:0	B _LUTs_ Address	00H	Read/Write Address for Blue Gamma LUTs
	18H		1:0	B_LUTs_Data[9:8]	00b	Read/Write Data[9:0] for Blue Gamma LUTs
	19H		7:0	B_LUTs_Data[7:0]	00H	
3D Function	20H	R/W	1	3D Mode	0b	0b : Disable 1b : Enable
			0	3D Polarity	0b	0b : Active when 3D pin is High 1b : Active when 3D pin is Low
Display Control	21H	R/W	7	Display On	0b	0b : Display Off 1b : Display On
			4	Discharge	1b	0b : Disable 1b : Enable
			3	Column 2×	0b	0b : Disable 1b : Enable (1 Col/Row expand to 2 Col/Rows)
			2	Row 2×	0b	
			1	Horizontal Mirror	0b	0b : Disable (Left to Right, Top to Bottom)
			0	Vertical Mirror	0b	1b : Enable (Right to Left, Bottom to Top)
Display Position Control	22H	R/W	0	Left Margin [8]	0b	Display Left Margin [8:0]
	23H		7:0	Left Margin [7:0]	02H	
	24H		0	Right Margin [8]	0b	Display Right Margin [8:0]
	25H		7:0	Right Margin [7:0]	02H	
	26H		0	Top Margin [8]	0b	Display Top Margin [8:0]
	27H		7:0	Top Margin [7:0]	02H	
	28H		0	Bottom Margin [8]	0b	Display Bottom Margin [8:0]
	29H		7:0	Bottom Margin [7:0]	02H	
DAC Control	30H	R/W	7:0	DAC Offset	80H	00H : -40% 80H : 0% FFH : +40%
	31H	R/W	6:4	DAC Current	100b	Adjust DAC Current
			2:0	DAC Buffer Current	100b	Adjust DAC Buffer Current
	32H	R/W	7:6	DAC CLK Delay	10b	00b : -1 VCLK 01b : -1/2 VCLK 10b : Normal 11b : +1/2 VCLK
			5	DAC Output	0b	0b : Disable 1b : Enable
			4	DAC Fly Speed	0b	0b : Slow 1b : Fast
			3	Test	0b	0b : Disable 1b : Enable
			2:0	Dummy Load	111b	000b : Disable 111b : Enable
DC-DC Control	33H	R/W	7	DC-DC CLK	0b	0b : VCLK 1b : Internsal OSC
			6:4	DC-DC Duty	100b	000b : 1:7 001b : 2:6 010b : 3:5 011b : 4:4 100b : 5:3 101b : 6:2 110b : 7:1
			3	DC-DC Driver 2×	0b	0b : Normal 1b : 2× Driver

Category	Register	R/W	Bit	Function	Default	Description
			2:0	DC-DC Divide	010b	000b : 8 001b : 16 010b : 32 011b : 64 100b : 128 101b : 256 110b : 512 111b : 1024
Vcom Setting	34H	R/W	0	VcomLevel [8]	1b	Programble Vcom Level [8:0]
	35H		7:0	VcomLevel [7:0]	FFH	
Temperature	39H	R	7:0	Temperature Value	0～FFH	Temperature Output Value
Power Down Mode	40H	R/W	7	All	0b	0b : Normal 1b : Power-Down
			3	DAC	0b	
			2	DAC Buffer	0b	
			1	DC-DC	0b	
			0	Temperature Sensor	0b	

4.3. Register Setting Examples

4.3.1. 24 bit 444 RGB Mode

Register	Setting	Description
01H	02H	SDR Mode, VCLK Falling, Polarity is High, External Sync Without DE
02H	4BH	Same as SAV, Progressive, DAC CLK=VCLK, 24Bit 444 RGB
03H	27H	V_Blank =39
04H	96H	H_Blank = 150
22:23H	002H	Left Margin = 2
24:25H	002H	Right Margin = 2
25:26H	002H	Top Margin = 2
27:28H	002H	Bottom Margin = 2
32H	**A0H**	**DAC Setting**
34:35H	0F0H	Vcom Setting
36H	**18H**	**Necessarily if Temp Sensor is used(Refer to Section 3.5)**
37H	**32H**	**Necessarily if Temp Sensor is used (Refer to Section 3.5)**
21H	80H	Display On, Mirror Disable

4.3.2. Display Position Setting

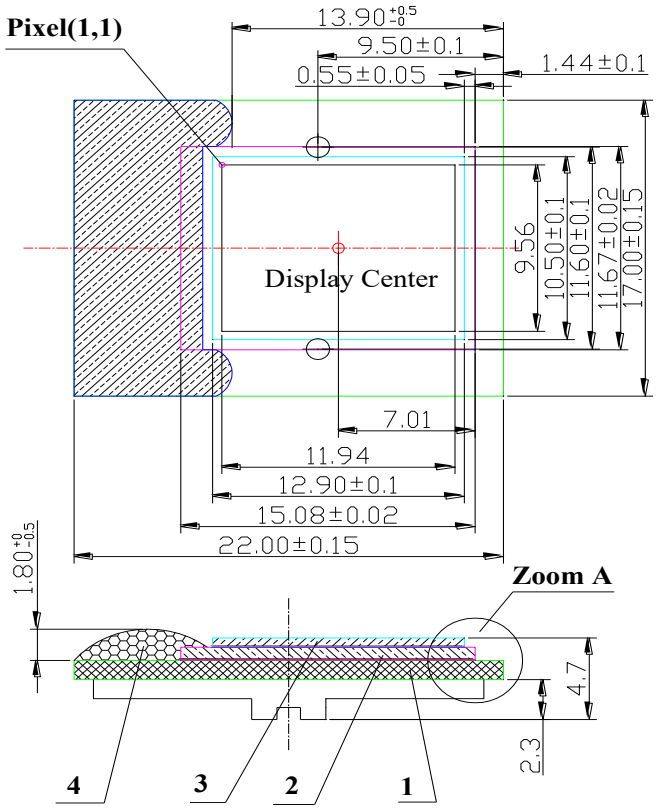
Left Margin = Right Margin = (1284 – X_Resolution) / 2

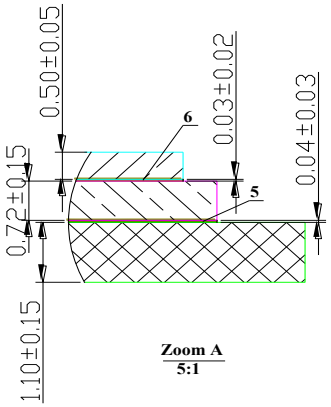
Top Margin = Bottom Margin = (1028 – Y_Resolution) / 2

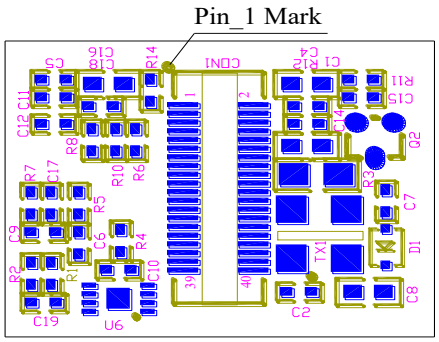
Table 4-2 Display Position Setting Example

Video Mode			Register Setting					
Mode	**Scan mode**	**Display**	**Reg(01 H)**	**Reg(07 H)**	**Reg(11 h)**	**Reg(12 H)**	**Reg(13 H)**	**Reg(14 H)**
SXGA	Progressive	800×600	3CH	00H	02H	02H	02H	02H
VGA	Progressive	640×480	3CH	00H	52H	52H	52H	3EH
SMPTE-170M-1	Interlaced	640×480	21H	00H	52H	52H	52H	3EH
SMPTE-170M-2	Interlaced	800×600	3DH	00H	02H	02H	02H	02H
NTSC	Interlaced	640×480	41H	04H	52H	52H	52H	3EH
PAL	Interlaced	640×480	41H	05H	52H	52H	52H	3EH
NTSC (SQ)	Interlaced	640×480	41H	00H	52H	52H	52H	3EH
PAL (SQ)	Interlaced	768×576	41H	00H	12H	12H	14H	0EH

5. MECHANICAL CHARACTERISTICS







6	Adhesive	Scale	OLiGHTEK Co., Ltd.			
5	OLED Layer & Adhesive	3.2:1				
4	Wirebond Encap		Title	SXGA060 Assembly Drawing		
3	Glass Cover					
2	Si-Base Sub		Designed	ZHQ	Version	V1.0
1	PCB Backboard		Checked	YXH	Date	Jul 18, 2013
Item	Name		Approved	LYW	Sheets	1/1

6. USAGE RECOMMENDATIONS

6.1. Cleaning

- Avoid using any acid, alkali and organic solvent to clean or contact to the display
- Using the lens paper or clean cloth to clean the surface is recommend

6.2. General Handling Considerations

- Do not expose the display to strong acids, alkalis, or solvents.
- Do not expose the display surface to UV or other strong ionizing radiation.
- Do not using sharp objects to contact the glass and silicon regions of display.
- Avoid applying force to the any region except the PCB backplane, especially apply the force to the region of sealing, silicon edge and cover glass is not allowed.
- Avoid immersion of the display in any liquid.
- Handing with PVC clean gloves is recommended.

6.3. Abnormal Prevention

The SXGA060 micro display may show an abnormal image while the sync signal is unstable especially the VSync. But user can prevent this situation by following steps:

1) When unstable signal is detected: clear the bit 7 of Reg(21H) to turn off the display;
2) When stable signal is detected: set the bit 7 of Reg(21H) to turn on the display;

6.4. Static Charge Prevention

The microdisplay is sensitive to electro-static discharge due to integrated CMOS circuit in the display. The following measures are recommended to minimize ESD occurrences:

- Operate on a region which is equipped with electro-static eliminator, such as ionizing air blowers.
- Wear the anti-static wrist strap
- wear the non-chargeable clothes
- Keep away from charged region.

Figure 6-1 Method of handing displays

6.5. Storage

6.5.1. Short Term Storage

The display should be stored in a dry environment with temperature range from -50℃ to 90℃ for a short period(≤100h).

6.5.2. Long Term Storage

If the display is stored in such an environment with excessive heat or cold or moisture, the lifetime of display will be shorten, even the environment can cause permanent damage to the display. Recommended long-term storage condition as follows:

- Room temperature: 25℃±5℃
- Dry environment: dry nitrogen or vacuum sealing cabinet
- Static placing: avoid violent vibration

7. APPENDIX

7.1. List of Figures

7.2. List of Tables