

DSVGA

800 X 600 LOW POWER COLOR XL AMOLED MICRODISPLAY



DATASHEET: Version 02

For Part Number:

Color XL DSVGA Microdisplay: EMA-101125

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Page 2 of 82

TABLE OF CONTENT

1. INTRODUCTION.....	5
2. GENERAL DESCRIPTION	6
3. INPUT / OUTPUT DESCRIPTION	9
4. PIXEL ARRAY LAYOUT	10
5. ELECTRICAL CHARACTERISTICS.....	11
5.1 TIMING CHARACTERISTICS	14
5.1.1 Interface Timing Diagrams.....	14
5.1.2 Gamma Sensor Timing Diagram	15
6. OPTICAL CHARACTERISTICS.....	17
7. MECHANICAL CHARACTERISTICS.....	18
7.1 COLOR/MONOCROME DSVGA CONFIGURATION	20
8. DETAILED FUNCTIONAL DESCRIPTION	21
8.1 VIDEO INPUT INTERFACE	21
8.1.1 Gamma Correction	21
8.2 D/A CONVERSION	22
8.3 FORMAT AND TIMING CONTROL	24
8.3.1 Vertical Position Control.....	24
8.3.2 Horizontal Position Control	24
8.3.3 Row Duty Rate Control.....	25
8.4 SENSOR FUNCTIONS	26
8.4.1 Temperature Readout	26
8.4.2 Luminance Regulation Sensor	26
8.4.3 Pixel Bias Sensor	26
8.4.4 Luminance Control (Analog Dimming)	26
8.4.5 Luminance Setting	27
8.4.6 Luminance Control (PWM Dimming).....	28
8.4.7 Gamma Correction Sensor	29
8.5 DC-DC CONVERTER	33
8.6 I ² C SERIAL INTERFACE.....	35
8.7 POWER-ON SEQUENCE.....	36
8.8 POWER-SAVINGS MODE.....	38
8.8.1 Display-Off Function	39
9. REGISTER MAP SUMMARY.....	40
10. DETAILED REGISTER DESCRIPTIONS	44
10.1 STAT (00H)	44
10.2 VINMODE (01H)	44
10.3 DISPMODE (02H).....	46
10.4 LFTPOS (03H).....	47
10.5 RGTPPOS (04H).....	47
10.6 TOPPOS (05H)	48
10.7 BOTPOS (06H).....	48
10.8 RESERVED (07H).....	48
10.9 RESERVED (08H).....	49
10.10 ROWRESET (09H, 0AH)	49
10.11 RAMPCTL (0BH).....	49
10.12 RAMPCM (0CH)	51
10.13 VDACMX (0DH).....	51

10.14	BIASN	52
10.15	GAMMASET (0Fh)	53
10.16	VCOMMODE (10H).....	54
10.17	VCOMCTL (11H).....	55
10.18	VGMAX (12H)	56
10.19	MVCOM (13H).....	56
10.20	IDRF (14H)	57
10.21	DIMCTL (15H).....	58
10.22	TREFDIV (16H)	58
10.23	TEMPOFF (17H)	59
10.24	TUPDATE (18H)	59
10.25	TEMPOUT (19H)	60
10.26	ANGPWRDN (1Ah)	62
10.27	SYSPWRDN (1Bh).....	63
10.28	TPMODE (1Ch)	64
10.29	TPLINWTH (1Dh).....	65
10.30	TPCOLSP (1Eh).....	66
10.31	TPROWSP (1Fh).....	66
10.32	TPCOLOR (20H)	66
10.33	LUT_ADDT (21H)	67
10.34	LUT_DATA (22H, 23H)	67
10.35	LUT_UPDATE (24H).....	67
10.36	PUCTRL (25H).....	68
10.37	V_BLANK (26H).....	68
10.38	H_BLANK (27H).....	69
10.39	V_OFFSET (28H).....	69
10.40	H_DLY (29H)	69
10.41	RESERVED (2Ah)	70
10.42	CSCC0 (2Bh)	70
10.43	CSCC1 (2Ch, 2Dh)	70
10.44	CSCC2 (2Eh, 2Fh)	70
10.45	CSCC3 (30H, 31H).....	71
10.46	CSCC4 (32H, 33H).....	71
10.47	CSCC5 (34H, 35H).....	71
10.48	RESERVED (36H)	71
10.49	DIGTEST (37H).....	71
10.50	NOFLINE (38H, 39H)	72
10.51	NOFPXL (3Ah, 3Bh)	72
10.52	RESERVED (3Ch~42H)	72
11.	APPENDIX A: APPLICATION SYSTEM DIAGRAM.....	73
12.	APPENDIX B: MICRODISPLAY CARRIER BOARD.....	74
13.	APPENDIX C: EEPROM MEMORY MAP	75
14.	APPENDIX D: RECOMMENDED REGISTER SETTINGS.....	79
15.	APPENDIX E: CLEANING, HANDLING AND STORAGE CONDITIONS	81
15.1	CLEANING	81
15.2	GENERAL HANDLING CONSIDERATIONS.....	81
15.3	STATIC CHARGE PREVENTION	81
15.4	PROTECTION FROM DUST AND DIRT.....	82
15.5	SHORT TERM STORAGE	82
15.6	LONG TERM STORAGE.....	82

1. INTRODUCTION

The DSVGA XL device from eMagin Corporation is an active-matrix organic light emitting diode (AMOLED) micro display intended for near-to-eye applications that demand high image quality, compact size, and very low power. Combining a total of 1,542,528 active OLED dots, the DSVGA display is built on a single crystal silicon backplane and features eMagin's proprietary thin-film OLED XL technology offering extended life and luminance performance.

The active array is comprised of 824 x 624 square pixels with a 15-micron pitch and a 75% fill factor. An extra 24 columns and 24 rows (beyond the 800 x 600 main array) are provided to enable the active DSVGA display to be shifted by steps of 1 pixel in the X and Y directions for temporal dithering or optical alignment purposes. Additional dummy and test pixels surround the active array. Each full pixel is laid out as three 5 x 15 micron identical sub-pixels, which together form the 15-micron square RGB color group. Three primary color filter stripes are applied in alignment with the sub-pixels on a white-emissive OLED layer to form the color display. Monochrome capability is accomplished by building the display without color filter, and configuring it for monochrome use. In this case, each pixel has a built-in triple redundancy (3 sub-pixels per pixel sharing the same information)

The DSVGA design features eMagin's proprietary "Deep Black" architecture that ensures off- pixels are truly black, automatically optimizes contrast under all conditions, and delivers improved pixel uniformity. In addition to its flexible matrix addressing circuitry, the DSVGA includes an internal 10-bit DAC that ensures a full 256 gamma-corrected gray level, an on-chip set of look-up-tables for digital gamma correction, and a novel pulse-width-modulation (PWM) function that, together with the standard analog control, provides an extended dimming range. The PWM function also enables an impulse drive mode of operation that significantly reduces motion artifacts in high speed scene changes

The DSVGA micro display has a 24-bit parallel RGB digital input as well as an 8-bit and a 16-bit 4:2:2 color input. In addition, the DSVGA support an 8-bit monochrome serial mode compatible with the BT-656 video standard.

In addition, the DSVGA display carrier board also includes a non-volatile memory component, accessible via the I2C serial bus. This component contains the preferred register settings for the DSVGA micro display.

Detailed device specifications and application information for the DSVGA XL micro display produced by eMagin Corporation are provided in this document.

2. GENERAL DESCRIPTION

Color DSVGA Micro display

Parameter	Specification ¹
Display Type	Emissive, Color Active Matrix Organic Light Emitting Diode on Silicon
Format	800 (x3) x 600 pixels
Total Pixel Array	824 (x3) x 624 pixels
Color Pixel Aspect Ratio	15 micron square color group
Color Pixel Arrangement	R, G, B Vertical Stripe
Display Area	12.36 x 9.36 mm (15.50 mm diagonal, 0.61")
Useable Display Area	12 x 9 mm (15.0 mm diagonal, 0.59")
Mechanical Envelope	18.0 x 16.0 x 5.01 mm (rigid carrier board)
Weight	~ 2 grams
Gray Levels	256 per primary color
Uniformity	> 85% end to end
Contrast Ratio	> 1000:1 typical
Dimming Ratio	>400:1 with CR> 1,000:1 typical
White Luminance (Color display)	≥ 150 cd/m ² (front luminance), DSVGA 60Hz VESA mode
Video Interface	RGB 24-bit Digital 1.8V CMOS
Video Source Clock	65 MHz maximum (VESA mode), up to 120 Hz frame rate
Control & Serial Interface	Digital 1.8V CMOS
Power Interface	
IO/Front-end Supply (VDD1.8)	1.8 Volts DC @ 10 mA maximum
Array/Analog Supply ² (VDD5)	5.0 Volts DC @ 50 mA maximum
Bias Supply (VPG)	-1.5 Volts DC @ 1 nA maximum
Operating Ambient Temperature	-45°C to +70°C
Storage Temperature	-55°C to +90°C
Humidity	85%RH non-condensing

Note 1: The above data represents performance specifications, measured at 20°C.

Note 2: Includes internally generated negative cathode supply.

Functional Overview

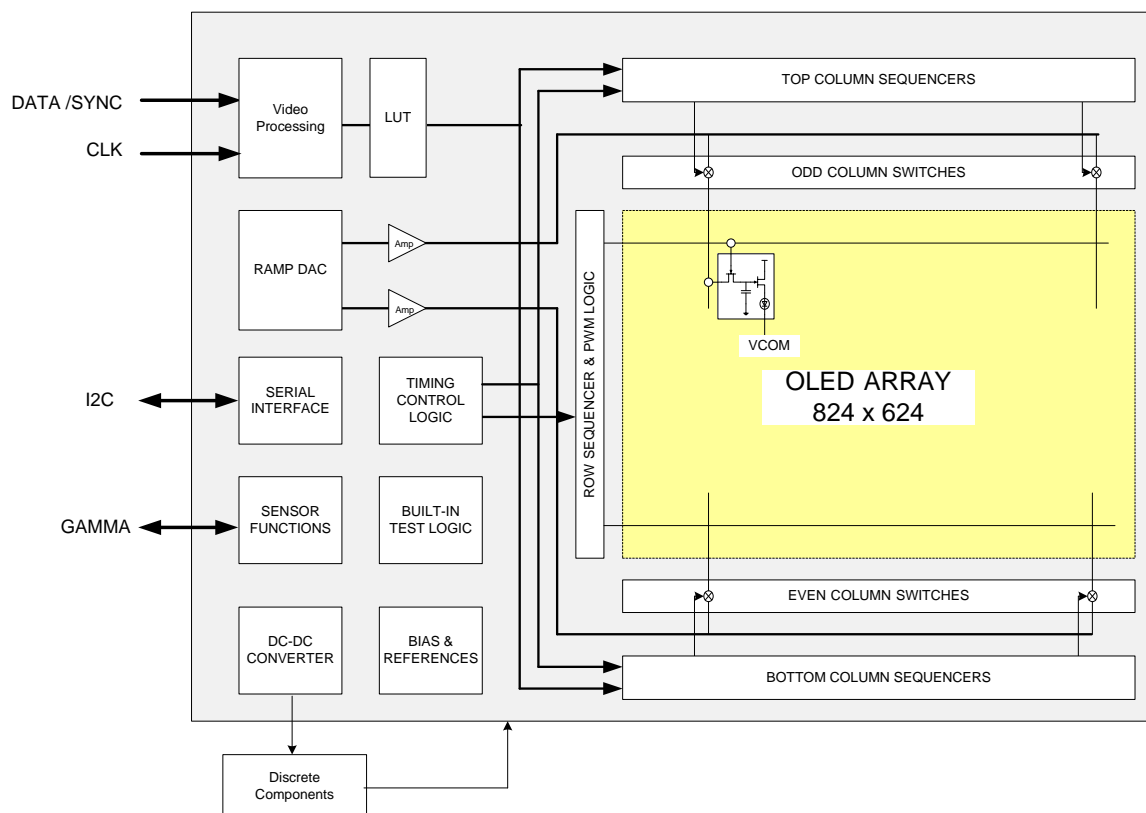


Figure 1 : Color DSVGA design block diagram

The top-level block diagram for the DSVGA micro display is shown in Figure 1. Bi-directional row and column sequencer circuits are used for addressing individual cells within the 824 x 624 x 3 pixel array, and internal digital-to-analog conversion circuits are included for converting the digital input data into the analog signals needed for programming the pixels. A storage element (capacitor) resides at each pixel cell that is used to set the gray level.

The digital video input data is applied individually to each of the three RGB sub-pixels of the color group in color mode. The RGB data inputs that make up the digital data port are configured as three 8-bit data busses. Odd columns are driven by data sequencers located at the top of the array and even columns by bottom side sequencers. To obtain a linear gray-scale response from the OLED pixels the digital input data must be formatted with Gamma correction.

Table 2-1 DSVGA Microdisplay Video Formats

Video Data Format	Color Space	DINR[7:0]	DING[7:0]	DINB[7:0]
8-bit Mono	Y	N.C.	Y[7:0]	N.C.
8-bit, 4:2:2 (BT656)	YCbCr	N.C.	YCbCr[7:0]	N.C.
16-bit, 4:2:2	YCbCr	N.C.	Y[7:0]	CbCr[7:0]
24-bit, 4:4:4	YCbCr	Cr[7:0]	Y[7:0]	Cb[7:0]
24-bit, 4:4:4	RGB	R[7:0]	G[7:0]	B[7:0]

The DSVGA supports a variety of input video formats as shown in Table 1. The different formats are set using the DATA_MODE bits of the VINMODE register (01h). The YCrCb formats allow for simpler integration with mobile consumer video systems.

Note that a color DSVGA can be used with a monochrome input provided the Red, Green and Blue input data pins are tied together.

The pixel clock and sync signals for various video formats are supplied externally and converted into individual control signals by the internal timing logic block.

The sensor block provides a number of signals for setting and regulating the display operation. These include a digital readout of the on-chip temperature, a reference level for maintaining constant luminance over temperature, a gamma correction feedback signal, and internal reference levels used for programming luminance over a wide range.

An on-chip dc-to-dc converter controller allows for the generation of the OLED cathode supply, relying on a few external passive components. The converter is an adjustable inverter that converts VDD5 to a negative supply used to bias the cathodes connected in common for all the array pixels via the VCOM input.

The 2-wire serial interface is a slave only I²C compatible controller with a programmable address via an external pin (LSB). The interface provides access (read and write) to on chip registers. The registers will allow the display to be configured for its various video modes and associated clock parameters. Additional control settings include luminance control, image orientation and position, internal vs. external function selection, self-test mode and various sensor settings.

The RESETB pin provides an asynchronous hardware reset function. When this pin is set to zero the display will turn off and the internal registers will be reset to their default state. After this pin is released (set to VDD5), bit DISPOFF in register DISPMODE must be set high in order for the display to turn-on. If unused, this pin may be left unconnected.

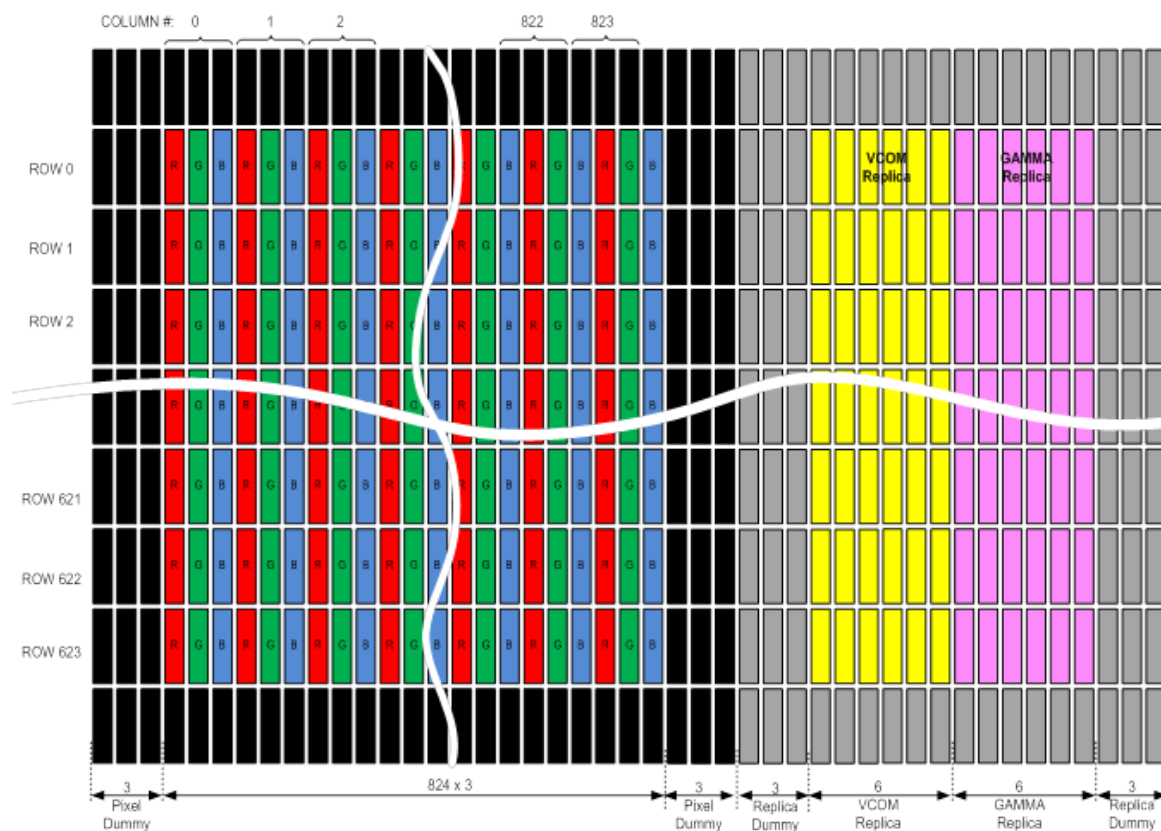
3. INPUT / OUTPUT DESCRIPTION

Miniature 40 pin connector part number: Hirose DF12D(3.0)-40DP-0.5V

Table 3-1 : Input / Output Pin Description for Color DSVGA Display

Pin #	Pin Name	Type	Description
1	GND	Power	Power return terminal.
2	SERADD	Logic In	I2C Address Bit (LSB)
3	R0	Logic In	Red Data Bit 0
4	G0	Logic In	Green Data Bit 0
5	R1	Logic In	Red Data Bit 1
6	G1	Logic In	Green Data Bit 1
7	R2	Logic In	Red Data Bit 2
8	G2	Logic In	Green Data Bit 2
9	R3	Logic In	Red Data Bit 3
10	G3	Logic In	Green Data Bit 3
11	R4	Logic In	Red Data Bit 4
12	G4	Logic In	Green Data Bit 4
13	R5	Logic In	Red Data Bit 5
14	G5	Power	Green Data Bit 5
15	R6	Power	Red Data Bit 6
16	G6	Logic In	Green Data Bit 6
17	R7	Logic In	Red Data Bit 7
18	G7	Logic In	Green Data Bit 7
19	VDD5 (VAN)	Power	Input power for Pixel Array and Analog Circuit (5 VDC).
20	VPG	Power In	-1.5 VDC Input Voltage
21	B0	Logic In	Blue Data Bit 0
22	PIXCLK (SCLK)	Logic In	Pixel Clock Input
23	B1	Logic In	Blue Data Bit 1
24	RESETB	Logic In	Asynchronous system reset (active low).
25	B2	Logic In	Blue Data Bit 2
26	HSYNC	Logic In	Horizontal Sync. Input
27	B3	Logic In	Blue Data Bit 3
28	VSYNC	Logic In	Vertical Sync. Input
29	B4	Logic In	Blue Data Bit 4
30	DATAEN	Logic In	DATA Enable Input
31	B5	Logic In	Blue Data Bit 5
32	SDA	Logi I/O	I2C Data Line - Internally tied to +5V via a 10K pull-up
33	B6	Logic In	Blue Data Bit 6
34	SCL	Logic In	I2C Input Clock
35	B7	Logic In	Blue Data Bit 7
36	VGN	Analog Out	Gamma Calibration Voltage
37	GND	Power	Power return terminal.
38	VDD1.8 (VDD)	Power	Input power for Logic Circuit (1.8 VDC).
39	BURNIN	Logic In	Reserved for Test – Keep tied to GND
40	VDD5 (VAN)	Power	Input power for Pixel Array and Analog Circuit (5 VDC).

4. PIXEL ARRAY LAYOUT



5. ELECTRICAL CHARACTERISTICS

Table 5-1 : Absolute Maximum Ratings

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD1.8	Front End Power Supply	-0.3		1.95	VDC
VDD5	Array Power Supply	-0.3		5.5	VDC
VCOM	Common electrode bias	-6		0	VDC
VPG	Array Bias Supply	-3		0	VDC
VI	Input Voltage Range	-0.3		VDD1.8+0.3	VDC
VO	Output Voltage Range	-0.3		VDD1.8+0.3	VDC
PD	Power Dissipation			1	W
Tst	Storage Temperature	-55		+90	°C
Tj	Junction Temperature	-45		+125	°C
Ilu	Latch up current			+100	mA
Vesd	Electrostatic Discharge – Human Body Model			±2000	V

Stresses at or above those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the following tables is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability (except for the reverse bias condition. See below). Prolonged exposure to high temperatures will shorten the luminance half-life.

Table 5-2 : Recommended Operating Conditions

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD1.8	Front End Power Supply	1.75	1.8	1.95	VDC
VDD5	Array Power Supply	4.75	5	5.25	VDC
VCOM	Common electrode bias	-5	-2.0	0	VDC
VPG	Array Bias Supply	-3	-1.5	0	VDC
Tst	Storage Temperature	-55		+90	°C
Ta	Ambient Operating Temp.	-45	+25	+70	°C

Table 5-3 : DC Characteristics

(Ta = 25°C, VDD1.8 = +1.8V, VDD5 = +5V, GND = 0V)

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD1.8	Front End Power Supply		1.8		V
VDD5	Array Power Supply		5		V
VCOM	Common electrode bias	-5	-2.0	0	V
VPG	Array Bias Supply		-1.5		V
Vil	Digital input low level	GND-0.3		1	V
Vih ⁽²⁾	Digital input high level	1.8		VDD1.8+0.3	V
Vol	Digital output low level			0.5	V
Voh ⁽²⁾	Digital output high level	1.8			V
Vsl	Hsync, Vsync input low	GND-0.3		1	V
Vsh	Hsync, Vsync input high	1.8		VDD1.8+0.3	V
VGN	Gamma feedback signal	0		2.5	V

(1) Assumes a gamma corrected display with a nominal gamma of 1.0

(2) Except for SCL which can be operated between +1.8V and +3.3VDC
SDA is internally tied to +5V via an internal 10K-Ohms pull up resistor (R8)

Table 5-4 : AC Characteristics

-45°C < Ta < +70°C, GND = 0V, VDD1.8= +1.8V, VDD5 = +5.0V VPG = -1.5V, I_{pix_avg} = 6 nA

Symbol	Parameter	Min	Typ.	Max.	Unit
SCLK	Video Clock Frequency	12	-	65	MHz
CLK_Duty	SCLK duty cycle	40		60	%
Fhs	Horizontal Sync frequency	15.734		80	KHz
Fvs	Vertical Sync Frequency	30		120	Hz
Trst	Reset Pulse Width	100		-	μs
Cin	Digital Pins Input Capacitance		3		pF
Cvpg	Pin VPG Input Capacitance		13.6		nF
Pd VDD5	Average Vdd5 Power Consumption (DSVGA Mode 60 Hz refresh rate)		120		mW color
Pd VDD1.8	Average VDD1.8 Power Consumption (DSVGA Mode 60 Hz refresh rate)		15		mW color
Pd VPG	Average VPG Power Consumption			1	mW
Pd PDWN	Total Power Consumption in PDWN (sleep) mode*		2.5		mW
Ta	Ambient Operating Temperature	-45		+70	°C

*Note: Input data, sync and clock lines must be inactive and held low

Power consumption measured at 60Hz refresh rate, room ambient temperature and with a TV-like color test pattern that represents an average video mode (See below Figure 2) and with 150 cd/m² when all pixels are on (white).

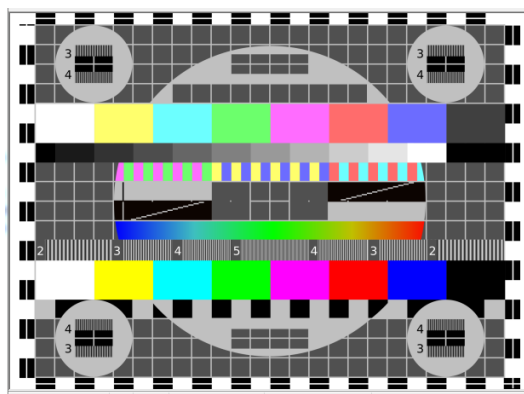


Figure 2: Color Test Pattern

5.1 Timing Characteristics

5.1.1 Interface Timing Diagrams

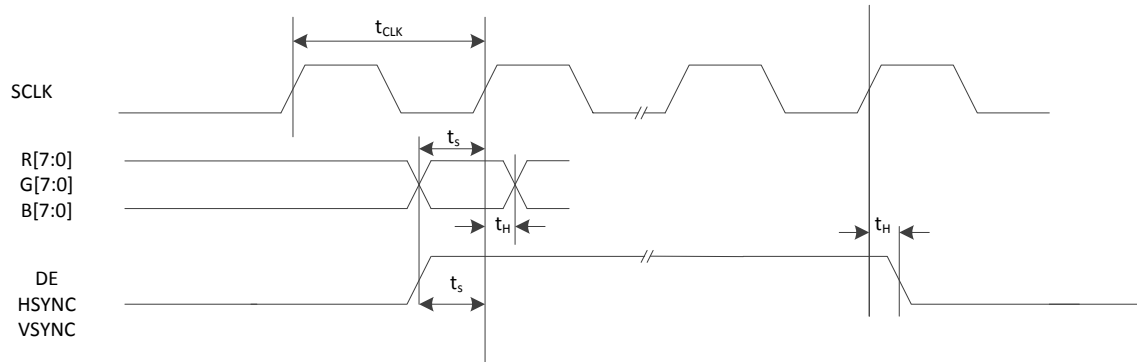


Figure 3: Pixel Timing

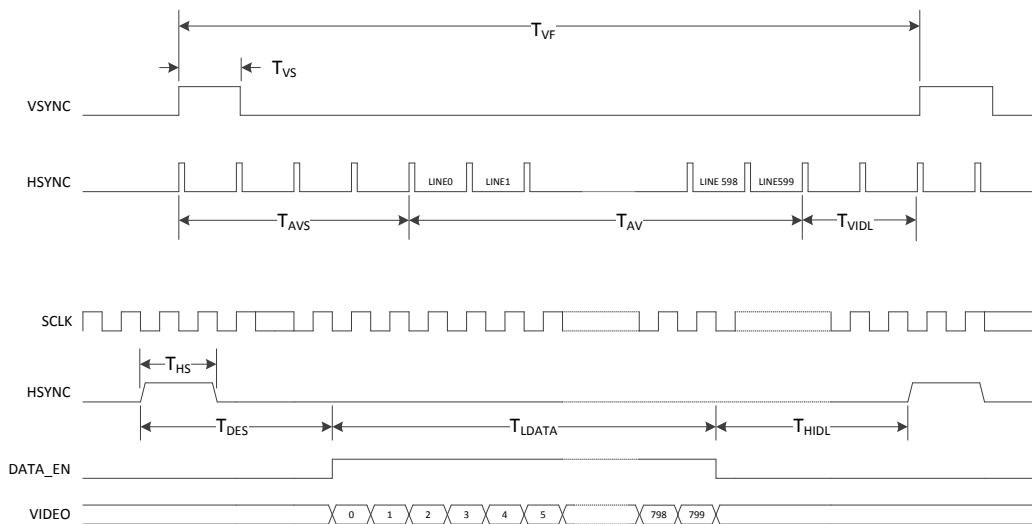


Figure 4: Line Timing

Table 5-5 : Input Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Video Input Setup/Hold (RIN/GIN/BIN)	t_S	4			ns
	t_H	1			ns
Control Signals Setup/Hold (DE/HSYNC/VSYNC)	t_S	4			ns
	t_H	1			ns
Clock Frequency	f_{CLK}		32 ¹		MHz
Clock Period	t_{CLK}		31.25		ns
Clock Duty	D_{CLK}	45		55	%
VSYNC Pulse Width	T_{VS}	2			Hsync period
Time to Active Video Start	T_{AVS}	5			Hsync period
Frame Blanking	T_{VIDL}	2			Hsync period
HSYNC Pulse Width	T_{HS}	8			SCLK period
Time to DE Start	T_{DES}	12			SCLK period
Line Overscan	T_{HIDL}	12			SCLK period

Note 1: DSVGA @ 60Hz frame rate

5.1.2 Gamma Sensor Timing Diagram

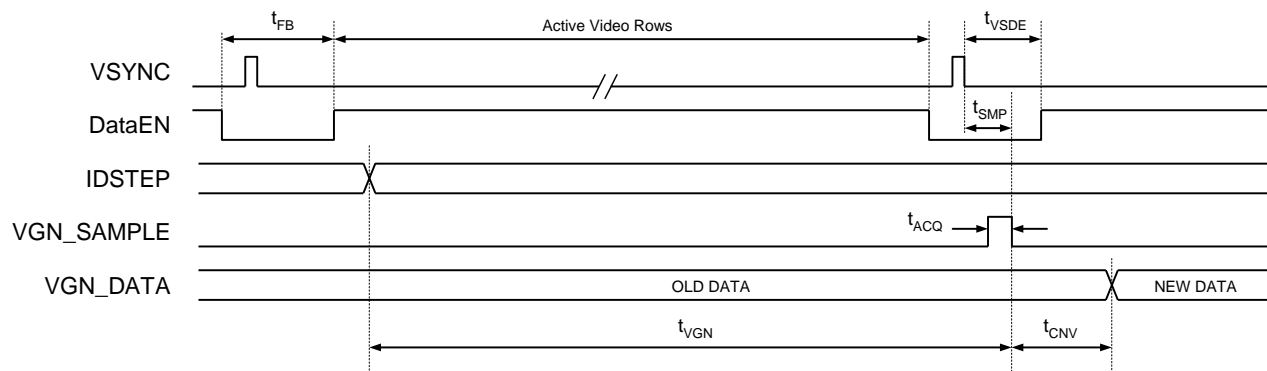


Figure 5: Gamma Sensor Timing

Table 5-6 : Gamma Sensor Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
IDSTEP to VGN Settling Time	t_{VGN}	10			ms
Frame Blanking (% of Frame Time)	t_{FB}	1			%
VGN Sampling Time	t_{SMP}	t_{ACQ}		t_{VSDE}	
A/D Acquisition Time	t_{ACQ}	20			μs
A/D Conversion Time	t_{CNV}				

6. OPTICAL CHARACTERISTICS

Table 6-1 : DSVGA Color XL Micro display Optical Characteristics

Conditions: Ta = +20°C, VDD1.8 = +1.8V, VDD5 = +5V, VPG = -1.5V, VCOM = internally generated

Symbol	Parameter	Min.	Typ.	Max.	Unit
LMAX	Front Luminance @ max gray level	0.01 ⁽¹⁾	150	250	cd/m ²
CR	White to Black Contrast Ratio		10000 : 1		
CIE White	CIE-X	0.27	0.32	0.37	
	CIE-Y	0.32	0.34	0.38	
CIE Red	CIE-X	0.570	0.600	-	
	CIE-Y	0.300	0.340	0.370	
CIE Green	CIE-X	0.180	0.250	0.330	
	CIE-Y	0.470	0.550	-	
CIE Blue	CIE-X	-	0.140	0.190	
	CIE-Y	-	0.150	0.180	
GL	Gray Levels Per Color			256	levels
F _R	Refresh Rate	30		120	Hz
FF	Emissive Area/Total Sub-pixel Area		0.74		
U _{LA}	End to end large-area uniformity	85 ⁽²⁾			%
S _{VH}	Pixel spatial noise at ½ gray level			5	%
S _{LOT}	Peak-to-peak luminance variation over operating temperature range			10 ⁽³⁾	%
T _{ON}	Time to recognizable image after application of power			0.5 ⁽⁴⁾	sec

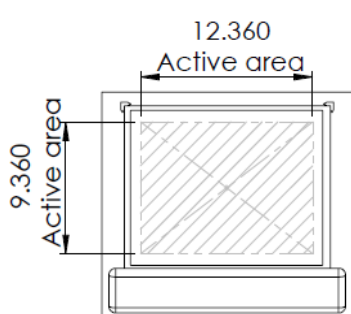
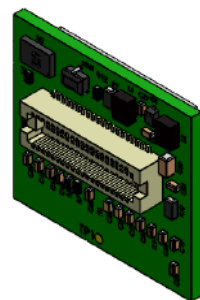
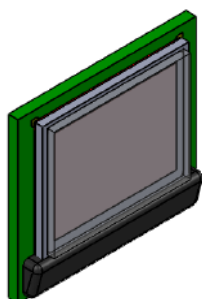
Note 1: Minimum dimming level obtained when using the ROWRESET (05h) function in addition to the IDRF and DIMCTL registers.

Note 2: At 100% of gray level brightness and 150 cd/m2 luminance. Luminance uniformity measured between the nominal values of five 1000 pixel zones located in the four extreme corners and the center zone of the display.

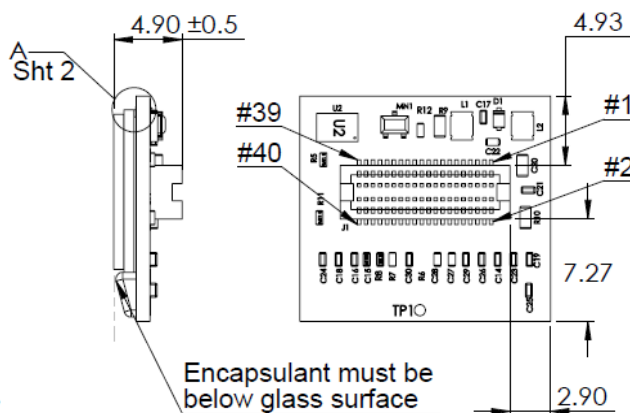
Note 3: Tighter regulation can be achieved with firmware providing temperature control of VDACMX setting.

Note 4: The actual timing may be affected by the software and firmware timing and register initializations to run the display.

REVISIONS				
ECN	REV.	DESCRIPTION	DATE	APPROVED
	01	Initial release	2/27/2013	SRM
2014-18	02	Added dimensions on sheet 2	1/28/2014	SRM
2014-49	03	Added resistor (R8) and moved components	4/22/2014	SRM



Additional dimensions
on sheet 2



1. 3D CAD models available upon request
2. Mating connector is Hirose #DF12A (3.0)-40DS
3. Component locations are approximate - do not scale
4. Glass is centered over active area, not DIE

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS LINEAR TOLERANCES: 0.0 +/- 0.05 0.00 +/- 0.15 0.000 +/- 0.05				FINISH:		DEBUR AND BREAK SHARP EDGES		DO NOT SCALE DRAWING		REVISION 03	
DRAWN: SRM		DATE: 02/27/13						TITLE: DSVGA Display Asm			
ENG: OP		02/27/13									
MFG: RK		02/27/13									
QA: CP		02/27/13									
								DWG NO.		A4	
								A04-501046			
								MATERIAL:			
								WEIGHT:			
								SCALE:10:1		SHEET 1 OF 2	

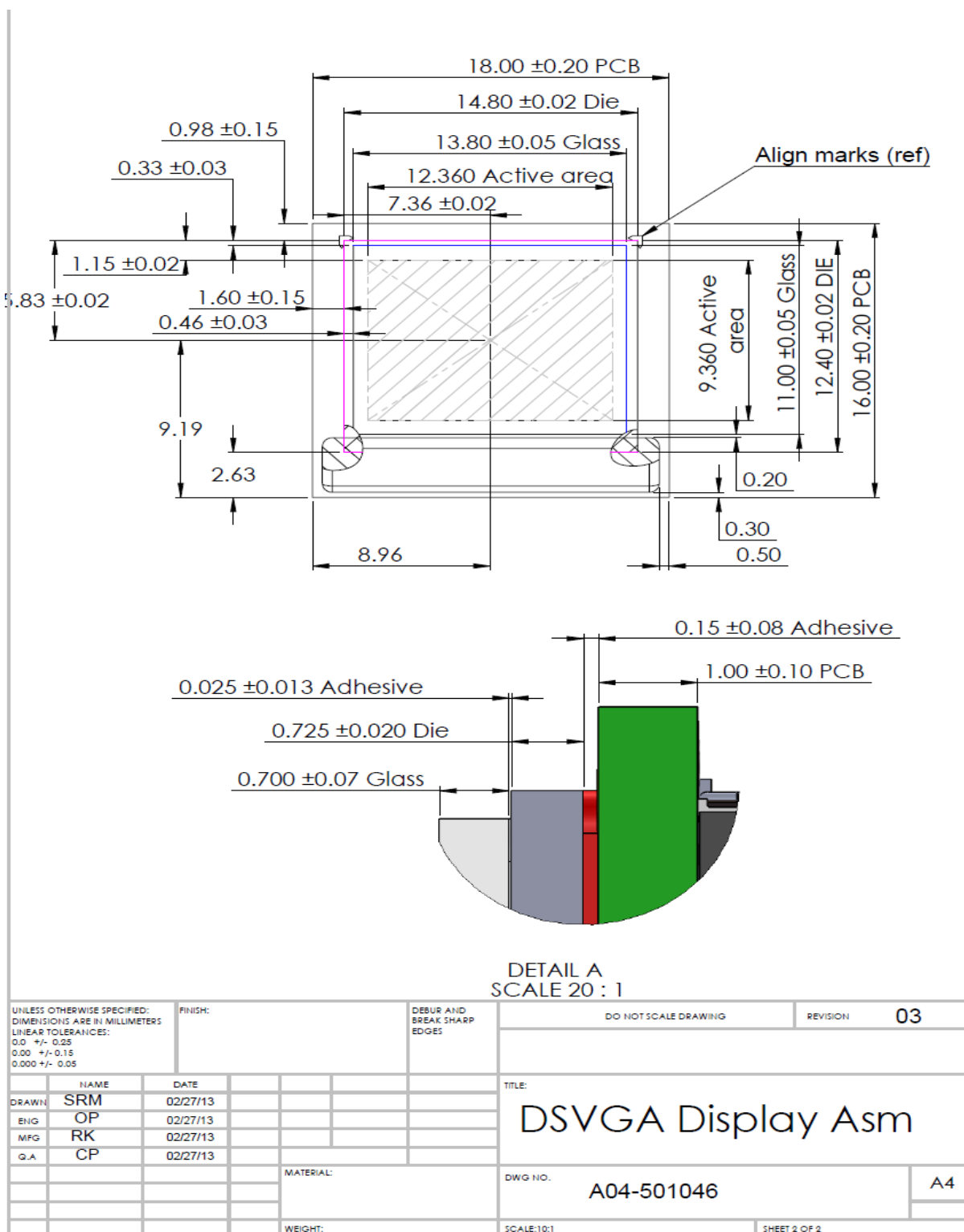


Figure 3: Color/Monochrome DSVGA Microdisplay Assembly Drawing

7.1 Color/Monochrome DSVGA Configuration

Connector J1

Manufacturer: Hirose
Manufacturer Part Number: DF12D(3.0)-40DP-0.5V

Mating Connector Information

Manufacturer: Hirose
Manufacturer Part Number: DF12A(3.0)-40DS-0.5V
Weight: < 2 grams

Printed Circuit Board Material: FR4
Printed Circuit Board Tolerances: ± 0.15 mm (both axes)

8. DETAILED FUNCTIONAL DESCRIPTION

8.1 Video Input Interface

The 24-bit digital input port is comprised of three 8-bit data busses that make up the RGB data inputs. Separate synchronization signals (VSYNC and HSYNC) and the pixel clock (SCLK) are to be provided by the external video source. The data valid signal (DE) is used to signal the start of loading a row of data into the internal line memory. An active ENABLE signal is required for the Stereovision mode (inactive for all other modes, except Interlaced Video). The timing diagram for the input data bus is shown in Figure 7.

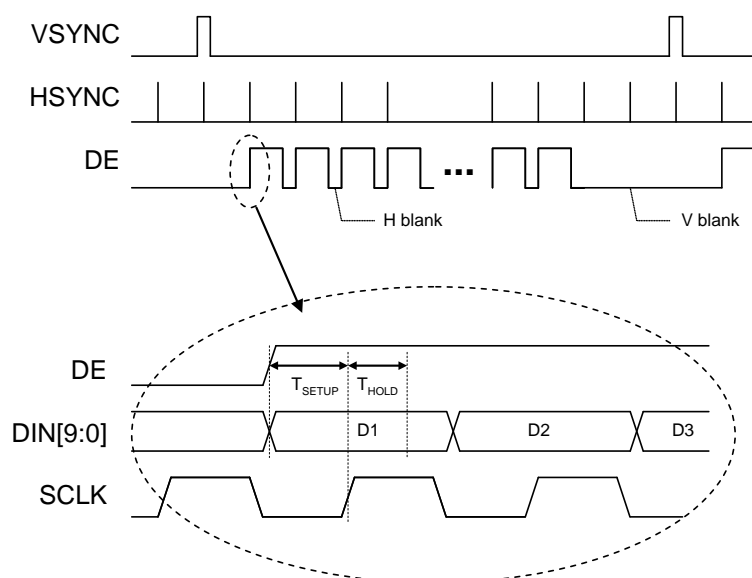


Figure 4 : Input Data timing diagram.

The input data to the display requires certain formatting that must be applied by the external drive electronics as described below.

8.1.1 Gamma Correction

Due to the non-linear electro-optic characteristic of the OLED pixel, a gamma correction signal must be applied to the video input signal to achieve a linear system response for the display. Since the optimum gamma curve will vary with temperature and luminance, it should also be regularly updated to account for changes in operating conditions. The display chip includes a LUT for each of the 3 color data paths consisting of 256 10-bit words. Each 8-bit input data value is converted to the appropriate 10-bit gamma corrected output value via the LUT. An extra LUT is included on-chip to buffer the externally generated LUT values that are provided via the serial port, and enables a fast update of the data path LUTs during

the frame overscan time. Each of the RGB LUTs can be programmed individually to control the color balance of the display.

The LUT values are generated by an external micro-controller using the VGN sensor information provided by the display chip as described in section 9.4.6. An example of a typical input transfer curve that was generated as a piecewise-linear function using a 9-entry table (Q0-Q8) is shown in Figure 8. The 8-bit source video byte is converted to a 10-bit word for input to the pixel driver. Intermediate data points are extrapolated linearly from the nearest table entries.

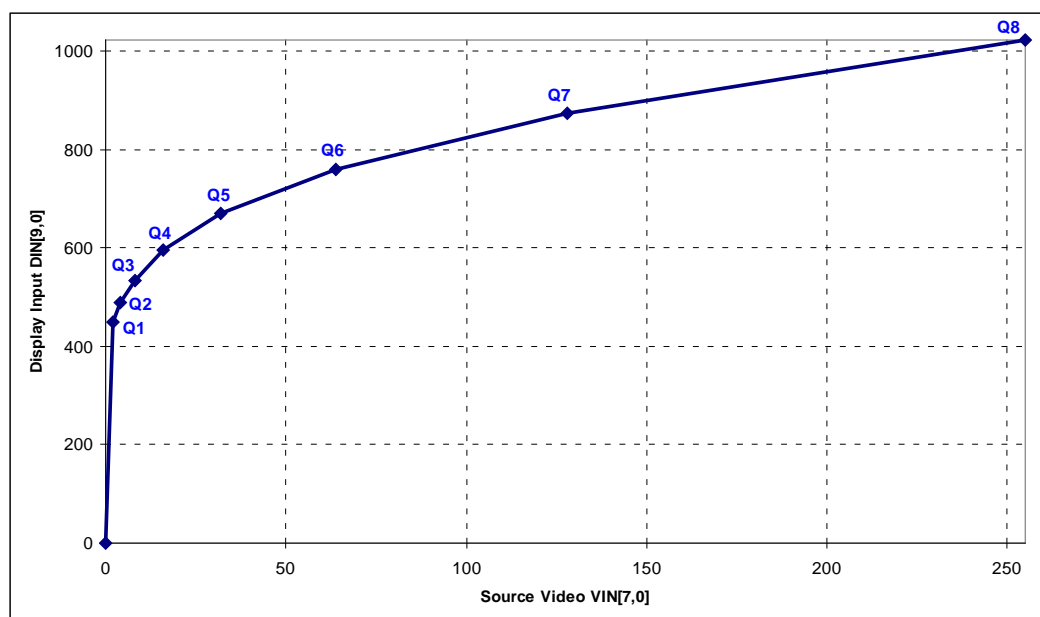


Figure 5: Typical DSVGA input transfer function

8.2 D/A Conversion

In this design the conversion of the video input signal into an analog drive signal at the pixel is carried out in a two-step process during each horizontal clock period. The digital input video data is first transformed into a precise time delay based on counts of the global RAMP clock. Second, the time delay triggers the column switch to sample the voltage of a linear ramp and to store the analog value on the column line capacitor. The selected pixel circuit copies the analog data and uses it for driving the OLED diode until it is refreshed during the next frame period.

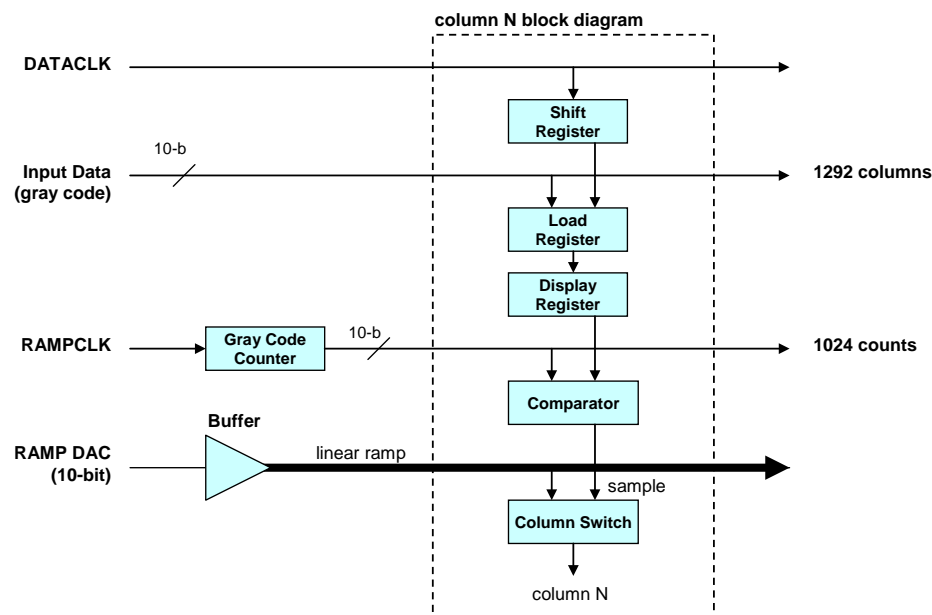


Figure 6 : Data sampling for Column N

A block diagram of one column drive circuit is shown in Figure 9. The 800 Display registers form a line memory that facilitates a pipeline mode of operation in which video data is converted to analog form and sampled by the pixels in row M during the same line period that video data for row M+1 is loading into the LOAD registers. At the end of each line period the data in the LOAD registers is transferred in parallel into the DISPLAY line memory. The externally supplied SCLK clock is used for both loading input data into the chip and for advancing the global column counter. There is a maximum latency of 2 line periods before data is displayed.

A timing diagram for the data sampling process is shown in Figure 10. The internal Ramp Generator operates at the HSYNC frequency and outputs a linear ramp with a slow rise-time and a fast reset capability that is buffered and applied to all the pixel array columns simultaneously. The RAMP signal starts synchronously with HSYNC (after a delay) with a positive slope from a zero voltage level and rises to a voltage near the VDD5 rail after 600 SCLK clock cycles as determined by a 10-bit counter. The start position of the RAMP can be adjusted via bit RAMPDLY in register RAMPCTL, its peak value can be set using register VDACMX, and the duration of the flyback transition can be selected between two options by the FLYBTIME bit in register RAMPCTL.

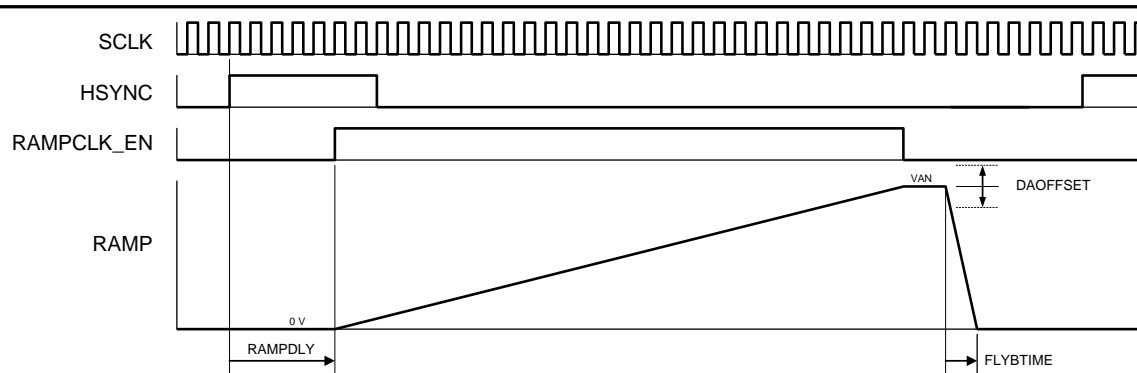


Figure 7 : Timing diagram for column data sampling

8.3 Format and Timing Control

Various control signals for the horizontal and vertical sequencers that are needed to implement the specified video formats are generated in the Timing & Control Logic block. The specific timing parameters are set by registers VINMODE, DISPMODE, LFTPOS, RGTPOS, TOPPOS, and BOTPOS using the serial interface.

The display starts up with the array in the off-state (black) by default and requires a command to the DISPOFF register bit via the serial interface to turn the display on. This provides the user with an opportunity to change the default startup conditions before the display lights up.

Bi-directional scanning is supported in both orientations via the DISPMODE register. Bit VSCAN sets the vertical scan direction, and bit HSCAN sets the horizontal scan direction.

8.3.1 Vertical Position Control

To support the vertical positioning of the display within the extra 24 pixels provided on each column of the array, an on-chip shift register function is provided in the Row sequencer logic, and controlled by registers TOPPOS and BOTPOS. The starting row for the active video is determined by register TOPPOS and the ending row by register BOTPOS, which are set by default so the active window in DSVGA mode is vertically centered in the array. The Vertical positioning logic will blank rows at the beginning and end of each frame of data to allow a vertical image shift of up to 24 pixels in steps of 1 or 2 pixels in DSVGA mode.

8.3.2 Horizontal Position Control

To support the horizontal positioning of the display within the extra 24 pixel provided on each row of the array, an on-chip shift register function is provided after the LUT block, and controlled by registers

LFTPOS and RGTPOS. The Horizontal Shifter adds black pixel data to the beginning and end of each line of data to allow a horizontal image shift of up to 24 pixels in steps of 1 pixel in DSVGA mode.

8.3.3 Row Duty Rate Control

The duty rate for a row of data is defined as the fraction of a frame period during which the pixels maintain a programmed value; for the remainder of the frame period the pixels will be driven to black.

A Row Reset function is provided in the DSVGA to allow the duty rate of rows to be controlled between 0 and 100% (default condition). The register ROWRSET[9,0] is used to set the number of Hsync cycles during which the pixel data is driven to black during a frame period. For ROWRSET=0 the pixel data is never driven to black and the duty rate for pixel data is equal to 100% (default). For ROWRSET=W the pixels in any row are driven to black for the final 2*W Hsync cycles in an active frame period.

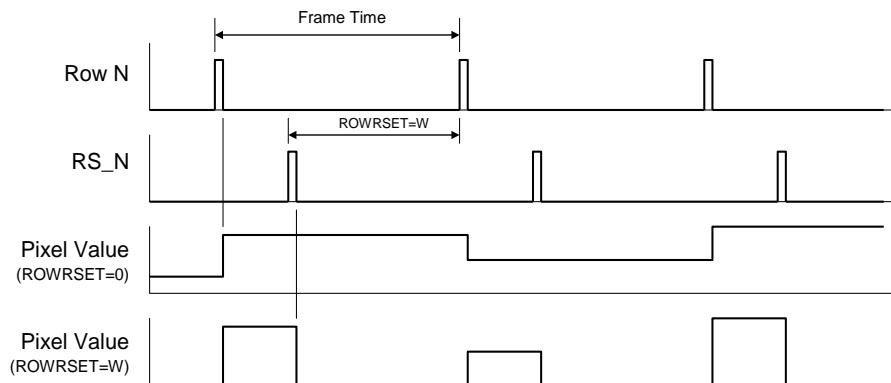


Figure 8: Timing diagram showing Row Reset functionality

The operation of the Row Reset function is depicted in the timing diagram shown in Figure 11. All the pixels contained in ROW N are programmed during the Nth horizontal line scan following the initialization line scans which occur at the beginning of a video frame. Normally this pixel data is stored in the pixel and remains unchanged until it is refreshed during the next frame period. When the Row Reset function is activated, the pulse RS_N is generated at a position determined by the value of register ROWRSET. For example, when the register value is equal to W the rising edge of RS_N occurs exactly 2*W Hsync cycles prior to the next programming cycle for ROW N. The pulse RS_N sets all the pixels in ROW N to black until the next programming cycle. All rows in the array will operate at the same duty rate. As a result the duty rate for all the rows in the pixel array will be given by

$$ROW_DUTY = \frac{2 * W * T_{Hsync}}{T_{FRAME}}$$

8.4 Sensor Functions

8.4.1 Temperature Readout

An on-chip temperature sensor provides continuous device temperature information via the serial interface. The sensing circuitry allows for calibration at power-up via dedicated registers, TREFDIV[5,0] and TEMPOFF[7,0]. The temperature reading is digitized on-chip and stored in a dedicated register, TEMPOUT[7,0]. A register bit, TSENPD in register ANGPWRDN, is able to power down the sensor.

The temperature sampling period is controlled by register TUPDATE[7,0] which allows the temperature reading to be updated between every 50msec to 4.25sec when operating at a 60Hz frame rate.

8.4.2 Luminance Regulation Sensor

Register VGMAX[7,0] controls the pixel drive voltage used for regulating the maximum luminance value. By default this level is set to about 4.95V when the VDD5 supply is equal to 5V to avoid saturating the video buffers. It can be adjusted over a range of 4 to 5V.

Register VDACMX[7,0] is used to set the maximum value of the internal Ramp DAC generator. This value should match the internal VGMAX setting for best luminance accuracy and control. The optimum setting can be derived by measuring luminance for different values of VDACMX as described in 10.13.

8.4.3 Pixel Bias Sensor

Register BIASN[1,0] sets a bias current for the OLED array in order to achieve improved control of black level and color saturation at the expense of a small increase in power consumption. In the default setting (BIASN=1) the bias contributes to a 10mW increase of power consumption for the array. It is recommended to use the BIASN=4 setting for best performance.

8.4.4 Luminance Control (Analog Dimming)

A variable luminance level is achieved by controlling the maximum pixel current while maintaining the largest possible dynamic range. Dimming control for the display is effected by adjusting the 7-bit register DIMCTL via the serial interface to provide 128 linear steps in brightness ranging from near zero to the maximum level set by register IDRFB. This functionality is only available for VCOMMODE=0 or 1.

The bits IDRFB_COARSE in register IDRFB provide a coarse adjustment of the maximum luminance level, while the IDRFB_FINE bits enable the coarse level to be fine-tuned. Figure 12 shows the typical luminance levels in a color display for various settings of the IDRFB register when DIMCTL is set for maximum brightness.

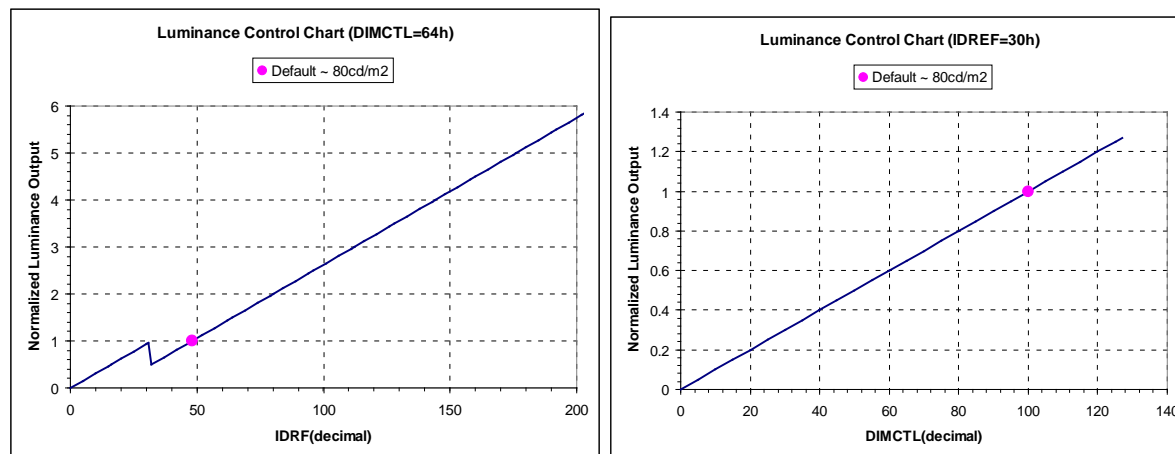


Figure 9: Typical maximum luminance for various IDRf settings

8.4.5 Luminance Setting

The DSVGA microdisplay luminance can be set to an absolute value using information included in the on-board eeprom at addresses 8E to 90.

The luminance is a linear function of IDRf for values of IDRf greater than 32 (decimal code).) that can be expressed as:

$$L = \text{slope} \times \text{IDRF (decimal)} - \text{intercept}$$

The information in registers 8E to 90 provide the slope and intercept values that govern the Luminance vs. IDRf linear equation.

Register 8E provides the integer part of the slope

Register 8F provides the fractional part of the slope

Register 90 provides the intercept value (Theoretical luminance value for IDRf = 0. It is theoretical because the linear equation is only valid for IDRf >20h (32 decimal)).

The slope and intercept values are calibrated for each display. With these values, the calculated luminance is in cd/m^2 units (nits).

The accuracy of the calculated value is smaller than or equal to 3% for luminances up to 200 cd/m^2 , and better than 5% beyond 200 cd/m^2 .

This allows precise matching between displays when used in a binocular application, as well as exceptional consistency of performance from display to display.

8.4.6 Luminance Control (PWM Dimming)

A variable luminance level can also be achieved by setting the frame on-time of the video image using register ROWRESET (05h). This register controls the fraction of a frame period during which the input video data is displayed (on-time). The display is set to black for the off-time or non-display portion of the frame period as shown in Figure 13.

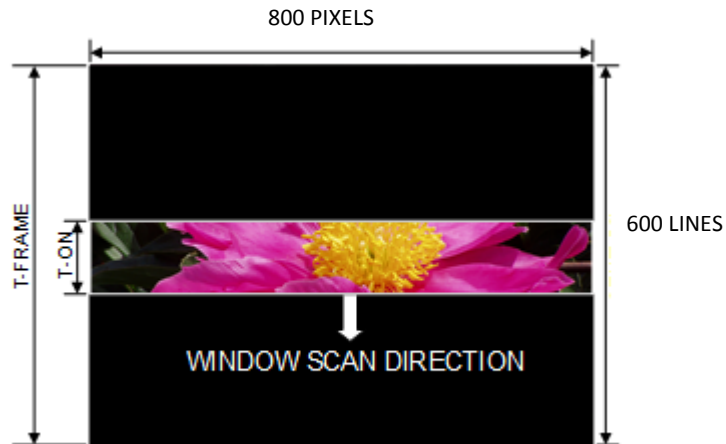


Figure 10: Video display during PWM dimming control

PWM dimming via ROWRESET can be used in combination with the analog dimming function to achieve an extended luminance control range since both modes operate independently. For any luminance level achieved via the IDRFB and DIMCTL settings, the ROWRESET function will enable the luminance to be varied over a range of 0.4 to 100%.

8.4.7 Gamma Correction Sensor

The gamma sensor is provided as an aid to generating a linear optical response from the DSVGA display system. As described previously, an external 256-entry look-up-table is required to transform input video data into a gamma-corrected data signal for driving the microdisplay input port. The DSVGA display generates an internal real-time representation of the gamma correction curve for the current operating conditions. This representation is in the form of an analog voltage waveform which can be sampled one point at a time at the VGN pin for eight specific values on the curve. A specific value VGN_i , corresponding to one of 8 internally fixed grayscale levels GL_i , is selected by setting bit IDSTEP in register GAMMASET via the serial port. The VGN signal is internally fixed for a full-scale output range of $VDD5/2$. Eight sequential measurements are required to complete the gamma table. The gamma table can then be used to reconstruct an approximation of the ideal gamma correction curve using piece-wise linear interpolation, or by employing a curve fitting algorithm to achieve more accuracy if desired. This function is only available for VCOMMODE=00h.

An external A/D converter is required to convert each VGN measurement into digitized form and to store the values in a microcontroller for further processing. A full frame period following a change in the IDSTEP bit should be provided to allow the VGN signal to settle before sampling it to 10-bit precision by the external A/D converter. It is recommended to sample the VGN signal during the frame blanking interval for best results.

The VGN readings are normalized and converted to a 10-bit full-scale word $DVGN_i[9,0]$ using the following expression:

$$DVGN_i[9,0] = \frac{VGN_i}{VGN_{MAX}} * 1023$$

Each of these data values must be further multiplied by a correction factor CF_i to obtain the Gamma table coefficients as follows:

$$GC_i[9,0] = DVGN_i * CF_i$$

NOTE

The GC_i coefficients are determined at factory test for each display and written to the on-board eeprom for retrieval by the host firmware starting at address 60h and ending at address 72h, with two bytes allocated for each GC value (see EEPROM map in Appendix D).

Typical values for factor CF_i are given in Table 8-1. The CF values are determined at the factory for the DSVGA product.

Table 8-1: Correction Factor values

CF0	CF1	CF2	CF3	CF4	CF5	CF6	CF7	CF8
0.886	0.886	0.893	0.918	0.943	0.960	0.979	0.987	1

Using the derived values for GC_i and their corresponding grayscale coordinates GL_i , the 8-entry Gamma Correction table consisting of data points $Q_i = (GL_i, GC_i)$ can be constructed. The outcome of a typical gamma sensor measurement and calculation procedure is shown in Table 9-2.

Table 8-2: Sample Gamma Correction Table

i	1	2	3	4	5	6	7	8
IDSTEP[0]	0h	1h	2h	3h	4h	5h	6h	7h
VGN_i(volt)	1.865	1.912	1.935	1.975	2.056	2.153	2.310	2.500
GC_i(dec)	504	534	562	603	664	743	862	1023
GL_i(dec)	2	4	8	16	32	64	128	255

The full 256-word LUT is derived from the Gamma Coefficient Table using linear interpolation to generate intermediate data points as illustrated in Figure 14. The input to the LUT for each color of the video source is represented by the 8-bit signal VIN [7,0], and the output of the LUT (which is also the input to the micro display) is represented by the 10-bit signal DIN[9,0]. For example, the Y coordinate for the intermediate point Q(x, y) on the line segment formed between the gamma table points Q6 and Q7 is obtained by:

$$Y = Y_6 + (Y_7 - Y_6) * \frac{(X - X_6)}{(X_7 - X_6)}$$

The intermediate points for other line segments are found in similar fashion. A software routine in the system microcontroller is used to perform the necessary calculations. A buffer LUT is used in the micro display to temporarily store the data as it is transferred from the microcontroller via the serial port. When the buffer LUT is full, the data can be rapidly transferred to the data-path LUTs during a frame blanking time to avoid disturbing the displayed image.

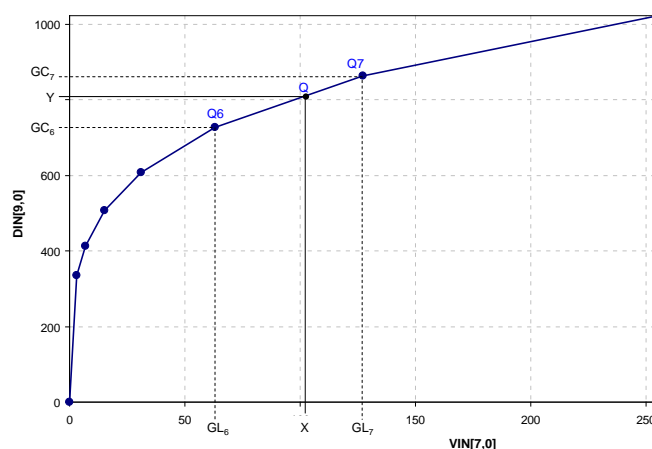


Figure 11: Gamma curve generated using PWL function

A smooth transition of the gamma curve at the lowest gray levels is essential for best performance of the display at the black end of the gray scale. Refer to Figure 15 for an illustration of the recommended approach for calculating the gamma curve at low gray levels. The LUT data points for gray levels 1 to 4 can all be generated by linear extrapolation from the gamma points Q1 and Q2. The LUT data point for gray level 0 (also defined as Q0) is a fixed value that is user-defined, and normally should be set to a very low value, e.g. 1, to ensure the best black level. The value for Q0 is shown on the graphical interface screen supplied with the DSVGA design reference kit for user convenience. It is not affected by the gamma sensor signal and can only be changed manually by user input.

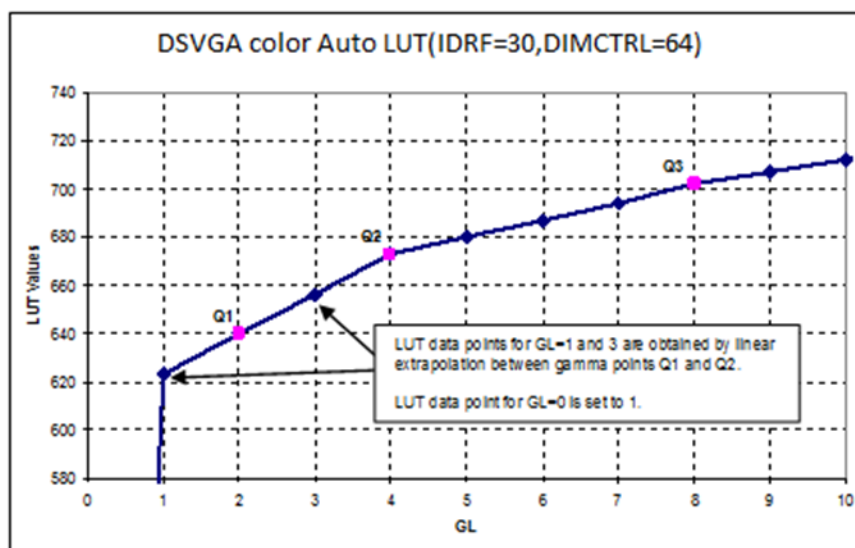


Figure 12: Gamma curve at low gray levels

An arbitrary optical response function for the microdisplay can be obtained by performing an additional operation on the gamma coefficients before generating the gamma correction curve as described previously. For example, the relationship between the output luminance of the display (y) and the gray level input to the LUT (x) can be defined in terms of the system gamma (γ) by the following expression:

$$y = x^\gamma$$

The corresponding gamma coefficients are then given by the following expression:

$$GC_i^\gamma = \left(\frac{VGN_i}{VGN_{MAX}} * CF_i \right)^\gamma * 1023$$

For the case of a linear optical response ($\gamma=1$) this expression reduces to the simpler form given previously. Examples of gamma curves generated from the same VGN values for different settings of the System Gamma parameter are shown in Figure 16 and the corresponding system response curves for the display are given in Figure 17.

The System Gamma function is implemented in the DSVGA DRK Firmware and is accessible to the user in the DRK UI Software.

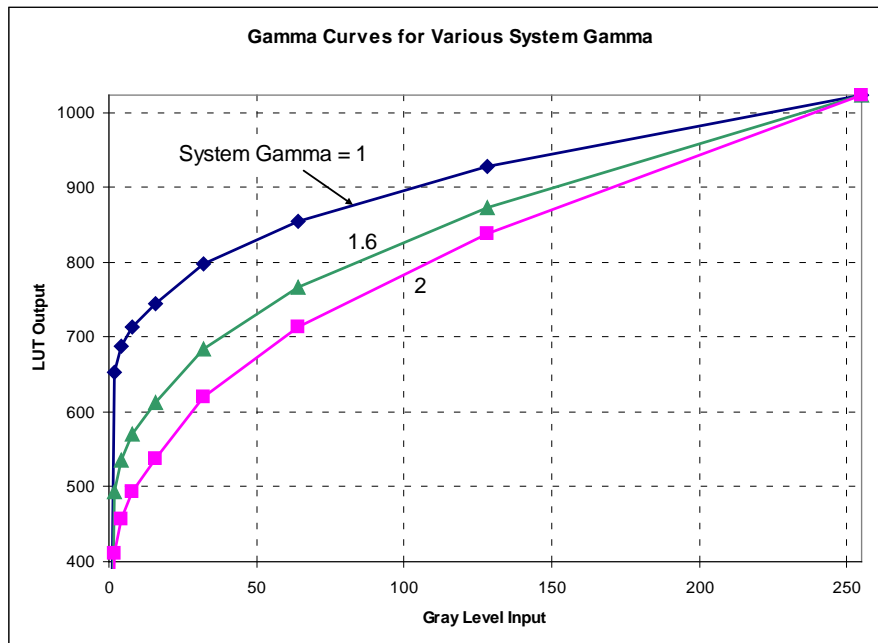


Figure 13: Gamma curves for arbitrary System Gamma

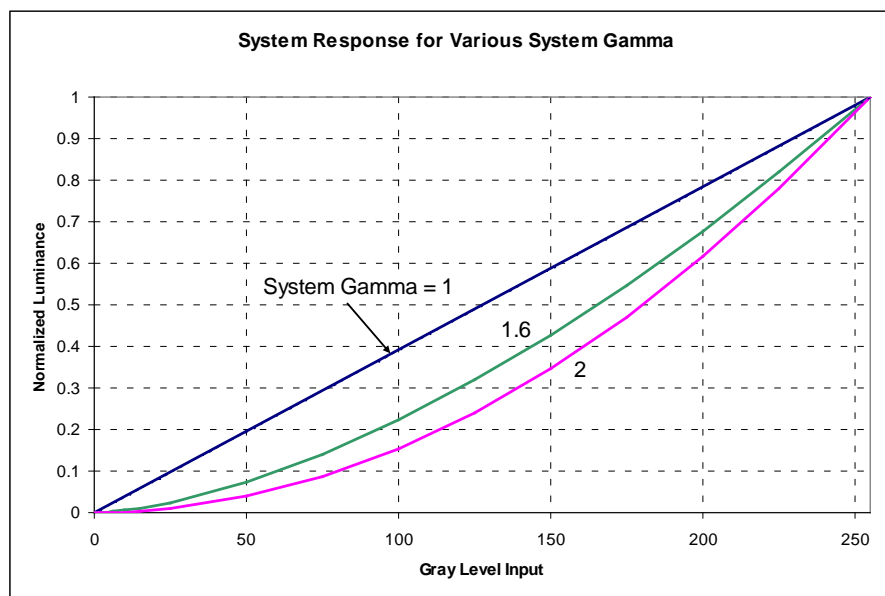


Figure 17 Display system response for arbitrary system gamma

8.5 DC-DC Converter

An on-chip dc to dc converter controller allows for the generation of the OLED cathode supply, relying on a few external passive components assembled on the display carrier board. The converter is an adjustable inverter that converts VDD5 to a negative supply used to bias the OLED via the VCOM input pin. Adjustment is managed by the control logic and registers VCOM [7,0] and VCOMMODE[1,0].

The converter adjustment comes from two sources:

- A nominal value set in a dedicated register that provides for the room temperature voltage level.
- The output of an internal VCOM sensor circuit. This feature can be enabled/disabled via register setting to allow full external control (via register VCOM).

A soft-start function is provided that allows the converter output to ramp up in a controlled fashion by sensing the switch current and limiting its peak value.

A block level schematic of the Cuk converter that is employed in the DSVGA application is shown in Figure 18.

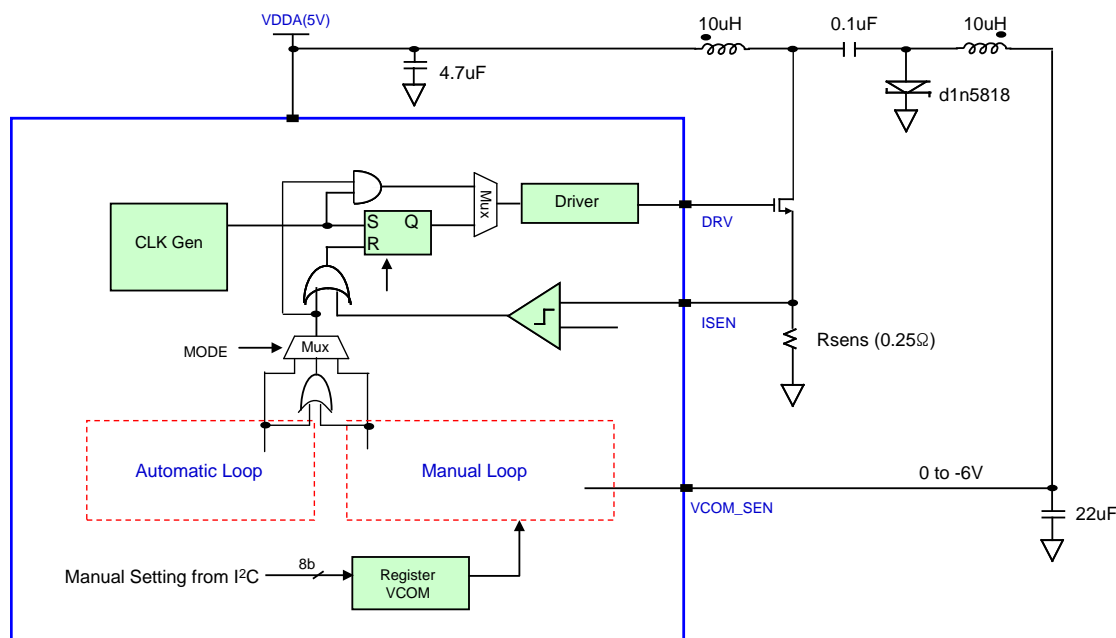


Figure 18: Schematic of DC-DC controller function

Three modes of operation, selected via register VCOMMmode, are provided for the controller function. Mode 1, selected by default (VCOMMmode=0), activates the Automatic Loop which provides VCOM regulation based on an internal current feedback sensor. In this mode the cathode supply is automatically regulated in order to maintain a constant maximum OLED array current over changes in temperature and luminance. The cathode voltage will tend to rise in absolute value as the luminance level is increased or the operating temperature is reduced.

Mode 2, selected by setting VCOMMODE=1h, is a hybrid control mode that prevents the absolute value of the cathode supply from becoming too small at higher temperatures, but allows it to increase at low temperatures where it is needed to ensure a stable regulated OLED current. Both the AUTO and MANUAL control loops are running simultaneously in this mode with one taking charge above a user defined threshold (set by register VCOM) and the other below that threshold. For relatively low temperatures and high luminance levels the AUTO mode will be in control and the cathode supply will follow the trajectory shown in Figure 19. If operating conditions try to force the absolute value of the cathode supply to drop below the threshold, then the control switches to MANUAL mode and the regulated supply remains fixed at the VCOM level.

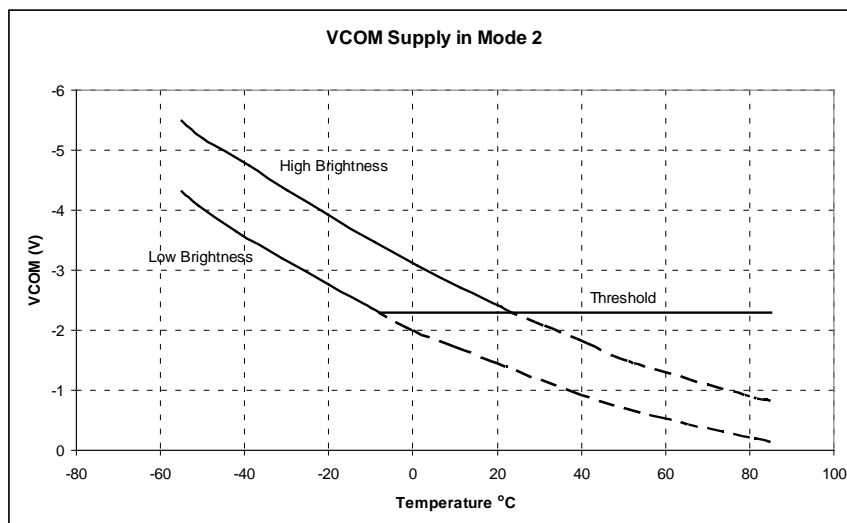


Figure 14: VCOM supply characteristic in Mode 2

Mode 3, selected by setting VCOMMODE=2h, activates the Manual Loop which provides a fixed cathode supply based on a cathode voltage feedback signal. The actual value of the cathode voltage is controlled over a range of 0 to -6V by setting register VCOM. Its default value is about -2.3V. In this mode the dimming and luminance regulation functions via IDRF and DIMCTL are not operational. Luminance is controlled directly via the VCOM register setting in this mode instead.

8.6 I²C Serial Interface

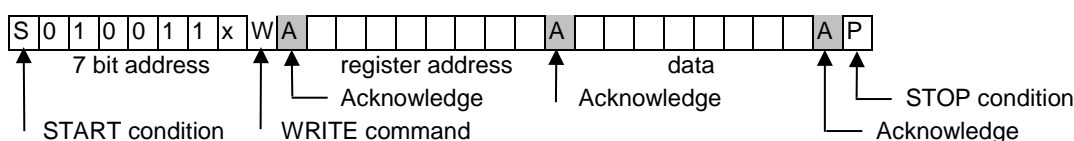
The serial interface consists of a serial controller and registers. The serial controller follows the I²C protocol. An internal address decoder transfers the content of the data into appropriate registers. The protocol will follow the address byte followed by register address data byte and register data byte sequence (3 bytes for each register access):

Serial address with write command
Register address
Register data

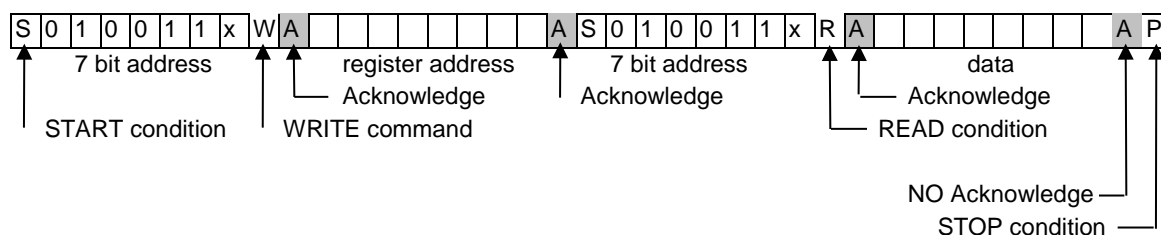
The registers are designed to be read/write. Read mode is accomplished via a 4 byte sequence:

Serial address with write command
Register address
Serial address with read command
Register data

RANDOM REGISTER WRITE PROCEDURE



RANDOM REGISTER READ PROCEDURE



The serial controller is capable of slave mode only.

The x in the 7-bit address code is set by the SERADD input pin and is provided to allow a dual display and single controller configuration.

Slave Address: 010011X where X = 0 or 1 depending on the status of the SERADD pin. This is summarized in Table 9-3.

Write Mode: Address is 4Ch (or 4Eh if SERADD = 1)

Read Mode: Address is 4Dh (or 4Fh if SERADD = 1)

Sequential Read/Write Operation:

The serial controller allows for both sequential and read operational modes. For either mode, the host needs only set the initial register address followed by as many data bytes as needed, taking care not to issue a STOP condition until all desired data bytes have been transmitted (or received).

Maximum interface frequency: 400 KHz.

Table 8-3 : I²C Address Summary

	SERADD	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Read	0	0	1	0	0	1	1	0	1
Write	0	0	1	0	0	1	1	0	0
Read	1	0	1	0	0	1	1	1	1
Write	1	0	1	0	0	1	1	1	0

NOTE: The SDA line is internally tied to +5V via resistor R8, a 10K-Ohm pull-up. This resistor can be removed if the serial interface needs to operate below +5V. SDA then becomes an open collector pin that be driven with a +3.3V power rail. The user must take care, if R8 is removed, that the maximum length of the circuit driving the SDA pin cannot exceed 250 mm without a risk of signal degradation.

8.7 Power-On Sequence

To ensure proper startup and stabilization of the display the following power-on sequence is recommended:

1. Turn on VDD1.8, VDD5, and VPG supplies (these can be simultaneous)
2. A ramp-up time of 1 to 40ms for VDD5 and VDD1.8 is recommended for best performance
3. VDD1.8 should stabilize at least 1ms ahead of VDD5

4. The ramp-up time for VPG is not critical and it can be turned on anytime
5. Configure the display registers to the desired startup state
6. Turn on the display by setting the DISPOFF bit in register DISPMODE to “0”

Figure 20 shows the timing diagram for the power supplies and control signals during startup when the display is first turned on. The external supply voltages (VDD5, VDD1.8, and VPG) can all be applied at the same time as in the diagram. An internal reset signal (rstn) is triggered when VDD5 exceeds a built-in threshold level. After a delay of about 40ms the VDD5 supply to the array is enabled (VDD5en). Following an additional 20ms the internal dc-dc controller is activated (VCOMen) which generates a negative supply for the common cathode of the array. The video display is enabled 20ms later (VIDEOen) and video is displayed on the array after the DISPOFF bit has been set to “0” via the serial port. Prior to this moment the pixels in the array are actively driven to the black state. The pin RESETB must also be logic high before any registers can be written.

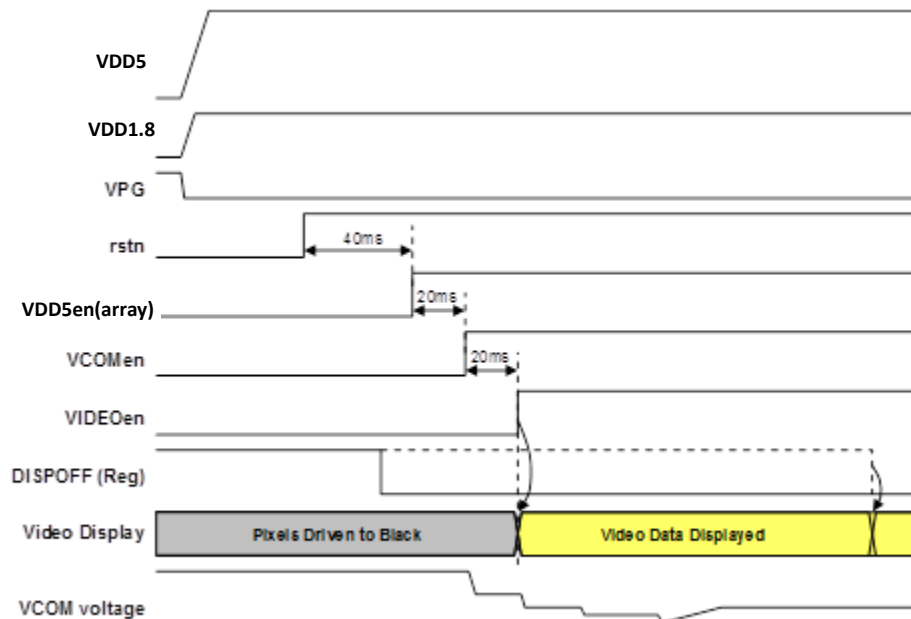


Figure 20: Power-Up sequence for supplies and control.

NOTE: Do not apply VDD5 without a VDD1.8 supply first. This will result in high current and possible device damage!

The supply currents drawn during a typical startup condition are illustrated in Figure 21.

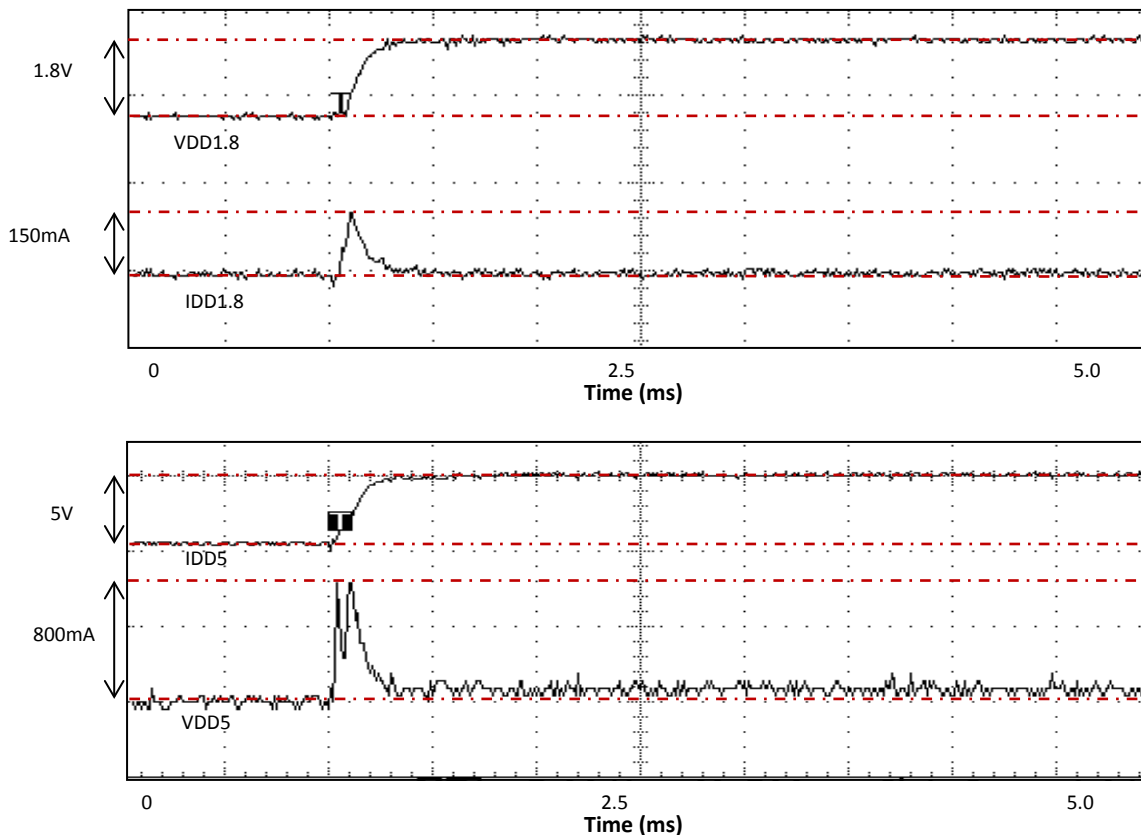


Figure 21: Typical startup currents

8.8 Power-Savings Mode

The display provides power down modes to minimize power consumption. This can occur in two ways:

- Sleep mode – manually controlled via the PDWN bit in register SYSPWRDN, the entire display chip is powered down except for the serial interface. The register settings are saved and restored on power up from this mode.
- Individual block control – several functional blocks have the option to be turned off manually via control of registers ANGPWRDN and SYSPWRDN.

The normal power-down sequence for supplies and control is given in Figure 22, while the power-down/power-on sequence for the sleep mode is shown in Figure 23. The data, sync and clock inputs should be inactive and held low to achieve the minimum sleep-mode power consumption.

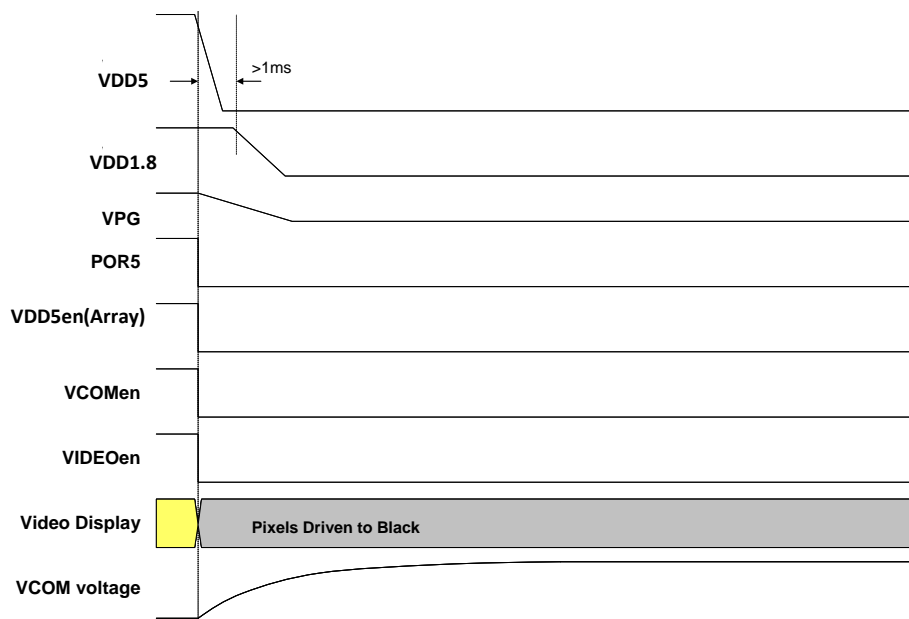


Figure 15: Power-Down sequence for supplies and control.

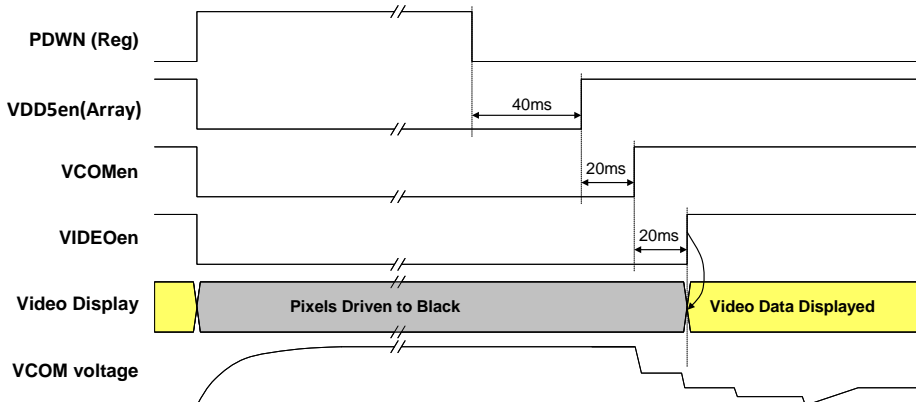


Figure 16: Soft power-down / power-on sequence for supplies and control.

8.8.1 Display-Off Function

On power-up the micro display sets all internal registers to their default values and holds the array in the off state (black) until a software reset is externally applied. The DISPOFF bit in the DISPMODE register must be set to zero via the serial port in order for the array to become active.

9. REGISTER MAP SUMMARY

I2C Address: 010011X

Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description
00	STAT	R	REV	2-0	1	Silicon Revision Number
01	VINMODE	R/W	WRDISABLE	7	0	I ² C Register Write Disable 0 = Write Enable, 1 = Write Protected (Read Only)
			NODATAEN	6	0	No DataEn with video 0=DataEn provided with Video, 1=No DataEn Provided with video
			EXT_SYNC	5	1	Embedded/External Sync select 0=Embedded Sync, 1=Saperate External Sync
			3D-MODE	4	0	3D Display Mode 0 = Normal Display, 1 = Time Sequential Mode
			SCMODE	3-2	0	Progressive or Interlaced scan mode select 00 = Progressive, 1X = Pseudo Interaced
			DATA_MODE	1-0	00	Input Video Type Select 00=24bit RGB, 01=24bit-YCbCr, 10=16bit-YCbCr, 11=8bit-YCbCr(BT656)
02	DISPMODE	R/W	DISPOFF	7	1	Display Off (BURNIN mode override to ON) 0 = Display On, 1 = Display Off
			AUTOSYNC	6	1	Auto VSYNC/HSYNC Polarity detection 0 = Negative Sync, 1 = Positive Sync
			VSYNCPOL	5	1	VSYNC Polarity 0 = Negative Sync, 1 = Positive Sync
			HSYNCPOL	4	1	HSYNC Polarity 0 = Negative Sync, 1 = Positive Sync
			SET_ENABLE	3	0	ENABLE Active Level 0=Enable low(cannot change)
			NOFIELD	2	0	Generate FIELD from SYNC enable 0 = use ENABLE as Field, 1 = Generate Field from SYNC
			VSCAN	1	0	Vertical Scan Direction 0 = Top to Bottom Scan, 1 = Bottom to Top Scan
			HSCAN	0	0	Horizontal Scan Direction 0 = Left to Right Scan, 1 = Right to Left Scan
03	LFTPOS	R/W		7-0	0C	Column Display Left Position
04	RGTPOS	R/W		7-0	0C	Column Display Right Position
05	TOPPOS	R/W		7-0	0C	Row Display Top Position
06	BOTPOS	R/W		7-0	0C	Row Display Bottom Position
07	BRIGHTNESS	R/W		7-0	80	Add -127 ~ +128 to Video Data (80h = No Change)
08	CONTRAST	R/W		7-0	80	Multiply 0 ~ 1.99 to Video Data (80h = No Change)
09	ROWRESET	R/W		7-0	0	Row Duty Control
9-8				0:Disable, Each line displayed ROWRESET*2 Line period		
0A				12		0

			Reserved	5	0	Do Not Change
0B	RAMPCTL	R/W	RAMP9B	4	0	Set Internal Ramp DAC resolution 0 = 10Bit Ramp, 1 = 9Bit Ramp
			RAMPHIGH	3	0	Internal Ramp DAC set All High 0 = Normal operation, 1 = DAC set All High
			FLYBTIME	2	0	Ramp Fly back Time 0 = 800 nSec, 1 = 500 nSec
			RAMPDLY	1-0	1	Ramp Delay by DCLK 00 = -1/2 DCLK, 01 = No Delay, 10 = +1/2 DCLK
0C	RAMPCM	R/W	RAMPBCM	6-4	3	Ramp Buffer Current Control (000=-75%(Don't use), 001=-75%, 010=-50%, 011=-25%, 100 = ±0%, 101 = +25%, 110 = +50%, 111 = +75%)
			RAMPMON	3	0	Internal Ramp Buffer Monitor Enable
			RAMPACM	2-0	2	Ramp Amp Current Control (000 = -75%(Don't use), 001 = -75%, 010 = -50%, 011 = -25%, 100 = ±0%, 101 = +25%, 110 = +50%, 111 = +75%)
0D	VDACMX	R/W		7-0	80	Ramp DAC Max Value Control, -40% ~ +40 %
0E	BIASN	R/W	EXT_VREF	3	0	External VREF Enable
			BIASN	2-0	1	000 = bias current off 001~101 = bias current set to 0.5nA, 1nA, 1.5nA, 2nA, 2.5nA 110~111 = Do Not Use (same as 2.5nA)
0F	GAMMASET	R/W	PMPHOLD_EN	4	0	VCOM PUMP hold enable when VGN sampling time 0 = Normal pumping, 1 = Pump hold function enable
			VGNSH_EN	3	0	VGN Sample & Hold Enable 0 = VGN SH Bypass, 1 = Enable VGN SH output
			IDSTEP	2-0	0	Current level for gamma sensor
10	VCOMMODE	R/W	ISEN_EN	3-2	0	VCOM I-Sensor Enable
			VCOMAUTO	1-0	0	00 = AUTO1 mode 01 = AUTO2 mode 10 = MANUAL mode
11	VCOMCTL	R/W	SS_BYPASS	7	0	VCOM Soft Start Bypass mode 0 = Soft Start function enable, 1 = Soft Start Bypass
			VCKDUTY	6-4	3	VCOM Clock Duty Control (High:Low) 0=1:7, 1=1:3, 2=3:5, 3=1:1, 4=5:3, 5=3:1, 6=7:1, 7=Don't use
			VCKSEL	3-2	3	VCOM Clock Select 0=125KHz, 1=250KHz, 2=500KHz, 3=800KHz
			VCOMSS	1-0	1	VCOM Soft Start Delay Time Mode 0 = 2mS, 1 = 4mS, 2 = 8mS, 3 = 16mS
12	VGMAX	R/W		7-0	0D	Fine adjustment for VGMAX level (default = 4.95V)
13	MVCOM	R/W		7-0	51	VCOM manual setting (used when VCOMMODE = 01 or 10 , default = -2.3V)
14	IDRF	R/W	IDRF_COARSE	7-5	0	Coarse adjustment for array reference current
			IDRF_FINE	4-0	0	Fine adjustment for array reference current
15	DIMCTL	R/W		6-0	01	Dimming level control (default = 1X IDRF)
16	TREFDIV	R/W		5-0	13	Temp. Sensor Reference Clock Divider
17	TEMPOFF	R/W		7-0	35	Temp. Sensor Offset

18	TUPDATE	R/W		7-0	FF	Number of frames per TEMPOUT update (Data range 02H ~ FFH) Update Time = (TUPDATE+1) * PERIOD _{FRAME} PERIOD _{FRAME} = 16.6 mSec when using 60Hz Video
19	TEMPOUT	RO		7-0	-	Temperature Sensor Readout
1A	ANGPWRDN	R/W	ISENPD	7	0	ISEN Power Down
			IDMAXPD	6	0	IDMAX Power Down
			VCOMPDP	5	0	VCOM Power Down
			VREFPD	4	0	VREF Power Down
			GMSENPD	3	0	Gamma Sensor Power Down
			VCSENPD	2	0	VCOM Sensor Power Down
			TSENPD	1	0	Temperature Sensor Power Down
1B	SYSPWRDN	R/W	TREFPD	0	0	Temperature Reference Power Down
			PDWN	5	0	All System Power Down (Override all analog power down, except POR50VPD, POR25VPD)
			RAMPBPD	4	0	RAMP BUF Power Down
			RAMPAPD	3	0	RAMP AMP Power Down
			RAMPDPD	2	0	RAMP DAC Power Down
			POR50VPD	1	0	5V POR Power Down
1C	TPMODE	R/W	POR25VPD	0	0	2.5V POR Power Down
			PATTEN	3	0	Test Pattern Display Enable when "1"
			PATTSEL	2-0	0	Select test pattern for Built-In-Test-Mode (BURNIN pin = 'High' or PATTEN = 1) 000= Burn-in (all white), 001=Color Bar, 010=16 level gray scale
						011=Checker Board, 100=Vertical Line, 101=Horizontal Line, 110=Grid Pattern
1D	TPLINWTH	R/W		7-0	0	Line Test Pattern Line Width (0=1pixel, 1=2pixel, ..., 255=256pixel)
1E	TPCOLSP	R/W		7-0	0	Line Test Pattern Column Space (0=1pixel, 1=2pixel, ..., 255=256pixel)
1F	TPROWSP	R/W		7-0	0	Line Test Pattern Row Spce (0=1pixel, 1=2pixel, ..., 255=256pixel)
20	TPCOLOR	R/W	TPBGCLR	6-4	0	Line Test Pattern Background Color (RGB)
			TPFGCLR	2-0	7	Line Test Pattern Forground Color (RGB)
21	LUT_ADDR	R/W		7-0	0	Gamma Look-Up Table template access Address
22	LUT_DATA	R/W	LUT_DATA_L	7-0	0	Gamma Look-Up Table template R/W Data LSB (Auto LUT_ADDR increase)
23			LUT_DATA_H	9-8	0	Gamma Look-Up Table template R/W Data MSB
24	LUT_UPDATE	R/W	GAMMAEN	4	0	Use Internal Gamma LUT (0: Bypass internal Gamma LUT, 1: Use internal Gamma LUT)
			UDGAMMA	3	0	Update LUT template ro R,G,B Gamma LUT enable (Auto cleared after update)
			UDRGB	2-0	7	Select R,G,B Gamma to update (ex. 100=R Gamma Update)
25	PUPCTL	R/W	PUPCTLEN	3	0	Power up sequence override enable (0=Normal Power Up sequence, 1= Power up seq. override enable)
			VIDEN	2	0	Power up sequence VIDEO enable override (0=Video display OFF, 1=Video display ON)
			VCOMEN	1	0	Power up sequence VCOM enable override (0=VCOM OFF, 1=VCOM ON)

			VANEN	0	0	Power up sequence VAN (5V Pixel Power) enable override (0=VAN OFF, 1=VAN ON)
26	V_BLANK	R/W		7-0	0	Set the number of Vertical blank lines when NOXTFE=1 and EXT_SYNC=1
27	H_BLANK	R/W		7-0	0	Set the number of Horizontal blank pixels when NOXTDE=1 and EXT_SYNC=1
28	V_OFFSET	R/W		1:0	0	Adjust V_BLANK number on Odd Field when Interlaced mode with NOXTDE=1 and EXT_SYNC=1 00= Odd field video start at same line as Even line, 01= Odd field start at 1 line fast 10= Do not use, 11=Odd field start at 1 line late
29	H_DLY	R/W		1:0	1	Adjust horizontal shync (-1, 0, +1, +2)
2A	MISCTL	R/W		1-0	0	Misc. Control (RBP_SWAP, RBCSWAP)
2B	CSCC0	R/W		7-0	10	Constant0 for YCbCr to RGB color space conversion
2C	CSCC1	R/W		7-0	2A	Constant1 for YCbCr to RGB color space conversion
2D				9-8	1	
2E	CSCC2	R/W		7-0	98	Constant2 for YCbCr to RGB color space conversion
2F				9-8	1	
30	CSCC3	R/W		7-0	D0	Constant3 for YCbCr to RGB color space conversion
31				9-8	0	
32	CSCC4	R/W		7-0	64	Constant4 for YCbCr to RGB color space conversion
33				9-8	0	
34	CSCC5	R/W		7-0	04	Constant5 for YCbCr to RGB color space conversion
35				9-8	2	
36	Reserved	R/W		2-0	0	Do not change
37	DIGTEST	R/W		7-0	0	Digital test mode and control register
38	NOFLINE	R		7-0	-	Number of active video lines read out
39				10-8	-	
3A	NOFPXL	R		7-0	-	Number of active video pixels readout
3B				10-8	-	
3c	Reserved	R/W		7-0	99	Do not change
3d	Reserved	R/W		7-0	99	Do not change
3e	Reserved	R/W		7-0	00	Do not change
3f	Reserved	R/W		7-0	FF	Do not change
40	Reserved	R/W		6-0	0	Do not change
41	Reserved	R/W		7-0	30	Do not change
42	Reserved	R/W		6-0	64	Do not change

10. DETAILED REGISTER DESCRIPTIONS

10.1 STAT (00h)

Name	STAT
Address	00h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
CID	3	-	Indicates monochrome or color display
REV	2-0	1	Silicon revision number; Rev. 1 = 1

Bits REV in this register indicate the revision number of the silicon backplane design, with 0 corresponding to the first silicon known as Rev. 1.

Bit CID indicates the version of silicon backplane with “0” for a monochrome display and “1” for the color version.

10.2 VINMODE (01h)

Name	VINMODE
Address	01h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
WRDISABLE	7	0	I ² C register write disable
NODATAEN	6	0	0 if DE is provided with video data
EXT_SYNC	5	1	Embedded/External Sync Select
3D-MODE	4	0	3D Display Mode Select
SCMODE	3-2	0	Progressive and Interlaced Scan Mode Select
DATAMODE	1-0	0	Input Video Type Select

WRDISABLE:

- 0 = write enable (all registers can be updated externally via I²C) (default)
- 1 = write protected (all other registers become read only)

NODATAEN

- 0 = DE is provided with video (default)
- 1 = DE is generated from V_BLANK, H_BLANK registers

EXT_SYNC

- 0 = SYNC are embedded in Green video data

1 = SYNC (VSYNC, HSYNC, DE) are provided externally through separate PADs (default)

3D-MODE:

- 0 = Normal display mode (default)
- 1 = Time Sequential 3D mode

This bit is used to set the 3D mode of operation in conjunction with SET_ENABLE (bit #3 of the VINMODE register) and the Enable input. In Frame Sequential Mode each video frame contains information for either the left or right eye. When 3D-MODE="1" the SCMODE bit in the DISPMODE register is overridden to Progressive Scan Mode (0h).

In the EMA101120-01 product, the 3D-MODE is not supported since the ENABLE input is tied to GND in the carrier board.

SCMODE:

- 00 = Progressive scan mode (default)
- 01 = Interlaced scan mode
- 1x = Pseudo Interlaced Mode

Interlaced modes are limited to a maximum of 512 and a minimum of 240 active rows per field. For the interlaced or pseudo-interlaced mode, the NOFIELD register should be set to high to get the field information from VSYNC.

DATA_MODE

- 00 = 24bit RGB (default)
- 01 = 24bit YCbCr
- 10 = 16bit YCbCr
- 11 = 8bit YCbCr (BT656)

Input video data is used directly for display in 24bit RGB mode. RGB color space conversion needed for all YCbCr video and additional data conversion needed for 16/8 bit YCbCr video mode.

10.3 DISPMODE (02h)

Name	DISPMODE
Address	02h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
DISPOFF	7	1	Display On/Off control
AUTOSYNC	6	1	Automatic sync polarity detection mode
VSYNCPOL	5	1	VSYNC polarity setting
HSYNCPOL	4	1	HSYNC polarity setting
SET_ENABLE	3	0	Active level of ENABLE input pin
NOFIELD	2	0	Generate FIELD from SYNC enable
VSCAN	1	0	Vertical Scan Direction
HSCAN	0	0	Horizontal Scan Direction

DISPOFF:

- 0 = Display is turned ON
- 1 = Display is turned OFF (default)

The display starts in the OFF state by default and requires a command via the serial port to be turned on.

AUTOSYNC

- 0 = Auto Sync detection mode OFF
- 1 = Auto Sync detection mode ON (default)

VSYNCPOL and HSYNCPOL are overridden by detected sync when AUTOSYNC=1.

VSYNCPOL:

- 0 = Negative Sync (default)
- 1 = Positive Sync

HSYNCPOL:

- 0 = Negative Sync (default)
- 1 = Positive Sync

The SYNCPOL registers are used to determine whether the positive or negative edge of the external synchronization clocks (HSYNC and VSYNC) is used as the active transition by the internal display sequencers and control logic.

SET_ENABLE:

- 0 = the active state of the ENABLE input is set “low” (default)
- ENABLE pin is set to ground hence SET_ENABLE should be always ‘0’

NOFIELD

- 0 = ENABLE input pin is used as FIELD when interlaced video mode
- 1 = FIELD is generated from Sync when interlaced video mode

In EMA101120-01 part, NOFIELD should be set to high (NOFIELD = 1) for the interlaced or pseudo interlaced mode since ENABLE pin is tied to GND in the carrier board.

FIELD is set to Even field when VSYNC rising edge located between -25% ~ 25% of HSYNC period.
FIELD is set to Odd field when VSYNC rising edge located between 25% ~75% of HSYNC period.

VSCAN:

- 0 = Top to Bottom vertical scan direction (default)
- 1 = Bottom to Top vertical scan direction

HSCAN:

- 0 = Left to Right horizontal scan direction (default)
- 1 = Right to Left horizontal scan direction

10.4 LFTPOS (03h)

Name	LFTPOS
Address	03h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0C	Left position of first active column

This register, along with register RGTPOS, is used to set the horizontal position of the active display window within the 824 available columns of pixels. In DSVGA mode the active window can be moved by +/-12 pixels from the center (default) position. When LFTPOS is increased, register RGTPOS must be decreased by the same value so that the sum of the two remains equal.

10.5 RGTPOS (04h)

Name	RGTPOS
Address	04h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0C	Right position of last active column

This register, along with register LFTPOS, is used to set the horizontal position of the active display window within the 824 available columns of pixels. In DSVGA mode the active window can be moved

by +/-12 pixels from the center (default) position. When RGTPOS is increased, register LFTPOS must be decreased by the same value so that the sum of the two remains equal.

10.6 TOPPOS (05h)

Name	TOPPOS
Address	05h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0C	Top position of first active row

This register, along with register BOTPOS, is used to set the vertical position of the active display window within the 624 available rows of pixels. In DSVGA mode the active window can be moved by +/- 12 pixels from the center (default) position. When TOPPOS is increased, register BOTPOS must be decreased by the same value so that the sum of the two remains equal.

10.7 BOTPOS (06h)

Name	BOTPOS
Address	06h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0C	Bottom position of last active row

This register, along with register TOPPOS, is used to set the vertical position of the active display window within the 624 available rows of pixels. In DSVGA mode the active window can be moved by +/- 12 pixels from the center (default) position. When BOTPOS is increased, register TOPPOS must be decreased by the same value so that the sum of the two remains equal.

10.8 RESERVED (07h)

Name	RESERVED
Address	07h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	80	Reserved – Do not change

10.9 RESERVED (08h)

Name	RESERVED
Address	08h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	80	Reserved – Do not change

10.10 ROWRESET (09h, 0Ah)

Name	ROWRESET
Address	09h, 0Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ROWRESETL (09h)	7-0	0	Row duty rate control (LSB)
ROWRESETH (0Ah)	0	0	Row duty rate control (MSB)
	4	0	ROWRESET work on UNENABLED frame in 3D mode

ROWRESETH:BIT4

0 = Active duty rate can be set 0 ~ 50%, 100% when 3D mode

1 = Active duty rate can be set 50 ~ 100% when 3D mode

This register is used to set the number of line cycles (in steps of 2) during which each row is active in any frame period. Each row is driven to black during the non-active line cycles.

ROWRESET (dec)	Active Line Cycles	Active Duty Rate (%)	Note
0	all	100	Pixels active for entire frame period
1	2	$2 \cdot T_{HSYNC} / T_{FRAME}$	624 total HS cycles / frame
n	$2 \cdot n$	$2 \cdot n \cdot T_{HSYNC} / T_{FRAME}$	
>312	all	100	Pixels active for entire frame period

10.11 RAMPCTL (0Bh)

Name	RAMPCTL
Address	0Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-5	0	Reserved (Do Not Change)
RAMP9B	4	0	Set Internal RAMP DAC resolution
RAMPHIGH	3	0	Set internal RAMP DAC high
FLYBTIME	2	0	RAMP Flyback time
RAMPDLY	1-0	1	RAMP delay in DCLK cycles

RAMP9B:

- 0 = 10 bit RAMP DAC select (default)
- 1 = 9 bit RAMP DAC select

RAMPHIGH:

- 0 = Normal operation (default)
- 1 = DAC set to all high output

The RAMPHIGH register is used to set internal RAMPDAC to all high output mode for test purposes.

FLYBTIME:

- 0 = 500 ns (default)
- 1 = 800 ns

The FLYBTIME register is used to set the fly-back time for the internal RAMP.

RAMPDLY:

- 00 = - ½ DLCK
- 01 = no delay (default)
- 10 = + ½ DCLK

The RAMPDLY2 register is used to adjust the starting position of the internal RAMP.

10.12 RAMPCM (0Ch)

Name	RAMPCM
Address	0Ch
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
RAMPBCM	6-4	3	RAMP Buffer current control
RAMPMON	3	0	Internal RAMP Buffer monitor enable
RAMPACM	2-0	2	RAMP Amp current control

RAMPBCM:

000 = -100% (power down)
 001 = -75%
 010 = -50%
 011 = -25% (default)
 100 = nominal
 101 = +25%
 110 = +50%
 111 = +75%

The RAMPBCM register is used to set the operating bias current for the internal RAMP buffer. The settings reduce or increase the current by a percentage of the nominal (default) value.

RAMPMON:

0 = Disable internal RAMP Buffer monitoring (default)
 1 = Enable internal RAMP Buffer monitoring

The RAMPMON register is used to enable monitoring of the internal RAMP amplifier output signal.

RAMPACM:

000 = -100% (power down)
 001 = -75%
 010 = -50%
 011 = -25% (default)
 100 = nominal
 101 = +25%
 110 = +50%
 111 = +75%

The RAMPACM register is used to set the operating bias current for the internal RAMP amplifier. The settings reduce or increase the current by a percentage of the nominal (default) value.

10.13 VDACMX (0Dh)

Name	VDACMX
Address	0Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	80h	RAMP DAC maximum value control

Register VDACMX is used to adjust the maximum value of the internal RAMP DAC signal by -40% to +40% of the nominal value.

NOTE: The normal operating value for VDACMX should be set to 74h.

The typical dependence of display luminance on VDACMX (dec) is shown in Figure 24. For normal operation VDACMX should be set to about 90 to 95% of the saturation value as shown in the figure.

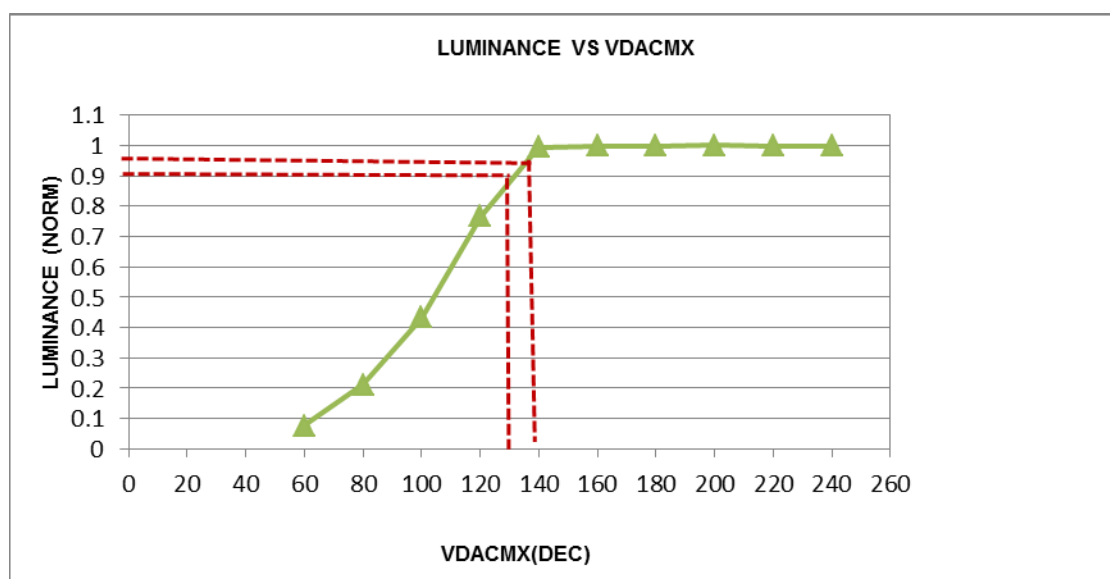


Figure 17: Luminance dependency on VDACMX

10.14 BIASN

Name	BIASN
Address	0Eh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
EXT_VREF	3	0	Enable external VREF

BIASN	2-0	1 (not same as register map)	Set pixel bias current
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EXT_VREF:

- 1 = enable the external VREF source
- 0 = use the internal VREF source (default)

Note: This option not available on the current package – use the default setting only.

BIASN:

- 000 = pixel bias current is turned off
- 111 = pixel bias current set to maximum

The BIASN register is used to set the sink current applied in each pixel cell. It is recommended to use the BIASN=04 setting in normal operation.

10.15 GAMMASET (0Fh)

Name	GAMMASET
Address	0Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
PMPHOLD_EN	4	0	VCOM pump hold enable
VGNSH_EN	3	0	VGN sample & hold enable
IDSTEP	2-0	0	Current level for gamma sensor

PMPHOLD_EN:

- 0 = Normal operation, pump hold disabled (default)
- 1 = Enable pump hold during VGN sampling time

The PMPHOLD_EN register is used to disable the VCOM converter switch during the VGN sampling time to reduce noise pickup.

VGNSH_EN:

- 0 = Bypass the VGN sample & hold function (default)
- 1 = Enable the VGN sample & hold function

The VGNSH_EN register is used to activate the internal sample & hold function provided at the VGN output pin.

IDSTEP:

0h \approx IDRF/128
 1h \approx IDRF/64
 2h \approx IDRF/32
 3h \approx IDRF/16
 4h \approx IDRF/8
 5h \approx IDRF/4
 6h \approx IDRF/2
 7h = IDRF

The IDSTEP register is used to set the current level for the gamma sensor. The corresponding output voltage is provided at pin VGN.

A minimum of 10msec following an IDSTEP register update should be allowed for the VGN signal to settle before sampling. In addition, sampling of the VGN signal should be carried out during the Frame Blanking time.

10.16 VCOMMODE (10h)

Name	VCOMMODE
Address	10h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ISEN_EN	3-2	0	Enable the VCOM current sensor
VCOMAUTO	1-0	0	Set internal VCOM supply mode

ISEN_EN:

00 = disable VCOM current sensor in DC-DC converter
 01 = enable VCOM current sensor in DC-DC converter
 10 = same as 01 setting
 11 = not used

The ISEN_EN register is used to enable the current sensor in DC-DC converter to prevent overcurrent situation of the external FET in the carrier board..**It is always recommended to use ISEN_EN = 01.**

VCOMAUTO:

This register sets the operating mode of the internal VCOM dc-dc converter.

00 = AUTO1 mode (default)
 01 = AUTO2 mode
 10 = MANUAL mode

In the AUTO1 mode, the VCOM converter uses an internal current reference to maintain a fixed OLED current level, which is defined by registers DIMCTL and IDRF.

In the AUTO2 mode, the VCOM converter regulates the OLED current level when the VCOM supply is below a set threshold (defined by the VCOM register), and clamps the output to the threshold level when conditions call for a VCOM output above the threshold level.

In the Auto 3 mode, the VCOM converter uses a voltage reference signal to maintain a fixed cathode supply voltage. The value of the cathode voltage is set by register VCOM.

10.17 VCOMCTL (11h)

Name	VCOMCTL
Address	11h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SS_BYPASS	7	0	Bypass the VCOM soft start mode
VCKDUTY	6-4	3	VCOM clock duty control
VCKSEL	3-2	3	VCOM clock select
VCOMSS	1-0	1	VCOM soft start delay time

SS_BYPASS:

- 0 = Normal operation, soft-start function enabled (default)
- 1 = Disable the VCOM soft-start function

VCKDUTY:

- 0h = 1:7
- 1h = 1:3
- 2h = 3:5
- 3h = 1:1 (default)
- 4h = 5:3
- 5h = 3:1
- 6h = 7:1
- 7h = don't use

Register VCKDUTY sets the VCOM clock duty ratio (high: low).

VCKSEL:

- 0h = 125 kHz
- 1h = 250 kHz
- 2h = 500 kHz
- 3h = 800 kHz (default)

Register VCKSEL sets the operating frequency of the VCOM clock.

VCOMSS:

0h = 2 ms
1h = 4 ms (default)
2h = 8 ms
3h = 16 ms

Register VCMOSS sets the soft-start duration during startup of the VCOM converter.

10.18 VGMAX (12h)

Name	VGMAX
Address	12h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0D	Fine adjustment for VGMAX level

00h = 5 (VDD5 = 5V)
0Dh = 4.95 (default)
FFh = 4

$$\text{VGMAX level} = \text{VDD5} * (1 - 0.2 * \text{VGMAX}(\text{dec}) / 255)$$

This register sets the pixel voltage at which the maximum OLED current is regulated. It should be slightly below the VDD5 supply to prevent saturation of the video buffer amplifiers.

10.19 MVCOM (13h)

Name	VCOM
Address	13h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	51	VCOM manual setting

Cathode supply as a function of VCOM setting:

VCOM(h)	FF	F0	E0	D0	C0	B0	A0	90	80	70	60	51*	40	30
Voltage	-0.29	-0.38	-0.47	-0.59	-0.72	-0.85	-1.0	-1.2	-1.43	-1.7	-2.0	-2.4	-2.97	-3.68

*default value

Register VCOM[7,0] sets the fixed output level for the internal VCOM inverter when VCOMMODE = 01 or 10. There is no compensation for the variation in OLED behavior with temperature in this mode of operation. As a result, a setting at room temperature will not necessarily result in optimal contrast and the same luminance at other temperatures. The default setting (51h) will result in a cathode supply \approx -2.3V.

The typical dependency of luminance on the VCOM setting in manual mode is given in Figure 25 for a color display.

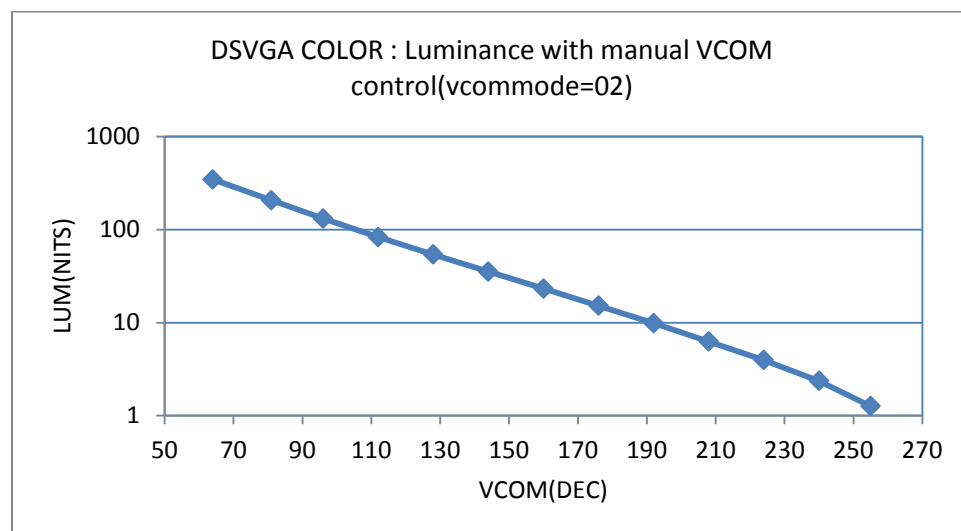


Figure 18: Typical luminance dependency on manual VCOM setting

10.20 IDRF (14h)

Name	IDRF
Address	14h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
IDRF_COARSE	7-5	0	Coarse adjustment for array reference current
IDRF_FINE	4-0	0	Fine adjustment for array reference current

IDRF_COARSE:

IC#
 0h = 0 (default)
 1h = 0.5
 2h = 1.5
 3h = 2.5
 4h = 3.5

IDRF_FINE:

IF#
 00h = 0 (default)
 01h = 1/32
 ...
 10h = 16/32

...
1Fh = 31/32

Register IDRF is used to set the maximum OLED current, which determines the luminance level for the display. The luminance will be directly proportional to the IDRF factor (sum of IC# and IF#) and the reference luminance LDEF given by the following expression:

$$LMAX = LDEF * (IC\# + IF\#) \quad \text{in cd/m}^2$$

where the luminance for a color display is $LDEF \approx 150 \text{cd/m}^2$ at the default settings (see table below).

IDRF (hex)	LMAX / LDEF
0	0
10	0.5
20	0.5
30	1 (default)
40	1.5
50	2
60	2.5
70	3
80	3.5

10.21 DIMCTL (15h)

Name	DIMCTL
Address	15h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	6-0	01	Dimming level control

00h = 0
 01h = 1% of LMAX
 ...
 64h = 100% of LMAX
 ...
 7Fh = 127% of LMAX

This register provides linear control of the display luminance level ranging from 0 to 127% in steps of 1%. The default value of 64h is equal to 100% of the luminance defined by register IDRF.

This register is only operational in Auto VCOM mode (VCOMMODE=00).

10.22 TREFDIV (16h)

Name	TREFDIV
-------------	---------

Address	16h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	5-0	13h	Temperature sensor reference clock divider adjust

The register TREFDIV is used to adjust the slope of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -45 to 70°C, although the setting is best determined by a calibration measurement of the display in its final assembly.

See the description for register TEMPOUT.

10.23 TEMPOFF (17h)

Name	TEMPOFF
Address	17h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	35	Temperature sensor offset adjust

The register TEMPOFF is used to adjust the offset of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of --45 to 70°C, although the setting is best determined by a calibration measurement of the display in its final assembly.

See the description for register TEMPOUT.

10.24 TUPDATE (18h)

Name	TUPDATE
Address	18h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	FF	Number of frames per TEMPOUT update

This register sets the update rate of the Temperature Sensor reading, TEMPOUT. The time between sensor updates is given by:

$$\text{Update Time} = (\text{TUPDATE}(\text{decimal}) + 1) * T_{\text{FRAME}}$$

where the frame period T_{FRAME} is equal to 16.6 ms for 60Hz video. The valid range for TUPDATE is 02h to FFh.

10.25 TEMPOUT (19h)

Name	TEMPOUT
Address	19h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
	7-0	-	Temperature sensor readout

Register TEMPOUT provides an 8bit digital output that is linearly proportional to the chip temperature. The DSVGA display temperature sensor is designed around a P-N junction. The output of the junction is sampled by an internal current to voltage converter, digitized and stored into a dedicated 8-bit register TEMPOUT. The sampling rate is controlled by configuration register TUPDATE (18H). By default the temperature sensor is updated once every 255 frames. Two registers are used to set the sensor gain (TREFDIV) and sensor offset (TEMPOFF). The temperature sensor can be powered down when not used by setting TSENPD =1 in the PWRDN register.

The temperature sensor is intended to provide a full-scale reading over a temperature range defined by the user. Assuming that the desired operating temperature range is defined by T_{MIN} and T_{MAX} , the expected sensor response would be as follows:

$$TEMPOUT(dec) = A * temp + B$$

where temp is the chip temperature in degrees Celsius, and A and B are given by:

$$A = \frac{255}{T_{MAX} - T_{MIN}}$$

$$B = \frac{-255 * T_{MIN}}{T_{MAX} - T_{MIN}}$$

The actual sensor response is determined by registers TREFDIV and TEMPOFF through the following relationship:

$$TEMPOUT(d) = k_1 * TREFDIV(d) * temp + k_2 + TEMPOFF(d)$$

The constants k_1 and k_2 are dependent on properties of the silicon and package assembly. For example, the average register settings needed to achieve a working temperature range of -60°C to +80°C are given by the following values:

$$TREFDIV(d) = 25$$

$$TEMPOFF(d) = 93$$

Using these values will result in a variation in temperature reading from part to part due to manufacturing tolerances. To get a reasonably good sensor performance it is usually enough to just find the optimum

value for TEMPOFF which requires only one measurement at room temperature. Increased accuracy can be obtained for a specific part by performing the calibration measurements described below.

To find the optimum value for TREFDIV do the following:

- Place the display in a temperature controlled environment, e.g. an oven
- Set TREFDIV=25d=19h and TEMPOFF=0
- Set DISPMODE=20h (turn off the display)
- Read TEMPOFF at several ambient temperatures, e.g. 0°C, 20°C, 40°C, 60°C
- Take the slope to find the sensor response, $A_{MEAS} = d\text{TEMPOUT}(d)/d\text{temp}$
- The optimum value for TREFDIV is then given by

$$TREFDIV_{OPT} = 25 * \frac{1.82}{A_{MEAS}}$$

To find the optimum value for TEMPOFF do the following:

- Set TREFDIV=25d=19h (or the optimum value) and TEMPOFF=0
- Set DISPMODE=20h (turn off the display)
- Allow several minutes to stabilize and then read TEMPOUT_{AMB} and the ambient temperature T_{AMB}
- The optimum value for TEMPOFF is then given by

$$TEMPOFF_{OPT} = 1.82 * T_{AMB} + 109 - \text{TEMPOUT}_{AMB}$$

With these settings, the microdisplay temperature can be found from the sensor reading through the following relationship:

$$T(^{\circ}\text{C}) = \frac{140}{255} * \text{TEMPOUT}(d) - 60$$

Temperatures below -60°C will return a TEMPOUT reading of 0 and temperatures above +80°C will return a hexadecimal value of FF.

10.26 ANGPWRDN (1Ah)

Name	ANGPWRDN
Address	1Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ISENPD	7	0	ISEN power down
IDMAXPD	6	0	IDMAX power down
VCOMPDP	5	0	VCOM power down
VREFPD	4	0	VREF power down
GMSENPD	3	0	Gamma sensor power down
VCSENPD	2	0	VCOM sensor power down
TSENDP	1	0	Temperature sensor power down
TREFPD	0	0	Temperature reference power down

ISENPD:

- 1 = VCOM current limit sensor is powered down
- 0 = normal operation (default)

IDMAXPD:

- 1 = IDMAX function is powered down
- 0 = normal operation (default)

VCOMPDP:

- 1 = VCOM generator is powered down
- 0 = normal operation (default)

VREFPD:

- 1 = the VREF reference source is powered down
- 0 = normal operation (default)

GMSENPD:

- 1 = the Gamma sensor is powered down
- 0 = normal operation (default)

VCSNEPD:

- 1 = the VCOM sensor is powered down
- 0 = normal operation (default)

TSENDP:

- 1 = the Temperature Sensor is powered down

0 = the Temperature Sensor is operating normally (default)

TREFPD:

1 = the Temperature reference is powered down

0 = normal operation (default)

10.27 SYSPWRDN (1Bh)

Name	SYSPWRDN
Address	1Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
PDWN	5	0	All systems power down
RAMPBPD	4	0	RAMP buffer power down
RAMPAPD	3	0	RAMP DAC amp power down
RAMPDPD	2	0	RAMP DAC power down
POR50VPD	1	0	5V power-on-reset power down
POR25VPD	0	0	2.5V power-on-reset power down

PDWN:

1 = all systems are powered down

0 = normal operation (default)

By setting the PDWN bit to a “1” the chip enters a deep sleep mode in which all functions including the I²C interface are powered down in order to minimize power consumption. The data, sync and clock inputs should be inactive and held low to achieve the lowest power consumption. An on-chip Address Detection circuit monitors the I²C input lines and resets the PDWN bit when it detects the correct I²C address, restoring the display to operating mode.

All register settings are saved in the power down mode and the display will restart in its previous state when normal operation is resumed.

RAMPBPD:

1 = internal RAMP buffer is powered down

0 = normal operation (default)

RAMPAPD:

1 = internal RAMP DAC amplifier is powered down

0 = normal operation (default)

RAMPDPD:

1 = internal RAMP DAC is powered down (use when external RAMP option is enabled)

0 = internal RAMP DAC is operational (default)

The internal RAMP DAC generator may be power down if an external RAMP source is used.

POR50VPD:

1 = the 5V power-on-reset circuit is powered down

0 = normal operation (default)

POR25VPD:

1 = the 1.8V power-on-reset circuit is powered down

0 = normal operation (default)

10.28 TPMODE (1Ch)

Name	TPMODE
Address	1Ch
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
Reserved	4	0	Do not change
PATTEN	3	0	Test pattern generation enable
PATTSEL	2-0	0	Select test pattern for Burn-In mode

The BI pin or PATTEN must be tied high to activate the Burn-In test mode which can be used to check display functionality without the presence of external video data or clock signals. In this mode the display generates data, syncs and the pixel clock internally for several different video patterns. The TPMODE register is used to select one of the built-in test patterns in Burn-In mode via the serial interface.

000 = all white pattern (default)

001 = color bars

010 = gray scale (without gamma correction)

011 = checkerboard pattern

100 = alternating columns pattern

101 = alternating rows pattern

110 = grid pattern

101 = all black

Use with registers TPLINWTH, TPCOLSP, TPROWSP and TPCOLOR to modify the patterns according to Figure 26.

Test Pattern Name	PATTSEL (1CH:2-0)	TPLINWTH (1DH)	TPCOLSP (1EH)	TPROWSP (1FH)	TPFGCLR (20H:2-0)	TPBGCLR (20H:6-4)
All White	000	X	X	X	X	X
Color Bar	001	X	X	X	X	X
Gray Scale	010	X	X	X	X	X
Checker Board	011	X	X	X	X	X
Alternating Column	100	LW	CS	X	111	000
Alternating Row	101	LW	X	RS	111	000
Grid Pattern	110	LW	CS	RS	111	000
All Black	101	X	X	X	000	000
All White	101	X	X	X	111	111
All Red	101	X	X	X	100	100
All Green	101	X	X	X	010	010
All Blue	101	X	X	X	001	001

Figure 19: Test Patterns

X: Don't care, LW: Line Width (0~255), CS: Column Space (0~255), RS: Row Space (0~255)

10.29 TPLINWTH (1Dh)

Name	TPLINWTH
Address	1Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Test pattern line width

This register is used to set the line width for the line-type test patterns.

0 = 1 pixel wide (default)

1 = 2 pixel wide

...

255 = 256 pixel wide

10.30 TPCOLSP (1Eh)

Name	TPCOLSP
Address	1Eh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Test pattern column spacing

This register is used to set the column spacing for the column-type test patterns.

0 = 1 pixel space (default)
 1 = 2 pixel space
 ...
 255 = 256 pixel space

10.31 TPROWSP (1Fh)

Name	TPROWSP
Address	1Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Test pattern row spacing

This register is used to set the row spacing for the row-type test patterns.

0 = 1 pixel space (default)
 1 = 2 pixel space
 ...
 255 = 256 pixel space

10.32 TPCOLOR (20h)

Name	TPCOLOR
Address	20h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
TPBGCLR	6-4	0	Test pattern background color
TPFGCLR	2-0	7	Test pattern foreground color

This register is used to set the background and foreground colors (RGB) for certain test patterns.

10.33 LUT_ADDT (21h)

Name	LUT_ADDR
Address	21h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Gamma Look-up table template access address

This register is pointing Read/Write address of Gamma LUT template memory. Read LUT_DATA after write LUT_ADDR can read Gamma LUT data at pointing LUT_ADDR address.

10.34 LUT_DATA (22h, 23h)

Name	LUT_DATA
Address	22h, 23h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT_DATAH (22h)	7-0	0	Gamma LUT template R/W data LSB
LUT_DATAH (23h)	9-8	0	Gamma LUT template R/W data MSB

Read those registers can get last written LUT_ADDR address data. When write LUT template register, first write LUT_DATAH than write LUT_DATAH. 10bit LUT data is written right after write LUT_DATAH register.

10.35 LUT_UPDATE (24h)

Name	LUT_UPDATE
Address	24h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
GAMMAEN	4	0	Internal Gamma LUT is used when set
UDGAMMA	3	0	Copy Gamma LUT template to R,G,B Gamma LUT
UDRGB	2-0	7	Select R,G,B Gamma to updated

GAMMAEN:

- 0 = Bypass Gamma Look-Up Table (default)
- 1 = Use internal Gamma Look-Up Table

UDGAMMA:

- 0 = Gamma LUT update is finished and use current RGB Gamma LUT (default)
- 1 = Waiting for Gamma LUT update until VSYNC rising edge

Writing UDGAMMA to “1” then wait until VSYNC rising. After VSYNC rising detected Gamma LUT template register copy to RGB Gamma LUT and UDGAMMA cleared to “0” automatically after finishing update.

UDRGB:

- 000 = No LUT is updated
- 001 = Blue Gamma LUT will be updated
- 010 = Green Gamma LUT will be updated
- 100 = Red Gamma LUT will be updated
- 111 = All RGB Gamma LUT will be updated (default)

UDRGB register select which Gamma LUT will be updated when UDGAMMA set to “1”.

10.36 PUCTRL (25h)

Name	PUCTRL
Address	25h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
PUCTLEN	3	0	Auto Power-up sequence override enable
VIDEN	2	0	Video display enable
VCMEN	1	0	VCOM enable
VANEN	0	0	VDD5 enable

These registers can be used to create a customized power-up sequence.

10.37 V_BLANK (26h)

Name	V_BLANK
Address	26h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	15	Set the number of Vertical Blank line

This register is used for generate DE when NODATAEN=1 and EXT_SYNC=1. This register set then number of vertical blank lines from VSYNC start.

10.38 H_BLANK (27h)

Name	H_BLANK
Address	27h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	C0	Set the number of Horizontal Blank pixel

This register is used for generate DE when NODATAEN=1 and EXT_SYNC=1. This register set then number of horizontal blank pixels from HSYNC start.

10.39 V_OFFSET (28h)

Name	V_OFFSET
Address	28h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	1-0	0	Adjust V_BLANK number on Odd Field

V_OFFSET:

- 00 = No changes on V_BLANK (default)
- 01 = Odd Field start one line fast (subtract one from V_BLANK)
- 10 = Do not use
- 11 = Odd Field start one line later (add one from V_BLANK)

This register is used for generate DE when NODATAEN=1 and EXT_SYNC=1 and SCMODE=01 or 1X.

10.40 H_DLY (29h)

Name	H_DLY
Address	29h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	1-0	1	Adjust horizontal sync in 8bit YCbCr Video

H_DLY:

- 00 = HSYNC move 1 pixel back
- 01 = No adjust (default)
- 10 = HSYNC move 1 pixel forward
- 11 = HSYNC move 2 pixel forward

This register is used when video format convert from YCbCr 422 to 444.

10.41 Reserved (2Ah)

Name	Reserved
Address	2Ah
Mode	Read / Write

This register is used for test purposes only and should not be modified by the user.

10.42 CSCC0 (2Bh)

Name	CSCC0
Address	2Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	10	Constant0 for YCbCr to RGB color space conversion

10.43 CSCC1 (2Ch, 2Dh)

Name	CSCC1
Address	2Ch, 2Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	9-0	12A	Constant1 for YCbCr to RGB color space conversion

10.44 CSCC2 (2Eh, 2Fh)

Name	CSCC2
Address	2Eh, 2Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	9-0	198	Constant2 for YCbCr to RGB color space conversion

10.45 CSCC3 (30h, 31h)

Name	CSCC3
Address	30h, 31h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	9-0	0D0	Constant3 for YCbCr to RGB color space conversion

10.46 CSCC4 (32h, 33h)

Name	CSCC4
Address	32h, 33h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	9-0	064	Constant4 for YCbCr to RGB color space conversion

10.47 CSCC5 (34h, 35h)

Name	CSCC5
Address	34h, 35h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	9-0	204	Constant5 for YCbCr to RGB color space conversion

10.48 Reserved (36h)

Name	Reserved
Address	36h
Mode	Read / Write

This register is used for test purposes only and should not be modified by the user.

10.49 DIGTEST (37h)

Name	DIGTEST
Address	37h
Mode	Read / Write

This register is used test purposes only and should not be modified by the user.

10.50 NOFLINE (38h, 39h)

Name	NOFLINE
Address	38h, 39h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
	10-0	-	Number of active video lines read out

10.51 NOFPXL (3Ah, 3Bh)

Name	NOFPXL
Address	3Ah, 3Bh
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
	10-0	-	Number of active video pixels read out

10.52 Reserved (3Ch~42h)

Name	Reserved
Address	3Ch~42h
Mode	Read / Write

These registers are used test purposes only and should not be modified by the user.

11. APPENDIX A: APPLICATION SYSTEM DIAGRAM

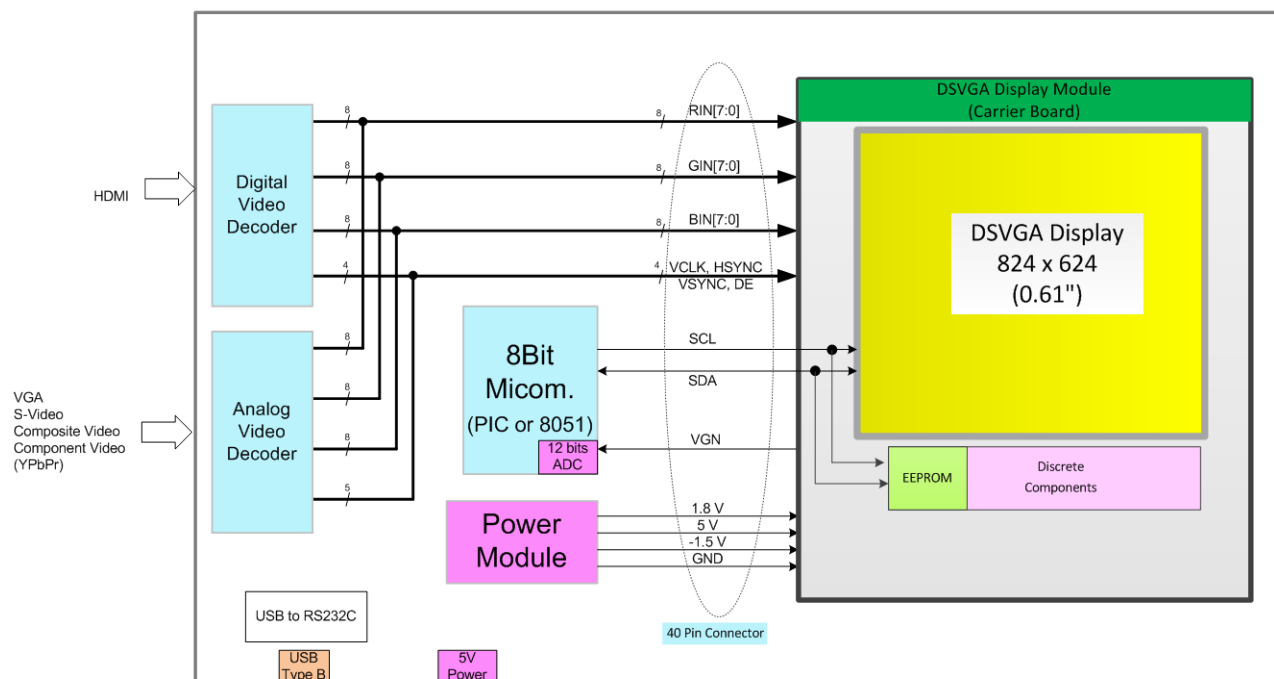


Figure 27: Block diagram of application reference system

Pin Name	Input Format				
	RGB 8 bits	4:4:4 YCbCr	4:2:2 YCbCr	BT656 (4:2:2 YCbCr)	MONO
R0	R[0]	Cr[0]	CbCr[0]	n.c	n.c
R1	R[1]	Cr[1]	CbCr[1]	n.c	n.c
R2	R[2]	Cr[2]	CbCr[2]	n.c	n.c
R3	R[3]	Cr[3]	CbCr[3]	n.c	n.c
R4	R[4]	Cr[4]	CbCr[4]	n.c	n.c
R5	R[5]	Cr[5]	CbCr[5]	n.c	n.c
R6	R[6]	Cr[6]	CbCr[6]	n.c	n.c
R7	R[7]	Cr[7]	CbCr[7]	n.c	n.c
G0	G[0]	Y[0]	Y[0]	YCbCr[0]	Y[0]
G1	G[1]	Y[1]	Y[1]	YCbCr[1]	Y[1]
G2	G[2]	Y[2]	Y[2]	YCbCr[2]	Y[2]
G3	G[3]	Y[3]	Y[3]	YCbCr[3]	Y[3]
G4	G[4]	Y[4]	Y[4]	YCbCr[4]	Y[4]
G5	G[5]	Y[5]	Y[5]	YCbCr[5]	Y[5]
G6	G[6]	Y[6]	Y[6]	YCbCr[6]	Y[6]
G7	G[7]	Y[7]	Y[7]	YCbCr[7]	Y[7]
B0	B[0]	Cb[0]	n.c	n.c	n.c
B1	B[1]	Cb[1]	n.c	n.c	n.c
B2	B[2]	Cb[2]	n.c	n.c	n.c
B3	B[3]	Cb[3]	n.c	n.c	n.c
B4	B[4]	Cb[4]	n.c	n.c	n.c
B5	B[5]	Cb[5]	n.c	n.c	n.c
B6	B[6]	Cb[6]	n.c	n.c	n.c
B7	B[7]	Cb[7]	n.c	n.c	n.c

Related Documents

Document Type	Document ID
Schematic:	D01-501043-03
PCB Fab:	C01-501044-02
PCB Assembly:	A01-501045-03

DSVGA Die Pinout Table

Pin	Signal	Pin	Signal
1	VSS DIG	27	PWCLK
2	VSS DIG	28	VSYN
3	VSS DIG	29	VSIN
4	VSS DIG	30	VSIN
5	VSS DIG	31	VSIN
6	VSS DIG	32	VSIN
7	VSS DIG	33	VSIN
8	VSS DIG	34	VSIN
9	VSS DIG	35	VSIN
10	VSS DIG	36	VSIN
11	VSS DIG	37	VSIN
12	VSS DIG	38	VSIN
13	VSS DIG	39	VSIN
14	VSS DIG	40	VSIN
15	VSS DIG	41	VSIN
16	VSS DIG	42	VSIN
17	VSS DIG	43	VSIN
18	VSS DIG	44	VSIN
19	VSS DIG	45	VSIN
20	VSS DIG	46	VSIN
21	VSS DIG	47	VSIN
22	VSS DIG	48	VSIN
23	VSS DIG	49	VSIN
24	VSS DIG	50	VSIN
25	VSS DIG	51	VSIN
26	VSS DIG	52	VSIN
27	VSS DIG	53	VSIN
28	VSS DIG	54	VSIN
29	VSS DIG	55	VSIN
30	VSS DIG	56	VSIN
31	VSS DIG	57	VSIN
32	VSS DIG	58	VSIN
33	VSS DIG	59	VSIN
34	VSS DIG	60	VSIN
35	VSS DIG	61	VSIN
36	VSS DIG	62	VSIN
37	VSS DIG	63	VSIN
38	VSS DIG	64	VSIN
39	VSS DIG	65	VSIN
40	VSS DIG	66	VSIN
41	VSS DIG	67	VSIN
42	VSS DIG	68	VSIN
43	VSS DIG	69	VSIN
44	VSS DIG	70	VSIN
45	VSS DIG	71	VSIN
46	VSS DIG	72	VSIN
47	VSS DIG	73	VSIN
48	VSS DIG	74	VSIN
49	VSS DIG	75	VSIN
50	VSS DIG	76	VSIN
51	VSS DIG	77	VSIN
52	VSS DIG	78	VSIN
53	VSS DIG	79	VSIN
54	VSS DIG	80	VSIN
55	VSS DIG	81	VSIN
56	VSS DIG	82	VSIN
57	VSS DIG	83	VSIN
58	VSS DIG	84	VSIN
59	VSS DIG	85	VSIN
60	VSS DIG	86	VSIN
61	VSS DIG	87	VSIN
62	VSS DIG	88	VSIN
63	VSS DIG	89	VSIN
64	VSS DIG	90	VSIN
65	VSS DIG	91	VSIN
66	VSS DIG	92	VSIN
67	VSS DIG	93	VSIN
68	VSS DIG	94	VSIN
69	VSS DIG	95	VSIN
70	VSS DIG	96	VSIN
71	VSS DIG	97	VSIN
72	VSS DIG	98	VSIN
73	VSS DIG	99	VSIN
74	VSS DIG	100	VSIN

DSVGA Carrier Board Schematic

The schematic shows the DSVGA die connected to various components including capacitors, resistors, and connectors. The die is labeled "DSVGA DIE" and has pins 1 through 100. The schematic includes a pinout table for the die and a table of related documents.

Pinout Table

Pin	Signal	Pin	Signal
1	VSS DIG	27	PWCLK
2	VSS DIG	28	VSYN
3	VSS DIG	29	VSIN
4	VSS DIG	30	VSIN
5	VSS DIG	31	VSIN
6	VSS DIG	32	VSIN
7	VSS DIG	33	VSIN
8	VSS DIG	34	VSIN
9	VSS DIG	35	VSIN
10	VSS DIG	36	VSIN
11	VSS DIG	37	VSIN
12	VSS DIG	38	VSIN
13	VSS DIG	39	VSIN
14	VSS DIG	40	VSIN
15	VSS DIG	41	VSIN
16	VSS DIG	42	VSIN
17	VSS DIG	43	VSIN
18	VSS DIG	44	VSIN
19	VSS DIG	45	VSIN
20	VSS DIG	46	VSIN
21	VSS DIG	47	VSIN
22	VSS DIG	48	VSIN
23	VSS DIG	49	VSIN
24	VSS DIG	50	VSIN
25	VSS DIG	51	VSIN
26	VSS DIG	52	VSIN
27	VSS DIG	53	VSIN
28	VSS DIG	54	VSIN
29	VSS DIG	55	VSIN
30	VSS DIG	56	VSIN
31	VSS DIG	57	VSIN
32	VSS DIG	58	VSIN
33	VSS DIG	59	VSIN
34	VSS DIG	60	VSIN
35	VSS DIG	61	VSIN
36	VSS DIG	62	VSIN
37	VSS DIG	63	VSIN
38	VSS DIG		

Figure 28: Color Carrier board schematic (D01-501043-03)

13. APPENDIX C: EEPROM MEMORY MAP

Each DSVGA micro display contains an EEPROM memory device to serve as non-volatile data storage for retrieving display specific information, such as its serial number and optimal registers values for proper operation. The data can be accessed via the same I²C serial interface that is used to communicate with the micro display. The EEPROM'S serial address is as follows:

Write Mode: Address is A6h

Read Mode: Address is A7h

The first 5 bytes represent the serial number of the DSVGA micro display. The following 48 bytes contain sequential data values that can be used to write to the micro display's internal registers starting with register address, "00h", to "55h".

Registers defined as RESERVED should not be changed.

Addresses beyond 8Dh are blank.

NOTE: The EEPROM is not write-protected and care should be taken not to activate the Write Mode. The values highlighted in gray are measured at the factory and are specific to each individual device.

Memory Addr (Dec)	Memory Addr (hex)	DSVGA Microdisplay	OLED
0	0	Serial Char #0	
1	1	Serial Char #1	
2	2	Serial Char #2	
3	3	Serial Char #3	
4	4	Serial Char #4	
5	5	Lot Char#0	
6	6	Lot Char#1	
7	7	Lot Char#2	
8	8	Lot Char#3	
9	9	Lot Char#4	
10	A	Lot Char#5	
11	B	Wafer Char#0	
12	C	Wafer Char#1	
13	D	Wafer Char#2	

14	E	Wafer Char#3
15	F	Data Format Version# (00h)
16	10	STATUS
17	11	VINMODE
18	12	DISPMODE
19	13	LFTPOS
20	14	RGTPOS
21	15	TOPPOS
22	16	BOTPOS
23	17	RESERVED
24	18	RESERVED
25	19	ROWRESETL
26	1A	ROWRESETH
27	1B	RAMPCTL
28	1C	RAMPCM
29	1D	VDACMX
30	1E	BIASN
31	1F	GAMMASET
32	20	VCOMMODE
33	21	VCOMCTL
34	22	VGMAX
35	23	MVCOM
36	24	IDRF
37	25	DIMCTL
38	26	TREFDIV
39	27	TEMPOFF
40	28	TUPDATE
41	29	TEMPOUT
42	2A	ANGPWRDN
43	2B	SYSPWRDN
44	2C	TMODE
45	2D	TPLINWITH
46	2E	TPCOLSP
47	2F	TPROWSP
48	30	TPCOLOR
49	31	LUT_ADDR
50	32	LUT_DATA1
51	33	LUT_DATAH
52	34	LUT_UPDATE
53	35	PUPCTL
54	36	V_BLANK
55	37	H_BLANK
56	38	V_OFFSET
57	39	H_DLY
58	3A	MISCCTL
59	3B	CSCCO
60	3C	CSCC1L
61	3D	CSS1H

62	3E	CSCC2L
63	3F	CSCC2H
64	40	CSCC3L
65	41	CSCC3H
66	42	CSCC4L
67	43	CSCC4H
68	44	CSCC5L
69	45	CSCC5H
70	46	RESERVED
71	47	DIGTEST
72	48	NOFLINEL
73	49	NOFLINEH
74	4A	NOFPXLL
75	4B	NOFPXLH
76	4C	RESERVED
77	4D	RESERVED
78	4E	RESERVED
79	4F	RESERVED
80	50	RESERVED
81	51	RESERVED
82	52	DISPMOD_BN
83	53	IDRF_BN
84	54	DIMCTL_BN
85	55	VGNA0_HI
86	56	VGNA0_LO
87	57	VGNA1_HI
88	58	VGNA1_LO
89	59	VGNA2_HI
90	5A	VGNA2_LO
91	5B	VGNA3_HI
92	5C	VGNA3_LO
93	5D	VGNA4_HI
94	5E	VGNA4_LO
95	5F	VGNA5_HI
96	60	VGNA5_LO
97	61	VGNA6_HI
98	62	VGNA6_LO
99	63	VGNA7_HI
100	64	VGNA7_LO
101	65	VGNB0_HI
102	66	VGNB0_LO
103	67	VGNB1_HI
104	68	VGNB1_LO
105	69	VGNB2_HI
106	6A	VGNB2_LO
107	6B	VGNB3_HI
108	6C	VGNB3_LO
109	6D	VGNB4_HI

110	6E	VGNB4_LO
111	6F	VGNB5_HI
112	70	VGNB5_LO
113	71	VGNB6_HI
114	72	VGNB6_LO
115	73	VGNB7_HI
116	74	VGNB7_LO
117	75	GMMA00_HI
118	76	GMMA00_LO
119	77	GMMA01_HI
120	78	GMMA01_LO
121	79	GMMA02_HI
122	7A	GMMA02_LO
123	7B	GMMA03_HI
124	7C	GMMA03_LO
125	7D	GMMA04_HI
126	7E	GMMA04_LO
127	7F	GMMA05_HI
128	80	GMMA05_LO
129	81	GMMA06_HI
130	82	GMMA06_LO
131	83	GMMA07_HI
132	84	GMMA07_LO
133	85	GMMA08_HI
134	86	GMMA08_LO
135	87	RESERVED
136	88	RESERVED
137	89	MM
138	8A	DD
139	8B	YY
140	8C	YY
141	8D	Carrier board version number
142	8E	IDRF Slope – Integer part
143	8F	IDRF Slope – Fractional part
144	90	IDRF Intercept

14. APPENDIX D: RECOMMENDED REGISTER SETTINGS

RECOMMENDED DSVGA REGISTER SETTING			
Register name	Register Addr (dec)	Register Addr (hex)	Register Value
STATUS	0	0	01
VINMODE	1	1	20
DISPMODE	2	2	70
LFTPOS	3	3	0C
RGTPPOS	4	4	0C
TOPPOS	5	5	0C
BOTPOS	6	6	0C
RESERVED	7	7	80
RESERVED	8	8	80
ROWRESETL	9	9	00
ROWRESETH	10	A	00
RAMPCTL	11	B	01
RAMPCM	12	C	77
VDACMX	13	D	74
BIASN	14	E	04
GAMMASET	15	F	07
VCOMMODE	16	10	04
VCOMCTL	17	11	3D
VGMAX	18	12	0D
MVCOM	19	13	51
IDRF	20	14	32
DIMCTL	21	15	64
TREFDIV	22	16	13
TEMPOFF	23	17	6E
TUPDATE	24	18	FF
TEMPOUT	25	19	00
ANGPWRDN	26	1A	00
SYSPWRDN	27	1B	00
TMODE	28	1C	00
TPLINWITH	29	1D	00
TPCOLSP	30	1E	00
TPROWSP	31	1F	00
TPCOLOR	32	20	07

LUT_ADDR	33	21	FF
LUT_DATA_L	34	22	00
LUT_DATA_H	35	23	00
LUT_UPDATE	36	24	17
PUPCTL	37	25	00
V_BLANK	38	26	00
H_BLANK	39	27	00
V_OFFSET	40	28	00
H_DLY	41	29	01
MISCTL	42	2A	00
CSCCO	43	2B	10
CSCC1L	44	2C	2A
CSS1H	45	2D	01
CSCC2L	46	2E	98
CSCC2H	47	2F	01
CSCC3L	48	30	D0
CSCC3H	49	31	00
CSCC4L	50	32	64
CSCC4H	51	33	00
CSCC5L	52	34	04
CSCC5H	53	35	02
RESERVED	54	36	00
DIGTEST	55	37	00
NOFLINEL	56	38	00
NOFLINEH	57	39	00
NOFPXLL	58	3A	00
NOFPXLH	59	3B	00

15. APPENDIX E: CLEANING, HANDLING AND STORAGE CONDITIONS

15.1 Cleaning

When cleaning the displays we recommend the use of TECH-SPEC lens cleaner, manufactured by Edmund Optics Inc. and Alpha wipes 1010

15.2 General handling considerations

- Do not expose the display to strong acids, bases, or solvents.
- Do not expose the display surface to UV or other strong ionizing radiation
- Temperatures in excess of the specified operating and storage range can cause irreversible damage to the display.
- Do not allow sharp objects to contact the exposed regions of the silicon display chip.
- Avoid immersion of the display in any liquid.
- The glass cover slip protects the display surface from most forms of damage and may be cleaned using techniques appropriate for fine lenses.
- Avoid applying force to the glass relative to the display chip in compressive, tensile, and sheer directions.

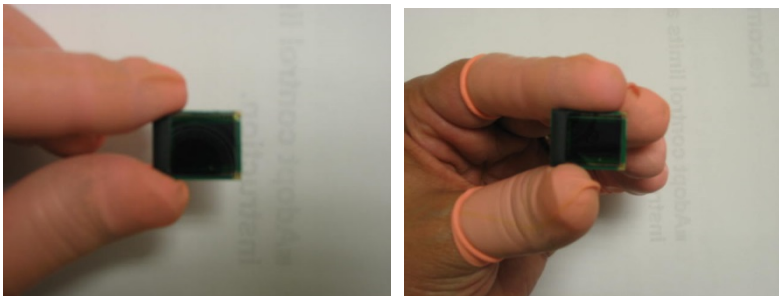


Fig. 3 Best method of handling the displays



Fig. 4 Avoid this method of display handling

15.3 Static Charge Prevention

The microdisplay is sensitive to electro-static discharge damage. The following measures are recommended to minimize ESD occurrences:

- When handling the microdisplay, operated under a flow of ionized air to discharge the panel
- Use a conductive wrist strap connected to earth ground via a 10 M-Ohm resistor.
- Wear non-chargeable clothes
- Keep stored displays away from charged materials

15.4 Protection from Dust and Dirt

It is also recommended that all display handling operations take place in a clean environment. The use of ionized nitrogen gas is the preferred method of removing particles from the surface.

15.5 Short Term Storage

For short term storage (one to two weeks or less), the displays should be kept in their original container at room ambient and the typical controlled office environment.

15.6 Long Term Storage

For displays that will be stored for a longer period (a few weeks and up), it is recommended to keep displays stored in a dry environment near or at room ambient (20°C typically) whenever possible prior to installation into an optical subsystem.

There are several ways to achieve this:

- Dry storage cabinet
- Dry Nitrogen cabinet
- Nitrogen sealed bag
- Vacuum sealed bag with desiccant