Final Project:
Hardware implementation of PDP8 Instruction Set Architecture (ISA) level simulator

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4th May 2015

Schedule update

Date	Day	What	# Lec	Chapter
30-Mar	Mon	Lecture - Introduction: Verification in the Chip Design Process	1	Chapter 1
1-Apr	Wed	Lecture - Verification Flow	1	Chapter 1 & 2
6-Apr	Mon	Lecture - Verification Strategy	1	Chapter 2
8-Apr	Wed	Lecture - Verilog/System Verilog	1	Online
13-Apr	Mon	Lecture - Verification Environment	1	Chapter 3
15-Apr	Wed	Lecture - Assertion Based Verification & Test Benches	1	Chapter 3
20-Apr	Mon	Lecture - Verification Plan - Part 1	1	Chapter 4
22-Apr	Wed	Lecture - Verification Plan - Part 2	1	Chapter 4
27-Apr	Mon	Mid-term	0	
29-Apr	Wed	Lecture - HDL, Simulation fundamentals and Coverage	1	Chapter 5/6
4-May	Mon	Project discussion	0	
6-May	Wed	Lecture - Stimulus Generation	1	Chapter 7
11-May	Mon	Lecture - Checking	1	Chapter 8
13-May	Wed	Lecture - Pervasive Functional Verification	1	Chapter 9
18-May	Mon	Project proposal Demo	0	
20-May	Wed	Lecture - Reuse and System Level Simulation	1	Chapter 10
25-May	Mon	No Class. Memorial Day	0	No Class
27-May	Wed	Lecture - Regression	1	Chapter 13/14
1-Jun	Mon	Lecture - Modern Verification technics - Introduction to OVM/UVM	1	OVM/UVM
3-Jun	Wed	Lecture - Introduction to Hardware Acceleration and Emulation	1	Emulation
8-Jun	Mon	Final	0	
10-Jun	Wed	Project demo - I	0	
11-Jun	Thu	Project demo - II	0	
Total			16	

Updates on Labs and HW assignments

- Homework#3 is due: Wednesday May 6th at noon (11:59am).

- Lab2 is due: Saturday May 9th at midnight (11:59pm).

- HW#1:

  – Grading is almost done. Hit a snafu with block diagram.

  – Will be posted by tomorrow night.

- Lab1 grading started. Hopefully by next Monday.

- Homework#2 grading: Not started yet. Probably by next Wed.

- Mid-term grading: Started. Will be posted by 18th.

  – Mid-term papers will not be returned. Solutions will be in class for review. Will have extended office hours to review your exam papers.

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Brief history of PDP8 minicomputer

- The PDP-8 was an important early mini-computer in the history of computing.

- Many are still running today performing their original function.

- The PDP-8 was used for industrial control, controlling experiments, running businesses, word processing, and many other uses.

- Let's go into details of PDP8 architecture http://en.wikipedia.org/wiki/PDP-8

Overview of the DUV

- Block diagram is a part of project proposal assignment.

Micro-architectural details

- The hardware simulator consists of an instruction fetch and decode unit (IFD), an execution unit (EXE) and a memory unit (MEM).

- The memory unit (4K words of 12bit each) is pre-loaded with data derived from a compiled PDP8 assembly language test.

- Once out of reset, instruction fetch & decode unit (IFD) fetches the first instruction from a pre-determined memory location (200o).

- IFD sends the instruction to execution unit (EXE) which processes the instruction and reads/writes from/to memory (if needed based on the instruction).

- Once the current instruction is completed, IFD fetches the next instruction from a new location (based on program counter).

- The whole process is repeated until the program counter is loaded with the address of the very first instruction (i.e. 200o).

HDL milestones

- Interface only – with description – By Wednesday this week.

- Initial drop – Full code: By Friday this week.

- Final drop – Some micro-architectural changes: Monday next week (05/11/2015)

Deliverables (Proposal)

1. Study the design HDL
2. Write a detailed micro-architectural specification (to make sure you understand the design)

    Block diagram

    All FSMs diagrams

    FSM state transitions

    How the whole design works

3. Write a detailed functional coverage based test plan

    I will spell out more details but it must include:

    unit level testing strategy

    unit level TB block diagrams (tentative)

Deliverables (Final)

1. Add assertions.

2. Add random testing capability (even though this would be challenging for assembly language based tests)

3. Add checker for instructions that are being decoded

4. Add checker for logical and arithmetic operation that are being performed

5. Add scoreboard to make sure all instructions are being completed

6. End-of-test memory check.

7. Add coverage measurement capability to report coverage.

8. Detailed project report at the end of term.

Logistics and Timelines

- Group size:
  - Two persons per group.
  - Tasks must be divided equally.
  - Ownership boundaries must be defined and documented.
- Select your project partner and submit both names to me: Monday 11th May 2015 (One week from today).
  - Just one email from either of the partners and cc the other.
  - If you want to work alone, please inform me ASAP.
- Proposal due: Monday 18th May 2015 (Two weeks from today)
  - In class presentation – 5 to 7 minutes per group
- Final report and demo/presentation: 11th June
  - In class presentation and demo – 15 minutes including Q&A.

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Questions??

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ECE510
Pre-Silicon Validation