Date : 03– 06 – 2020

Name : Kulvir Singh

Reg. No.: 19BCE2074

ASSESSMENT (Test) -2

Implement and Verify 4 bit Johnson's counter (synchronous counter) for the given input:

1). "0100 1110" and
2). "1010 1110

Construct the logic using Altera Quartus II or Logisim.

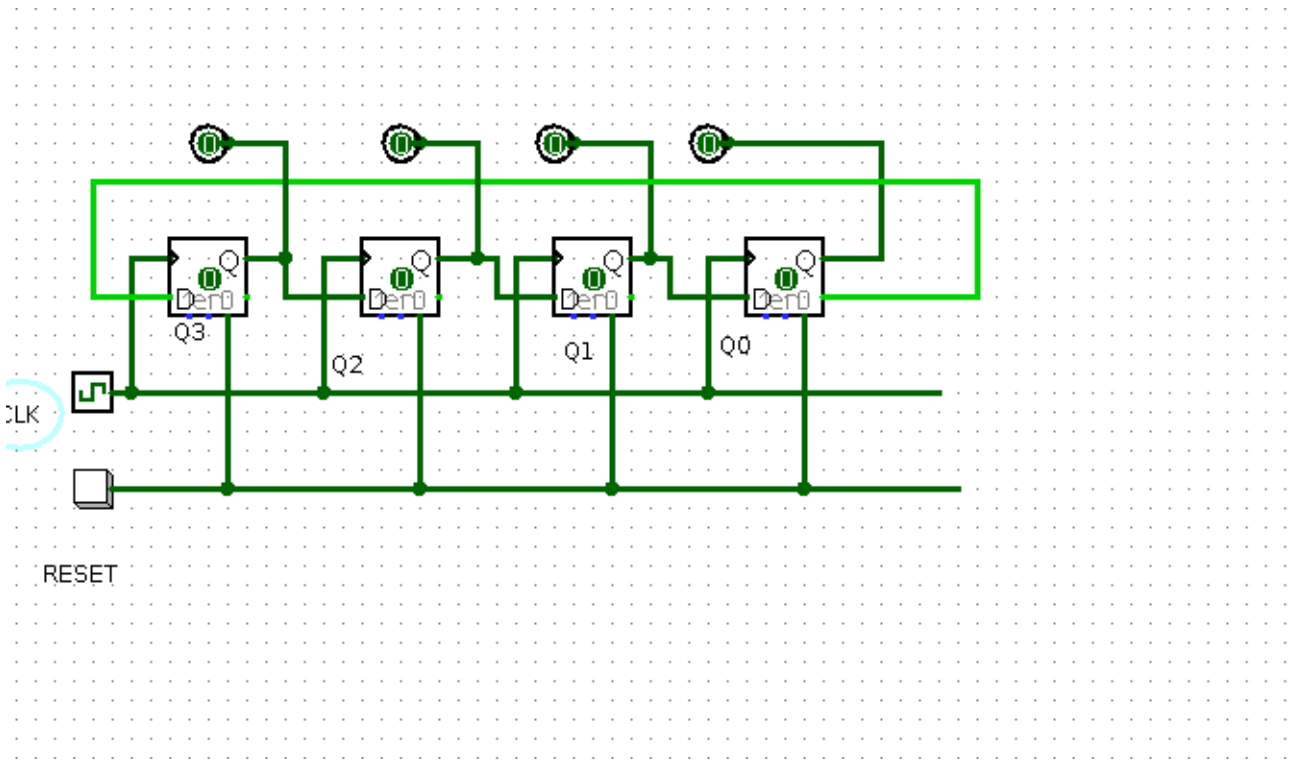
EXPERIMENTAL SCENARIO:

Truth Table

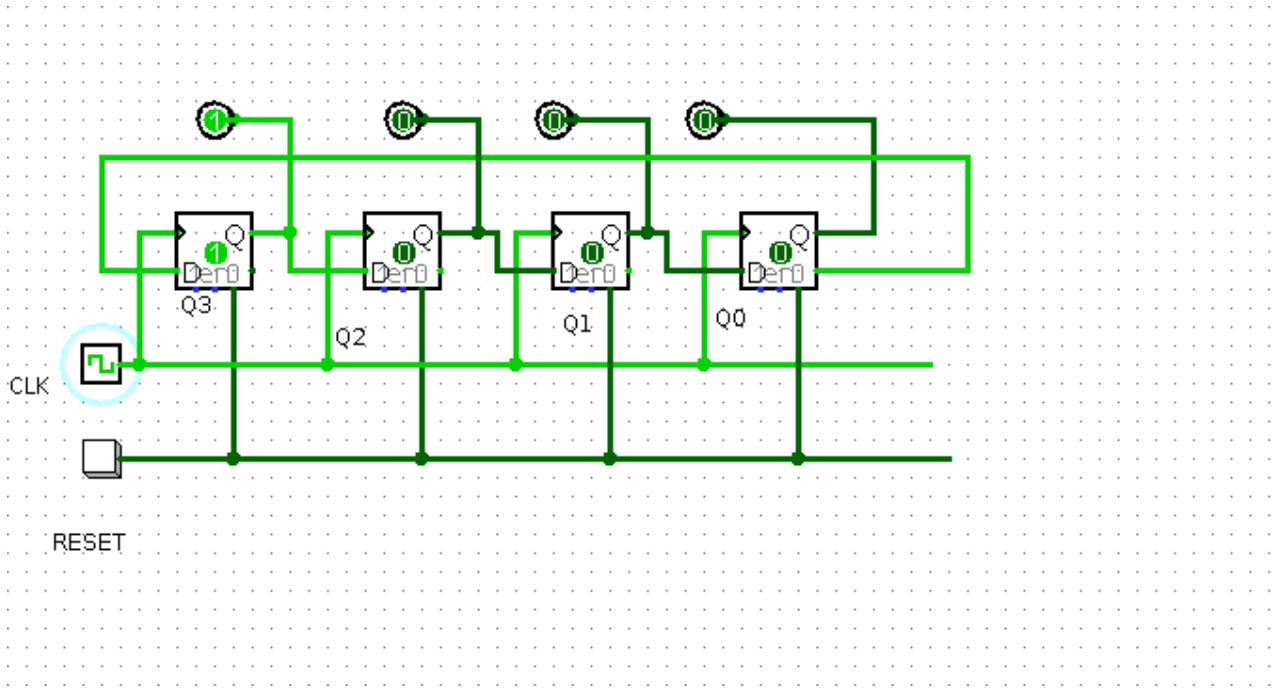
CLK	Q3	Q2	Q1	Q0
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Execution in RTL VIEWER:

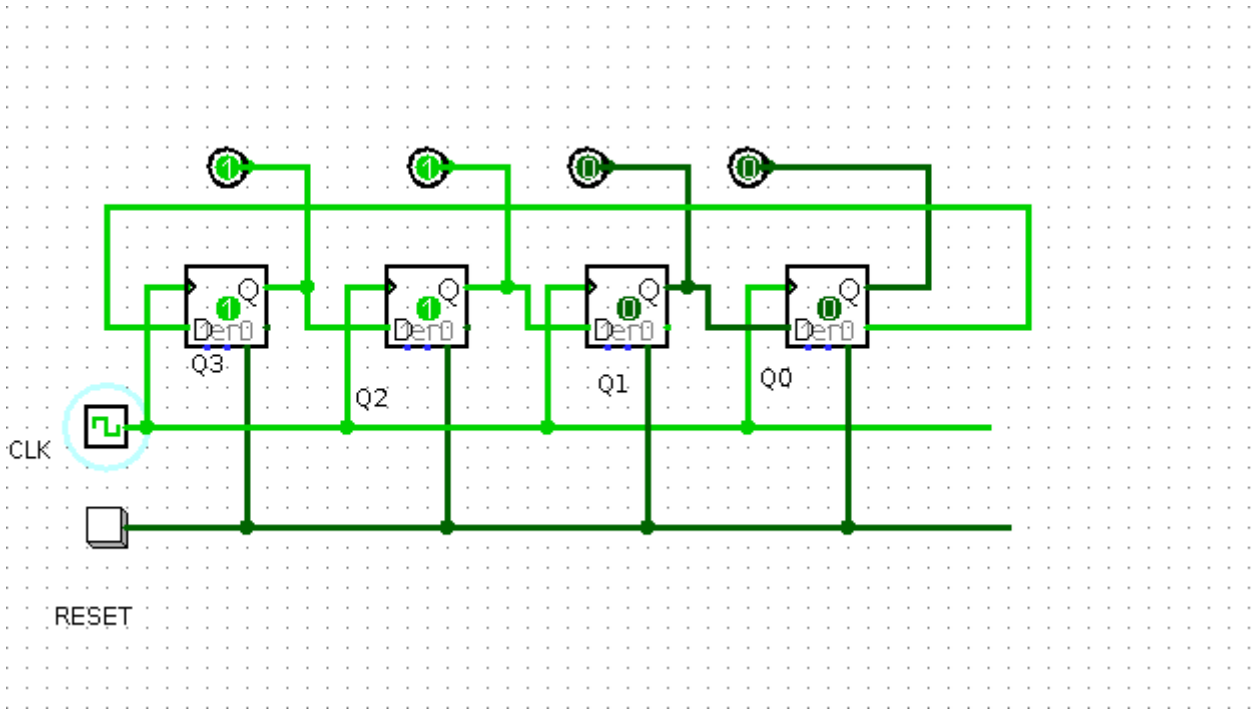
Initial



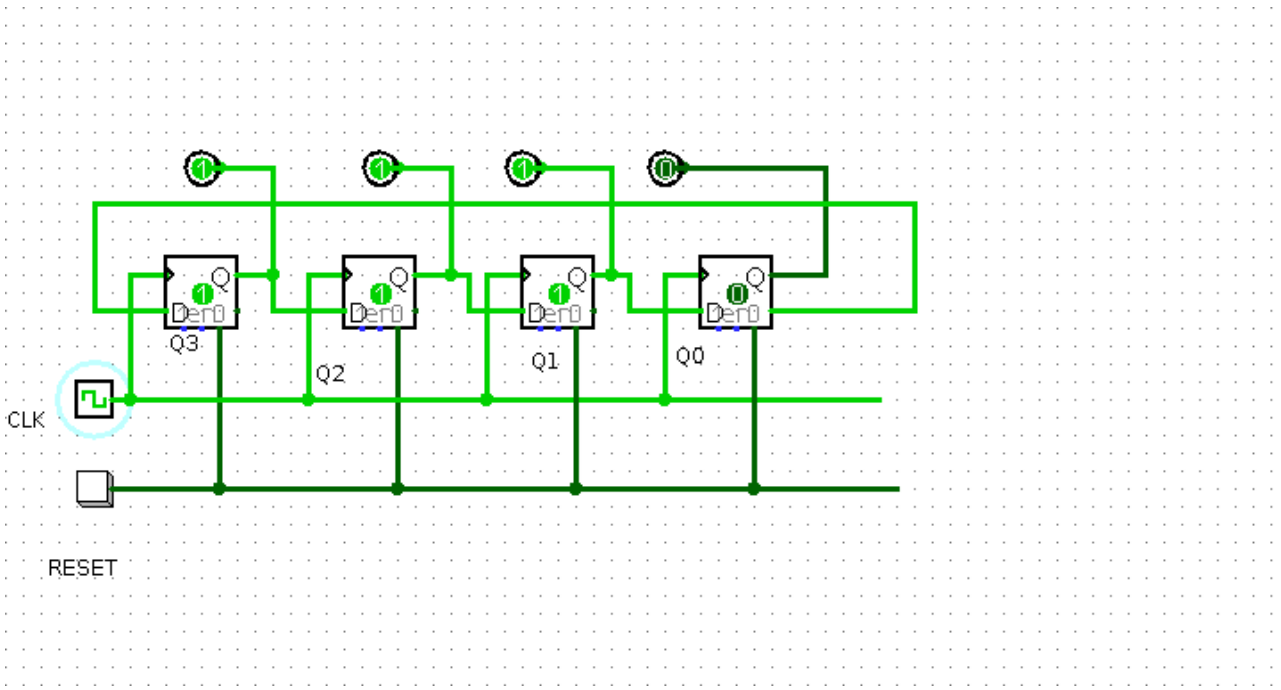
Stage 1



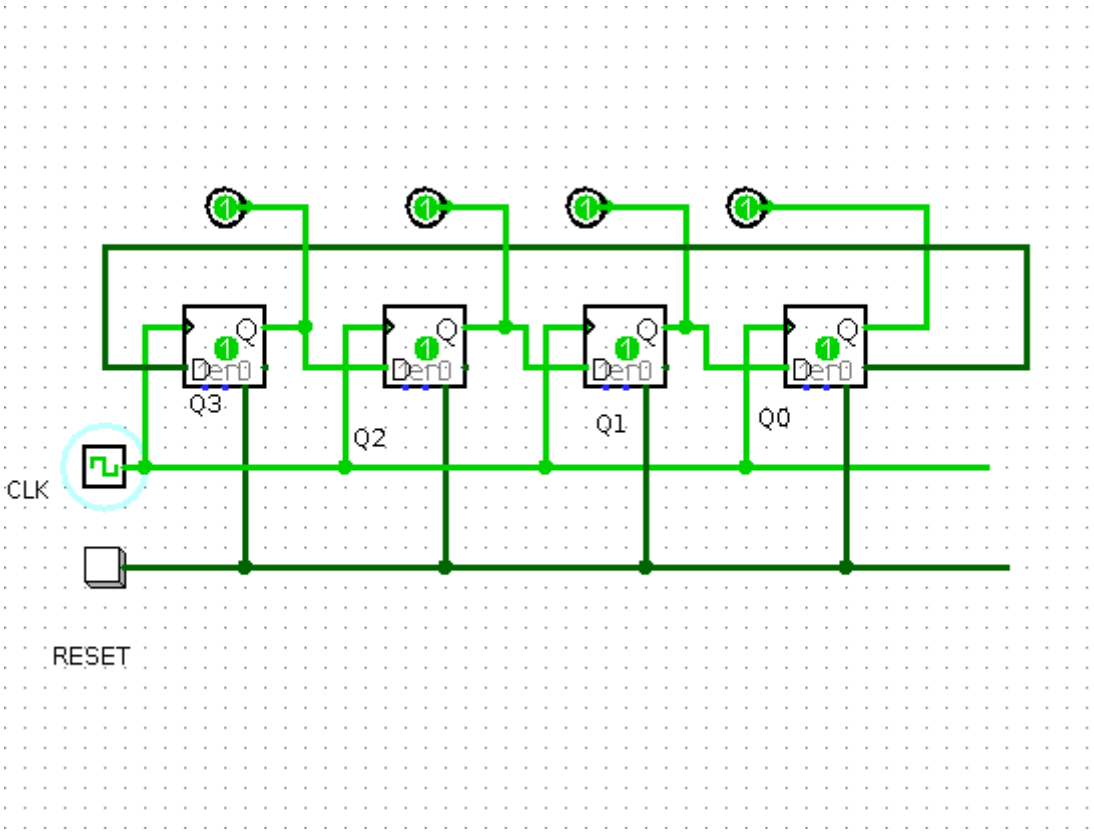
Stage 2



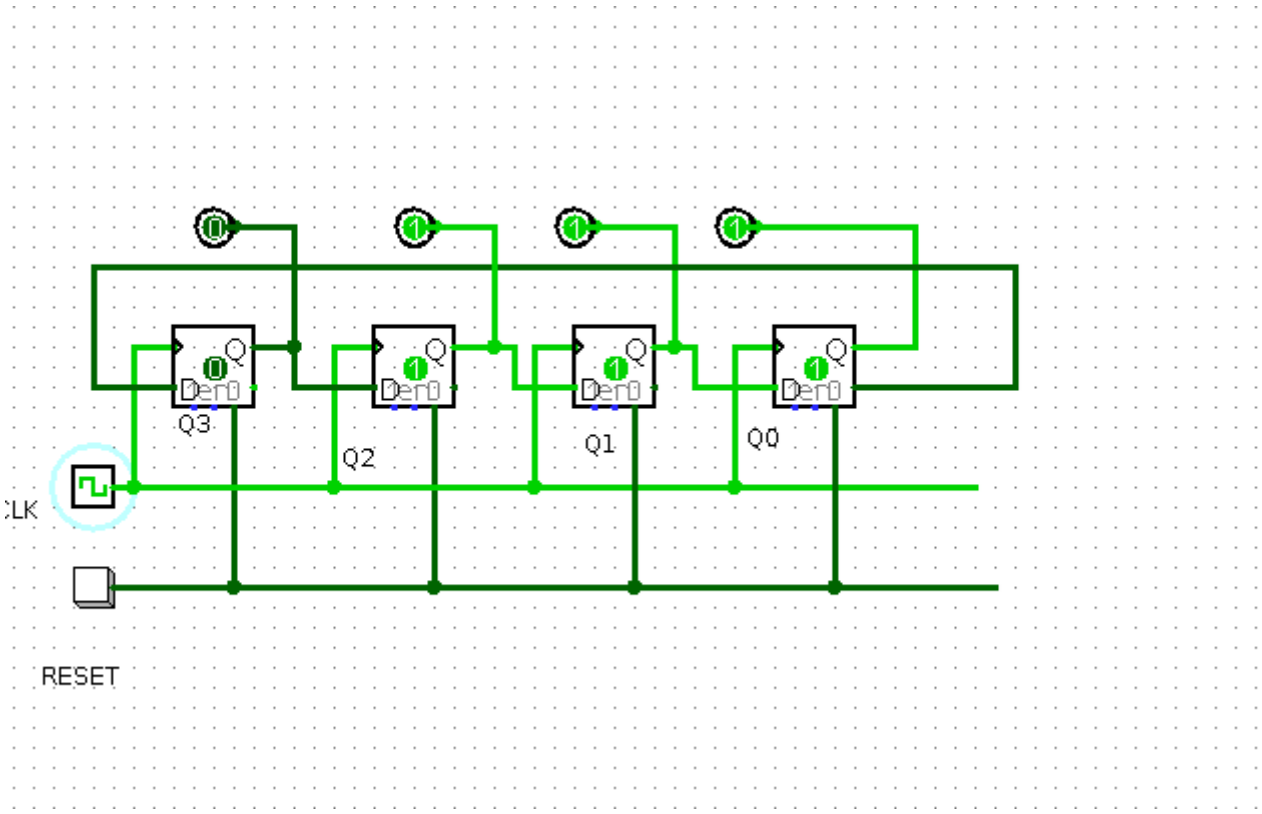
Stage 3



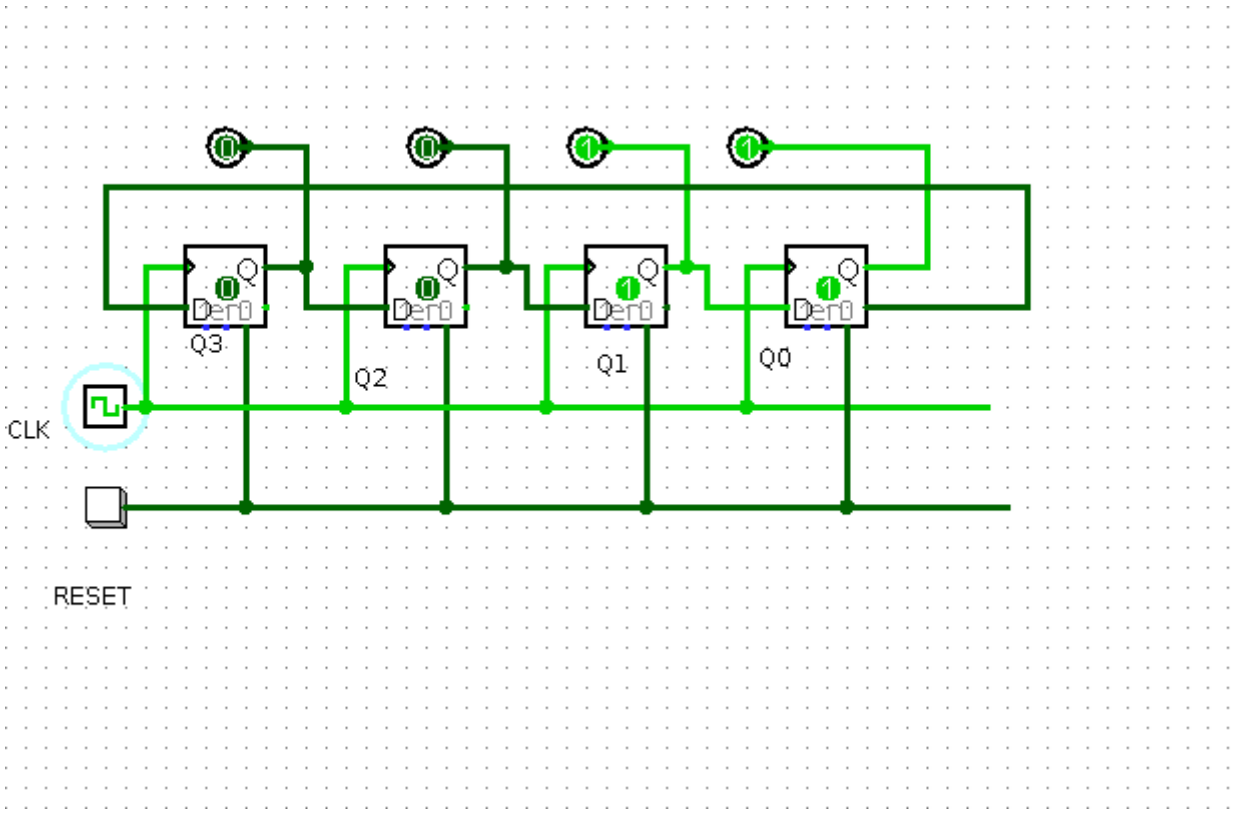
Stage 4



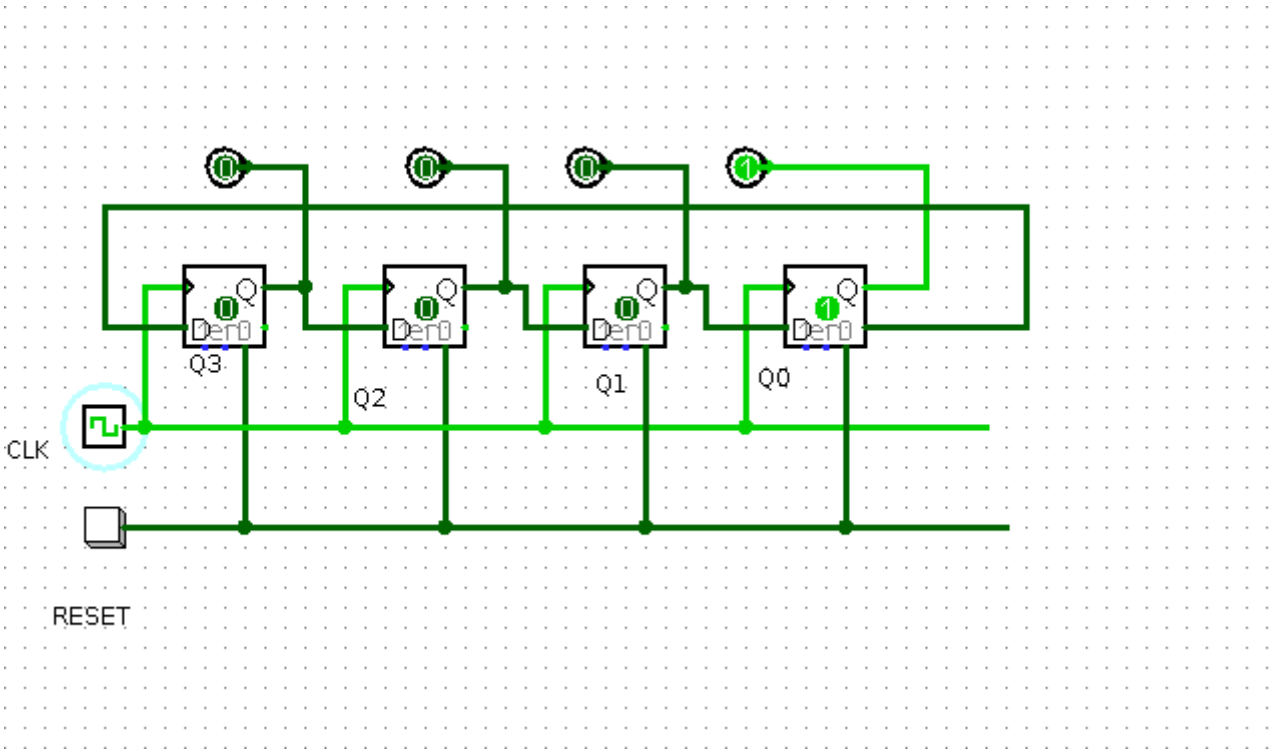
Stage 5



Stage 6



Stage 7


Q
Der0
Q3
Q2
Q1
Q0
CLK
RESET