Ex. No.: 4

Date: 17.10.19

Design of Half Adder and Full Adder circuits

Aim: To verify the truth tables of halfadder and fulladder circuit and its corresponding output waveform in Captch (CIS)

Apparatus/Tool required:

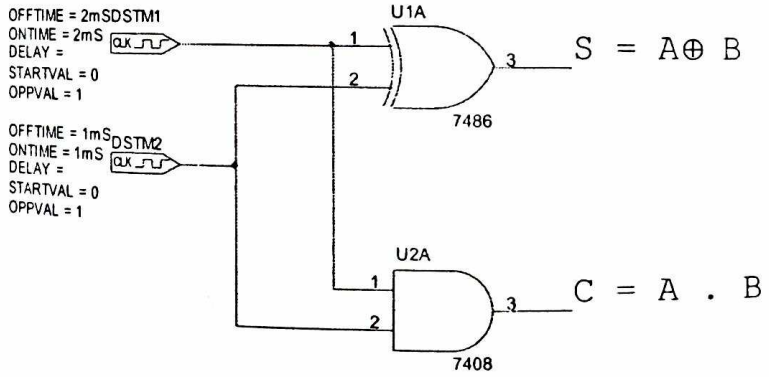
ORCAD / PSpice simulator - > **7400 Library – 7408, 7432 & 7486**
Source Library - Digclock

Simulation Settings: **Analysis Type - Time Domain**

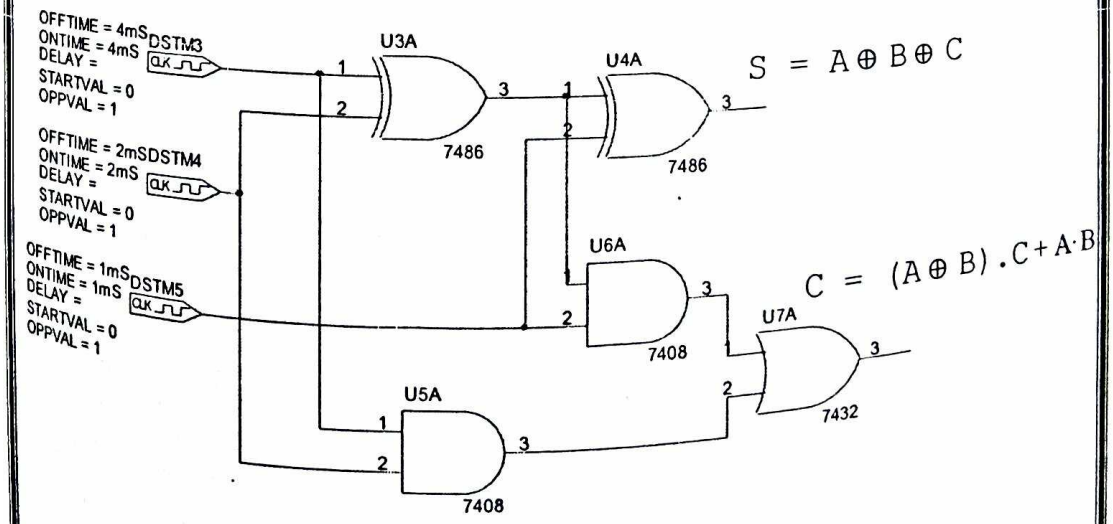
Run to time: 4ms (for Half Adder)
Run to time: 8ms (for Full Adder)

Circuit Diagram:

Half – Adder Circuit



Full – Adder Circuit



Theory:

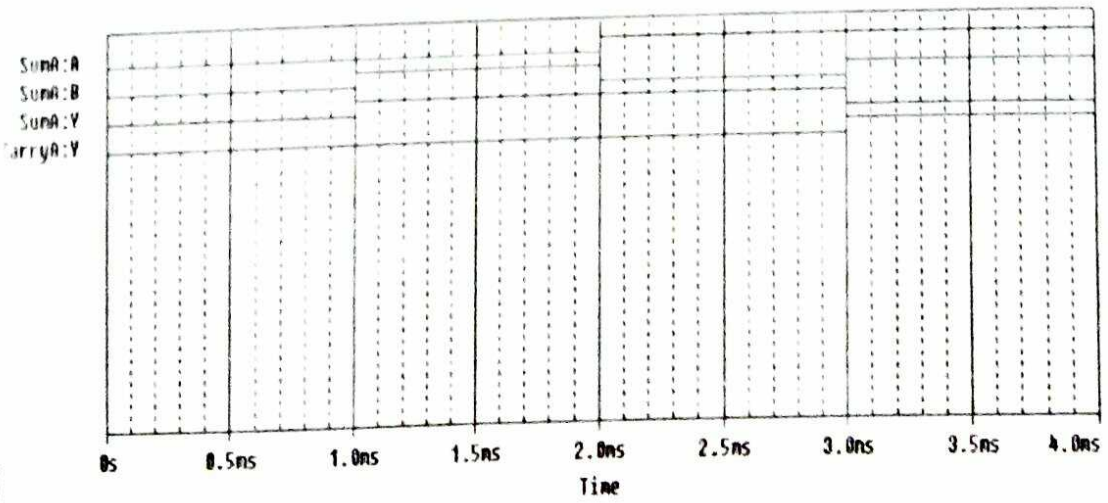
Half Adder Circuit:

Truth Table

A	B	S=A⊕B	C=A.B
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Model Timing Diagram:

Half – Adder



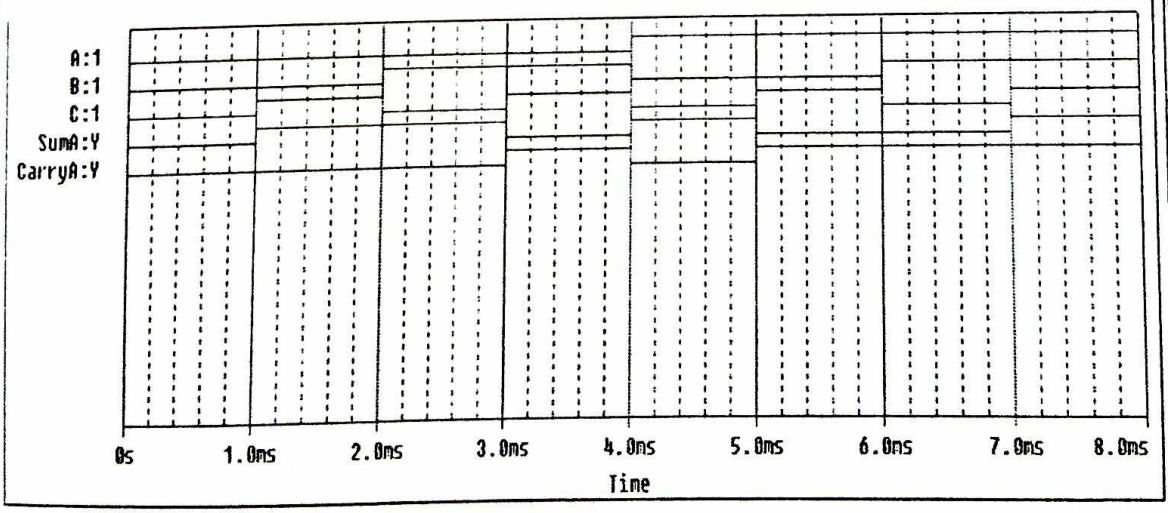
Full Adder Circuit

Truth Table

A	B	C	S=A⊕B⊕C	C= (A⊕B).C+A.B
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Model Timing Diagram:

Full – Adder

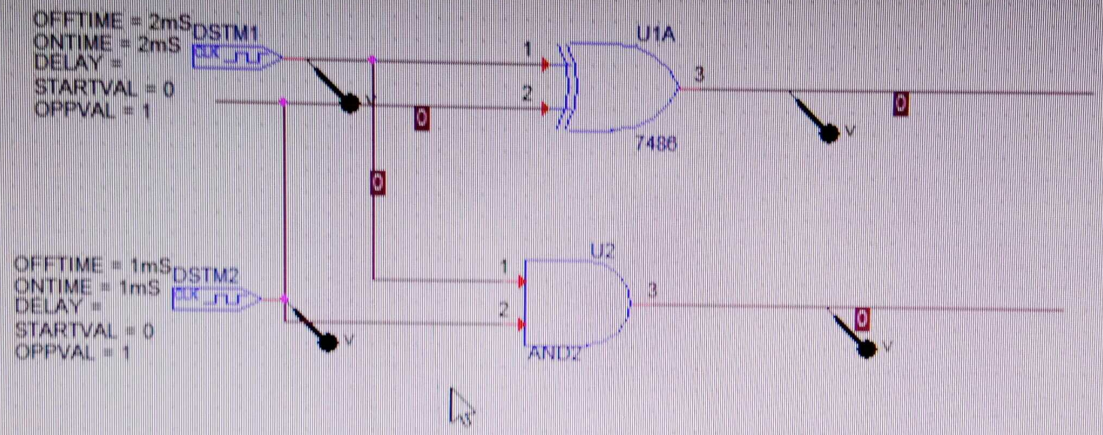


Procedure:

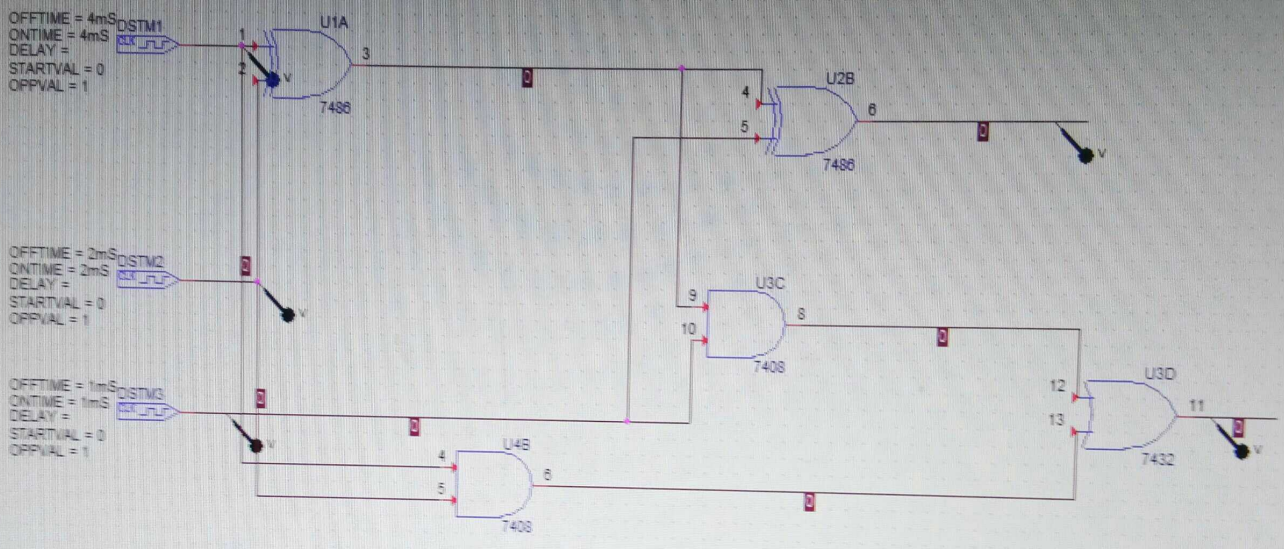
Result: The halfadder and fulladder circuit experiment performed in capture (CIS), the truthtable and its corresponding output have been verified.

Inference:

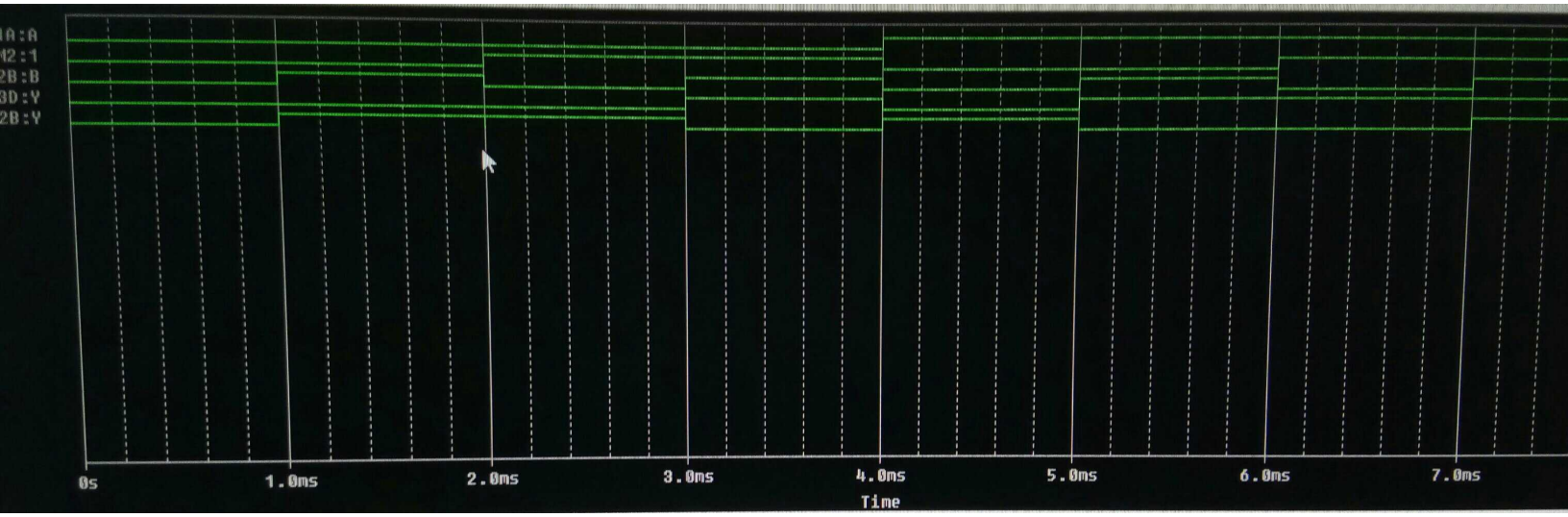
Reg. No: 19BCE2074 Name: KULVIR SINGH Date: 17.10.19

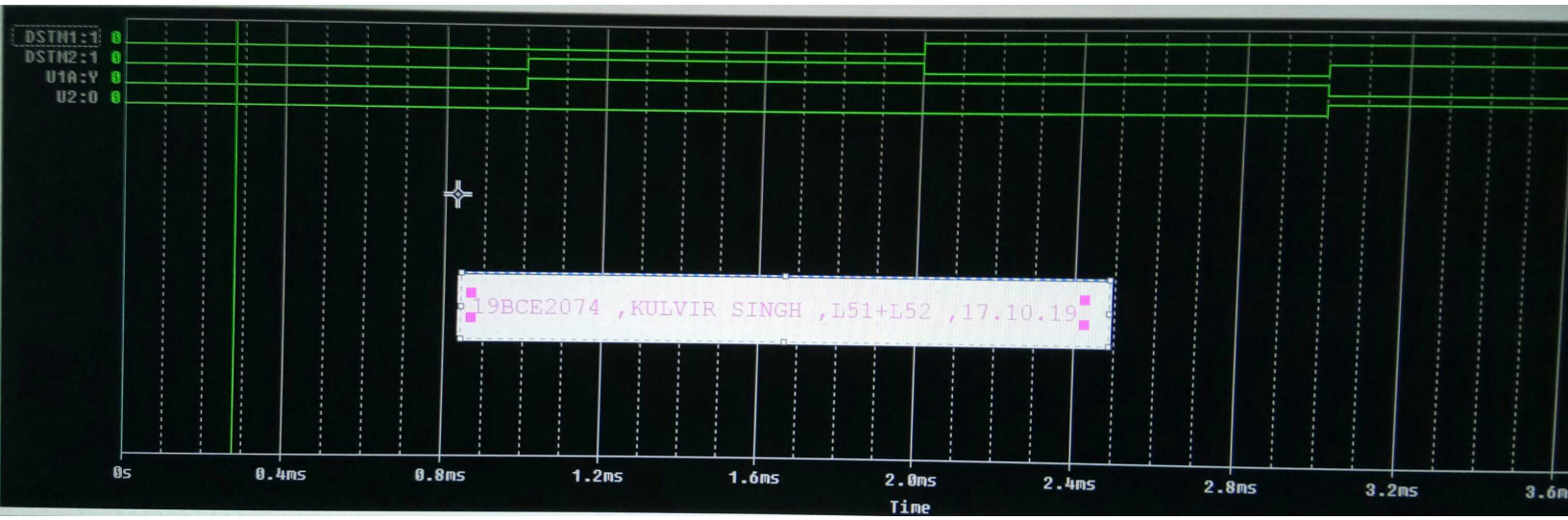


19BCE2074 ,KULVIR SINGH ,L51+L52 ,17.10.19



19BCE2074, KULVIR SINGH, L51+L52,17.10.19


1A:A
12:1
2B:B
3D:Y
2B:Y
0s
1.0ms
2.0ms
3.0ms
4.0ms
5.0ms
6.0ms
7.0ms
Time


DSTM1:1
DSTM2:1
U1A:Y
U2:O
19BCE2074 ,KULVIR SINGH ,L51+L52 ,17.10.19
0s
0.4ms
0.8ms
1.2ms
1.6ms
2.0ms
2.4ms
2.8ms
3.2ms
Time