Experiment No. - 3.

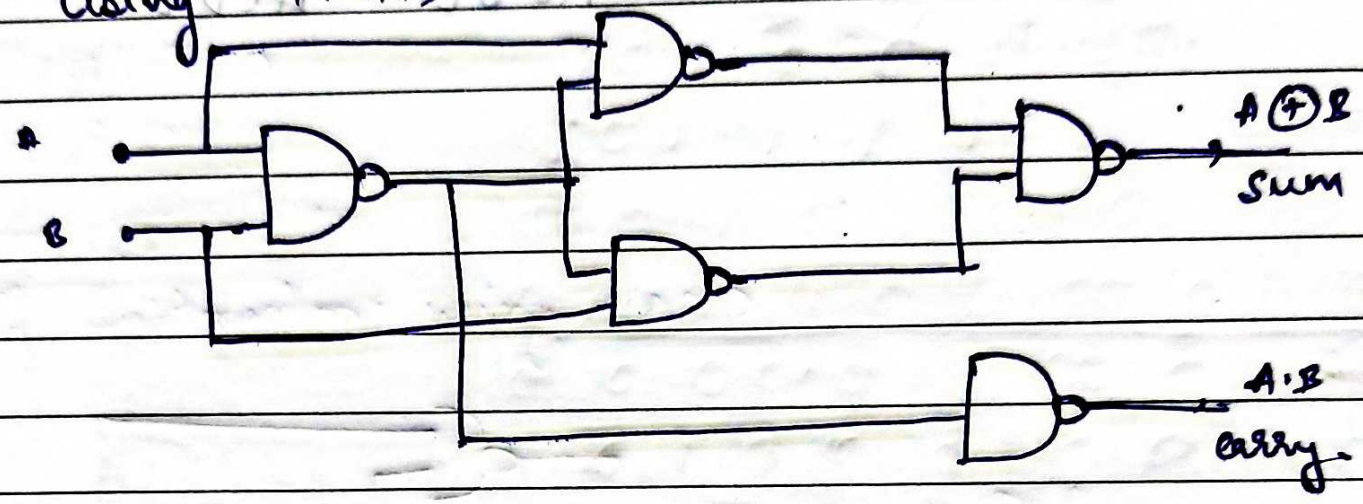
Date : 30-01-2020

Aim :

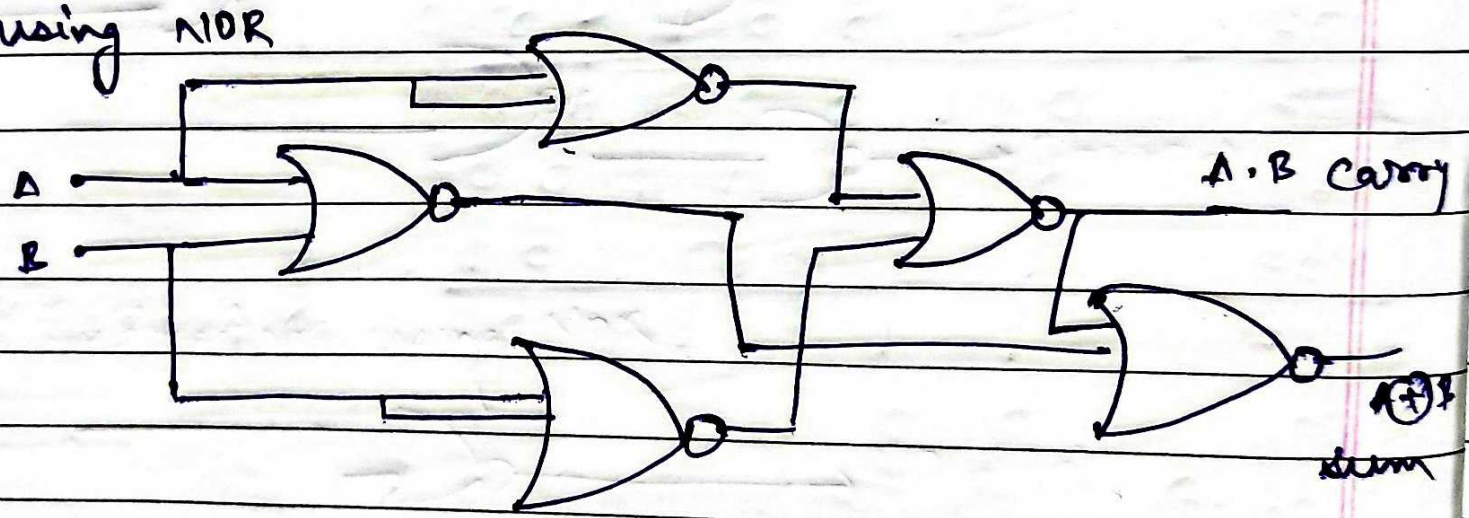
Design a half adder, full adder, half subtractor, full subtractor using NAND and NOR gates.

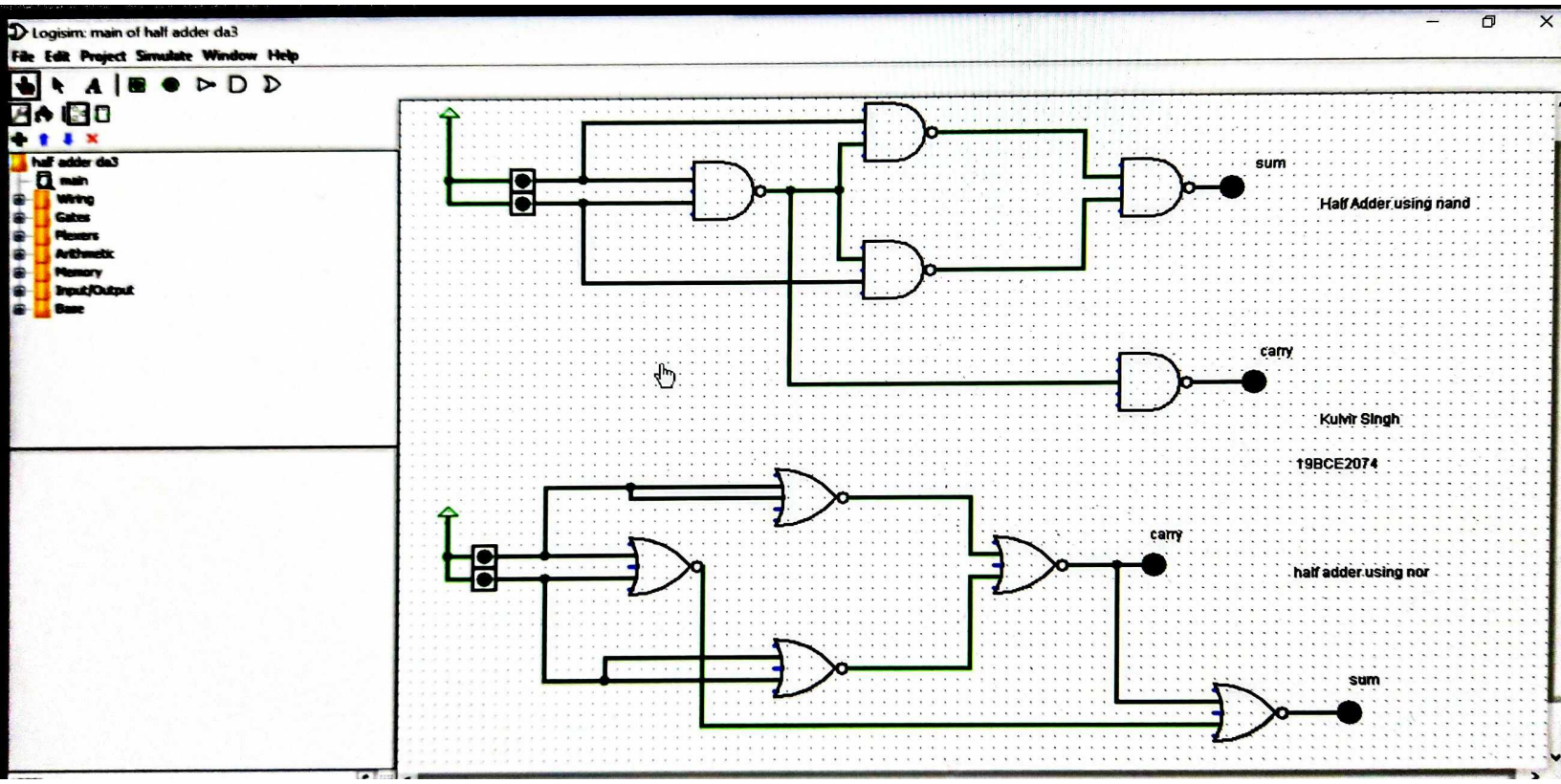
Half adder.

→ Using NAND



Using NOR

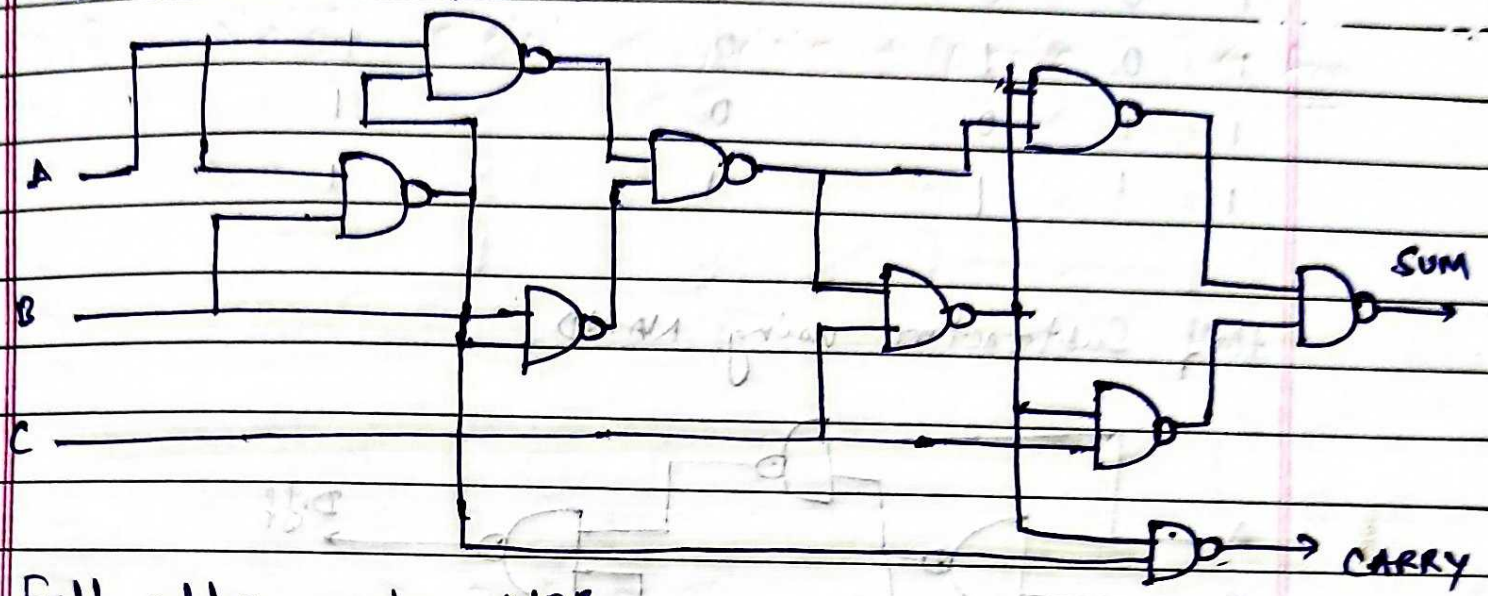



Logisim: main of half adder da3
File Edit Project Simulate Window Help
half adder da3
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
sum
Half Adder using nand
carry
Kulvir Singh
19BCE2074
carry
half adder using nor
sum

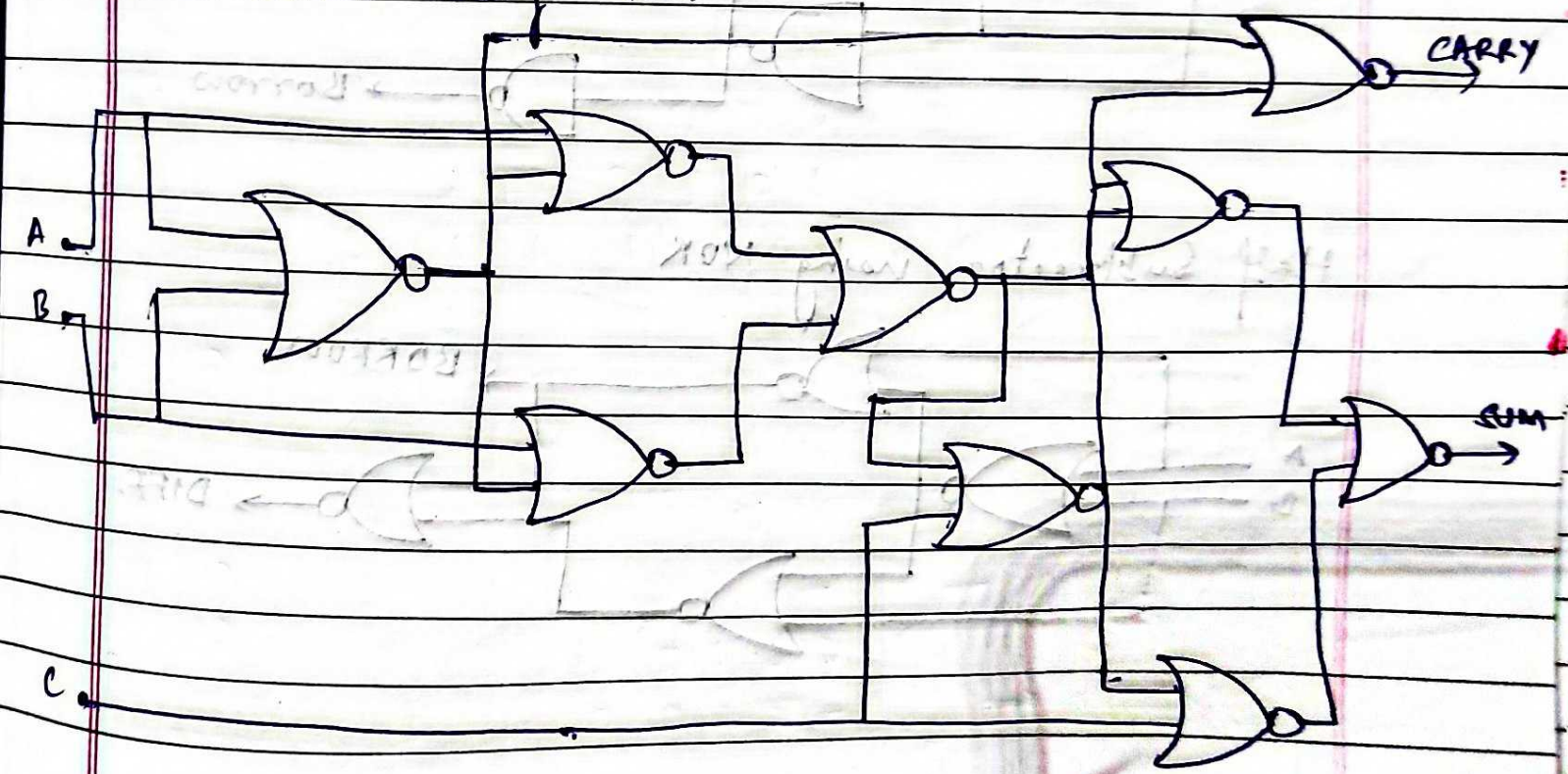
Truth Table

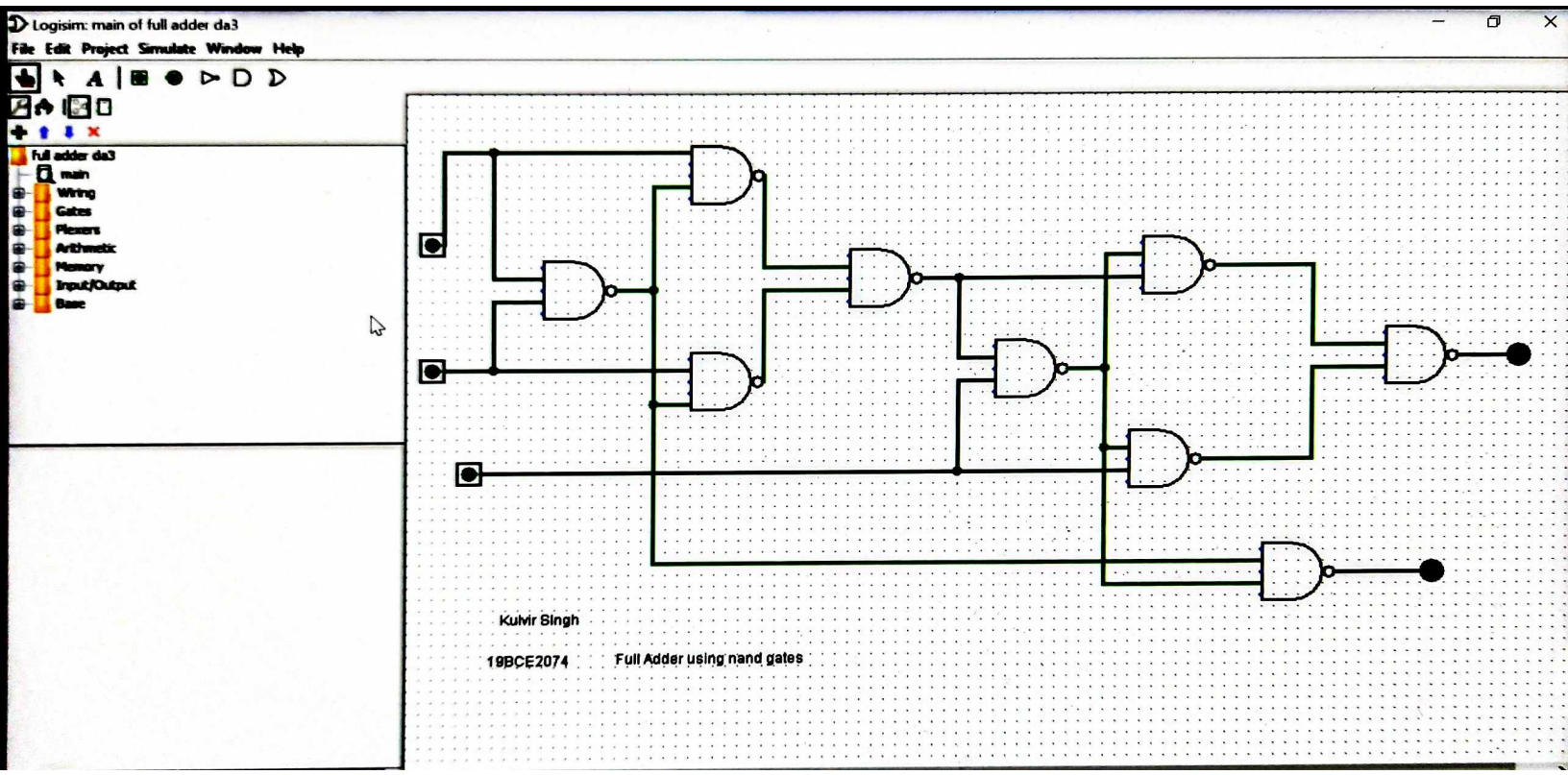
A	B	SUM $A \oplus B$	Carry $A \cdot B$
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

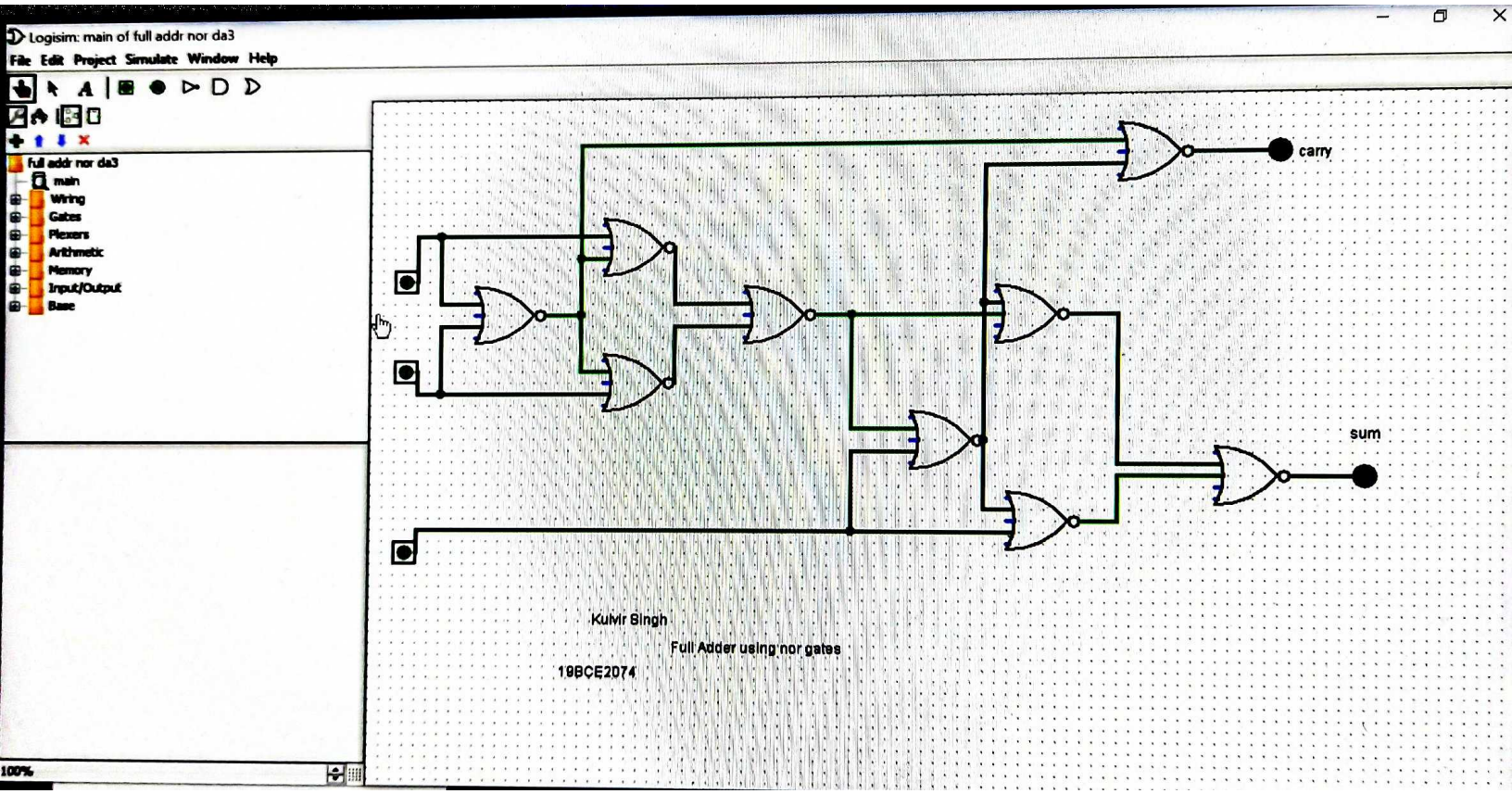
Full adder using NAND



Full adder using NOR



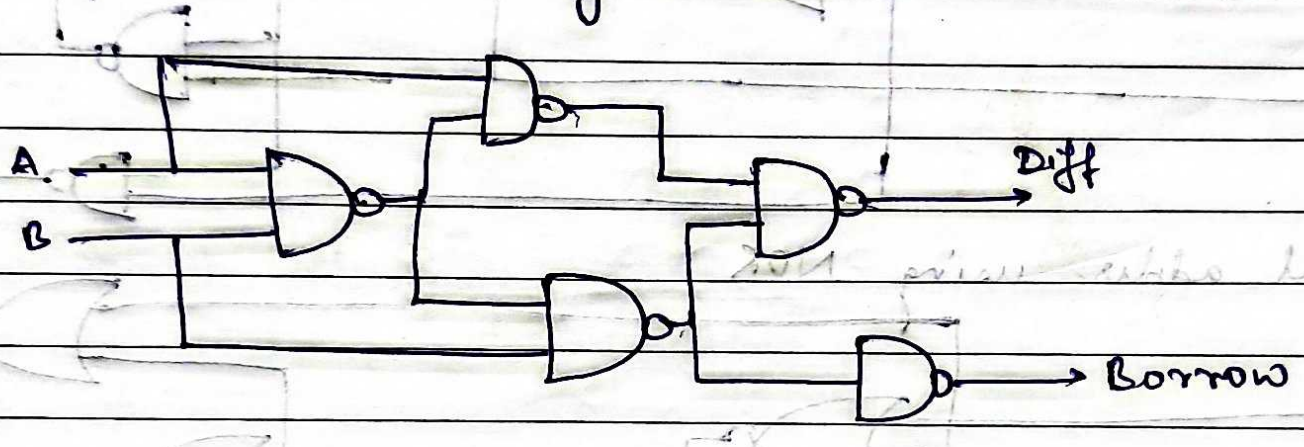

Logisim: main of full adder da3
File Edit Project Simulate Window Help
full adder da3
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Kulvir Singh
19BCE2074
Full Adder using nand gates


Logisim: main of full addr nor da3
File Edit Project Simulate Window Help
full addr nor da3
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
carry
sum
Kulvir Singh
Full Adder using nor gates
19BCE2074
100%

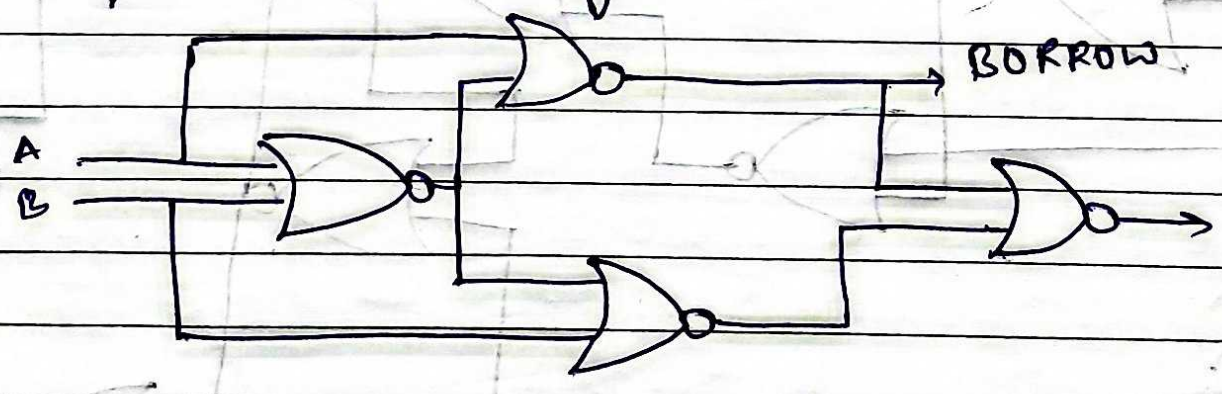
Truth Table

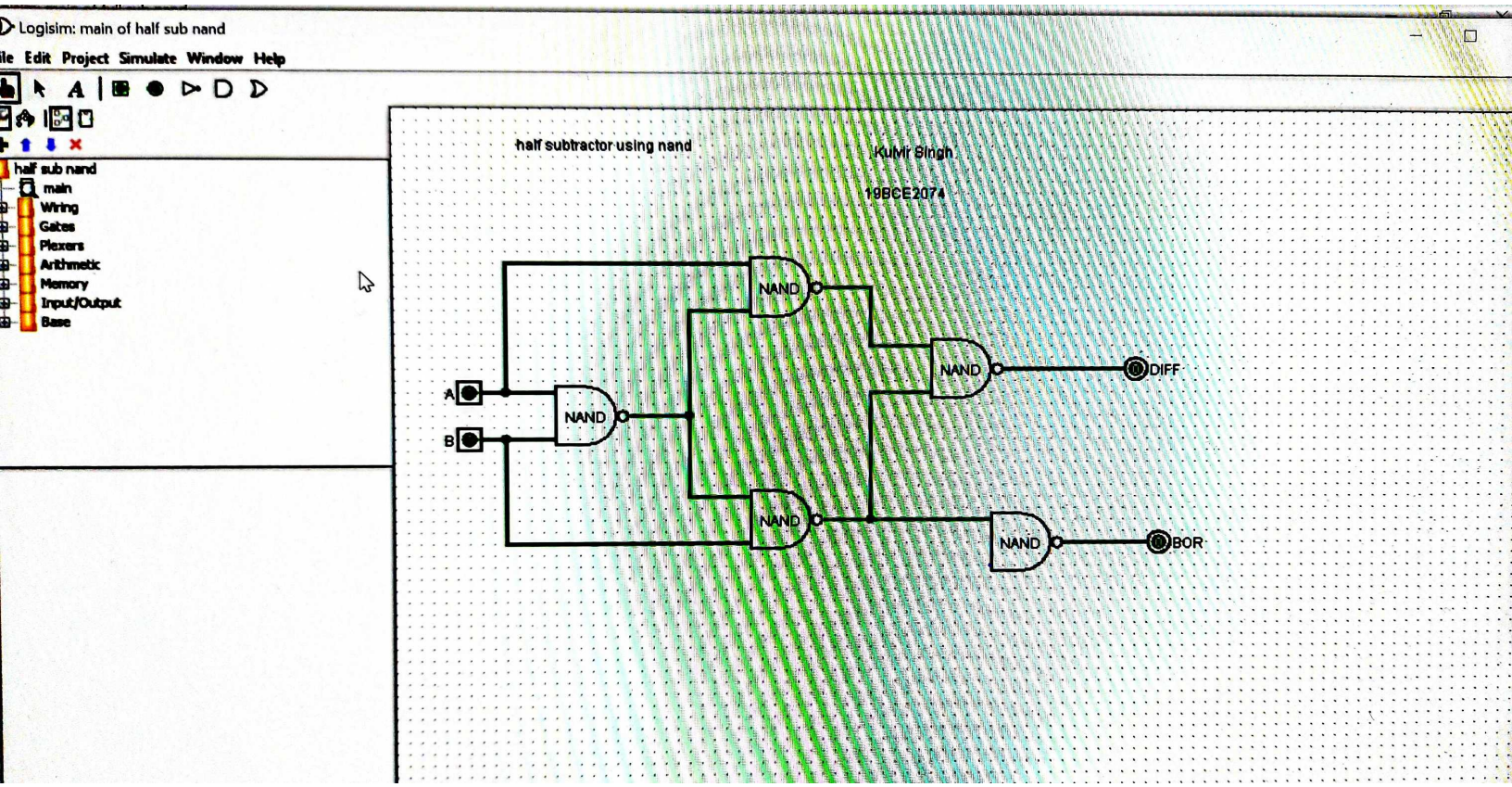
A	B	C	A ⊕ B ⊕ C	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

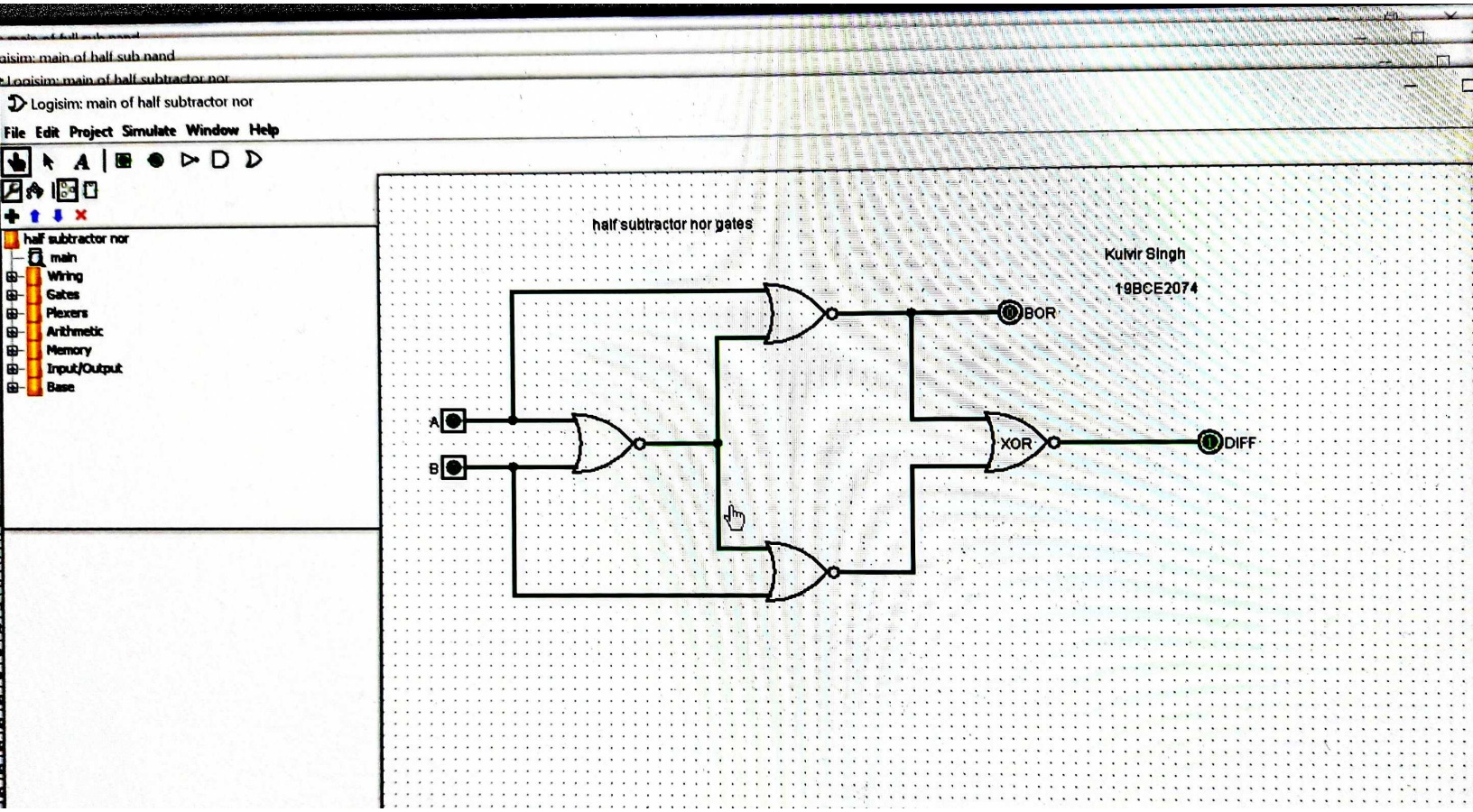
Half Subtractor using NAND



Half Subtractor using NOR



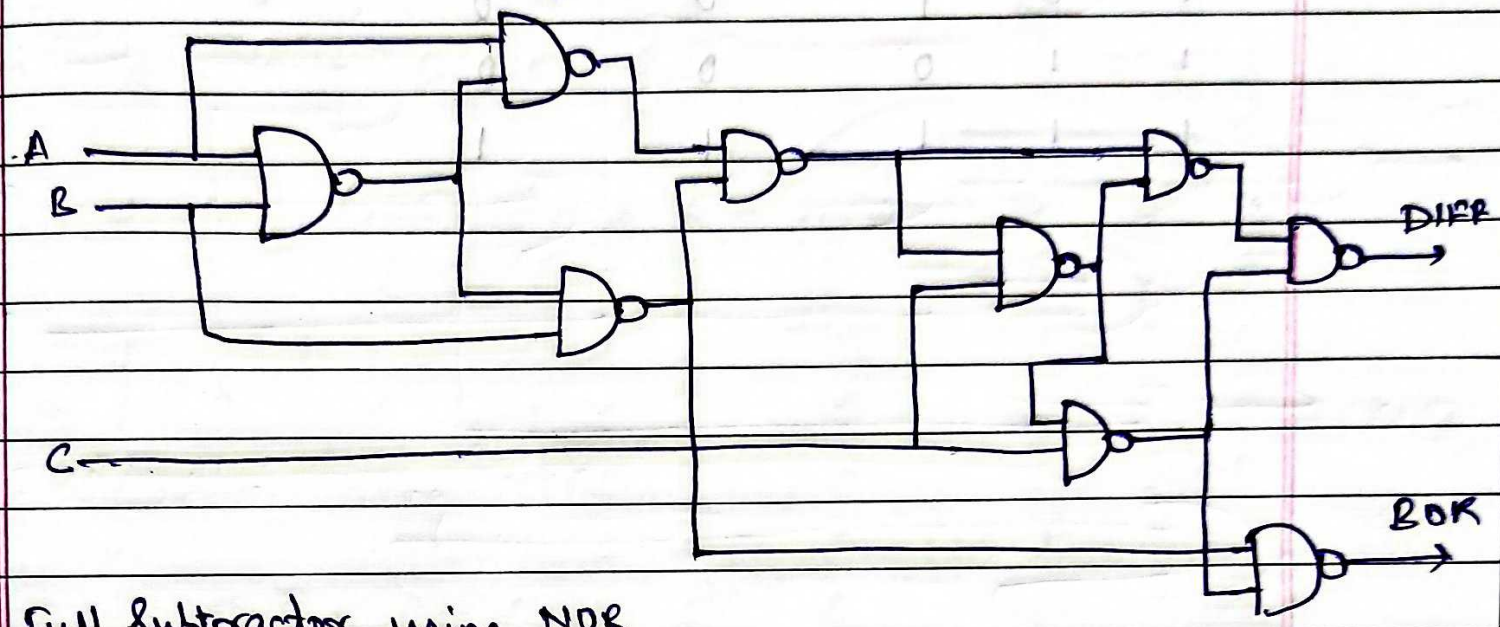

Logisim: main of half sub nand
File Edit Project Simulate Window Help
half sub nand
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
half subtractor using nand
Kulvir Singh
19BCE2074
A
B
NAND
NAND
NAND
NAND
NAND
DIFF
BOR


aisim: main of half sub nand
Logisim: main of half subtractor nor
Logisim: main of half subtractor nor
File Edit Project Simulate Window Help
half subtractor nor
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
half subtractor nor gates
Kulvir Singh
19BCE2074
A
B
BOR
XOR
DIFF

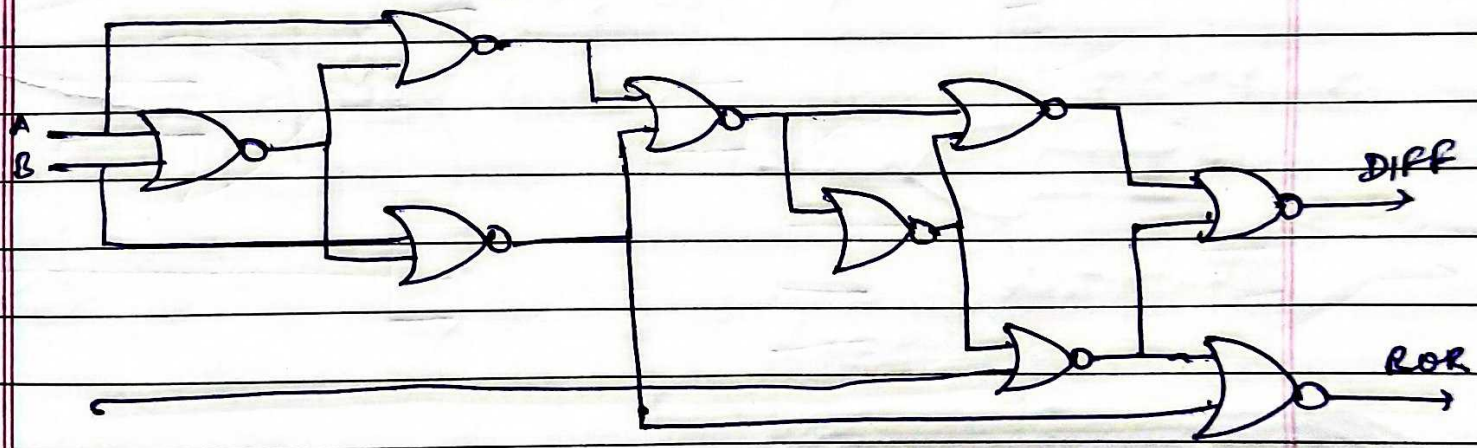
Truth Table.

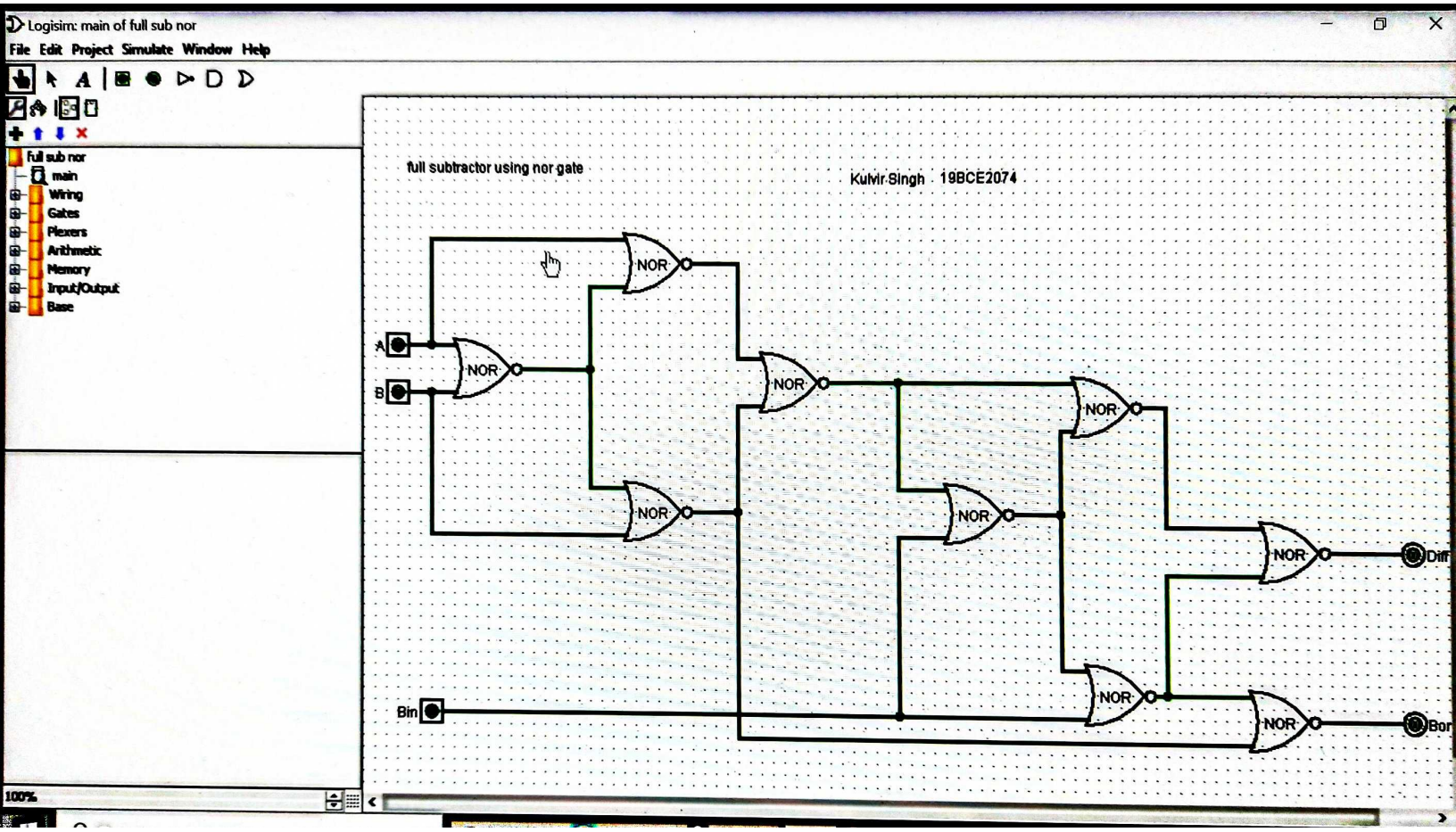
A	B	DIFF	BOR
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

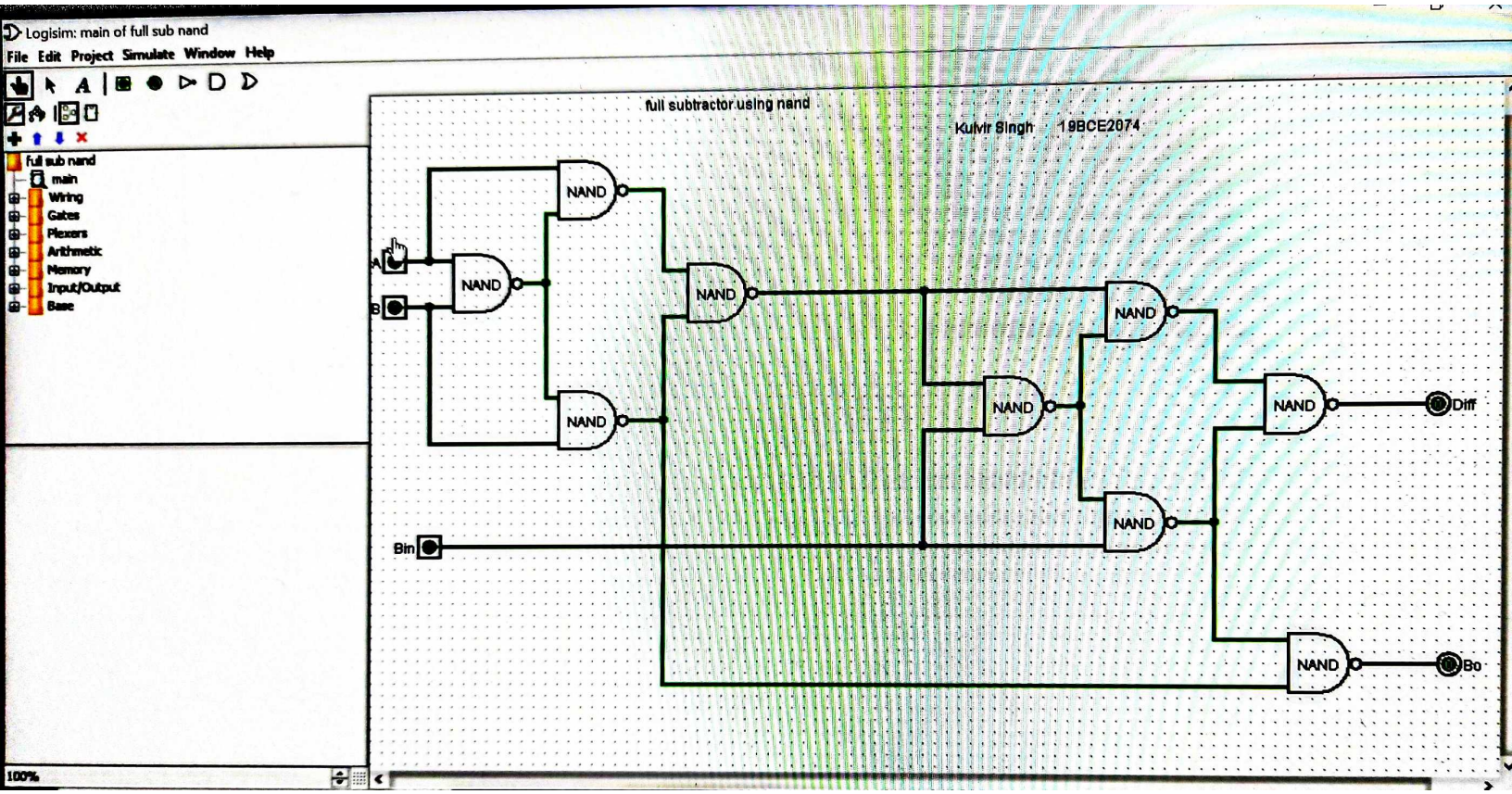
Full Subtractor using NAND



Full Subtractor using NOR




Logisim: main of full sub nor
File Edit Project Simulate Window Help
Full sub nor
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
full subtractor using nor gate
Kulvir Singh 19BCE2074
A
B
Bin
NOR
Diff
Bor
100%


Logisim: main of full sub nand
File Edit Project Simulate Window Help
full sub nand
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
100%
full subtractor using nand
Kulvir Singh 19BCE2074
NAND
NAND
NAND
NAND
NAND
NAND
NAND
NAND
B
Bin
Diff
Bo

a

Truth Table

A	B	C	DIFF	BOR
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1