Ex. No.:4

Design of Half Adder Circuit using gates

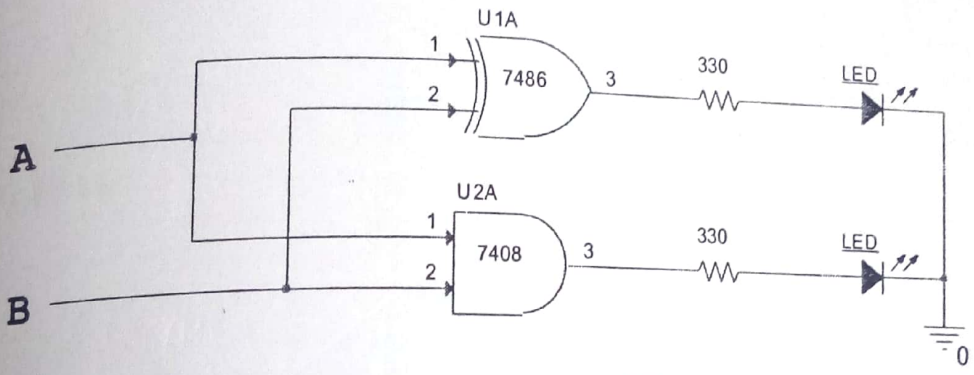
Date: 29.8.19

Aim: To verify the truth tables for half adder circuit using logic gates

Apparatus Required:

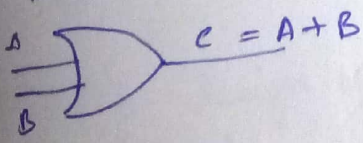
S. No.	Name of the apparatus	Range / Type	Quantity
1	7486 gate	-	1 No.
2	7408 gate	-	1 No.
3	LED	-	2 Nos.
4	RPS	0 – 15 V	1 No.
5	Resistor	330 Ω	2 Nos.
6	Breadboard	-	1 No.
7	Wires	-	Few

Circuit Diagram:

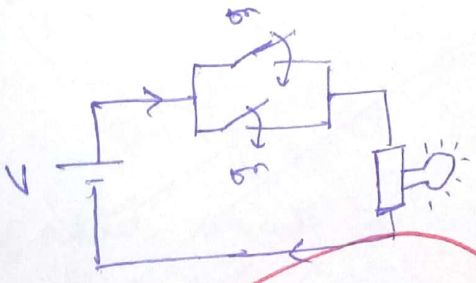


Theory: Logic Gates

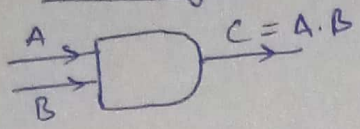
OR-gate



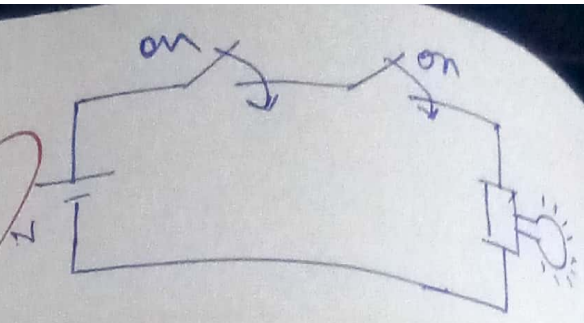
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1



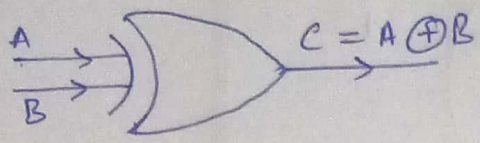
AND - gate



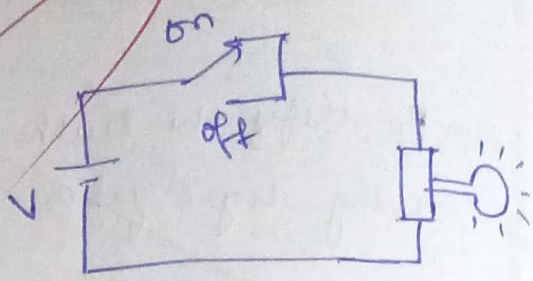
A	B	C
0	0	0
0	1	0
0	0	0
1	0	0
1	1	1



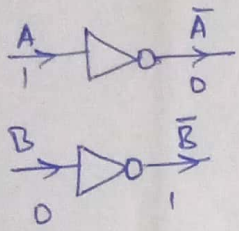
XOR - gate



A	B	C
0	0	0
0	1	1
1	0	1
1	1	0



NOT - gate



$\bar{1} = 0$

$\bar{0} = 1$

Truth Table

A	B	S=A⊕B	C=A.B
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Observation:

Procedure:

29/08/19
Verified

Result: The design of half adder circuit has been verified with truth tables

Reg. No: 19BCE2074 Name: Kulvir Singh Date: 29.8.19