Experiment No. : 10
Date : 03– 06 – 2020
Name: Kulvir Singh
Reg. No: 19BCE2074

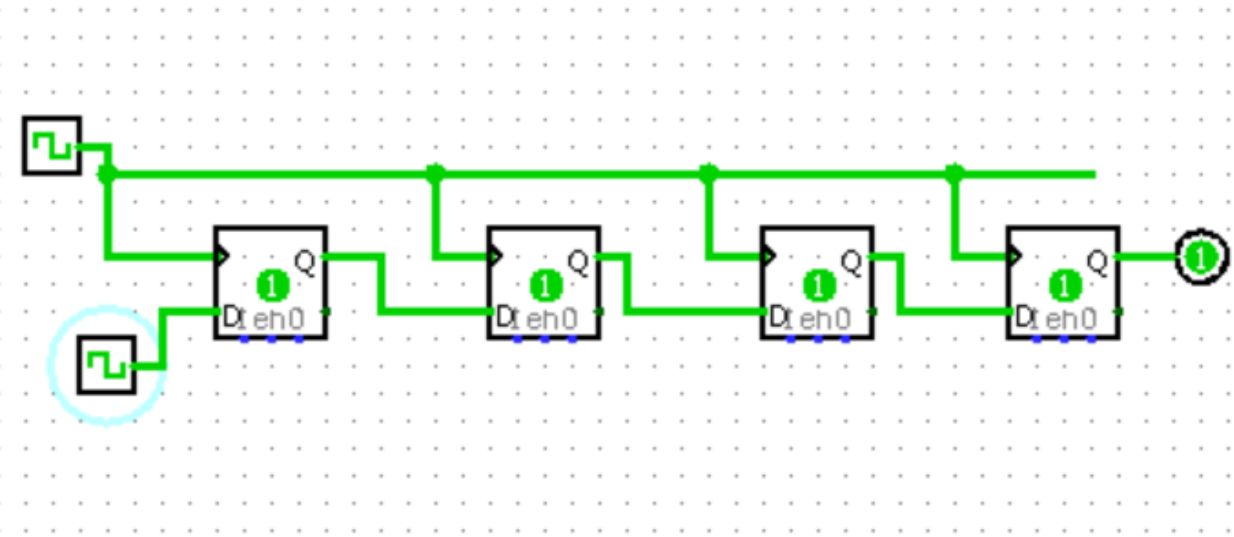
SERIAL IN SERIAL OUT USING D FLIP-FLOP

EXPERIMENTAL SCENARIO:

Truth Table

Clock Pulse	Q1	Q2	Q3	Q4
0	0	0	0	1
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1

Execution Snapshot:



Conclusion Remarks:

The above circuit has produced the truth table during simulation and has correct output for both parts.