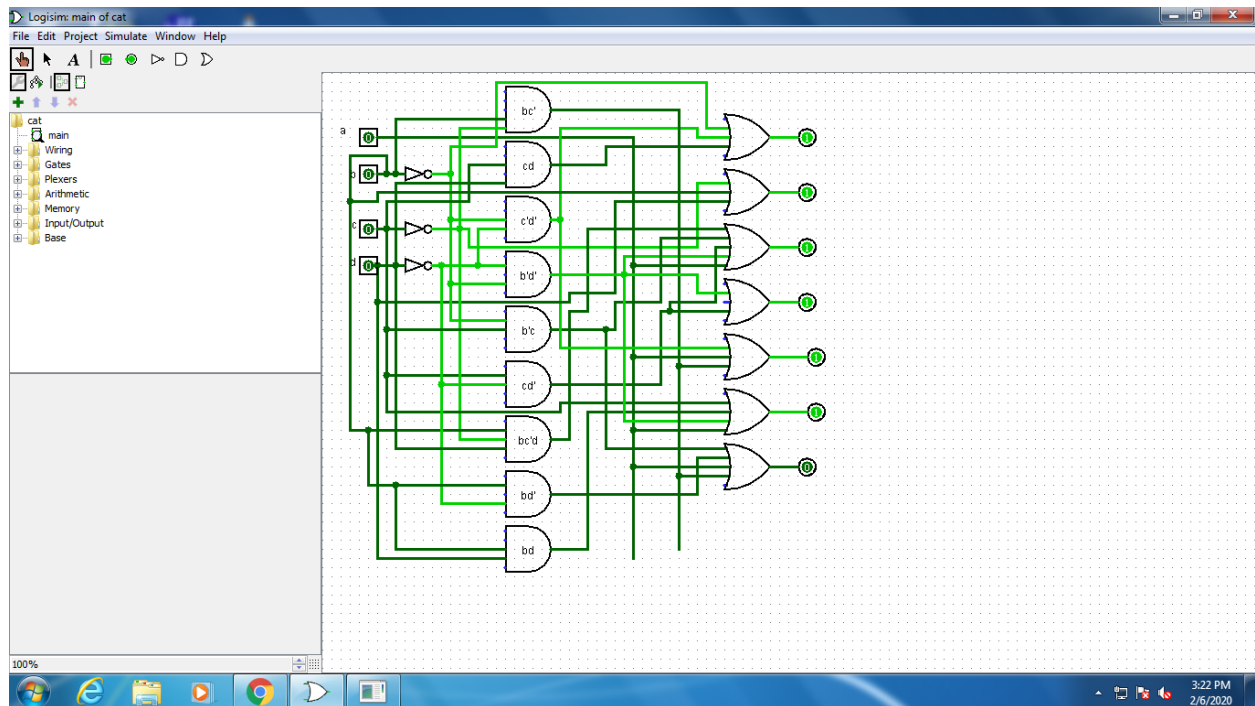


19BCE2074

Kulvir Singh



Combinational Analysis

File Edit Project Simulate Window Help

Inputs Outputs Table Expression Minimized

a	b	c	d	x	y	z	u	v	w	s
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	1	1	0	0	0	0	0
0	0	1	0	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	0	1	1
0	1	0	0	0	1	0	0	1	0	1
0	1	0	1	0	1	1	0	1	1	1
0	1	1	0	0	1	1	1	0	1	1
0	1	1	1	1	1	0	0	0	1	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	0	1	0	1	1	1	1	1
1	0	1	1	1	1	1	0	1	1	1
1	1	0	0	0	1	1	0	1	1	1
1	1	0	1	0	1	1	0	1	1	1
1	1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	0	1	1	1

Build Circuit

3:23 PM
2/6/2020

