Experiment No. : 9
Date : 03 – 06 – 2020

FLIP-FLOPS

AIM:
Implement and Verify the state tables of R-S flip-flop, D Flip-Flop Using NAND and NOR gates.
a. Determine the logic operation of the flip flops.
b. Connect and observe the state transition of each flip flops
c. Create the truth table to derive the Boolean equation
d. Construct the logic circuit using Altera Quartus II or Logisim.

EXPERIMENTAL SCENARIO:

i) RS Flip flop:

Truth Table:

Clock	S	R	Q(n+1)(Next State)
0	X	X	Q(n)(current state)
1	0	0	Q(n)
1	0	1	0
1	1	0	1
1	1	1	Invalid

Characteristic table of RS Flip flop:

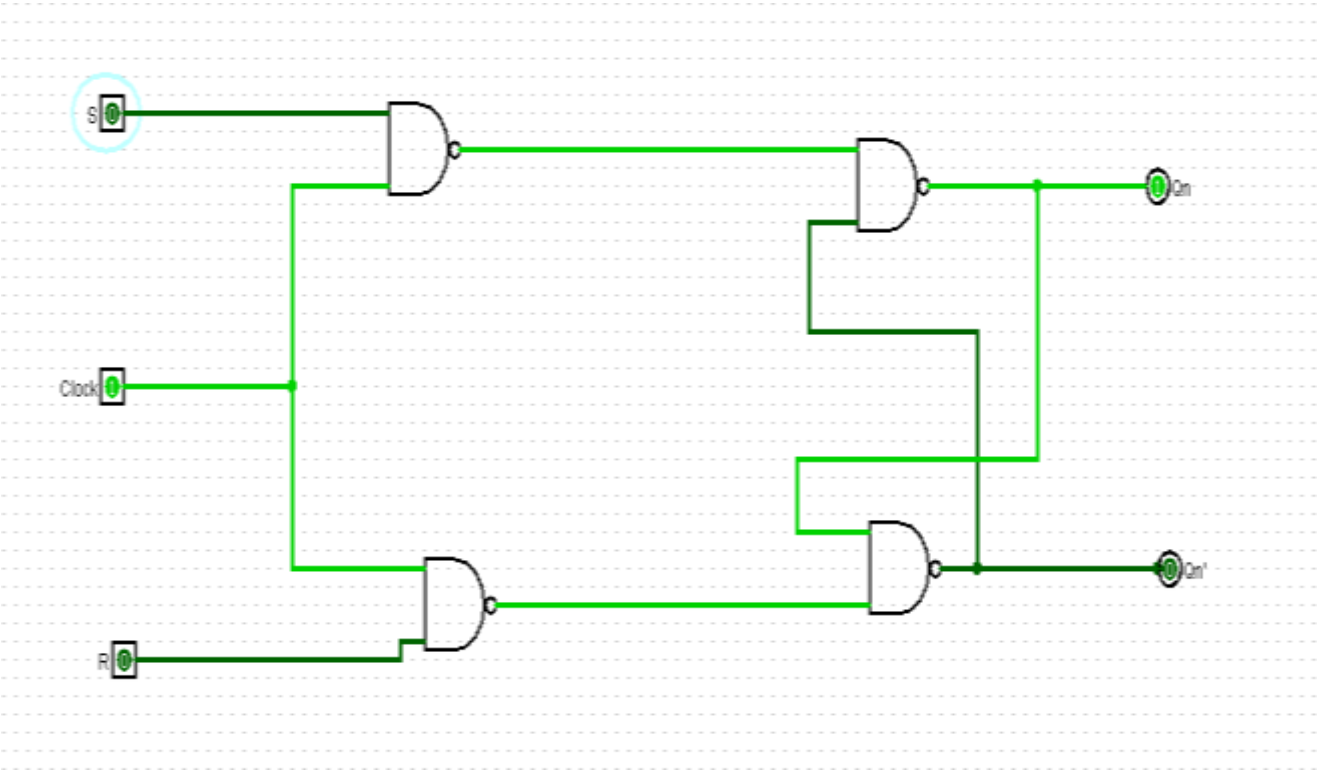
Qn	S	R	QN
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	x
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	x

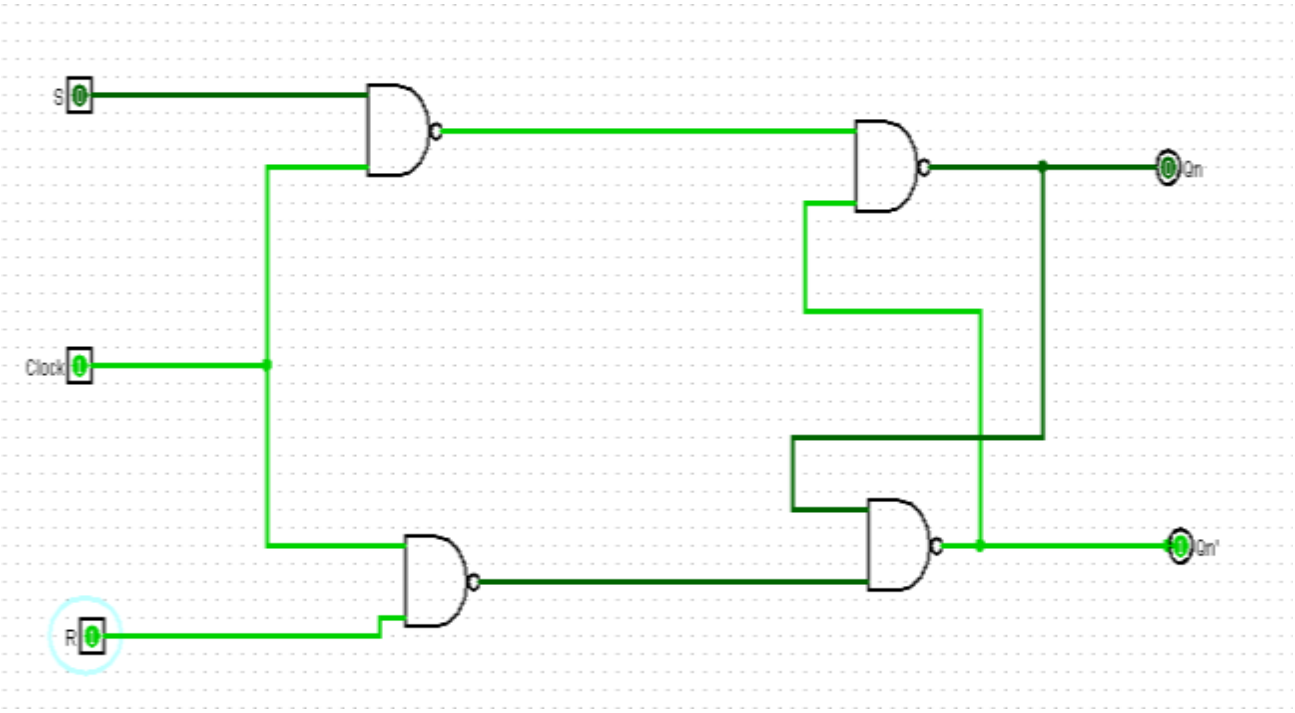
***Here QN represents Q(n+1) which implies the next state of the flip flop.**

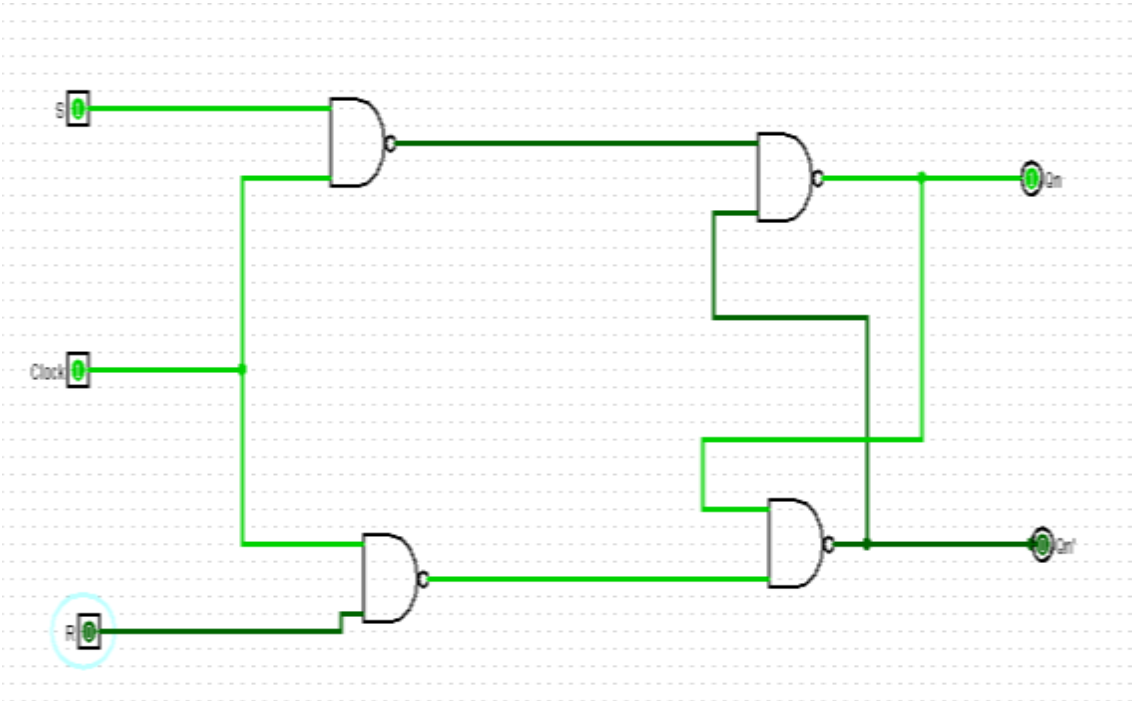
Boolean Equation:

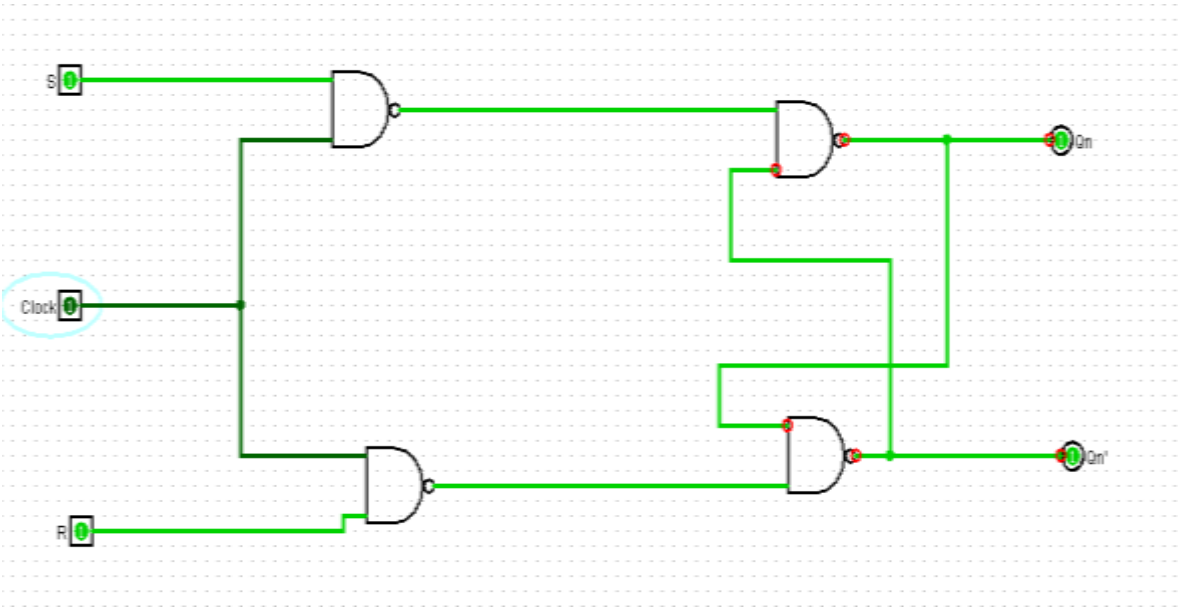
Q(n+1)=S+Q(n)

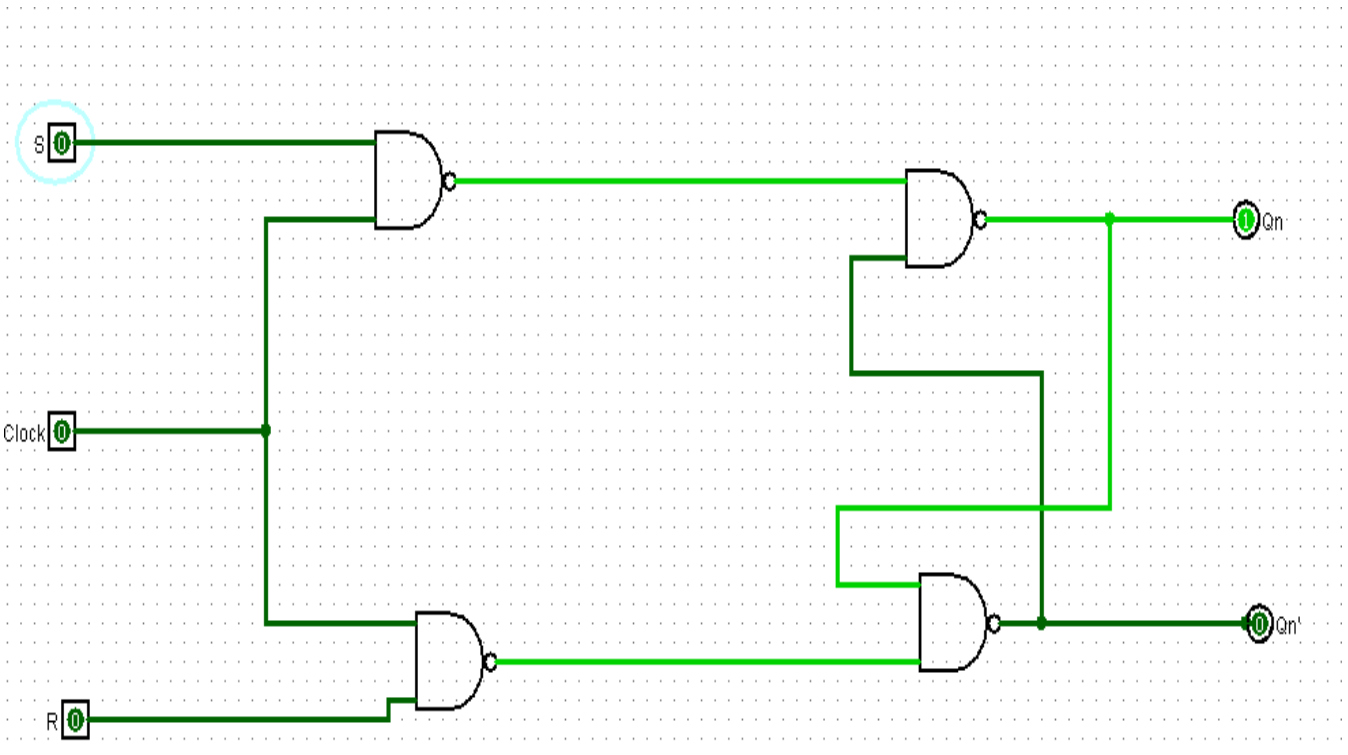
RTL Viewer




S
Clock
R
Qn
Qn'


S
Clock
R
Qn
Qn'





ii) D flip flop:

Truth Table:

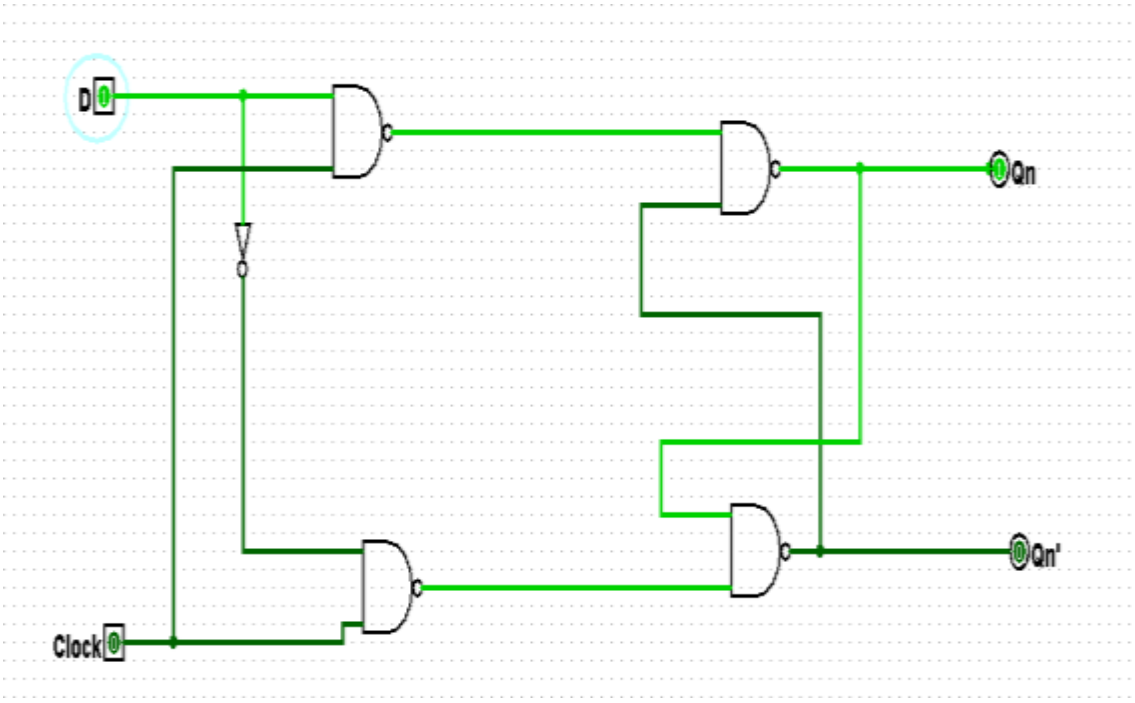
Clock	D	Qn+1	(Qn+1)’
0	0	Qn	Qn’
0	1	Qn	Qn’
1	0	0	1
1	1	1	0

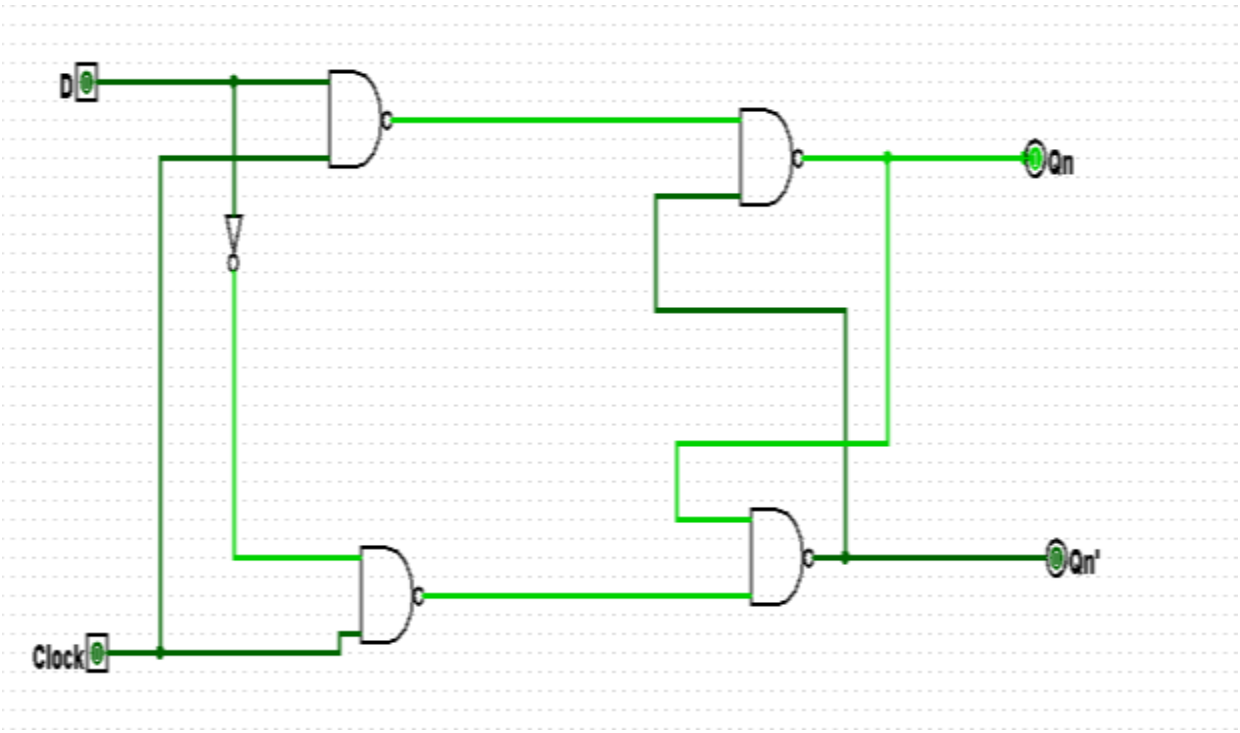
Characteristic Table:

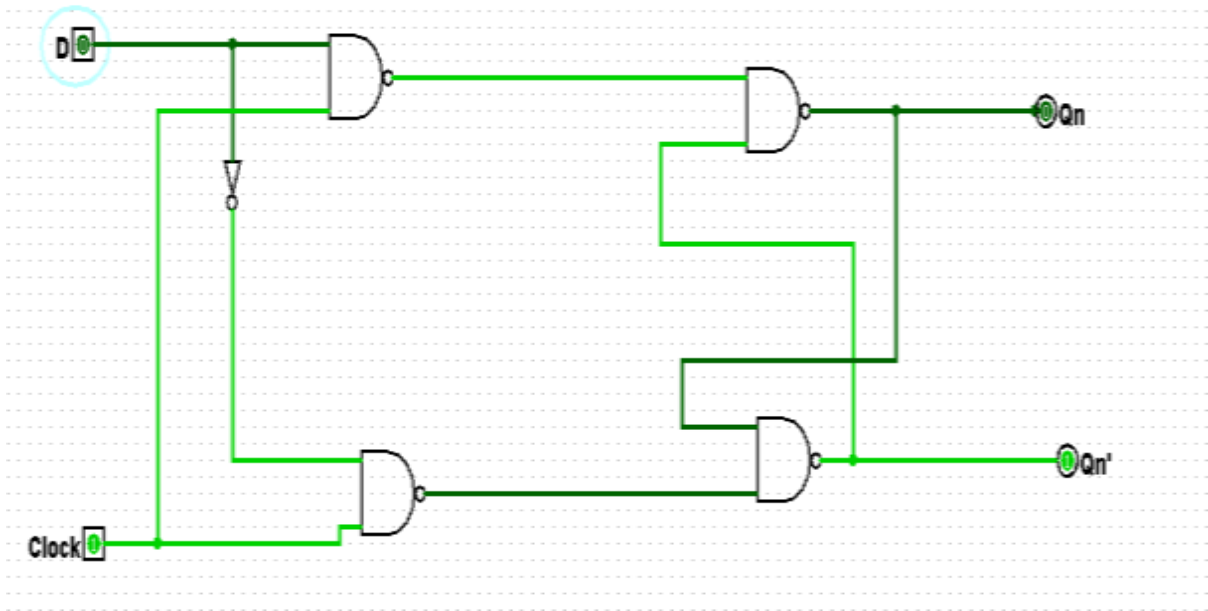
Qn	D	QN
0	0	0
0	1	1
1	0	0
1	1	1

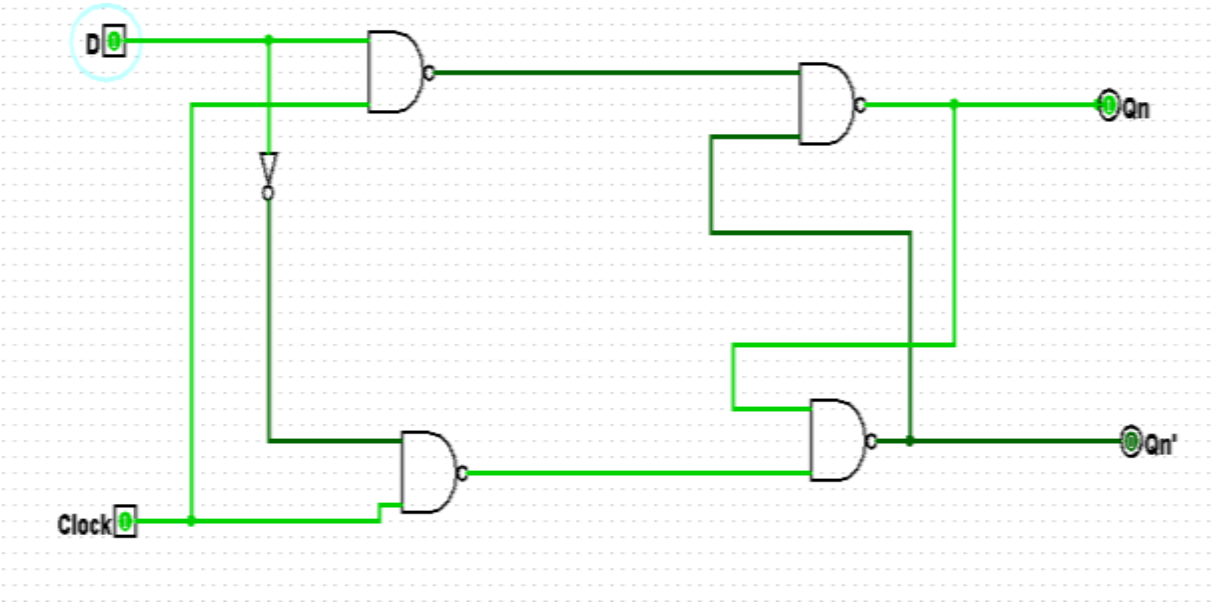
***Here QN represents Q(n+1) which implies the next state of the flip flop.**

RTL Viewer:


D
Qn
Qn'
Clock


D
Qn
Qn'
Clock


D
Qn
Qn'
Clock



Boolean Equation:

Q(n)= Clock(D)
Q(n+1)= ~Clock+ ~D

Conclusion Remarks: Thus the circuit helps us to see the function of SR Flip flop and D Flip flop.

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