

SSD1289

Advance Information

240 RGB x 320 TFT LCD Controller Driver integrated Power Circuit, Gate and Source Driver with built-in RAM

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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SSD1289

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1 GENERAL DESCRIPTION

SSD1289 is an all in one TFT LCD Controller Driver that integrated the RAM, power circuits, gate driver and source driver into a single chip. It can drive up to 262k color amorphous TFT panel with resolution of 240 RGB x 320.

It also integrated the controller function and consists of 172,800 bytes (240 x 320 x 18 / 8) Graphic Display Data RAM (GDDRAM) such that it interfaced with common MPU through 8-/9-/16-/18-bit 6800-series / 8080-series compatible parallel interface or serial peripheral interface and stored the data in the GDDRAM. Auxiliary 18-/16-/6-bit video interface (VSYNC, HSYNC, DOTCLK, DEN) are integrated into SSD1289 for animation image display.

SSD1289 embeds DC-DC Converter and Voltage generator to provide all necessary voltage required by the driver with minimum external components. A Common Voltage Generation Circuit is included to drive the TFT-display counter electrode. An Integrated Gamma Control Circuit is also included that can be adjusted by software commands to provide maximum flexibility and optimal display quality.

SSD1289 can be operated down to 1.4V and provide different power save modes. It is suitable for any portable battery-driven applications requiring long operation period and compact size.

2 FEATURES

- 240RGBx320 single chip controller driver IC for 262k color amorphous TFT LCD
- Power Supply
 - VDDEXT = 1.4V – 3.6V (Internal Logic)
 - VDDIO = 1.4V – 3.6V (I/O Interface)
 - VCI = 2.5V – 3.6V (power supply for internal analog circuit)
- Output Voltages
 - Gate Driver:
 - VGH-GND = 9V ~ 15V
 - VGL-GND = -7 ~ -15V
 - VGH-VGL = 30Vp-p
 - Source Driver:
 - V0 – V63 = 0 – 5V
 - Typical Source Output Voltage variation: ± 10 mV
 - VCOM drive:
 - VCOMH = 3.0V ~ 5.0V
 - VCOML = -2.0V ~ -3.0V
 - VCOMHA = 5.5V
- System Interface
 - High-speed interface by 8-/9-/16-/18-bit 6800-series / 8080-series parallel ports
 - Serial Peripheral Interface (SPI)
 - Moving picture display interface
 - 6-/16-/18-bit RGB interface (DEN, DOTCLK, HSYNC, VSYNC, DB17-0)
 - VSYNC interface (system interface + VSYNC)
 - WSYNC interface (system interface + WSYNC)
- Support low power consumption:
 - Low voltage supply
 - Low current sleep mode
 - 8-color display mode for power saving
 - Charge sharing function for step-up circuits
- High-speed RAM addressing functions
 - RAM write synchronization function
 - Window address function
 - Display by RAM data and generic data selectively and simultaneously
 - Vertical scrolling function
 - Picture in Picture mode
 - Partial display mode
- Internal power supply circuit
 - Voltage generator
 - DC-DC converter up to 6x/-6x
- Built-in internal oscillator
- Internal GDDRAM capacity: 172800Byte
- Support Frame and Line inversion AC drive
- TFT storage capacitance: Cs on common and Cs on gate
- Support source and gate scan direction control
- Programmable gamma correction curve
- 4 Preset gamma correction curve
- Built-in Non Volatile Memory for VCOM calibration Display Size: 240 RGB x 320
- Support flexible arrangement of gate circuits on both sides of the glass substrate

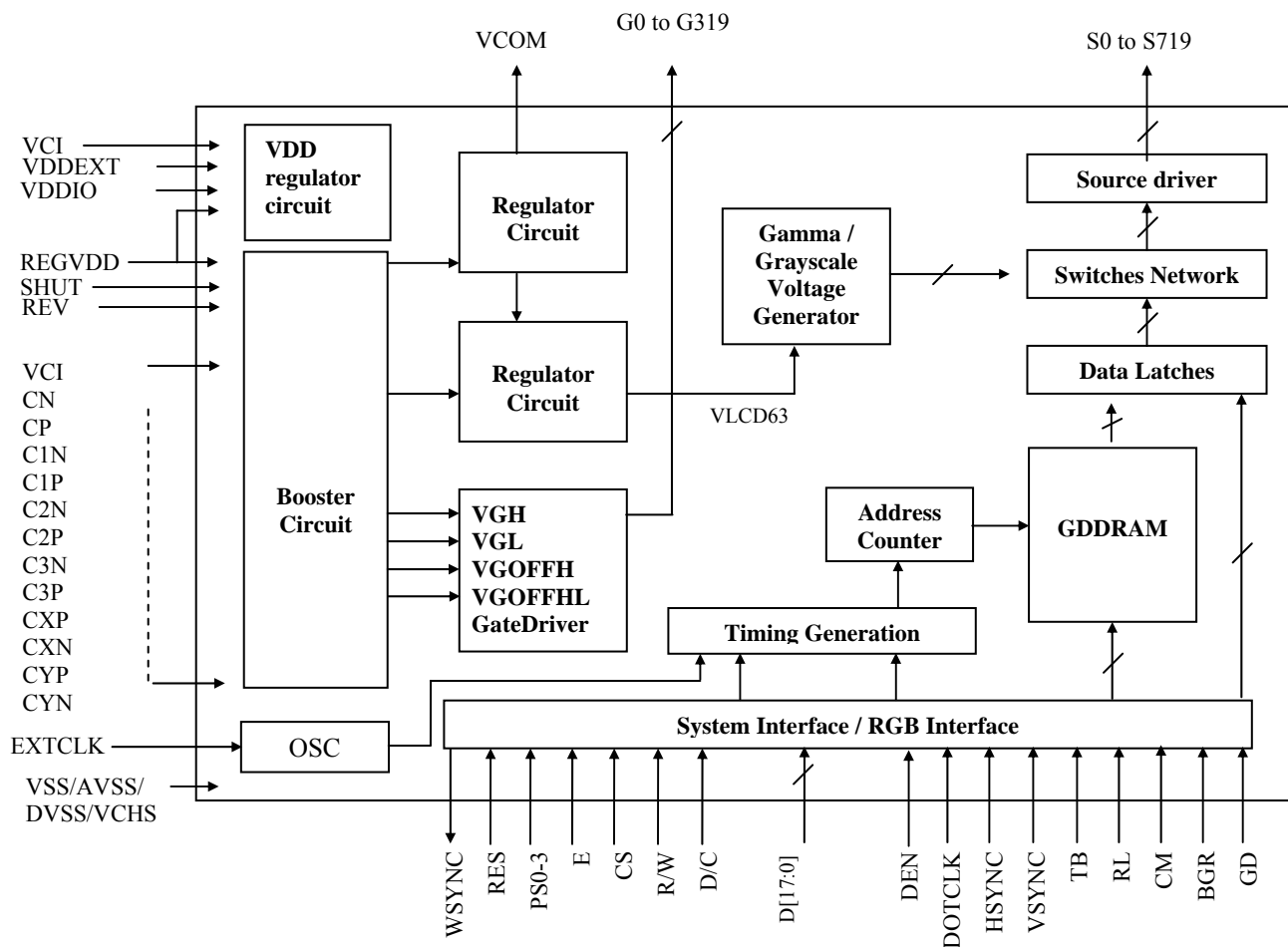
3 ORDERING INFORMATION

Table 3-1 – Ordering Information

| Ordering Part Number | Source | Gate | Package Form | Reference |
|-----------------------------|---------------|-------------|---------------------|------------------|
| SSD1289Z | 240 x 3 (720) | 320 | Gold Bump Die | |

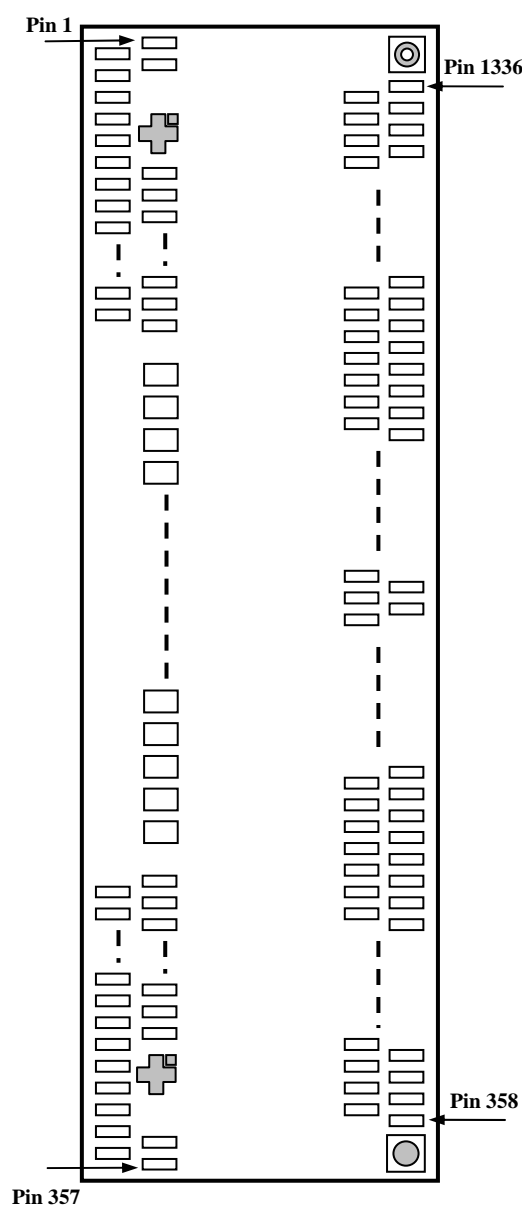
4 BLOCK DIAGRAM

Figure 4-1 - SSD1289 Block Diagram Description



5 DIE PAD FLOOR PLAN

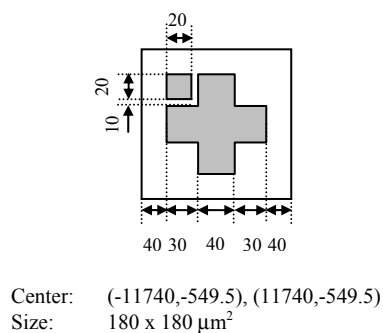
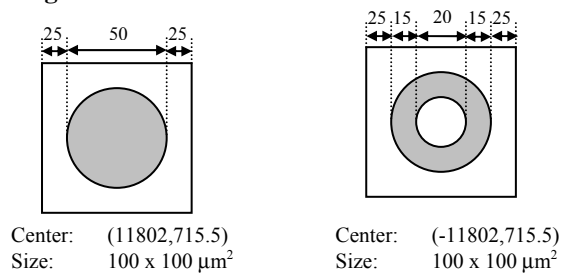
Figure 5-1 - SSD1289 Pad Arrangement (Bump face up)



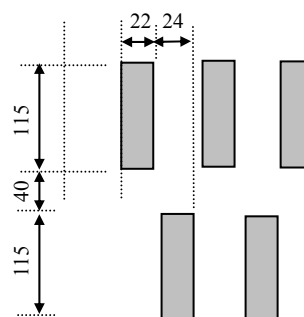
Note

- (1) Diagram showing the die face up.
- (2) Coordinates are referenced to center of the chip.
- (3) Coordinate units and size of all alignment marks are in μm .
- (4) All alignment keys do not contain gold bump.

Alignment Marks:



Output Pad Pitch (Gate and source):



| | |
|--------------------------------|--|
| Die Size | 23.984 x 1.600 mm ² |
| Die Thickness | 406 ± 25 μm |
| Typical Bump Height | 15 μm |
| Bump Co-planarity (within die) | ≤ 3 μm |
| Bump Size 1 | 55 x 117 μm^2 (Pin 58-300) |
| Pad Pitch 1 | 85 μm |
| Bump Size 2 | 22 x 115 μm^2 (Pin 1-57, 301-357, 358-1336) |
| Pad Pitch 2 | 24 μm stagger |

Table 5-1 - SSD1289 Bump Pad Coordinate (Bump Center)

Note: IC material temperature expansion factor is 2.6ppm, customer should take into account during panel design

| Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos |
|------|----------|--------|--------|------|--------|-------|--------|------|--------|-------|--------|
| 1 | NC | -11928 | -547.5 | 68 | C2N | -9435 | -701.5 | 135 | D17 | -3740 | -701.5 |
| 2 | NC | -11904 | -702.5 | 69 | C2N | -9350 | -701.5 | 136 | D16 | -3655 | -701.5 |
| 3 | NC | -11880 | -547.5 | 70 | C1P | -9265 | -701.5 | 137 | D16 | -3570 | -701.5 |
| 4 | NC | -11856 | -702.5 | 71 | C1P | -9180 | -701.5 | 138 | D15 | -3485 | -701.5 |
| 5 | NC | -11808 | -702.5 | 72 | C1N | -9095 | -701.5 | 139 | D15 | -3400 | -701.5 |
| 6 | NC | -11760 | -702.5 | 73 | C1N | -9010 | -701.5 | 140 | D14 | -3315 | -701.5 |
| 7 | NC | -11712 | -702.5 | 74 | CP | -8925 | -701.5 | 141 | D14 | -3230 | -701.5 |
| 8 | NC | -11664 | -702.5 | 75 | CP | -8840 | -701.5 | 142 | D13 | -3145 | -701.5 |
| 9 | THROUGH1 | -11640 | -547.5 | 76 | CN | -8755 | -701.5 | 143 | D13 | -3060 | -701.5 |
| 10 | THROUGH2 | -11616 | -702.5 | 77 | CN | -8670 | -701.5 | 144 | D12 | -2975 | -701.5 |
| 11 | G87 | -11592 | -547.5 | 78 | C3P | -8585 | -701.5 | 145 | D12 | -2890 | -701.5 |
| 12 | G85 | -11568 | -702.5 | 79 | C3P | -8500 | -701.5 | 146 | D11 | -2805 | -701.5 |
| 13 | G83 | -11544 | -547.5 | 80 | C3P | -8415 | -701.5 | 147 | D11 | -2720 | -701.5 |
| 14 | G81 | -11520 | -702.5 | 81 | C3P | -8330 | -701.5 | 148 | D10 | -2635 | -701.5 |
| 15 | G79 | -11496 | -547.5 | 82 | C3N | -8245 | -701.5 | 149 | D10 | -2550 | -701.5 |
| 16 | G77 | -11472 | -702.5 | 83 | C3N | -8160 | -701.5 | 150 | D9 | -2465 | -701.5 |
| 17 | G75 | -11448 | -547.5 | 84 | C3N | -8075 | -701.5 | 151 | D9 | -2380 | -701.5 |
| 18 | G73 | -11424 | -702.5 | 85 | C3N | -7990 | -701.5 | 152 | D8 | -2295 | -701.5 |
| 19 | G71 | -11400 | -547.5 | 86 | VCI | -7905 | -701.5 | 153 | D8 | -2210 | -701.5 |
| 20 | G69 | -11376 | -702.5 | 87 | VCI | -7820 | -701.5 | 154 | D7 | -2125 | -701.5 |
| 21 | G67 | -11352 | -547.5 | 88 | VCI | -7735 | -701.5 | 155 | D7 | -2040 | -701.5 |
| 22 | G65 | -11328 | -702.5 | 89 | VCI | -7650 | -701.5 | 156 | D6 | -1955 | -701.5 |
| 23 | G63 | -11304 | -547.5 | 90 | VGL | -7565 | -701.5 | 157 | D6 | -1870 | -701.5 |
| 24 | G61 | -11280 | -702.5 | 91 | VGL | -7480 | -701.5 | 158 | D5 | -1785 | -701.5 |
| 25 | G59 | -11256 | -547.5 | 92 | VCHS | -7395 | -701.5 | 159 | D5 | -1700 | -701.5 |
| 26 | G57 | -11232 | -702.5 | 93 | VCHS | -7310 | -701.5 | 160 | D4 | -1615 | -701.5 |
| 27 | G55 | -11208 | -547.5 | 94 | VCHS | -7225 | -701.5 | 161 | D4 | -1530 | -701.5 |
| 28 | G53 | -11184 | -702.5 | 95 | VDDIO | -7140 | -701.5 | 162 | D3 | -1445 | -701.5 |
| 29 | G51 | -11160 | -547.5 | 96 | GD | -7055 | -701.5 | 163 | D3 | -1360 | -701.5 |
| 30 | G49 | -11136 | -702.5 | 97 | VSS | -6970 | -701.5 | 164 | D2 | -1275 | -701.5 |
| 31 | G47 | -11112 | -547.5 | 98 | CAD | -6885 | -701.5 | 165 | D2 | -1190 | -701.5 |
| 32 | G45 | -11088 | -702.5 | 99 | VDDIO | -6800 | -701.5 | 166 | D1 | -1105 | -701.5 |
| 33 | G43 | -11064 | -547.5 | 100 | REV | -6715 | -701.5 | 167 | D1 | -1020 | -701.5 |
| 34 | G41 | -11040 | -702.5 | 101 | VSS | -6630 | -701.5 | 168 | D0 | -935 | -701.5 |
| 35 | G39 | -11016 | -547.5 | 102 | GAMAS0 | -6545 | -701.5 | 169 | D0 | -850 | -701.5 |
| 36 | G37 | -10992 | -702.5 | 103 | VDDIO | -6460 | -701.5 | 170 | /RD | -765 | -701.5 |
| 37 | G35 | -10968 | -547.5 | 104 | GAMAS1 | -6375 | -701.5 | 171 | /RD | -680 | -701.5 |
| 38 | G33 | -10944 | -702.5 | 105 | VSS | -6290 | -701.5 | 172 | /WR | -595 | -701.5 |
| 39 | G31 | -10920 | -547.5 | 106 | GAMAS2 | -6205 | -701.5 | 173 | /WR | -510 | -701.5 |
| 40 | G29 | -10896 | -702.5 | 107 | VDDIO | -6120 | -701.5 | 174 | DC | -425 | -701.5 |
| 41 | G27 | -10872 | -547.5 | 108 | BGR | -6035 | -701.5 | 175 | DC | -340 | -701.5 |
| 42 | G25 | -10848 | -702.5 | 109 | VSS | -5950 | -701.5 | 176 | SDO | -255 | -701.5 |
| 43 | G23 | -10824 | -547.5 | 110 | TB | -5865 | -701.5 | 177 | SDO | -170 | -701.5 |
| 44 | G21 | -10800 | -702.5 | 111 | VDDIO | -5780 | -701.5 | 178 | SDI | -85 | -701.5 |
| 45 | G19 | -10776 | -547.5 | 112 | RL | -5695 | -701.5 | 179 | SDI | 0 | -701.5 |
| 46 | G17 | -10752 | -702.5 | 113 | VSS | -5610 | -701.5 | 180 | SCK | 85 | -701.5 |
| 47 | G15 | -10728 | -547.5 | 114 | REGVDD | -5525 | -701.5 | 181 | SCK | 170 | -701.5 |
| 48 | G13 | -10704 | -702.5 | 115 | VDDIO | -5440 | -701.5 | 182 | /CS | 255 | -701.5 |
| 49 | G11 | -10680 | -547.5 | 116 | PS2 | -5355 | -701.5 | 183 | /CS | 340 | -701.5 |
| 50 | G9 | -10656 | -702.5 | 117 | VSS | -5270 | -701.5 | 184 | WSYNC | 425 | -701.5 |
| 51 | G7 | -10632 | -547.5 | 118 | PS1 | -5185 | -701.5 | 185 | WSYNC | 510 | -701.5 |
| 52 | G5 | -10608 | -702.5 | 119 | VDDIO | -5100 | -701.5 | 186 | TESTA | 595 | -701.5 |
| 53 | G3 | -10584 | -547.5 | 120 | PS0 | -5015 | -701.5 | 187 | TESTB | 680 | -701.5 |
| 54 | G1 | -10560 | -702.5 | 121 | PS3 | -4930 | -701.5 | 188 | TESTC | 765 | -701.5 |
| 55 | DUMMY | -10536 | -547.5 | 122 | SHUT | -4845 | -701.5 | 189 | EXTCLK | 850 | -701.5 |
| 56 | NC | -10512 | -702.5 | 123 | CM | -4760 | -701.5 | 190 | VREGC | 935 | -701.5 |
| 57 | NC | -10488 | -547.5 | 124 | /RES | -4675 | -701.5 | 191 | VREGC | 1020 | -701.5 |
| 58 | DUMMY | -10285 | -701.5 | 125 | /RES | -4590 | -701.5 | 192 | VCORE | 1105 | -701.5 |
| 59 | VCOM | -10200 | -701.5 | 126 | VSYN | -4505 | -701.5 | 193 | VCORE | 1190 | -701.5 |
| 60 | VCOM | -10115 | -701.5 | 127 | VSYN | -4420 | -701.5 | 194 | VREGR | 1275 | -701.5 |
| 61 | NC | -10030 | -701.5 | 128 | HSYN | -4335 | -701.5 | 195 | VREGR | 1360 | -701.5 |
| 62 | VGH | -9945 | -701.5 | 129 | HSYN | -4250 | -701.5 | 196 | VRAM | 1445 | -701.5 |
| 63 | VGH | -9860 | -701.5 | 130 | DOTCLK | -4165 | -701.5 | 197 | VRAM | 1530 | -701.5 |
| 64 | VGH | -9775 | -701.5 | 131 | DOTCLK | -4080 | -701.5 | 198 | VDDEXT | 1615 | -701.5 |
| 65 | VGH | -9690 | -701.5 | 132 | DEN | -3995 | -701.5 | 199 | VDDEXT | 1700 | -701.5 |
| 66 | C2P | -9605 | -701.5 | 133 | DEN | -3910 | -701.5 | 200 | VDDEXT | 1785 | -701.5 |
| 67 | C2P | -9520 | -701.5 | 134 | D17 | -3825 | -701.5 | 201 | VDDEXT | 1870 | -701.5 |

| Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos |
|------|---------|-------|--------|------|--------|-------|--------|------|----------|-------|--------|
| 202 | VSSRC | 1955 | -701.5 | 269 | VCIX2 | 7650 | -701.5 | 336 | G64 | 11328 | -702.5 |
| 203 | VSSRC | 2040 | -701.5 | 270 | CYP | 7735 | -701.5 | 337 | G66 | 11352 | -547.5 |
| 204 | CDUM0 | 2125 | -701.5 | 271 | CYP | 7820 | -701.5 | 338 | G68 | 11376 | -702.5 |
| 205 | CDUM0 | 2210 | -701.5 | 272 | CYP | 7905 | -701.5 | 339 | G70 | 11400 | -547.5 |
| 206 | CDUM1 | 2295 | -701.5 | 273 | CYP | 7990 | -701.5 | 340 | G72 | 11424 | -702.5 |
| 207 | CDUM1 | 2380 | -701.5 | 274 | CYP | 8075 | -701.5 | 341 | G74 | 11448 | -547.5 |
| 208 | VSS | 2465 | -701.5 | 275 | CYP | 8160 | -701.5 | 342 | G76 | 11472 | -702.5 |
| 209 | VSS | 2550 | -701.5 | 276 | CYN | 8245 | -701.5 | 343 | G78 | 11496 | -547.5 |
| 210 | VSS | 2635 | -701.5 | 277 | CYN | 8330 | -701.5 | 344 | G80 | 11520 | -702.5 |
| 211 | VSS | 2720 | -701.5 | 278 | CYN | 8415 | -701.5 | 345 | G82 | 11544 | -547.5 |
| 212 | VSS | 2805 | -701.5 | 279 | CYN | 8500 | -701.5 | 346 | G84 | 11568 | -702.5 |
| 213 | VSS | 2890 | -701.5 | 280 | CYN | 8585 | -701.5 | 347 | G86 | 11592 | -547.5 |
| 214 | VSS | 2975 | -701.5 | 281 | CYN | 8670 | -701.5 | 348 | THROUGH3 | 11616 | -702.5 |
| 215 | VSS | 3060 | -701.5 | 282 | VCHS | 8755 | -701.5 | 349 | THROUGH4 | 11640 | -547.5 |
| 216 | AVSS | 3145 | -701.5 | 283 | VCHS | 8840 | -701.5 | 350 | NC | 11664 | -702.5 |
| 217 | AVSS | 3230 | -701.5 | 284 | VCHS | 8925 | -701.5 | 351 | NC | 11712 | -702.5 |
| 218 | AVSS | 3315 | -701.5 | 285 | VCHS | 9010 | -701.5 | 352 | NC | 11760 | -702.5 |
| 219 | AVSS | 3400 | -701.5 | 286 | VCHS | 9095 | -701.5 | 353 | NC | 11808 | -702.5 |
| 220 | AVSS | 3485 | -701.5 | 287 | VCHS | 9180 | -701.5 | 354 | NC | 11856 | -702.5 |
| 221 | AVSS | 3570 | -701.5 | 288 | CXN | 9265 | -701.5 | 355 | NC | 11880 | -547.5 |
| 222 | VDDIO | 3655 | -701.5 | 289 | CXN | 9350 | -701.5 | 356 | NC | 11904 | -702.5 |
| 223 | VDDIO | 3740 | -701.5 | 290 | CXN | 9435 | -701.5 | 357 | NC | 11928 | -547.5 |
| 224 | VDDIO | 3825 | -701.5 | 291 | CXP | 9520 | -701.5 | 358 | DUMMY | 11736 | 702.5 |
| 225 | VDDIO | 3910 | -701.5 | 292 | CXP | 9605 | -701.5 | 359 | VGL | 11712 | 547.5 |
| 226 | VCI | 3995 | -701.5 | 293 | CXP | 9690 | -701.5 | 360 | DUMMY | 11688 | 702.5 |
| 227 | VCI | 4080 | -701.5 | 294 | VGOFFH | 9775 | -701.5 | 361 | DUMMY | 11664 | 547.5 |
| 228 | VCI | 4165 | -701.5 | 295 | VGOFFH | 9860 | -701.5 | 362 | THROUGH5 | 11640 | 702.5 |
| 229 | VCI | 4250 | -701.5 | 296 | VCOM | 9945 | -701.5 | 363 | THROUGH6 | 11616 | 547.5 |
| 230 | VCI | 4335 | -701.5 | 297 | VCOM | 10030 | -701.5 | 364 | G88 | 11592 | 702.5 |
| 231 | VCI | 4420 | -701.5 | 298 | VCOM | 10115 | -701.5 | 365 | G90 | 11568 | 547.5 |
| 232 | VCIP | 4505 | -701.5 | 299 | VCOM | 10200 | -701.5 | 366 | G92 | 11544 | 702.5 |
| 233 | VCIP | 4590 | -701.5 | 300 | VCOMR | 10285 | -701.5 | 367 | G94 | 11520 | 547.5 |
| 234 | VCIP | 4675 | -701.5 | 301 | NC | 10488 | -547.5 | 368 | G96 | 11496 | 702.5 |
| 235 | VCIP | 4760 | -701.5 | 302 | NC | 10512 | -702.5 | 369 | G98 | 11472 | 547.5 |
| 236 | VGOFFHL | 4845 | -701.5 | 303 | GTESTR | 10536 | -547.5 | 370 | G100 | 11448 | 702.5 |
| 237 | VGOFFHL | 4930 | -701.5 | 304 | G0 | 10560 | -702.5 | 371 | G102 | 11424 | 547.5 |
| 238 | NC | 5015 | -701.5 | 305 | G2 | 10584 | -547.5 | 372 | G104 | 11400 | 702.5 |
| 239 | NC | 5100 | -701.5 | 306 | G4 | 10608 | -702.5 | 373 | G106 | 11376 | 547.5 |
| 240 | VLCD63 | 5185 | -701.5 | 307 | G6 | 10632 | -547.5 | 374 | G108 | 11352 | 702.5 |
| 241 | VLCD63 | 5270 | -701.5 | 308 | G8 | 10656 | -702.5 | 375 | G110 | 11328 | 547.5 |
| 242 | VLCD63 | 5355 | -701.5 | 309 | G10 | 10680 | -547.5 | 376 | G112 | 11304 | 702.5 |
| 243 | VLCD63 | 5440 | -701.5 | 310 | G12 | 10704 | -702.5 | 377 | G114 | 11280 | 547.5 |
| 244 | VCOML | 5525 | -701.5 | 311 | G14 | 10728 | -547.5 | 378 | G116 | 11256 | 702.5 |
| 245 | VCOML | 5610 | -701.5 | 312 | G16 | 10752 | -702.5 | 379 | G118 | 11232 | 547.5 |
| 246 | VCOML | 5695 | -701.5 | 313 | G18 | 10776 | -547.5 | 380 | G120 | 11208 | 702.5 |
| 247 | VCOML | 5780 | -701.5 | 314 | G20 | 10800 | -702.5 | 381 | G122 | 11184 | 547.5 |
| 248 | VCOMH | 5865 | -701.5 | 315 | G22 | 10824 | -547.5 | 382 | G124 | 11160 | 702.5 |
| 249 | VCOMH | 5950 | -701.5 | 316 | G24 | 10848 | -702.5 | 383 | G126 | 11136 | 547.5 |
| 250 | VCOMH | 6035 | -701.5 | 317 | G26 | 10872 | -547.5 | 384 | G128 | 11112 | 702.5 |
| 251 | VCOMH | 6120 | -701.5 | 318 | G28 | 10896 | -702.5 | 385 | G130 | 11088 | 547.5 |
| 252 | VCIM | 6205 | -701.5 | 319 | G30 | 10920 | -547.5 | 386 | G132 | 11064 | 702.5 |
| 253 | VCIM | 6290 | -701.5 | 320 | G32 | 10944 | -702.5 | 387 | G134 | 11040 | 547.5 |
| 254 | VCIM | 6375 | -701.5 | 321 | G34 | 10968 | -547.5 | 388 | G136 | 11016 | 702.5 |
| 255 | VCIM | 6460 | -701.5 | 322 | G36 | 10992 | -702.5 | 389 | G138 | 10992 | 547.5 |
| 256 | NC | 6545 | -701.5 | 323 | G38 | 11016 | -547.5 | 390 | G140 | 10968 | 702.5 |
| 257 | NC | 6630 | -701.5 | 324 | G40 | 11040 | -702.5 | 391 | G142 | 10944 | 547.5 |
| 258 | VCI | 6715 | -701.5 | 325 | G42 | 11064 | -547.5 | 392 | G144 | 10920 | 702.5 |
| 259 | VCI | 6800 | -701.5 | 326 | G44 | 11088 | -702.5 | 393 | G146 | 10896 | 547.5 |
| 260 | VCI | 6885 | -701.5 | 327 | G46 | 11112 | -547.5 | 394 | G148 | 10872 | 702.5 |
| 261 | VCI | 6970 | -701.5 | 328 | G48 | 11136 | -702.5 | 395 | G150 | 10848 | 547.5 |
| 262 | VCIX2J | 7055 | -701.5 | 329 | G50 | 11160 | -547.5 | 396 | G152 | 10824 | 702.5 |
| 263 | VCIX2J | 7140 | -701.5 | 330 | G52 | 11184 | -702.5 | 397 | G154 | 10800 | 547.5 |
| 264 | VCIX2G | 7225 | -701.5 | 331 | G54 | 11208 | -547.5 | 398 | G156 | 10776 | 702.5 |
| 265 | VCIX2G | 7310 | -701.5 | 332 | G56 | 11232 | -702.5 | 399 | G158 | 10752 | 547.5 |
| 266 | VCIX2 | 7395 | -701.5 | 333 | G58 | 11256 | -547.5 | 400 | G160 | 10728 | 702.5 |
| 267 | VCIX2 | 7480 | -701.5 | 334 | G60 | 11280 | -702.5 | 401 | G162 | 10704 | 547.5 |
| 268 | VCIX2 | 7565 | -701.5 | 335 | G62 | 11304 | -547.5 | 402 | G164 | 10680 | 702.5 |

| Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos |
|------|--------|-------|-------|------|--------|-------|-------|------|--------|-------|-------|
| 403 | G166 | 10656 | 547.5 | 470 | G300 | 9048 | 702.5 | 537 | S669 | 7440 | 547.5 |
| 404 | G168 | 10632 | 702.5 | 471 | G302 | 9024 | 547.5 | 538 | S668 | 7416 | 702.5 |
| 405 | G170 | 10608 | 547.5 | 472 | G304 | 9000 | 702.5 | 539 | S667 | 7392 | 547.5 |
| 406 | G172 | 10584 | 702.5 | 473 | G306 | 8976 | 547.5 | 540 | S666 | 7368 | 702.5 |
| 407 | G174 | 10560 | 547.5 | 474 | G308 | 8952 | 702.5 | 541 | S665 | 7344 | 547.5 |
| 408 | G176 | 10536 | 702.5 | 475 | G310 | 8928 | 547.5 | 542 | S664 | 7320 | 702.5 |
| 409 | G178 | 10512 | 547.5 | 476 | G312 | 8904 | 702.5 | 543 | S663 | 7296 | 547.5 |
| 410 | G180 | 10488 | 702.5 | 477 | G314 | 8880 | 547.5 | 544 | S662 | 7272 | 702.5 |
| 411 | G182 | 10464 | 547.5 | 478 | G316 | 8856 | 702.5 | 545 | S661 | 7248 | 547.5 |
| 412 | G184 | 10440 | 702.5 | 479 | G318 | 8832 | 547.5 | 546 | S660 | 7224 | 702.5 |
| 413 | G186 | 10416 | 547.5 | 480 | DUMMY | 8808 | 702.5 | 547 | S659 | 7200 | 547.5 |
| 414 | G188 | 10392 | 702.5 | 481 | DUMMY | 8784 | 547.5 | 548 | S658 | 7176 | 702.5 |
| 415 | G190 | 10368 | 547.5 | 482 | VCOM | 8760 | 702.5 | 549 | S657 | 7152 | 547.5 |
| 416 | G192 | 10344 | 702.5 | 483 | VCOM | 8736 | 547.5 | 550 | S656 | 7128 | 702.5 |
| 417 | G194 | 10320 | 547.5 | 484 | DUMMY | 8712 | 702.5 | 551 | S655 | 7104 | 547.5 |
| 418 | G196 | 10296 | 702.5 | 485 | DUMMY | 8688 | 547.5 | 552 | S654 | 7080 | 702.5 |
| 419 | G198 | 10272 | 547.5 | 486 | DUMMY | 8664 | 702.5 | 553 | S653 | 7056 | 547.5 |
| 420 | G200 | 10248 | 702.5 | 487 | S719 | 8640 | 547.5 | 554 | S652 | 7032 | 702.5 |
| 421 | G202 | 10224 | 547.5 | 488 | S718 | 8616 | 702.5 | 555 | S651 | 7008 | 547.5 |
| 422 | G204 | 10200 | 702.5 | 489 | S717 | 8592 | 547.5 | 556 | S650 | 6984 | 702.5 |
| 423 | G206 | 10176 | 547.5 | 490 | S716 | 8568 | 702.5 | 557 | S649 | 6960 | 547.5 |
| 424 | G208 | 10152 | 702.5 | 491 | S715 | 8544 | 547.5 | 558 | S648 | 6936 | 702.5 |
| 425 | G210 | 10128 | 547.5 | 492 | S714 | 8520 | 702.5 | 559 | S647 | 6912 | 547.5 |
| 426 | G212 | 10104 | 702.5 | 493 | S713 | 8496 | 547.5 | 560 | S646 | 6888 | 702.5 |
| 427 | G214 | 10080 | 547.5 | 494 | S712 | 8472 | 702.5 | 561 | S645 | 6864 | 547.5 |
| 428 | G216 | 10056 | 702.5 | 495 | S711 | 8448 | 547.5 | 562 | S644 | 6840 | 702.5 |
| 429 | G218 | 10032 | 547.5 | 496 | S710 | 8424 | 702.5 | 563 | S643 | 6816 | 547.5 |
| 430 | G220 | 10008 | 702.5 | 497 | S709 | 8400 | 547.5 | 564 | S642 | 6792 | 702.5 |
| 431 | G222 | 9984 | 547.5 | 498 | S708 | 8376 | 702.5 | 565 | S641 | 6768 | 547.5 |
| 432 | G224 | 9960 | 702.5 | 499 | S707 | 8352 | 547.5 | 566 | S640 | 6744 | 702.5 |
| 433 | G226 | 9936 | 547.5 | 500 | S706 | 8328 | 702.5 | 567 | S639 | 6720 | 547.5 |
| 434 | G228 | 9912 | 702.5 | 501 | S705 | 8304 | 547.5 | 568 | S638 | 6696 | 702.5 |
| 435 | G230 | 9888 | 547.5 | 502 | S704 | 8280 | 702.5 | 569 | S637 | 6672 | 547.5 |
| 436 | G232 | 9864 | 702.5 | 503 | S703 | 8256 | 547.5 | 570 | S636 | 6648 | 702.5 |
| 437 | G234 | 9840 | 547.5 | 504 | S702 | 8232 | 702.5 | 571 | S635 | 6624 | 547.5 |
| 438 | G236 | 9816 | 702.5 | 505 | S701 | 8208 | 547.5 | 572 | S634 | 6600 | 702.5 |
| 439 | G238 | 9792 | 547.5 | 506 | S700 | 8184 | 702.5 | 573 | S633 | 6576 | 547.5 |
| 440 | G240 | 9768 | 702.5 | 507 | S699 | 8160 | 547.5 | 574 | S632 | 6552 | 702.5 |
| 441 | G242 | 9744 | 547.5 | 508 | S698 | 8136 | 702.5 | 575 | S631 | 6528 | 547.5 |
| 442 | G244 | 9720 | 702.5 | 509 | S697 | 8112 | 547.5 | 576 | S630 | 6504 | 702.5 |
| 443 | G246 | 9696 | 547.5 | 510 | S696 | 8088 | 702.5 | 577 | S629 | 6480 | 547.5 |
| 444 | G248 | 9672 | 702.5 | 511 | S695 | 8064 | 547.5 | 578 | S628 | 6456 | 702.5 |
| 445 | G250 | 9648 | 547.5 | 512 | S694 | 8040 | 702.5 | 579 | S627 | 6432 | 547.5 |
| 446 | G252 | 9624 | 702.5 | 513 | S693 | 8016 | 547.5 | 580 | S626 | 6408 | 702.5 |
| 447 | G254 | 9600 | 547.5 | 514 | S692 | 7992 | 702.5 | 581 | S625 | 6384 | 547.5 |
| 448 | G256 | 9576 | 702.5 | 515 | S691 | 7968 | 547.5 | 582 | S624 | 6360 | 702.5 |
| 449 | G258 | 9552 | 547.5 | 516 | S690 | 7944 | 702.5 | 583 | S623 | 6336 | 547.5 |
| 450 | G260 | 9528 | 702.5 | 517 | S689 | 7920 | 547.5 | 584 | S622 | 6312 | 702.5 |
| 451 | G262 | 9504 | 547.5 | 518 | S688 | 7896 | 702.5 | 585 | S621 | 6288 | 547.5 |
| 452 | G264 | 9480 | 702.5 | 519 | S687 | 7872 | 547.5 | 586 | S620 | 6264 | 702.5 |
| 453 | G266 | 9456 | 547.5 | 520 | S686 | 7848 | 702.5 | 587 | S619 | 6240 | 547.5 |
| 454 | G268 | 9432 | 702.5 | 521 | S685 | 7824 | 547.5 | 588 | S618 | 6216 | 702.5 |
| 455 | G270 | 9408 | 547.5 | 522 | S684 | 7800 | 702.5 | 589 | S617 | 6192 | 547.5 |
| 456 | G272 | 9384 | 702.5 | 523 | S683 | 7776 | 547.5 | 590 | S616 | 6168 | 702.5 |
| 457 | G274 | 9360 | 547.5 | 524 | S682 | 7752 | 702.5 | 591 | S615 | 6144 | 547.5 |
| 458 | G276 | 9336 | 702.5 | 525 | S681 | 7728 | 547.5 | 592 | S614 | 6120 | 702.5 |
| 459 | G278 | 9312 | 547.5 | 526 | S680 | 7704 | 702.5 | 593 | S613 | 6096 | 547.5 |
| 460 | G280 | 9288 | 702.5 | 527 | S679 | 7680 | 547.5 | 594 | S612 | 6072 | 702.5 |
| 461 | G282 | 9264 | 547.5 | 528 | S678 | 7656 | 702.5 | 595 | S611 | 6048 | 547.5 |
| 462 | G284 | 9240 | 702.5 | 529 | S677 | 7632 | 547.5 | 596 | S610 | 6024 | 702.5 |
| 463 | G286 | 9216 | 547.5 | 530 | S676 | 7608 | 702.5 | 597 | S609 | 6000 | 547.5 |
| 464 | G288 | 9192 | 702.5 | 531 | S675 | 7584 | 547.5 | 598 | S608 | 5976 | 702.5 |
| 465 | G290 | 9168 | 547.5 | 532 | S674 | 7560 | 702.5 | 599 | S607 | 5952 | 547.5 |
| 466 | G292 | 9144 | 702.5 | 533 | S673 | 7536 | 547.5 | 600 | S606 | 5928 | 702.5 |
| 467 | G294 | 9120 | 547.5 | 534 | S672 | 7512 | 702.5 | 601 | S605 | 5904 | 547.5 |
| 468 | G296 | 9096 | 702.5 | 535 | S671 | 7488 | 547.5 | 602 | S604 | 5880 | 702.5 |
| 469 | G298 | 9072 | 547.5 | 536 | S670 | 7464 | 702.5 | 603 | S603 | 5856 | 547.5 |

| Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos |
|------|--------|-------|-------|------|--------|-------|-------|------|--------|-------|-------|
| 604 | S602 | 5832 | 702.5 | 671 | S535 | 4224 | 547.5 | 738 | S468 | 2616 | 702.5 |
| 605 | S601 | 5808 | 547.5 | 672 | S534 | 4200 | 702.5 | 739 | S467 | 2592 | 547.5 |
| 606 | S600 | 5784 | 702.5 | 673 | S533 | 4176 | 547.5 | 740 | S466 | 2568 | 702.5 |
| 607 | S599 | 5760 | 547.5 | 674 | S532 | 4152 | 702.5 | 741 | S465 | 2544 | 547.5 |
| 608 | S598 | 5736 | 702.5 | 675 | S531 | 4128 | 547.5 | 742 | S464 | 2520 | 702.5 |
| 609 | S597 | 5712 | 547.5 | 676 | S530 | 4104 | 702.5 | 743 | S463 | 2496 | 547.5 |
| 610 | S596 | 5688 | 702.5 | 677 | S529 | 4080 | 547.5 | 744 | S462 | 2472 | 702.5 |
| 611 | S595 | 5664 | 547.5 | 678 | S528 | 4056 | 702.5 | 745 | S461 | 2448 | 547.5 |
| 612 | S594 | 5640 | 702.5 | 679 | S527 | 4032 | 547.5 | 746 | S460 | 2424 | 702.5 |
| 613 | S593 | 5616 | 547.5 | 680 | S526 | 4008 | 702.5 | 747 | S459 | 2400 | 547.5 |
| 614 | S592 | 5592 | 702.5 | 681 | S525 | 3984 | 547.5 | 748 | S458 | 2376 | 702.5 |
| 615 | S591 | 5568 | 547.5 | 682 | S524 | 3960 | 702.5 | 749 | S457 | 2352 | 547.5 |
| 616 | S590 | 5544 | 702.5 | 683 | S523 | 3936 | 547.5 | 750 | S456 | 2328 | 702.5 |
| 617 | S589 | 5520 | 547.5 | 684 | S522 | 3912 | 702.5 | 751 | S455 | 2304 | 547.5 |
| 618 | S588 | 5496 | 702.5 | 685 | S521 | 3888 | 547.5 | 752 | S454 | 2280 | 702.5 |
| 619 | S587 | 5472 | 547.5 | 686 | S520 | 3864 | 702.5 | 753 | S453 | 2256 | 547.5 |
| 620 | S586 | 5448 | 702.5 | 687 | S519 | 3840 | 547.5 | 754 | S452 | 2232 | 702.5 |
| 621 | S585 | 5424 | 547.5 | 688 | S518 | 3816 | 702.5 | 755 | S451 | 2208 | 547.5 |
| 622 | S584 | 5400 | 702.5 | 689 | S517 | 3792 | 547.5 | 756 | S450 | 2184 | 702.5 |
| 623 | S583 | 5376 | 547.5 | 690 | S516 | 3768 | 702.5 | 757 | S449 | 2160 | 547.5 |
| 624 | S582 | 5352 | 702.5 | 691 | S515 | 3744 | 547.5 | 758 | S448 | 2136 | 702.5 |
| 625 | S581 | 5328 | 547.5 | 692 | S514 | 3720 | 702.5 | 759 | S447 | 2112 | 547.5 |
| 626 | S580 | 5304 | 702.5 | 693 | S513 | 3696 | 547.5 | 760 | S446 | 2088 | 702.5 |
| 627 | S579 | 5280 | 547.5 | 694 | S512 | 3672 | 702.5 | 761 | S445 | 2064 | 547.5 |
| 628 | S578 | 5256 | 702.5 | 695 | S511 | 3648 | 547.5 | 762 | S444 | 2040 | 702.5 |
| 629 | S577 | 5232 | 547.5 | 696 | S510 | 3624 | 702.5 | 763 | S443 | 2016 | 547.5 |
| 630 | S576 | 5208 | 702.5 | 697 | S509 | 3600 | 547.5 | 764 | S442 | 1992 | 702.5 |
| 631 | S575 | 5184 | 547.5 | 698 | S508 | 3576 | 702.5 | 765 | S441 | 1968 | 547.5 |
| 632 | S574 | 5160 | 702.5 | 699 | S507 | 3552 | 547.5 | 766 | S440 | 1944 | 702.5 |
| 633 | S573 | 5136 | 547.5 | 700 | S506 | 3528 | 702.5 | 767 | S439 | 1920 | 547.5 |
| 634 | S572 | 5112 | 702.5 | 701 | S505 | 3504 | 547.5 | 768 | S438 | 1896 | 702.5 |
| 635 | S571 | 5088 | 547.5 | 702 | S504 | 3480 | 702.5 | 769 | S437 | 1872 | 547.5 |
| 636 | S570 | 5064 | 702.5 | 703 | S503 | 3456 | 547.5 | 770 | S436 | 1848 | 702.5 |
| 637 | S569 | 5040 | 547.5 | 704 | S502 | 3432 | 702.5 | 771 | S435 | 1824 | 547.5 |
| 638 | S568 | 5016 | 702.5 | 705 | S501 | 3408 | 547.5 | 772 | S434 | 1800 | 702.5 |
| 639 | S567 | 4992 | 547.5 | 706 | S500 | 3384 | 702.5 | 773 | S433 | 1776 | 547.5 |
| 640 | S566 | 4968 | 702.5 | 707 | S499 | 3360 | 547.5 | 774 | S432 | 1752 | 702.5 |
| 641 | S565 | 4944 | 547.5 | 708 | S498 | 3336 | 702.5 | 775 | S431 | 1728 | 547.5 |
| 642 | S564 | 4920 | 702.5 | 709 | S497 | 3312 | 547.5 | 776 | S430 | 1704 | 702.5 |
| 643 | S563 | 4896 | 547.5 | 710 | S496 | 3288 | 702.5 | 777 | S429 | 1680 | 547.5 |
| 644 | S562 | 4872 | 702.5 | 711 | S495 | 3264 | 547.5 | 778 | S428 | 1656 | 702.5 |
| 645 | S561 | 4848 | 547.5 | 712 | S494 | 3240 | 702.5 | 779 | S427 | 1632 | 547.5 |
| 646 | S560 | 4824 | 702.5 | 713 | S493 | 3216 | 547.5 | 780 | S426 | 1608 | 702.5 |
| 647 | S559 | 4800 | 547.5 | 714 | S492 | 3192 | 702.5 | 781 | S425 | 1584 | 547.5 |
| 648 | S558 | 4776 | 702.5 | 715 | S491 | 3168 | 547.5 | 782 | S424 | 1560 | 702.5 |
| 649 | S557 | 4752 | 547.5 | 716 | S490 | 3144 | 702.5 | 783 | S423 | 1536 | 547.5 |
| 650 | S556 | 4728 | 702.5 | 717 | S489 | 3120 | 547.5 | 784 | S422 | 1512 | 702.5 |
| 651 | S555 | 4704 | 547.5 | 718 | S488 | 3096 | 702.5 | 785 | S421 | 1488 | 547.5 |
| 652 | S554 | 4680 | 702.5 | 719 | S487 | 3072 | 547.5 | 786 | S420 | 1464 | 702.5 |
| 653 | S553 | 4656 | 547.5 | 720 | S486 | 3048 | 702.5 | 787 | S419 | 1440 | 547.5 |
| 654 | S552 | 4632 | 702.5 | 721 | S485 | 3024 | 547.5 | 788 | S418 | 1416 | 702.5 |
| 655 | S551 | 4608 | 547.5 | 722 | S484 | 3000 | 702.5 | 789 | S417 | 1392 | 547.5 |
| 656 | S550 | 4584 | 702.5 | 723 | S483 | 2976 | 547.5 | 790 | S416 | 1368 | 702.5 |
| 657 | S549 | 4560 | 547.5 | 724 | S482 | 2952 | 702.5 | 791 | S415 | 1344 | 547.5 |
| 658 | S548 | 4536 | 702.5 | 725 | S481 | 2928 | 547.5 | 792 | S414 | 1320 | 702.5 |
| 659 | S547 | 4512 | 547.5 | 726 | S480 | 2904 | 702.5 | 793 | S413 | 1296 | 547.5 |
| 660 | S546 | 4488 | 702.5 | 727 | S479 | 2880 | 547.5 | 794 | S412 | 1272 | 702.5 |
| 661 | S545 | 4464 | 547.5 | 728 | S478 | 2856 | 702.5 | 795 | S411 | 1248 | 547.5 |
| 662 | S544 | 4440 | 702.5 | 729 | S477 | 2832 | 547.5 | 796 | S410 | 1224 | 702.5 |
| 663 | S543 | 4416 | 547.5 | 730 | S476 | 2808 | 702.5 | 797 | S409 | 1200 | 547.5 |
| 664 | S542 | 4392 | 702.5 | 731 | S475 | 2784 | 547.5 | 798 | S408 | 1176 | 702.5 |
| 665 | S541 | 4368 | 547.5 | 732 | S474 | 2760 | 702.5 | 799 | S407 | 1152 | 547.5 |
| 666 | S540 | 4344 | 702.5 | 733 | S473 | 2736 | 547.5 | 800 | S406 | 1128 | 702.5 |
| 667 | S539 | 4320 | 547.5 | 734 | S472 | 2712 | 702.5 | 801 | S405 | 1104 | 547.5 |
| 668 | S538 | 4296 | 702.5 | 735 | S471 | 2688 | 547.5 | 802 | S404 | 1080 | 702.5 |
| 669 | S537 | 4272 | 547.5 | 736 | S470 | 2664 | 702.5 | 803 | S403 | 1056 | 547.5 |
| 670 | S536 | 4248 | 702.5 | 737 | S469 | 2640 | 547.5 | 804 | S402 | 1032 | 702.5 |

| Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos |
|------|--------|-------|-------|------|--------|-------|-------|------|--------|-------|-------|
| 805 | S401 | 1008 | 547.5 | 872 | S335 | -600 | 702.5 | 939 | S268 | -2208 | 547.5 |
| 806 | S400 | 984 | 702.5 | 873 | S334 | -624 | 547.5 | 940 | S267 | -2232 | 702.5 |
| 807 | S399 | 960 | 547.5 | 874 | S333 | -648 | 702.5 | 941 | S266 | -2256 | 547.5 |
| 808 | S398 | 936 | 702.5 | 875 | S332 | -672 | 547.5 | 942 | S265 | -2280 | 702.5 |
| 809 | S397 | 912 | 547.5 | 876 | S331 | -696 | 702.5 | 943 | S264 | -2304 | 547.5 |
| 810 | S396 | 888 | 702.5 | 877 | S330 | -720 | 547.5 | 944 | S263 | -2328 | 702.5 |
| 811 | S395 | 864 | 547.5 | 878 | S329 | -744 | 702.5 | 945 | S262 | -2352 | 547.5 |
| 812 | S394 | 840 | 702.5 | 879 | S328 | -768 | 547.5 | 946 | S261 | -2376 | 702.5 |
| 813 | S393 | 816 | 547.5 | 880 | S327 | -792 | 702.5 | 947 | S260 | -2400 | 547.5 |
| 814 | S392 | 792 | 702.5 | 881 | S326 | -816 | 547.5 | 948 | S259 | -2424 | 702.5 |
| 815 | S391 | 768 | 547.5 | 882 | S325 | -840 | 702.5 | 949 | S258 | -2448 | 547.5 |
| 816 | S390 | 744 | 702.5 | 883 | S324 | -864 | 547.5 | 950 | S257 | -2472 | 702.5 |
| 817 | S389 | 720 | 547.5 | 884 | S323 | -888 | 702.5 | 951 | S256 | -2496 | 547.5 |
| 818 | S388 | 696 | 702.5 | 885 | S322 | -912 | 547.5 | 952 | S255 | -2520 | 702.5 |
| 819 | S387 | 672 | 547.5 | 886 | S321 | -936 | 702.5 | 953 | S254 | -2544 | 547.5 |
| 820 | S386 | 648 | 702.5 | 887 | S320 | -960 | 547.5 | 954 | S253 | -2568 | 702.5 |
| 821 | S385 | 624 | 547.5 | 888 | S319 | -984 | 702.5 | 955 | S252 | -2592 | 547.5 |
| 822 | S384 | 600 | 702.5 | 889 | S318 | -1008 | 547.5 | 956 | S251 | -2616 | 702.5 |
| 823 | S383 | 576 | 547.5 | 890 | S317 | -1032 | 702.5 | 957 | S250 | -2640 | 547.5 |
| 824 | S382 | 552 | 702.5 | 891 | S316 | -1056 | 547.5 | 958 | S249 | -2664 | 702.5 |
| 825 | S381 | 528 | 547.5 | 892 | S315 | -1080 | 702.5 | 959 | S248 | -2688 | 547.5 |
| 826 | S380 | 504 | 702.5 | 893 | S314 | -1104 | 547.5 | 960 | S247 | -2712 | 702.5 |
| 827 | S379 | 480 | 547.5 | 894 | S313 | -1128 | 702.5 | 961 | S246 | -2736 | 547.5 |
| 828 | S378 | 456 | 702.5 | 895 | S312 | -1152 | 547.5 | 962 | S245 | -2760 | 702.5 |
| 829 | S377 | 432 | 547.5 | 896 | S311 | -1176 | 702.5 | 963 | S244 | -2784 | 547.5 |
| 830 | S376 | 408 | 702.5 | 897 | S310 | -1200 | 547.5 | 964 | S243 | -2808 | 702.5 |
| 831 | S375 | 384 | 547.5 | 898 | S309 | -1224 | 702.5 | 965 | S242 | -2832 | 547.5 |
| 832 | S374 | 360 | 702.5 | 899 | S308 | -1248 | 547.5 | 966 | S241 | -2856 | 702.5 |
| 833 | S373 | 336 | 547.5 | 900 | S307 | -1272 | 702.5 | 967 | S240 | -2880 | 547.5 |
| 834 | S372 | 312 | 702.5 | 901 | S306 | -1296 | 547.5 | 968 | S239 | -2904 | 702.5 |
| 835 | S371 | 288 | 547.5 | 902 | S305 | -1320 | 702.5 | 969 | S238 | -2928 | 547.5 |
| 836 | S370 | 264 | 702.5 | 903 | S304 | -1344 | 547.5 | 970 | S237 | -2952 | 702.5 |
| 837 | S369 | 240 | 547.5 | 904 | S303 | -1368 | 702.5 | 971 | S236 | -2976 | 547.5 |
| 838 | S368 | 216 | 702.5 | 905 | S302 | -1392 | 547.5 | 972 | S235 | -3000 | 702.5 |
| 839 | S367 | 192 | 547.5 | 906 | S301 | -1416 | 702.5 | 973 | S234 | -3024 | 547.5 |
| 840 | S366 | 168 | 702.5 | 907 | S300 | -1440 | 547.5 | 974 | S233 | -3048 | 702.5 |
| 841 | S365 | 144 | 547.5 | 908 | S299 | -1464 | 702.5 | 975 | S232 | -3072 | 547.5 |
| 842 | S364 | 120 | 702.5 | 909 | S298 | -1488 | 547.5 | 976 | S231 | -3096 | 702.5 |
| 843 | S363 | 96 | 547.5 | 910 | S297 | -1512 | 702.5 | 977 | S230 | -3120 | 547.5 |
| 844 | S362 | 72 | 702.5 | 911 | S296 | -1536 | 547.5 | 978 | S229 | -3144 | 702.5 |
| 845 | S361 | 48 | 547.5 | 912 | S295 | -1560 | 702.5 | 979 | S228 | -3168 | 547.5 |
| 846 | S360 | 24 | 702.5 | 913 | S294 | -1584 | 547.5 | 980 | S227 | -3192 | 702.5 |
| 847 | DUMMY | 0 | 547.5 | 914 | S293 | -1608 | 702.5 | 981 | S226 | -3216 | 547.5 |
| 848 | S359 | -24 | 702.5 | 915 | S292 | -1632 | 547.5 | 982 | S225 | -3240 | 702.5 |
| 849 | S358 | -48 | 547.5 | 916 | S291 | -1656 | 702.5 | 983 | S224 | -3264 | 547.5 |
| 850 | S357 | -72 | 702.5 | 917 | S290 | -1680 | 547.5 | 984 | S223 | -3288 | 702.5 |
| 851 | S356 | -96 | 547.5 | 918 | S289 | -1704 | 702.5 | 985 | S222 | -3312 | 547.5 |
| 852 | S355 | -120 | 702.5 | 919 | S288 | -1728 | 547.5 | 986 | S221 | -3336 | 702.5 |
| 853 | S354 | -144 | 547.5 | 920 | S287 | -1752 | 702.5 | 987 | S220 | -3360 | 547.5 |
| 854 | S353 | -168 | 702.5 | 921 | S286 | -1776 | 547.5 | 988 | S219 | -3384 | 702.5 |
| 855 | S352 | -192 | 547.5 | 922 | S285 | -1800 | 702.5 | 989 | S218 | -3408 | 547.5 |
| 856 | S351 | -216 | 702.5 | 923 | S284 | -1824 | 547.5 | 990 | S217 | -3432 | 702.5 |
| 857 | S350 | -240 | 547.5 | 924 | S283 | -1848 | 702.5 | 991 | S216 | -3456 | 547.5 |
| 858 | S349 | -264 | 702.5 | 925 | S282 | -1872 | 547.5 | 992 | S215 | -3480 | 702.5 |
| 859 | S348 | -288 | 547.5 | 926 | S281 | -1896 | 702.5 | 993 | S214 | -3504 | 547.5 |
| 860 | S347 | -312 | 702.5 | 927 | S280 | -1920 | 547.5 | 994 | S213 | -3528 | 702.5 |
| 861 | S346 | -336 | 547.5 | 928 | S279 | -1944 | 702.5 | 995 | S212 | -3552 | 547.5 |
| 862 | S345 | -360 | 702.5 | 929 | S278 | -1968 | 547.5 | 996 | S211 | -3576 | 702.5 |
| 863 | S344 | -384 | 547.5 | 930 | S277 | -1992 | 702.5 | 997 | S210 | -3600 | 547.5 |
| 864 | S343 | -408 | 702.5 | 931 | S276 | -2016 | 547.5 | 998 | S209 | -3624 | 702.5 |
| 865 | S342 | -432 | 547.5 | 932 | S275 | -2040 | 702.5 | 999 | S208 | -3648 | 547.5 |
| 866 | S341 | -456 | 702.5 | 933 | S274 | -2064 | 547.5 | 1000 | S207 | -3672 | 702.5 |
| 867 | S340 | -480 | 547.5 | 934 | S273 | -2088 | 702.5 | 1001 | S206 | -3696 | 547.5 |
| 868 | S339 | -504 | 702.5 | 935 | S272 | -2112 | 547.5 | 1002 | S205 | -3720 | 702.5 |
| 869 | S338 | -528 | 547.5 | 936 | S271 | -2136 | 702.5 | 1003 | S204 | -3744 | 547.5 |
| 870 | S337 | -552 | 702.5 | 937 | S270 | -2160 | 547.5 | 1004 | S203 | -3768 | 702.5 |
| 871 | S336 | -576 | 547.5 | 938 | S269 | -2184 | 702.5 | 1005 | S202 | -3792 | 547.5 |

| Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos |
|------|--------|-------|-------|------|--------|-------|-------|------|--------|-------|-------|
| 1006 | S201 | -3816 | 702.5 | 1073 | S134 | -5424 | 547.5 | 1140 | S67 | -7032 | 702.5 |
| 1007 | S200 | -3840 | 547.5 | 1074 | S133 | -5448 | 702.5 | 1141 | S66 | -7056 | 547.5 |
| 1008 | S199 | -3864 | 702.5 | 1075 | S132 | -5472 | 547.5 | 1142 | S65 | -7080 | 702.5 |
| 1009 | S198 | -3888 | 547.5 | 1076 | S131 | -5496 | 702.5 | 1143 | S64 | -7104 | 547.5 |
| 1010 | S197 | -3912 | 702.5 | 1077 | S130 | -5520 | 547.5 | 1144 | S63 | -7128 | 702.5 |
| 1011 | S196 | -3936 | 547.5 | 1078 | S129 | -5544 | 702.5 | 1145 | S62 | -7152 | 547.5 |
| 1012 | S195 | -3960 | 702.5 | 1079 | S128 | -5568 | 547.5 | 1146 | S61 | -7176 | 702.5 |
| 1013 | S194 | -3984 | 547.5 | 1080 | S127 | -5592 | 702.5 | 1147 | S60 | -7200 | 547.5 |
| 1014 | S193 | -4008 | 702.5 | 1081 | S126 | -5616 | 547.5 | 1148 | S59 | -7224 | 702.5 |
| 1015 | S192 | -4032 | 547.5 | 1082 | S125 | -5640 | 702.5 | 1149 | S58 | -7248 | 547.5 |
| 1016 | S191 | -4056 | 702.5 | 1083 | S124 | -5664 | 547.5 | 1150 | S57 | -7272 | 702.5 |
| 1017 | S190 | -4080 | 547.5 | 1084 | S123 | -5688 | 702.5 | 1151 | S56 | -7296 | 547.5 |
| 1018 | S189 | -4104 | 702.5 | 1085 | S122 | -5712 | 547.5 | 1152 | S55 | -7320 | 702.5 |
| 1019 | S188 | -4128 | 547.5 | 1086 | S121 | -5736 | 702.5 | 1153 | S54 | -7344 | 547.5 |
| 1020 | S187 | -4152 | 702.5 | 1087 | S120 | -5760 | 547.5 | 1154 | S53 | -7368 | 702.5 |
| 1021 | S186 | -4176 | 547.5 | 1088 | S119 | -5784 | 702.5 | 1155 | S52 | -7392 | 547.5 |
| 1022 | S185 | -4200 | 702.5 | 1089 | S118 | -5808 | 547.5 | 1156 | S51 | -7416 | 702.5 |
| 1023 | S184 | -4224 | 547.5 | 1090 | S117 | -5832 | 702.5 | 1157 | S50 | -7440 | 547.5 |
| 1024 | S183 | -4248 | 702.5 | 1091 | S116 | -5856 | 547.5 | 1158 | S49 | -7464 | 702.5 |
| 1025 | S182 | -4272 | 547.5 | 1092 | S115 | -5880 | 702.5 | 1159 | S48 | -7488 | 547.5 |
| 1026 | S181 | -4296 | 702.5 | 1093 | S114 | -5904 | 547.5 | 1160 | S47 | -7512 | 702.5 |
| 1027 | S180 | -4320 | 547.5 | 1094 | S113 | -5928 | 702.5 | 1161 | S46 | -7536 | 547.5 |
| 1028 | S179 | -4344 | 702.5 | 1095 | S112 | -5952 | 547.5 | 1162 | S45 | -7560 | 702.5 |
| 1029 | S178 | -4368 | 547.5 | 1096 | S111 | -5976 | 702.5 | 1163 | S44 | -7584 | 547.5 |
| 1030 | S177 | -4392 | 702.5 | 1097 | S110 | -6000 | 547.5 | 1164 | S43 | -7608 | 702.5 |
| 1031 | S176 | -4416 | 547.5 | 1098 | S109 | -6024 | 702.5 | 1165 | S42 | -7632 | 547.5 |
| 1032 | S175 | -4440 | 702.5 | 1099 | S108 | -6048 | 547.5 | 1166 | S41 | -7656 | 702.5 |
| 1033 | S174 | -4464 | 547.5 | 1100 | S107 | -6072 | 702.5 | 1167 | S40 | -7680 | 547.5 |
| 1034 | S173 | -4488 | 702.5 | 1101 | S106 | -6096 | 547.5 | 1168 | S39 | -7704 | 702.5 |
| 1035 | S172 | -4512 | 547.5 | 1102 | S105 | -6120 | 702.5 | 1169 | S38 | -7728 | 547.5 |
| 1036 | S171 | -4536 | 702.5 | 1103 | S104 | -6144 | 547.5 | 1170 | S37 | -7752 | 702.5 |
| 1037 | S170 | -4560 | 547.5 | 1104 | S103 | -6168 | 702.5 | 1171 | S36 | -7776 | 547.5 |
| 1038 | S169 | -4584 | 702.5 | 1105 | S102 | -6192 | 547.5 | 1172 | S35 | -7800 | 702.5 |
| 1039 | S168 | -4608 | 547.5 | 1106 | S101 | -6216 | 702.5 | 1173 | S34 | -7824 | 547.5 |
| 1040 | S167 | -4632 | 702.5 | 1107 | S100 | -6240 | 547.5 | 1174 | S33 | -7848 | 702.5 |
| 1041 | S166 | -4656 | 547.5 | 1108 | S99 | -6264 | 702.5 | 1175 | S32 | -7872 | 547.5 |
| 1042 | S165 | -4680 | 702.5 | 1109 | S98 | -6288 | 547.5 | 1176 | S31 | -7896 | 702.5 |
| 1043 | S164 | -4704 | 547.5 | 1110 | S97 | -6312 | 702.5 | 1177 | S30 | -7920 | 547.5 |
| 1044 | S163 | -4728 | 702.5 | 1111 | S96 | -6336 | 547.5 | 1178 | S29 | -7944 | 702.5 |
| 1045 | S162 | -4752 | 547.5 | 1112 | S95 | -6360 | 702.5 | 1179 | S28 | -7968 | 547.5 |
| 1046 | S161 | -4776 | 702.5 | 1113 | S94 | -6384 | 547.5 | 1180 | S27 | -7992 | 702.5 |
| 1047 | S160 | -4800 | 547.5 | 1114 | S93 | -6408 | 702.5 | 1181 | S26 | -8016 | 547.5 |
| 1048 | S159 | -4824 | 702.5 | 1115 | S92 | -6432 | 547.5 | 1182 | S25 | -8040 | 702.5 |
| 1049 | S158 | -4848 | 547.5 | 1116 | S91 | -6456 | 702.5 | 1183 | S24 | -8064 | 547.5 |
| 1050 | S157 | -4872 | 702.5 | 1117 | S90 | -6480 | 547.5 | 1184 | S23 | -8088 | 702.5 |
| 1051 | S156 | -4896 | 547.5 | 1118 | S89 | -6504 | 702.5 | 1185 | S22 | -8112 | 547.5 |
| 1052 | S155 | -4920 | 702.5 | 1119 | S88 | -6528 | 547.5 | 1186 | S21 | -8136 | 702.5 |
| 1053 | S154 | -4944 | 547.5 | 1120 | S87 | -6552 | 702.5 | 1187 | S20 | -8160 | 547.5 |
| 1054 | S153 | -4968 | 702.5 | 1121 | S86 | -6576 | 547.5 | 1188 | S19 | -8184 | 702.5 |
| 1055 | S152 | -4992 | 547.5 | 1122 | S85 | -6600 | 702.5 | 1189 | S18 | -8208 | 547.5 |
| 1056 | S151 | -5016 | 702.5 | 1123 | S84 | -6624 | 547.5 | 1190 | S17 | -8232 | 702.5 |
| 1057 | S150 | -5040 | 547.5 | 1124 | S83 | -6648 | 702.5 | 1191 | S16 | -8256 | 547.5 |
| 1058 | S149 | -5064 | 702.5 | 1125 | S82 | -6672 | 547.5 | 1192 | S15 | -8280 | 702.5 |
| 1059 | S148 | -5088 | 547.5 | 1126 | S81 | -6696 | 702.5 | 1193 | S14 | -8304 | 547.5 |
| 1060 | S147 | -5112 | 702.5 | 1127 | S80 | -6720 | 547.5 | 1194 | S13 | -8328 | 702.5 |
| 1061 | S146 | -5136 | 547.5 | 1128 | S79 | -6744 | 702.5 | 1195 | S12 | -8352 | 547.5 |
| 1062 | S145 | -5160 | 702.5 | 1129 | S78 | -6768 | 547.5 | 1196 | S11 | -8376 | 702.5 |
| 1063 | S144 | -5184 | 547.5 | 1130 | S77 | -6792 | 702.5 | 1197 | S10 | -8400 | 547.5 |
| 1064 | S143 | -5208 | 702.5 | 1131 | S76 | -6816 | 547.5 | 1198 | S9 | -8424 | 702.5 |
| 1065 | S142 | -5232 | 547.5 | 1132 | S75 | -6840 | 702.5 | 1199 | S8 | -8448 | 547.5 |
| 1066 | S141 | -5256 | 702.5 | 1133 | S74 | -6864 | 547.5 | 1200 | S7 | -8472 | 702.5 |
| 1067 | S140 | -5280 | 547.5 | 1134 | S73 | -6888 | 702.5 | 1201 | S6 | -8496 | 547.5 |
| 1068 | S139 | -5304 | 702.5 | 1135 | S72 | -6912 | 547.5 | 1202 | S5 | -8520 | 702.5 |
| 1069 | S138 | -5328 | 547.5 | 1136 | S71 | -6936 | 702.5 | 1203 | S4 | -8544 | 547.5 |
| 1070 | S137 | -5352 | 702.5 | 1137 | S70 | -6960 | 547.5 | 1204 | S3 | -8568 | 702.5 |
| 1071 | S136 | -5376 | 547.5 | 1138 | S69 | -6984 | 702.5 | 1205 | S2 | -8592 | 547.5 |
| 1072 | S135 | -5400 | 702.5 | 1139 | S68 | -7008 | 547.5 | 1206 | S1 | -8616 | 702.5 |

| Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos | Pad# | Signal | X-pos | Y-pos |
|------|--------|--------|-------|------|----------|--------|-------|------|--------|-------|-------|
| 1207 | S0 | -8640 | 547.5 | 1274 | G201 | -10248 | 702.5 | | | | |
| 1208 | NC | -8664 | 702.5 | 1275 | G199 | -10272 | 547.5 | | | | |
| 1209 | DUMMY | -8688 | 547.5 | 1276 | G197 | -10296 | 702.5 | | | | |
| 1210 | DUMMY | -8712 | 702.5 | 1277 | G195 | -10320 | 547.5 | | | | |
| 1211 | VCOM | -8736 | 547.5 | 1278 | G193 | -10344 | 702.5 | | | | |
| 1212 | VCOM | -8760 | 702.5 | 1279 | G191 | -10368 | 547.5 | | | | |
| 1213 | DUMMY | -8784 | 547.5 | 1280 | G189 | -10392 | 702.5 | | | | |
| 1214 | GTESTL | -8808 | 702.5 | 1281 | G187 | -10416 | 547.5 | | | | |
| 1215 | G319 | -8832 | 547.5 | 1282 | G185 | -10440 | 702.5 | | | | |
| 1216 | G317 | -8856 | 702.5 | 1283 | G183 | -10464 | 547.5 | | | | |
| 1217 | G315 | -8880 | 547.5 | 1284 | G181 | -10488 | 702.5 | | | | |
| 1218 | G313 | -8904 | 702.5 | 1285 | G179 | -10512 | 547.5 | | | | |
| 1219 | G311 | -8928 | 547.5 | 1286 | G177 | -10536 | 702.5 | | | | |
| 1220 | G309 | -8952 | 702.5 | 1287 | G175 | -10560 | 547.5 | | | | |
| 1221 | G307 | -8976 | 547.5 | 1288 | G173 | -10584 | 702.5 | | | | |
| 1222 | G305 | -9000 | 702.5 | 1289 | G171 | -10608 | 547.5 | | | | |
| 1223 | G303 | -9024 | 547.5 | 1290 | G169 | -10632 | 702.5 | | | | |
| 1224 | G301 | -9048 | 702.5 | 1291 | G167 | -10656 | 547.5 | | | | |
| 1225 | G299 | -9072 | 547.5 | 1292 | G165 | -10680 | 702.5 | | | | |
| 1226 | G297 | -9096 | 702.5 | 1293 | G163 | -10704 | 547.5 | | | | |
| 1227 | G295 | -9120 | 547.5 | 1294 | G161 | -10728 | 702.5 | | | | |
| 1228 | G293 | -9144 | 702.5 | 1295 | G159 | -10752 | 547.5 | | | | |
| 1229 | G291 | -9168 | 547.5 | 1296 | G157 | -10776 | 702.5 | | | | |
| 1230 | G289 | -9192 | 702.5 | 1297 | G155 | -10800 | 547.5 | | | | |
| 1231 | G287 | -9216 | 547.5 | 1298 | G153 | -10824 | 702.5 | | | | |
| 1232 | G285 | -9240 | 702.5 | 1299 | G151 | -10848 | 547.5 | | | | |
| 1233 | G283 | -9264 | 547.5 | 1300 | G149 | -10872 | 702.5 | | | | |
| 1234 | G281 | -9288 | 702.5 | 1301 | G147 | -10896 | 547.5 | | | | |
| 1235 | G279 | -9312 | 547.5 | 1302 | G145 | -10920 | 702.5 | | | | |
| 1236 | G277 | -9336 | 702.5 | 1303 | G143 | -10944 | 547.5 | | | | |
| 1237 | G275 | -9360 | 547.5 | 1304 | G141 | -10968 | 702.5 | | | | |
| 1238 | G273 | -9384 | 702.5 | 1305 | G139 | -10992 | 547.5 | | | | |
| 1239 | G271 | -9408 | 547.5 | 1306 | G137 | -11016 | 702.5 | | | | |
| 1240 | G269 | -9432 | 702.5 | 1307 | G135 | -11040 | 547.5 | | | | |
| 1241 | G267 | -9456 | 547.5 | 1308 | G133 | -11064 | 702.5 | | | | |
| 1242 | G265 | -9480 | 702.5 | 1309 | G131 | -11088 | 547.5 | | | | |
| 1243 | G263 | -9504 | 547.5 | 1310 | G129 | -11112 | 702.5 | | | | |
| 1244 | G261 | -9528 | 702.5 | 1311 | G127 | -11136 | 547.5 | | | | |
| 1245 | G259 | -9552 | 547.5 | 1312 | G125 | -11160 | 702.5 | | | | |
| 1246 | G257 | -9576 | 702.5 | 1313 | G123 | -11184 | 547.5 | | | | |
| 1247 | G255 | -9600 | 547.5 | 1314 | G121 | -11208 | 702.5 | | | | |
| 1248 | G253 | -9624 | 702.5 | 1315 | G119 | -11232 | 547.5 | | | | |
| 1249 | G251 | -9648 | 547.5 | 1316 | G117 | -11256 | 702.5 | | | | |
| 1250 | G249 | -9672 | 702.5 | 1317 | G115 | -11280 | 547.5 | | | | |
| 1251 | G247 | -9696 | 547.5 | 1318 | G113 | -11304 | 702.5 | | | | |
| 1252 | G245 | -9720 | 702.5 | 1319 | G111 | -11328 | 547.5 | | | | |
| 1253 | G243 | -9744 | 547.5 | 1320 | G109 | -11352 | 702.5 | | | | |
| 1254 | G241 | -9768 | 702.5 | 1321 | G107 | -11376 | 547.5 | | | | |
| 1255 | G239 | -9792 | 547.5 | 1322 | G105 | -11400 | 702.5 | | | | |
| 1256 | G237 | -9816 | 702.5 | 1323 | G103 | -11424 | 547.5 | | | | |
| 1257 | G235 | -9840 | 547.5 | 1324 | G101 | -11448 | 702.5 | | | | |
| 1258 | G233 | -9864 | 702.5 | 1325 | G99 | -11472 | 547.5 | | | | |
| 1259 | G231 | -9888 | 547.5 | 1326 | G97 | -11496 | 702.5 | | | | |
| 1260 | G229 | -9912 | 702.5 | 1327 | G95 | -11520 | 547.5 | | | | |
| 1261 | G227 | -9936 | 547.5 | 1328 | G93 | -11544 | 702.5 | | | | |
| 1262 | G225 | -9960 | 702.5 | 1329 | G91 | -11568 | 547.5 | | | | |
| 1263 | G223 | -9984 | 547.5 | 1330 | G89 | -11592 | 702.5 | | | | |
| 1264 | G221 | -10008 | 702.5 | 1331 | THROUGH7 | -11616 | 547.5 | | | | |
| 1265 | G219 | -10032 | 547.5 | 1332 | THROUGH8 | -11640 | 702.5 | | | | |
| 1266 | G217 | -10056 | 702.5 | 1333 | DUMMY | -11664 | 547.5 | | | | |
| 1267 | G215 | -10080 | 547.5 | 1334 | DUMMY | -11688 | 702.5 | | | | |
| 1268 | G213 | -10104 | 702.5 | 1335 | VGL | -11712 | 547.5 | | | | |
| 1269 | G211 | -10128 | 547.5 | 1336 | DUMMY | -11736 | 702.5 | | | | |
| 1270 | G209 | -10152 | 702.5 | | | | | | | | |
| 1271 | G207 | -10176 | 547.5 | | | | | | | | |
| 1272 | G205 | -10200 | 702.5 | | | | | | | | |
| 1273 | G203 | -10224 | 547.5 | | | | | | | | |

6 PIN DESCRIPTION

Remark:

I = Input;
O = Output;
IO = Bi-directional;
P = Power;
VCC = System VDD;
GND = System VSS;

Table 6-1: Power Supply Pins

| Name | Type | Connect to | Function | Description | When not in use |
|---------------------|------|---|--------------------------------------|--|-----------------|
| V _{SS} | P | GND | Ground of the Power Supply | System ground pin of the IC. | - |
| AV _{SS} | | GND | | Grounding for analog circuit. | - |
| V _{SSRC} | | GND | | Grounding for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages. | - |
| V _{CHS} | | AV _{SS} | | Grounding for booster circuit. | - |
| V _{CI} | P | Power Supply | Power Supply for Analog Circuits | Booster input voltage pin. - Connect to voltage source between 2.5V to 3.6V | - |
| V _{CIP} | | V _{CI} | | Voltage supply pin for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages. - Connect to same source of V _{CI} | - |
| V _{CIM} | O | Stabilizing capacitor | Booster voltages | Negative voltage of V _{CI} . | - |
| V _{CIX2} | | Stabilizing capacitor | | Equals to 2x V _{CI} | - |
| V _{CIX2J} | P | V _{CIX2} on FPC | Voltage for analog | They are the power supply used by on chip analog blocks and VGH/VGL dedc. | - |
| V _{CIX2G} | | V _{CIX2} on FPC | | | - |
| V _{COMR} | I | External voltage source or Open | External Reference | This pin provides voltage reference for internal voltage regulator when register VDV[4:0] of Power Control 4 set to “01111”. - Connect to an external voltage source for reference | Open |
| V _{COMH} | O | Stabilizing capacitor | Voltages for VCOM Signal | This pin indicates a HIGH level of VCOM generated in driving the VCOM alternation. | - |
| V _{COML} | | Stabilizing capacitor | | This pin indicates a LOW level of VCOM generated in driving the VCOM alternation. | - |
| V _{LCD63} | O | Stabilizing capacitor | LCD Driving Voltages | This pin is the maximum source driver voltage. | - |
| V _{GH} | | Stabilizing capacitor | | A positive power output pin for gate driver. This pin is ESD sensitive. It can achieve 2000V ESD (HBM) with connection of external components in application circuit. | - |
| V _{GL} | | Stabilizing capacitor | | A negative power output pin for gate driver. | - |
| V _{GOFFH} | | Stabilizing capacitor or open | | When the VGOFF alternation is driven, this pin indicates a high level of VGOFF. - Connect a capacitor for stabilization if Cs on gate structure is used - This pin can be open if Cs on common structure is used | Open |
| V _{GOFFHL} | I | Stabilizing capacitor to V _{COM} or open | | - Connect a capacitor to V _{COM} if Cs on gate application. | Open |
| CXP | I | Booster capacitor | Booster and Stabilization Capacitors | - Connect a capacitor to CXN | - |
| CXN | | | | - Connect a capacitor to CXP | - |
| CYP | | Booster capacitor | | - Connect a capacitor to CYN | - |
| CYN | | | | - Connect a capacitor to CYP | - |
| CP | | Booster capacitor | | - Connect a capacitor to CN | - |
| CN | | | | - Connect a capacitor to CP | - |
| C1P | | Booster capacitor | | - Connect a capacitor to C1N | - |
| C1N | | | | - Connect a capacitor to C1P This pin is ESD sensitive. It can achieve 2000V ESD (HBM) with connection of external components in application circuit. | - |
| C2P | | Booster capacitor | | - Connect a capacitor to C2N | - |
| C2N | | | | - Connect a capacitor to C2P This pin is ESD sensitive. It can achieve 2000V ESD (HBM) with connection of external components in application circuit. | - |
| C3P | | Booster capacitor | | - Connect a capacitor to C3N | - |
| C3N | | | | - Connect a capacitor to C3P | - |
| CDUM0 | | Stabilizing capacitor | Stabilization Capacitors | - Connect a capacitor to V _{SS} | Open |
| CDUM1 | | Stabilizing capacitor | | - Connect a capacitor to V _{SS} | Open |
| EXTCLK | I | V _{SS} | OSC input | A clock input pin for internal oscillator. Connect to V _{SS} when using the internal oscillator. | GND |

| | | | | | |
|--------------------|---|--------------------------------------|--|---|-----|
| REGVDD | I | V _{DDIO} or V _{SS} | Logic Control | Input pin to enable internal vdd regulation. - Connect to V _{DDIO} if system Vdd > 1.95V or system Vdd < 1.65V, internal Vdd regulator will be enabled - Connect to V _{SS} if system Vdd is 1.65V – 1.95V. Internal vdd regulator will be disabled. | GND |
| V _{CORE} | P | Stabilizing capacitor | Power for Core Logic | Vdd for core use. Connect a capacitor for stabilization | - |
| V _{REGC} | P | V _{CORE} | Regulator output for logic circuits | Regulator output for V _{CORE} use. | - |
| V _{RAM} | P | Stabilizing capacitor | Power for RAM | Vdd for RAM use. Connect a capacitor for stabilization | - |
| V _{REGR} | P | V _{RAM} | Regulator output for RAM | Regulator output for RAM use. | - |
| V _{DDEXT} | P | Power Supply | Power for internal V _{DD} regulator | Voltage input pin for internal logic, connect to system VDD. - Connect to voltage source between 1.4V to 3.6V | - |
| V _{DDIO} | P | Power Supply | Power for interface logic pins | Voltage input pin for logic I/O, connect to system VDD. - Connect to voltage source between 1.4V to 3.6V | - |

Table 6-2 - Interface Logic Pins

| Name | Type | Connect to | Function | Description | When not in use |
|--------------------|------|--------------------------------------|------------------------|---|--------------------------------------|
| DEN | I | MPU | Display Timing Signals | Display enable pin from controller. Data will be treated as dummy regardless the DEN status during front/back porch setting at registers R16 and R17. | V _{DDIO} |
| VS _Y NC | | MPU | | Frame synchronization signal. - Fixed to V _{DDIO} or V _{SS} if not used | V _{DDIO} or V _{SS} |
| HS _Y NC | | MPU | | Line synchronization signal. - Fixed to V _{DDIO} or V _{SS} if not used | V _{DDIO} or V _{SS} |
| DOTCLK | | MPU | | Dot-clock signal and oscillator source. A non-stop external clock must be provided to that pin even at front or black porch non-display period. | V _{DDIO} or V _{SS} |
| SHUT | I | V _{DDIO} or V _{SS} | Logic Control | When using the RGB interface, it is a input pin put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. - Connect to V _{DDIO} for sleep mode - Connect to V _{SS} for normal operating mode This pin has no effect in system interface and should be connected to V _{DDIO} / V _{SS} | V _{DDIO} or V _{SS} |
| DC | I | MPU | Logic Control | Data or command | V _{DDIO} or V _{SS} |
| E (RD) | | MPU | | 6800-system : E (enable signal) 8080-system : /RD (read strobe signal) Serial mode : Not used and should be connected to V _{DDIO} or V _{SS} | V _{DDIO} or V _{SS} |
| R/ W (WR) | | MPU | | 68-system : R/ W (indicates read cycle when High, write cycle when Low) 80-system : WR (write strobe signal) Serial mode : Not used and should be connected to V _{DDIO} or V _{SS} | V _{DDIO} or V _{SS} |
| D0-D17 | IO | MPU | Data bus | For parallel mode, 8/9/16/18 bit interface. For generic mode, RGB interface. Please refer to Section 15 Interface Mapping for definition. Unused pins must be float or connect to V _{SS} . | V _{SS} |
| WS _Y NC | O | MPU | Logic Control | Ram Write Synchronization output | Open |
| RES | I | MPU | System Reset | System reset pin. - Connect to V _{DDIO} when not used | V _{DDIO} |
| CS | I | MPU | Serial Interface | Chip select pin of serial interface. - Leave it OPEN when not used | Open |
| SCK | | MPU | | Clock pin of serial interface. - Leave it OPEN when not used | Open |
| SDI | | MPU | | Data input pin in serial mode. - Leave it OPEN when not used | Open |
| SDO | O | MPU | | Data output pin in serial mode. - Leave it OPEN when not used | Open |

Table 6-3: Mode Selection Pins

| Name | Type | Connect to | Function | Description | When not in use | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|--------------------------------------|--------------------------------------|------------------------|---|--------------------------------------|---------------------------------|-----|-----|----------------|---|---|---|---|------------|---|---|---|---|------------|---|---|---|---|--------------------------------|---|---|---|---|-------------------------------|---|---|---|---|--------------------------------|---|---|---|---|-------------------------------|---|---|---|---|---------------------------------|---|---|---|---|--------------------------------|---|---|---|---|--------------------------------|---|---|---|---|-------------------------------|---|---|---|---|----------------------------|---|---|---|---|-----------------------------------|---|---|---|---|-----------------------------------|---|
| CM | I | V _{DDIO} or V _{SS} | Logic Control | When using the RGB interface, it is a input pin to select 262k-color or 8-color display mode. After entered 8-color display mode, the driver will switch to Frame-Inversion-Mode, and only MSB of the data Red, Green and Blue will be considered. - Connect to V _{DDIO} for 8-color display mode - Connect to V _{SS} for 262k-color display mode This pin has no effect in system interface and should be connected to V _{DDIO} / V _{SS} | V _{DDIO} or V _{SS} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RL | I | V _{DDIO} or V _{SS} | Panel Mapping Controls | Input pin to select the Source driver data shift direction. - Connect to V _{DDIO} for display first RGB data at S0-S2 - Connect to V _{SS} for display first RGB data at S719-S717 | V _{DDIO} or V _{SS} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GD | | V _{DDIO} or V _{SS} | | Input pin to select the 1st output Gate GD = ‘0’, G0 is 1st output Gate, Gate sequence G0, G1, G2, G3, ..., G318, G319 GD = ‘1’, G1 is 1st output Gate, Gate sequence G1, G0, G3, G2, ..., G319, G318 | V _{DDIO} or V _{SS} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TB | | V _{DDIO} or V _{SS} | | Input pin to select the Gate driver scan direction. - Connect to V _{DDIO} for Gate scan from G0 to G319 - Connect to V _{SS} for Gate scan from G319 to G0 | V _{DDIO} or V _{SS} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BGR | | V _{DDIO} or V _{SS} | | Input pin to select the color mapping. - Connect to V _{DDIO} for Blue-Green-Red mapping - Connect to V _{SS} for Red-Green-Blue mapping (Refer to S0-S719 pin description on Page 19 for details) | V _{DDIO} or V _{SS} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| REV | | V _{DDIO} or V _{SS} | | Input pin to select the display reversion. - Connect to V _{DDIO} mapping data “0” to maximum pixel voltage for normal white panel - Connect to V _{SS} mapping data “0” to minimum pixel voltage for normal black panel | V _{DDIO} or V _{SS} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CAD | | V _{DDIO} or V _{SS} | | Panel structure selection pin. - Connect to V _{DDIO} if Cs on gate structure is used - Connect to V _{SS} if Cs on common structure is used | V _{DDIO} or V _{SS} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PS0 | I | V _{DDIO} or V _{SS} | Interface Selection | <table><tr><th>PS3</th><th>PS2</th><th>PS1</th><th>PS0</th><th>Interface Mode</th></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>3-wire SPI</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire SPI</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>16-bit 6800 parallel interface</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8-bit 6800 parallel interface</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>16-bit 8080 parallel interface</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8-bit 8080 parallel interface</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>18-bits 6800 parallel interface</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>9-bits 6800 parallel interface</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>18-bit 8080 parallel interface</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>9-bit 8080 parallel interface</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>6-bit serial RGB interface</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>16-bit RGB interface + 4-wire SPI</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>18-bit RGB interface + 4-wire SPI</td></tr></table> | PS3 | PS2 | PS1 | PS0 | Interface Mode | 1 | 1 | 1 | 1 | 3-wire SPI | 1 | 1 | 1 | 0 | 4-wire SPI | 1 | 0 | 1 | 1 | 16-bit 6800 parallel interface | 1 | 0 | 1 | 0 | 8-bit 6800 parallel interface | 1 | 0 | 0 | 1 | 16-bit 8080 parallel interface | 1 | 0 | 0 | 0 | 8-bit 8080 parallel interface | 0 | 1 | 1 | 1 | 18-bits 6800 parallel interface | 0 | 1 | 1 | 0 | 9-bits 6800 parallel interface | 0 | 1 | 0 | 1 | 18-bit 8080 parallel interface | 0 | 1 | 0 | 0 | 9-bit 8080 parallel interface | 0 | 0 | 1 | 1 | 6-bit serial RGB interface | 0 | 0 | 1 | 0 | 16-bit RGB interface + 4-wire SPI | 0 | 0 | 0 | 1 | 18-bit RGB interface + 4-wire SPI | - |
| PS3 | | PS2 | | PS1 | PS0 | Interface Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | 1 | | 1 | 1 | 3-wire SPI | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | 1 | | 1 | 0 | 4-wire SPI | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | 0 | | 1 | 1 | 16-bit 6800 parallel interface | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | 0 | | 1 | 0 | 8-bit 6800 parallel interface | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | 0 | | 0 | 1 | 16-bit 8080 parallel interface | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | 0 | | 0 | 0 | 8-bit 8080 parallel interface | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | | 1 | | 1 | 1 | 18-bits 6800 parallel interface | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | | 1 | | 1 | 0 | 9-bits 6800 parallel interface | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | | 1 | | 0 | 1 | 18-bit 8080 parallel interface | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | | 1 | | 0 | 0 | 9-bit 8080 parallel interface | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | 6-bit serial RGB interface | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | 16-bit RGB interface + 4-wire SPI | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 18-bit RGB interface + 4-wire SPI | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PS1 | V _{DDIO} or V _{SS} | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PS2 | V _{DDIO} or V _{SS} | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PS3 | V _{DDIO} or V _{SS} | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GAMAS0 | I | V _{DDIO} or V _{SS} | Logic Control | Gamma selection pin. This pin should be connected to V _{DDIO} / V _{SS} | V _{DDIO} or V _{SS} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GAMAS1 | | V _{DDIO} or V _{SS} | | Gamma selection pin. This pin should be connected to V _{DDIO} / V _{SS} | V _{DDIO} or V _{SS} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GAMAS2 | | V _{DDIO} or V _{SS} | | Gamma selection pin. This pin should be connected to V _{DDIO} / V _{SS} | V _{DDIO} or V _{SS} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 6-4: Driver Output Pins

| Name | Type | Connect to | Function | Description | When not in use |
|---------|------|------------|---------------------|--|-----------------|
| VCOM | O | LCD | LCD Driving Signals | A power supply for the TFT-display common electrode. | Open |
| G0-G319 | | LCD | | Gate driver output pins. These pins output V_{GH} , V_{GL} or V_{GOFFH} level. | Open |
| GTESTR | | LCD | | Gate driver output test pins, leave these pins no connection when using Cs on common | Open |
| GTESTL | | LCD | | | Open |
| S0-S719 | | LCD | | Source driver output pins. S(3n) : display Red if BGR = LOW, Blue if BGR = HIGH. S(3n+1) : display Green. S(3n+2) : display Blue if BGR = LOW, Red if BGR = HIGH. | Open |

Table 6-5: Miscellaneous Pins

| Name | Type | Connect to | Function | Description | When not in use |
|----------|------|------------|-------------------|---|-----------------|
| NC | - | - | - | These pins must be left open and cannot be connected together | Open |
| THROUGH1 | - | - | - | Dummy pads. Used to measure the COG contact resistance. | Open |
| THROUGH7 | - | - | - | These two pads are short circuited within the chip | Open |
| THROUGH2 | - | - | - | Dummy pads. Used to measure the COG contact resistance. | Open |
| THROUGH8 | - | - | - | These two pads are short circuited within the chip | Open |
| THROUGH3 | - | - | - | Dummy pads. Used to measure the COG contact resistance. | Open |
| THROUGH5 | - | - | - | These two pads are short circuited within the chip | Open |
| THROUGH4 | - | - | - | Dummy pads. Used to measure the COG contact resistance. | Open |
| THROUGH6 | - | - | - | These two pads are short circuited within the chip | Open |
| DUMMY | - | - | - | Floating pins and no connection inside the IC. These pins should be open. | Open |
| TESTA | IO | FPC | IC Testing Signal | Test pin of the internal circuit. - Leave this pin open and insert test point in FPC | Open |
| TESTB | | FPC | | Test pin of the internal circuit. - Leave this pin open and insert test point in FPC | Open |
| TESTC | | FPC | | Test pin of the internal circuit. - Leave this pin open and insert test point in FPC | Open |

7 BLOCK FUNCTION DESCRIPTION

7.1 System Interface

The System Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series high speed parallel interface, 3-lines serial peripheral interface and 4-lines serial peripheral interface. The selection of different interface is done by PS3, PS2, PS1 and PS0 pins. Please refer to the pin descriptions on page 19.

a) MPU Parallel 6800-series Interface

The parallel Interface consists of 18 bi-directional data pins $D[17:0]$, R/\overline{W} , D/\overline{C} , E and \overline{CS} . R/\overline{W} input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or the status register. R/\overline{W} input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/\overline{C} input. The E input serves as data latch signal (clock) when high provided that \overline{CS} is low. Please refer to Parallel Interface Timing Diagram of 6800-series microprocessors. In order to match the operating frequency of the GDDRAM with that of the MCU, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.

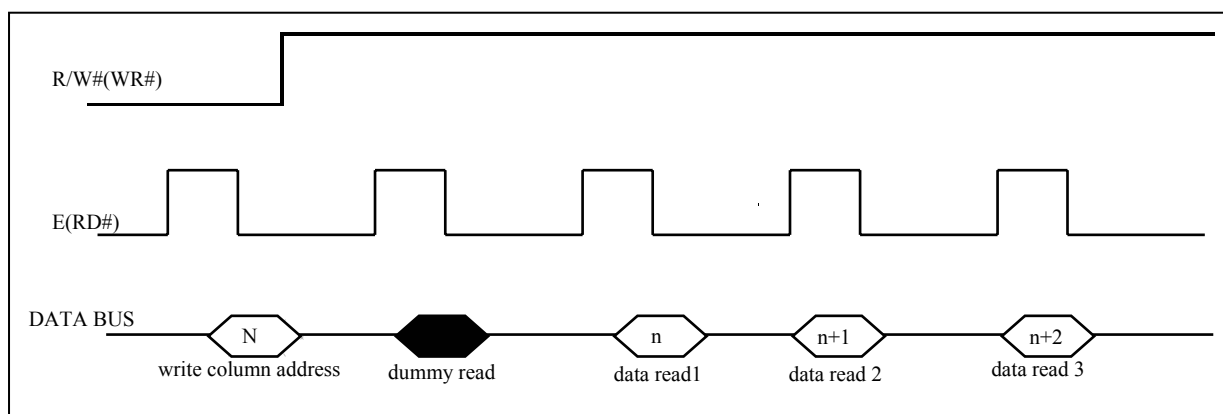


Figure 7-1 – Read Display Data

b) MPU Parallel 8080-series Interface

The parallel interface consists of 18 bi-directional data pins $D[17:0]$, \overline{RD} , \overline{WR} , D/\overline{C} and \overline{CS} . \overline{RD} input serves as data read latch signal (clock) when low provided that \overline{CS} is low. Whether reading the display data from GDDRAM or reading the status from the status register is controlled by D/\overline{C} . \overline{WR} input serves as data write latch signal (clock) when low provided that \overline{CS} is low. Whether writing the display data to the GDDRAM or writing the command to the command register is controlled by D/\overline{C} . A dummy read is also required before the first actual display data read for 8080-series interface. Please refer Figure 7-1.

c) MPU 4-lines Serial Peripheral Interface

The 4-lines serial peripheral Interface consists of serial clock SCK , serial data SDI , D/\overline{C} and \overline{CS} . SDI is shifted into 8-bit shift register on every rising edge of SCK in the order of data bit 7, data bit 6 data bit 0. D/\overline{C} is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock.

d) MPU 3-lines Serial Peripheral Interface

The operation is similar to 4-lines serial peripheral interface while $\overline{D/C}$ is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: $\overline{D/C}$ bit, D7 to D0 bit. The $\overline{D/C}$ bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM ($\overline{D/C}$ bit = 1) or the command register ($\overline{D/C}$ bit = 0).

| | 6800 – series Parallel Interface | 8080 – series Parallel Interface | MCU Serial Interface |
|---------------|----------------------------------|----------------------------------|----------------------|
| Data Read | 18/16/9/8-bits | 18/16/9/8-bits | No |
| Data Write | 18/16/9/8-bits | 18/16/9/8-bits | 8-bits |
| Command Read | Status only | Status only | No |
| Command Write | Yes | Yes | 8-bits |

Table 7-1 - Data bus selection modes

7.2 RGB Interface

SSD1289 supports RGB interface and VSYNC interface as the moving display interface to display animation image. RGB interface unit consists of D[17:0], HSYNC, VSYNC, DOTCLK and DEN signals for display moving pictures. When the RGB interface is selected, the display operation is synchronized with external control signals (HSYNC, VSYNC and DOTCLK). In this operation, Data D[17:0] will be treated as RR[5:0], GG[5:0] and BB[0:5], is written in synchronization with the control signals when DEN is enabled for write operation in order to avoid flicker or tearing effect while updating display data.

Table 7-2: RGB signal matching in data bus

| Data Bus | RGB signals |
|----------|-------------|
| D[17:12] | RR[5:0] |
| D[11:6] | GG[5:0] |
| D[5:0] | BB[0:5] |

In VSYNC interface operation, the display operation is synchronized with the internal clock, which synchronizes the display operation with the VSYNC signal. The display data is written to the GDDRAM through the system interface. When writing data via VSYNC interface, the speed of writing data in the internal RAM is faster from the falling edge of frame synchronous (VSYNC) than calculated minimum speed. The display may be updated even the data written in the RAM is not completed. In this operation, some restrictions in setting the frequency and the method to write data to the internal RAM are required.

7.3 Address Counter (AC)

The address counter (AC) assigns address to the GDDRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading the data, the AC is not updated. A window address function allows for data to be written only to a window area specified by GRAM.

7.4 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is $240 \text{ RGB} \times 320 \times 18 / 8 = 172,800$ bytes. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Please refer to the command “Data Output/Scan direction” for detail description.

Four pages of display data forms a RAM address block and stored in the GDDRAM. Each block will form the fundamental units of scrolling addresses. Various types of area scrolling can be performed by software program according to the command “Set area Scroll” and “Set Scroll Start”.

7.5 Gamma/Grayscale Voltage Generator

The grayscale voltage circuit generates a LCD driver circuit that corresponds to the grayscale levels as specified in the grayscale gamma adjustment register. 262,144 possible colors can be displayed when 1 pixel = 18 bit. For details, see the gamma adjustment register.

7.6 Booster and Regulator Circuit

These two functional blocks generate the voltage of VGH, VGL, VCOM levels and VLCD0~63 which are necessary for operating a TFT LCD.

7.7 Timing Generator

The timing generator generates a timing signal for the operation of internal circuit such as the internal RAM accessing, data output timing etc.

7.8 Oscillation Circuit (OSC)

This module is an on-chip low power RC oscillator circuitry. The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the display timing generator.

7.9 Data Latches

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

7.10 Liquid Crystal Driver Circuit

SSD1289 consists of a 720-output source driver (S0-S719) and a 320-output gate driver (G0-G319). The display image data is latched when 720 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source output from the source driver can be changed by setting the RL bit and the shift direction of gate output from the gate driver can be changed by setting the TB bit. The scan mode by the gate driver can be changed by setting the SM bit. Sets the gate driver pin arrangement in combination with the TB bit to select the optimal scan mode for the module.

8 COMMAND TABLE

Table 8-1 - Command Table

| Reg# | Register | R/W | D/C | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|--|-----|-----|---------|------|-------|-------|-------|-------|--------|--------|------|------|------|------|--------|---------|---------|-----------|
| R | Index | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| SR | Status Read | 1 | 0 | L7 | L6 | L5 | L4 | L3 | L2 | L1 | L0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R00h | Oscillation Start (0000h) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OSCE N |
| R01h | Driver output control [0XXX][X0X1]3F | 0 | 1 | 0 | RL | REV | CAD | BGR | SM | TB | MUX8 | MUX7 | MUX6 | MUX5 | MUX4 | MUX3 | MUX2 | MUX1 | MUX0 |
| R02h | LCD drive AC control (0000h) | 0 | 1 | 0 | 0 | 0 | FLD | ENWS | B/C | EOR | WSMD | NW7 | NW6 | NW5 | NW4 | NW3 | NW2 | NW1 | NW0 |
| R03h | Power control (1) All GAMAS[2:0] setting 8 color (6A64h) | 0 | 1 | DCT3 | DCT2 | DCT1 | DCT0 | BT2 | BT1 | BT0 | 0 | DC3 | DC2 | DC1 | DC0 | AP2 | AP1 | AP0 | 0 |
| R05h | Compare register (1) (0000h) | 0 | 1 | CPR5 | CPR4 | CPR3 | CPR2 | CPR1 | CPR0 | 0 | 0 | CPG5 | CPG4 | CPG3 | CPG2 | CPG1 | CPG0 | 0 | 0 |
| R06h | Compare register (2) (0000h) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CPB5 | CPB4 | CPB3 | CPB2 | CPB1 | CPB0 | 0 | 0 |
| R07h | Display control (0000h) | 0 | 1 | 0 | 0 | 0 | PT1 | PT0 | VLE2 | VLE1 | SPT | 0 | 0 | GON | DTE | CM | 0 | D1 | D0 |
| R0Bh | Frame cycle control (5308h) | 0 | 1 | NO1 | NO0 | SDT1 | SDT0 | 0 | EQ2 | EQ1 | EQ0 | DIV1 | DIV0 | SDIV | SRTN | RTN3 | RTN2 | RTN1 | RTN0 |
| R0Ch | Power control (2) (0004h) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VRC2 | VRC1 | VRC0 |
| R0Dh | Power control (3) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VRH3 | VRH2 | VRH1 | VRH0 |
| R0Eh | Power control (4) | 0 | 1 | 0 | 0 | VCOMG | VDV4 | VDV3 | VDV2 | VDV1 | VDV0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ROFh | Gate scan start position (0000h) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SCN8 | SCN7 | SCN6 | SCN5 | SCN4 | SCN3 | SCN2 | SCN1 |
| R10h | Sleep mode (0001h) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLP |
| R11h | Entry mode (6830h) | 0 | 1 | VS mode | DFM1 | DFM0 | TRANS | OEDef | WMode | DMode1 | DMode0 | TY1 | TY0 | ID1 | ID0 | AM | LG2 | LG1 | LG0 |
| R15h | Generic Interface Contrl (00D0h) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | INVDOT | INV DEN | INN VHS | INN VS |
| R16h | Horizontal Porch (EF1Ch) | 0 | 1 | XL7 | XL6 | XL5 | XL4 | XL3 | XL2 | XL1 | XL0 | HBP7 | HBP6 | HBP5 | HBP4 | HBP3 | HBP2 | HBP1 | HBP0 |
| R17h | Vertical Porch (0103h) | 0 | 1 | VFP7 | VFP6 | VFP5 | VFP4 | VFP3 | VFP2 | VFP1 | VFP0 | VBP7 | VBP6 | VBP5 | VBP4 | VBP3 | VBP2 | VBP1 | VBP0 |

(continued)

| Reg# | Register | R/W | D/C | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-------------------------------------|-----|-----|---|------|------|-------|-------|-------|-------|-------|------|------|------|------|-------|-------|-------|-------|
| R1Eh | Power control (5) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | nOTP | 0 | VCM5 | VCM4 | VCM3 | VCM2 | VCM1 | VCM0 |
| R22h | RAM data write | 0 | 1 | Data[17:0] mapping depends on the interface setting | | | | | | | | | | | | | | | |
| | RAM data read | 1 | 1 | | | | | | | | | | | | | | | | |
| R23h | RAM write data mask (1) | 0 | 1 | WMR5 | WMR4 | WMR3 | WMR2 | WMR1 | WMR0 | 0 | 0 | WMG5 | WMG4 | WMG3 | WMG2 | WMG1 | WMG0 | 0 | 0 |
| | (0000h) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R24h | RAM write data mask (2) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | WMB5 | WMB4 | WMB3 | WMB2 | WMB1 | WMB0 | 0 | 0 |
| | (0000h) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R25h | Frame Frequency | 0 | 1 | OSC3 | OSC2 | OSC1 | OSC0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | (8000h) | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R28h | VCOM OTP (000Ah) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| R29h | VCOM OTP (80C0h) | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| R30h | γ control (1) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | PKP12 | PKP11 | PKP10 | 0 | 0 | 0 | 0 | 0 | PKP02 | PKP01 | PKP00 |
| R31h | γ control (2) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | PKP32 | PKP31 | PKP30 | 0 | 0 | 0 | 0 | 0 | PKP22 | PKP21 | PKP20 |
| R32h | γ control (3) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | PKP52 | PKP51 | PKP50 | 0 | 0 | 0 | 0 | 0 | PKP42 | PKP41 | PKP40 |
| R33h | γ control (4) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | PRP12 | PRP11 | PRP10 | 0 | 0 | 0 | 0 | 0 | PRP02 | PRP01 | PRP00 |
| R34h | γ control (5) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | PKN12 | PKN11 | PKN10 | 0 | 0 | 0 | 0 | 0 | PKN02 | PKN01 | PKN00 |
| R35h | γ control (6) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | PKN32 | PKN31 | PKN30 | 0 | 0 | 0 | 0 | 0 | PKN22 | PKN21 | PKN20 |
| R36h | γ control (7) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | PKN52 | PKN51 | PKN50 | 0 | 0 | 0 | 0 | 0 | PKN42 | PKN41 | PKN40 |
| R37h | γ control (8) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | PRN12 | PRN11 | PRN10 | 0 | 0 | 0 | 0 | 0 | PRN02 | PRN01 | PRN00 |
| R3Ah | γ control (9) | 0 | 1 | 0 | 0 | 0 | VRP14 | VRP13 | VRP12 | VRP11 | VRP10 | 0 | 0 | 0 | 0 | VRP03 | VRP02 | VRP01 | VRP00 |
| R3Bh | γ control (10) | 0 | 1 | 0 | 0 | 0 | VRN14 | VRN13 | VRN12 | VRN11 | VRN10 | 0 | 0 | 0 | 0 | VRN03 | VRN02 | VRN01 | VRN00 |
| R41h | Vertical scroll control (1) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VL18 | VL17 | VL16 | VL15 | VL14 | VL13 | VL12 | VL11 | VL10 |
| | (0000h) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R42h | Vertical scroll control (2) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VL28 | VL27 | VL26 | VL25 | VL24 | VL23 | VL22 | VL21 | VL20 |
| | (0000h) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R44h | Horizontal RAM address position | 0 | 1 | HEA7 | HEA6 | HEA5 | HEA4 | HEA3 | HEA2 | HEA1 | HEA0 | HSA7 | HSA6 | HSA5 | HSA4 | HSA3 | HSA2 | HSA1 | HSA0 |
| | (EF00h) | | | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R45h | Vertical RAM address start position | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VSA8 | VSA7 | VSA6 | VSA5 | VSA4 | VSA3 | VSA2 | VSA1 | VSA0 |
| | (0000h) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R46h | Vertical RAM address end position | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VEA8 | VEA7 | VEA6 | VEA5 | VEA4 | VEA3 | VEA2 | VEA1 | VEA0 |
| | (013Fh) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| R48h | First window start | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SS18 | SS17 | SS16 | SS15 | SS14 | SS13 | SS12 | SS11 | SS10 |
| | (0000h) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R49h | First window end | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SE18 | SE17 | SE16 | SE15 | SE14 | SE13 | SE12 | SE11 | SE10 |
| | (013Fh) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| R4Ah | Second window start | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SS28 | SS27 | SS26 | SS25 | SS24 | SS23 | SS22 | SS21 | SS20 |
| | (0000h) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R4Bh | Second window end | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SE28 | SE27 | SE26 | SE25 | SE24 | SE23 | SE22 | SE21 | SE20 |
| | (013Fh) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| R4Eh | Set GDDRAM X address counter | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | XAD7 | XAD6 | XAD5 | XAD4 | XAD3 | XAD2 | XAD1 | XAD0 |
| | (0000h) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R4Fh | Set GDDRAM Y address counter | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | YAD8 | YAD7 | YAD6 | YAD5 | YAD4 | YAD3 | YAD2 | YAD1 | YAD0 |
| | (0000h) | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: In R01h, bits REV, CAD, BGR, TB, RL, CM will override the corresponding hardware pins settings.
Setting R28h as 0x0006 is required before setting R25h and R29h registers.

Table 8-2 – Gamma Registers POR value

| Command R30h-R3Bh | GAMAS[2:0] 000, 100 | GAMAS[2:0] 001, 101 | GAMAS[2:0] 010, 110 | GAMAS[2:0] 011, 111 |
|----------------------|------------------------|------------------------|------------------------|------------------------|
| PKP0 | 000 | 000 | 000 | 000 |
| PKP1 | 000 | 000 | 000 | 000 |
| PKP2 | 111 | 101 | 111 | 111 |
| PKP3 | 111 | 100 | 111 | 111 |
| PKP4 | 110 | 101 | 110 | 110 |
| PKP5 | 100 | 010 | 100 | 100 |
| PRP0 | 000 | 000 | 000 | 000 |
| PRP1 | 000 | 010 | 000 | 000 |
| VRP0 | 0100 | 1101 | 0100 | 0000 |
| VRP1 | 00100 | 10110 | 00100 | 11110 |
| PKN0 | 011 | 101 | 011 | 011 |
| PKN1 | 001 | 010 | 001 | 001 |
| PKN2 | 000 | 010 | 000 | 000 |
| PKN3 | 000 | 001 | 000 | 000 |
| PKN4 | 111 | 101 | 111 | 111 |
| PKN5 | 111 | 110 | 111 | 111 |
| PRN0 | 000 | 010 | 000 | 000 |
| PRN1 | 000 | 000 | 000 | 000 |
| VRN0 | 0110 | 1010 | 0110 | 1111 |
| VRN1 | 00000 | 00111 | 00000 | 00000 |

Table 8-3: Registers POR value at GAMAS[2:0] = 000,100

| Reg# | Register | Hex code | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-------------------|-------------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R03h | Power control (1) | 6664 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| R0Dh | Power control (3) | 0009 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| R0Eh | Power control (4) | 3200 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R1Eh | Power control (5) | 0029 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |

Table 8-4: Registers POR value at GAMAS[2:0] = 001,101

| Reg# | Register | Hex code | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-------------------|-------------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R03h | Power control (1) | 6A64 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| R0Dh | Power control (3) | 000A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| R0Eh | Power control (4) | 2C00 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R1Eh | Power control (5) | 0034 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

Table 8-5: Registers POR value at GAMAS[2:0] = 010,110

| Reg# | Register | Hex code | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-------------------|-------------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R03h | Power control (1) | 6264 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| R0Dh | Power control (3) | 0009 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| R0Eh | Power control (4) | 3200 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R1Eh | Power control (5) | 002F | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

Table 8-6: Registers POR value at GAMAS[2:0] = 011,111

| Reg# | Register | Hex code | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-------------------|-------------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R03h | Power control (1) | 6464 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| R0Dh | Power control (3) | 000A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| R0Eh | Power control (4) | 3000 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R1Eh | Power control (5) | 0031 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

9 COMMAND DESCRIPTION

Index (IR)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |

The index instruction specifies the RAM control indexes (R00h to RFFh). It sets the register number in the range of 00000000 to 11111111 in binary form. But do not access to Index register and instruction bits which do not have it's own index register.

Device Code Read (R00h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

If this register is read forcibly, 8989h is read.

Oscillator (R00h) (POR = 0000h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OSCEN |
| POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

OSCEN: The oscillator will be turned on when OSCEN = 1, off when OSCEN = 0.

Driver Output Control (R01h) (POR = [0XXXX0X1]3Fh)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|------|------|------|------|------|------|------|------|------|
| W | 1 | 0 | RL | REV | CAD | BGR | SM | TB | MUX8 | MUX7 | MUX6 | MUX5 | MUX4 | MUX3 | MUX2 | MUX1 | MUX0 |
| POR | | 0 | X | X | X | X | 0 | X | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

Note: The POR value of REV, CAD, BGR, TB and RL are determined by the corresponding hardware pin state. The software bit setting will override hardware setting if this command is sent.

REV: Displays all character and graphics display sections with reversal when REV = "1". Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.

| REV | RGB data | Source Output level | |
|-----|----------|---------------------|------------|
| | | Vcom = "L" | Vcom = "H" |
| 0 | 00000H | V63 | V0 |
| | : | : | : |
| | 3FFFFH | V0 | V63 |
| 1 | 00000H | V0 | V63 |
| | : | : | : |
| | 3FFFFH | V63 | V0 |

CAD: Set up based on retention capacitor configuration of the TFT panel.

| CAD | Retention capacitor configuration |
|-----|-----------------------------------|
| 0 | Cs on Common |
| 1 | Cs on Gate |

BGR: Selects the order from RGB to BGR in writing 18-bit pixel data in the GDDRAM.

When BGR = "0" <R><G> color is assigned from S0.

When BGR = "1" <G><R> color is assigned from S0.

SM: Change scanning order of gate driver.

| SM | Gate scan sequence (GD='0') |
|----|--|
| 0 | G0, G1, G2, G3.....G219 (left and right gate interlaced) |
| 1 | G0, G2,G318, G1, G3,G319 |

See “Scan mode setting” on next page.

TB: Selects the output shift direction of the gate driver.

When TB = 1, G0 shifts to G319.

When TB = 0, G319 shifts to G0.

RL: Selects the output shift direction of the source driver.

When RL = “1”, S0 shifts to S719 and <R><G> color is assigned from S0.

When RL = “0”, S719 shifts to S0 and <R><G> color is assigned from S719.

Set RL bit and BGR bit when changing the dot order of R, G and B. RL setting will be ignored when display with RAM (Dmode[1:0] = 00).

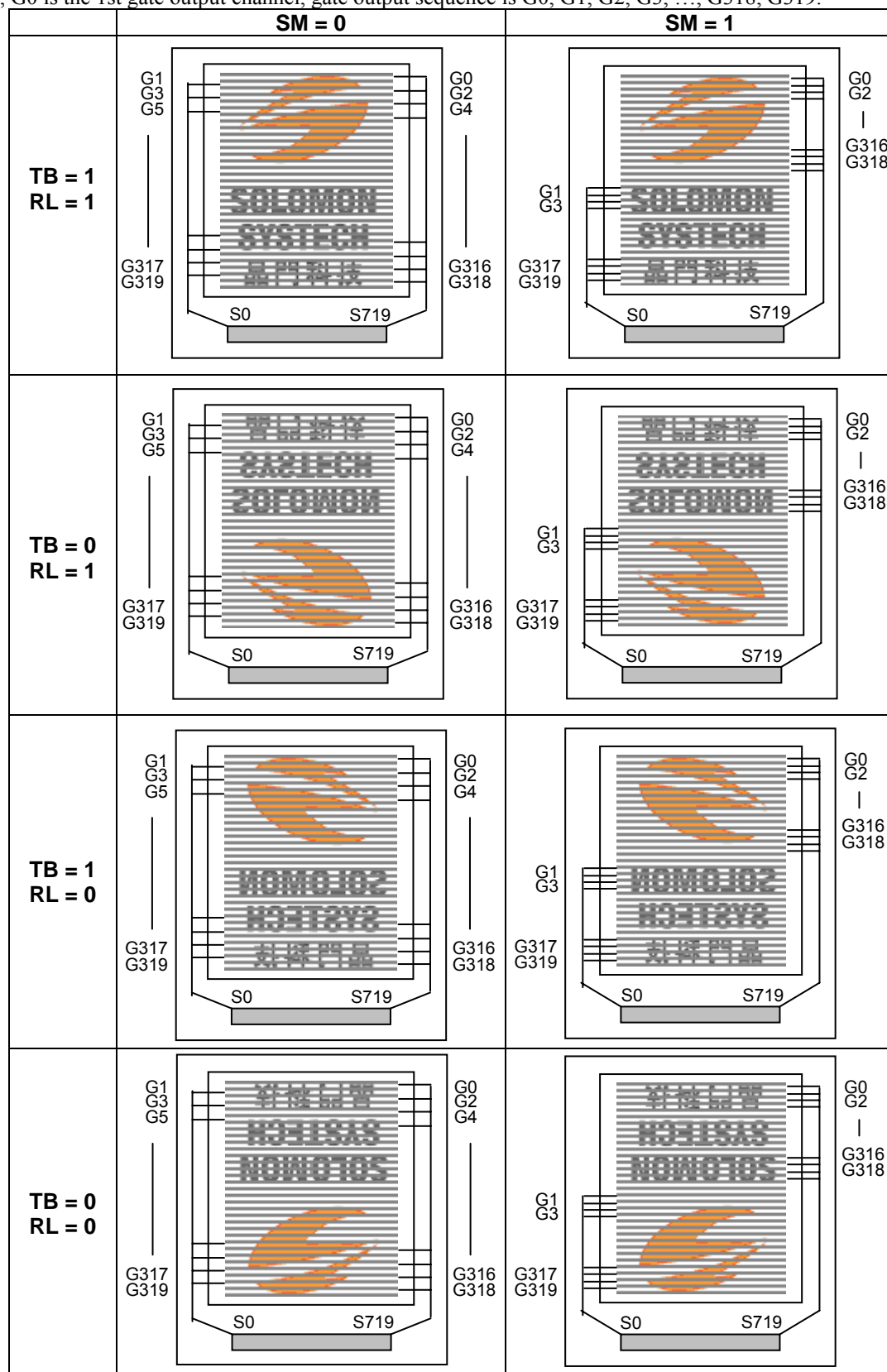
MUX[8:0]: Specify number of lines for the LCD driver. MUX[8:0] settings cannot exceed 319.

Remark: When using the partial display, the output for non-display area will be minimum voltage.

GD='1', G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, ..., G319, G318.

| | SM = 0 | SM = 1 |
|------------------|--------|--------|
| TB = 1 RL = 1 | | |
| TB = 0 RL = 1 | | |
| TB = 1 RL = 0 | | |
| TB = 0 RL = 0 | | |

GD='0', G0 is the 1st gate output channel, gate output sequence is G0, G1, G2, G3, ..., G318, G319.



LCD-Driving-Waveform Control (R02h) (POR = 0000h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|------|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | 0 | 0 | 0 | FLD | ENWS | B/C | EOR | WSMD | NW7 | NW6 | NW5 | NW4 | NW3 | NW2 | NW1 | NW0 |
| POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FLD: Set display in interlace drive mode to protect from flicker. It splits one frame into 3 fields and drive.

When FLD = 1, it is 3 field driving, which also limit VBP = 1 and cannot be used for Cs on gate panel type.

That is CAD = 1 & FLD=1 cannot be coexist.

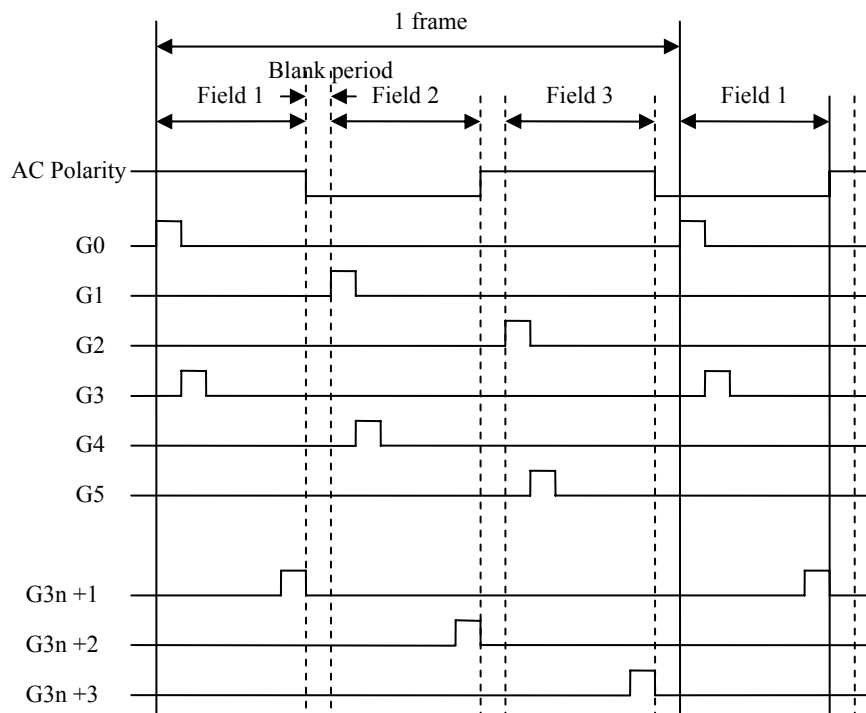
When FLD = 0, it is normal driving.

The following figure shows the gate selection when the 3-field inversion is enabled and the output waveform of the 3-field interlaced driving.

Table 9-1: 3-field interlace driving

| TB = 1 | | | TB = 0 | | |
|--------|---------|---------|--------|---------|---------|
| Gate | FLD = 0 | FLD = 1 | Gate | FLD = 0 | FLD = 1 |
| G0 | X | | G319 | X | |
| G1 | X | | G318 | X | |
| G2 | X | X | G317 | X | X |
| G3 | X | | G316 | X | |
| G4 | X | | G315 | X | |
| | X | X | | X | X |
| | X | | | X | |
| | X | | | x | |
| G317 | X | | G2 | X | |
| G318 | X | | G1 | X | |
| G319 | X | X | G0 | X | X |

Figure 9-1: gate output timing in 3-field interlacing driving



B/C: Select the liquid crystal drive waveform VCOM.

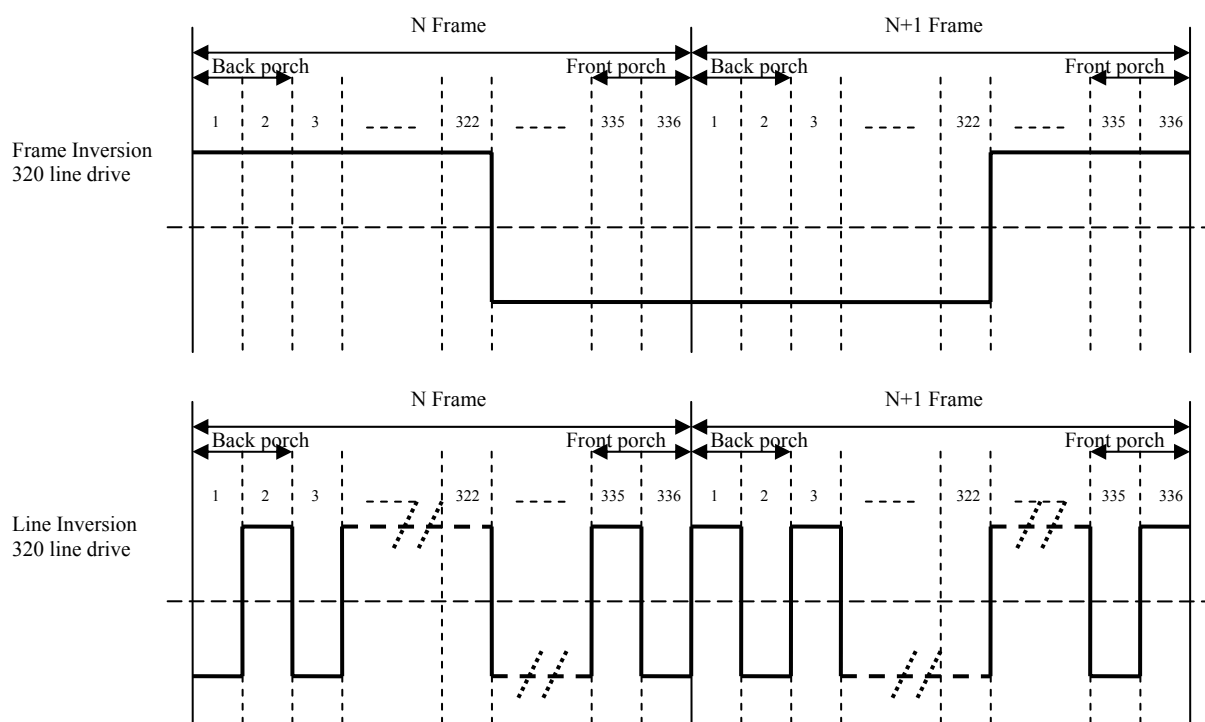
When B/C = 0, frame inversion of the LCD driving signal is enabled.

When B/C = 1, a N-line inversion waveform is generated and alternates in a N-line equals to NW[7:0]+1.

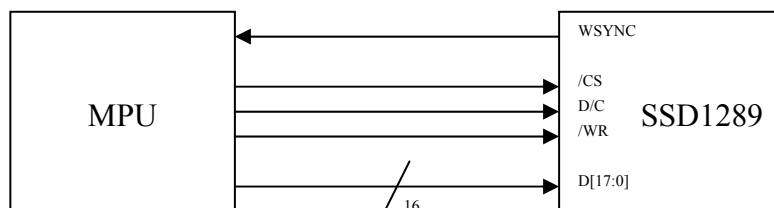
EOR: When B/C = 1 and EOR = 1, the odd/even frame-select signals and the N-line inversion signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the lines of the LCD driven and the N-lines.

NW[7:0]: Specify the number of lines that will alternate at the N-line inversion setting (B/C = 1). N-line is equal to NW[7:0]+1.

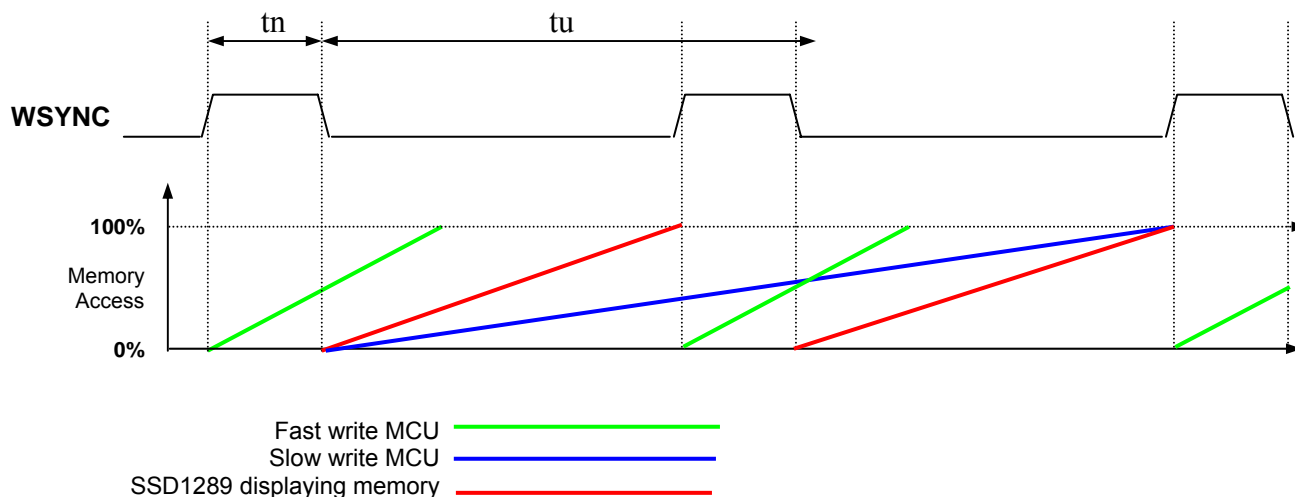
Figure 9-2: Line Inversion AC Driver



ENWS: When ENWS = 1, it enables WSYNC output pin. Model1 or Mode2 is selected by WSMD. When ENWS = 0(POR), it disables WSYNC feature, the WSYNC output pin will be high-impedance.

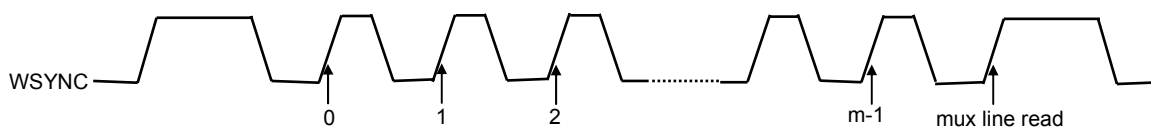


WSMD = 0 is mode1, the waveform of WSYNC output will be:



tn is the time when there is No Update of LCD screen from on-chip ram content.
tu is the time when the LCD screen is updating based on on-chip ram content.
 e.g. fosc = 510KHz, for 320mux, tn = 282us (6 lines), tu = 15.06ms (320 lines)

WSMD = 1 is mode2, the waveform of WSYNC output will be:



For fast write MCU: MCU should start to write new frame of ram data just after rising edge of long WSYNC pulse and should be finished well before the rising edge of the next long WSYNC pulse.
 e.g. 5MHz 8 bit parallel write cycle for 18 bit color depth, or 3MHz 8 bit parallel write cycle for 16 bit color depth.

For slow write MCU (Half the write speed of fast write): MCU should start to write new frame ram data after the rising edge of the first short WSYNC pulse and must be finished within 2 frames time.
 e.g. 2.5MHz 8 bit parallel write cycle for 18 bit color depth.

* Usually, **mode2** is for slower MCU, while **mode1** is for fast MCU.

Power control 1 (R03h) (POR = 6664h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | DCT3 | DCT2 | DCT1 | DCT0 | BT2 | BT1 | BT0 | 0 | DC3 | DC2 | DC1 | DC0 | AP2 | AP1 | AP0 | 0 |
| POR | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

*note: this POR value is for GAMAS[2:0] = 000, for POR values of all GAMAS[2:0] setting please refer to Table 5.

DCT[3:0]: Set the step-up cycle of the step-up circuit for 8-color mode ($CM = V_{DDIO}$). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

| DCT3 | DCT2 | DCT1 | DCT0 | Step-up cycle |
|------|------|------|------|-------------------|
| 0 | 0 | 0 | 0 | Fline \times 24 |
| 0 | 0 | 0 | 1 | Fline \times 16 |
| 0 | 0 | 1 | 0 | Fline \times 12 |
| 0 | 0 | 1 | 1 | Fline \times 8 |
| 0 | 1 | 0 | 0 | Fline \times 6 |
| 0 | 1 | 0 | 1 | Fline \times 5 |
| 0 | 1 | 1 | 0 | Fline \times 4 |
| 0 | 1 | 1 | 1 | Fline \times 3 |
| 1 | 0 | 0 | 0 | Fline \times 2 |
| 1 | 0 | 0 | 1 | Fline \times 1 |
| 1 | 0 | 1 | 0 | fosc / 4 |
| 1 | 0 | 1 | 1 | fosc / 6 |
| 1 | 1 | 0 | 0 | fosc / 8 |
| 1 | 1 | 0 | 1 | fosc / 10 |
| 1 | 1 | 1 | 0 | fosc / 12 |
| 1 | 1 | 1 | 1 | fosc / 16 |

* Fline = Line frequency

fosc = Internal oscillator frequency (~510KHz)

BT[2:0]: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power-supply voltage to be used.

| BT2 | BT1 | BT0 | V _{GH} output | V _{GL} output | V _{GH} booster ratio | V _{GL} booster ratio |
|-----|-----|-----|------------------------------|---------------------------------|-------------------------------|-------------------------------|
| 0 | 0 | 0 | $V_{CIX2} + 4 \times V_{CI}$ | $-(V_{CIX2} \times 3) + V_{CI}$ | +6 | -5 |
| 0 | 0 | 1 | $V_{CIX2} + 4 \times V_{CI}$ | $-(V_{GH}) + V_{CIX2}$ | +6 | -4 |
| 0 | 1 | 0 | $V_{CIX2} + 4 \times V_{CI}$ | $-(V_{GH})$ | +6 | -6 |
| 0 | 1 | 1 | $V_{CI} \times 5$ | $-(V_{GH})$ | +5 | -5 |
| 1 | 0 | 0 | $V_{CI} \times 5$ | $-(V_{GH}) + V_{CI}$ | +5 | -4 |
| 1 | 0 | 1 | $V_{CI} \times 5$ | $-(V_{GH}) + V_{CIX2}$ | +5 | -3 |
| 1 | 1 | 0 | $V_{CI} \times 4$ | $-(V_{GH})$ | +4 | -4 |
| 1 | 1 | 1 | $V_{CI} \times 4$ | $-(V_{GH}) + V_{CI}$ | +4 | -3 |

DC[3:0]: Set the step-up cycle of the step-up circuit for 262k-color mode ($CM = V_{SS}$). When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

| DC3 | DC2 | DC1 | DC0 | Step-up cycle |
|-----|-----|-----|-----|-------------------|
| 0 | 0 | 0 | 0 | Fline \times 24 |
| 0 | 0 | 0 | 1 | Fline \times 16 |
| 0 | 0 | 1 | 0 | Fline \times 12 |
| 0 | 0 | 1 | 1 | Fline \times 8 |
| 0 | 1 | 0 | 0 | Fline \times 6 |
| 0 | 1 | 0 | 1 | Fline \times 5 |
| 0 | 1 | 1 | 0 | Fline \times 4 |
| 0 | 1 | 1 | 1 | Fline \times 3 |
| 1 | 0 | 0 | 0 | Fline \times 2 |
| 1 | 0 | 0 | 1 | Fline \times 1 |
| 1 | 0 | 1 | 0 | fosc / 4 |
| 1 | 0 | 1 | 1 | fosc / 6 |
| 1 | 1 | 0 | 0 | fosc / 8 |
| 1 | 1 | 0 | 1 | fosc / 10 |
| 1 | 1 | 1 | 0 | fosc / 12 |
| 1 | 1 | 1 | 1 | fosc / 16 |

* Fline = Line frequency

fosc = Internal oscillator frequency (~510KHz)

AP[2:0]: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no display, such as when the system is in a sleep mode.

| AP2 | AP1 | AP0 | Op-amp power |
|-----|-----|-----|------------------|
| 0 | 0 | 0 | Least |
| 0 | 0 | 1 | Small |
| 0 | 1 | 0 | Small to medium |
| 0 | 1 | 1 | Medium |
| 1 | 0 | 0 | Medium to large |
| 1 | 0 | 1 | Large |
| 1 | 1 | 0 | Large to Maximum |
| 1 | 1 | 1 | Maximum |

Compare register (R05h-R06h) (POR = 0000h)

| Reg# | R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-----|----|------|------|------|------|------|------|-----|-----|------|------|------|------|------|------|-----|-----|
| R05h | W | 1 | CPR5 | CPR4 | CPR3 | CPR2 | CPR1 | CPR0 | 0 | 0 | CPG5 | CPG4 | CPG3 | CPG2 | CPG1 | CPG0 | 0 | 0 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R06h | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CPB5 | CPB4 | CPB3 | CPB2 | CPB1 | CPB0 | 0 | 0 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

CPR[5:0], CPG[5:0], CPB[5:0]: Set the value for the compare register, of which the data read out from the GDDRAM or data written to the GDDRAM by the microcomputer are compared. This function is not available in the external display interface mode. In the external display mode, make sure LG[2:0] = "000". CPR[5:0] compares the pins RR[5:0], CPG[5:0] compares the pins GG[5:0], and CPB[5:0] compares the pins BB[5:0]. Refer to Section 14 Interface Mapping for writing methods in RGB data.

Display Control (R07h) (POR = 0000h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | 0 | 0 | 0 | PT1 | PT0 | VLE2 | VLE1 | SPT | 0 | 0 | GON | DTE | CM | 0 | D1 | D0 |
| POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PT[1:0]: Normalize the source outputs when non-displayed area of the partial display is driven.

VLE[2:1]: When VLE1 = 1 or VLE2 = 1, a vertical scroll is performed in the 1st screen by taking data VL17-0 in R41h register. When VLE1 = 1 and VLE2 = 1, a vertical scroll is performed in the 1st and 2nd screen by VL1[8:0] and VL2[8:0] respectively.

SPT: When SPT = “1”, the 2-division LCD drive is performed.

CM: 8-color mode setting.

When CM = 1, 8-color mode is selected.

When CM = 0, 8-color mode is disable.

GON: Gate off level becomes VGH when GON = “0”.

DTE: When GON = “1” and DTE = “0”, all gate outputs become VGL. When GON = “1” and DTE = “1”, selected gate wire becomes VGH, and non-selected gate wires become VGL.

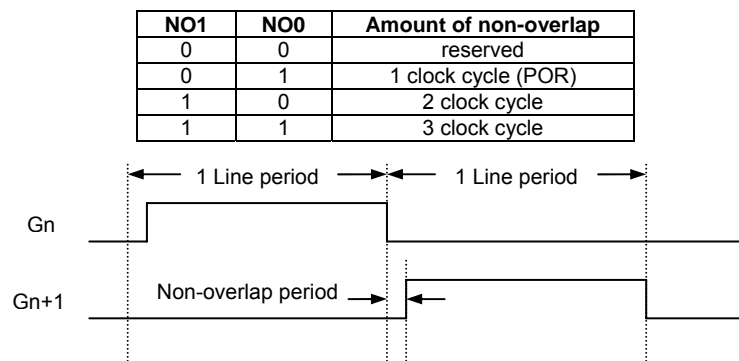
D[1:0]: Display is on when D1 = “1” and off when D1 = “0”. When off, the display data remains in the GDDRAM, and can be displayed instantly by setting D1 = “1”. When D1 = “0”, the display is off with all of the source outputs set to the GND level. Because of this, the driver can control the charging current for the LCD with AC driving. When D[1:0] = “01”, the internal display is performed although the display is off. When D[1:0] = “00”, the internal display operation halts and the display is off. Control the display on/off while control GON and DTE.

| GON | DTE | D1 | D0 | Internal Display Operation | Source output | Gate output |
|-----|-----|----|----|----------------------------|------------------------|--|
| 0 | 0 | 0 | 0 | Halt | GND | V _{GH} |
| 0 | 0 | 0 | 1 | Operation | GND | V _{GH} |
| 1 | 0 | 0 | 1 | Operation | GND | V _{G OFFL} |
| 1 | 0 | 1 | 1 | Operation | Grayscale level output | V _{G OFFL} |
| 1 | 1 | 1 | 1 | Operation | Grayscale level output | Selected gate line: V _{GH} Non-selected gate line: V _{G OFFL} |

Frame Cycle Control (R0Bh) (POR = 5308h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|------|------|------|------|------|------|------|------|
| W | 1 | NO1 | NO0 | SDT1 | SDT0 | 0 | EQ2 | EQ1 | EQ0 | DIV1 | DIV0 | SDIV | SRTN | RTN3 | RTN2 | RTN1 | RTN0 |
| POR | | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

NO[1:0]: Sets amount of non-overlap of the gate output.

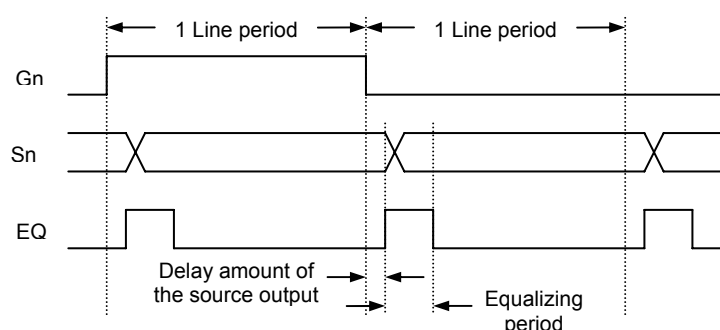


SDT[1:0]: Set delay amount from the gate output signal falling edge of the source outputs.

| SDT1 | SDT0 | Delay amount of the source output |
|------|------|-----------------------------------|
| 0 | 0 | 0 clock cycle |
| 0 | 1 | 1 clock cycle (POR) |
| 1 | 0 | 2 clock cycle |
| 1 | 1 | 3 clock cycle |

EQ[2:0]: Sets the equalizing period.

| EQ2 | EQ1 | EQ0 | EQ period |
|-----|-----|-----|---------------|
| 0 | 0 | 0 | No EQ |
| 0 | 0 | 1 | 2 clock cycle |
| 0 | 1 | 0 | 3 clock cycle |
| 0 | 1 | 1 | 4 clock cycle |
| 1 | 0 | 0 | 5 clock cycle |
| 1 | 0 | 1 | 6 clock cycle |
| 1 | 1 | 0 | 7 clock cycle |
| 1 | 1 | 1 | 8 clock cycle |



DIV[1:0]: Set the division ratio of clocks for internal operation. Internal operations are driven by clocks which frequency is divided according to the DIV1-0 setting.

| DIV1 | DIV0 | Division Ratio |
|------|------|----------------|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 8 |

* fosc = internal oscillator frequency, ~510kHz

SDIV: When SDIV = 1, DIV1-0 value will be count. When SDIV = 0, DIV1-0 value will be auto determined.

SRTN: When SRTN=1, RTN3-0 value will be count. When SRTN = 0, RTN3-0 value will be auto determined.

RTN[3:0]: Set the no. of clocks in each line. The total number will be the decimal value of RTN3-0 plus 16. e.g. if RTN3-0 = "1010h", the total number of clocks in each line = 10 +16 = 26 clocks.

Frame frequency calculation

For DMode[1:0] = '00'

$$\text{Frame_frequency} = \frac{F_{osc}}{\text{div} \times (\text{rtn} + 16) \times (\text{mux} + \text{vbp} + \text{vfp} + 3)}$$

where F_{osc} = internal oscillator frequency
 div = Division ratio determined by DIV[1:0]
 rtn = RTN[3:0]
 mux = MUX[8:0]
 vbp = VBP[7:0]
 vfp = VFT[7:0]

for default values of SSD1289

$F_{osc} = \sim 510\text{KHz}$, DIV[1:0] = '00', RTN[3:0] = 8, MUX[8:0] = 319, VBP[7:0] = 3, VFP[7:0] = 1,

$$\text{Frame frequency} = \frac{510K}{1 \times (8 + 16) \times (319 + 3 + 1 + 3)} = \frac{510K}{1 \times 24 \times 326} = 65\text{Hz}$$

Power Control 2 (R0Ch) (POR = 0004h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|------|------|------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VRC2 | VRC1 | VRC0 |
| POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

VRC[2:0]: Adjust VCIX2 output voltage. The adjusted level is indicated in the chart below VRC2-0 setting.

| VRC2 | VRC1 | VRC0 | VCIX2 voltage |
|------|------|------|---------------|
| 0 | 0 | 0 | 5.1V |
| 0 | 0 | 1 | 5.2V |
| 0 | 1 | 0 | 5.3V |
| 0 | 1 | 1 | 5.4V |
| 1 | 0 | 0 | 5.5V |
| 1 | 0 | 1 | 5.6V |
| 1 | 1 | 0 | 5.7V |
| 1 | 1 | 1 | 5.8V |

Note: The above setting is valid when VCI has high enough voltage supply for boosting up the required voltage.
The above setting is assumed 100% booster efficiency. Please refer to DC Characteristics for detail.

Power Control 3 (R0Dh) (POR = 0009h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|------|------|------|------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VRH3 | VRH2 | VRH1 | VRH0 |
| POR* | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

*note: this POR value is for GAMAS[2:0] = 000, for POR values of all GAMAS[2:0] setting please refer to Table 5.

VRH[3:0]: Set amplitude magnification of V_{LCD63} . These bits amplify the V_{LCD63} voltage 1.54 to 2.725 times the Vref voltage set by VRH[3:0].

| VRH3 | VRH2 | VRH1 | VRH0 | V_{LCD63} Voltage |
|------|------|------|------|---------------------|
| 0 | 0 | 0 | 0 | Vref x 1.540 |
| 0 | 0 | 0 | 1 | Vref x 1.620 |
| 0 | 0 | 1 | 0 | Vref x 1.700 |
| 0 | 0 | 1 | 1 | Vref x 1.780 |
| 0 | 1 | 0 | 0 | Vref x 1.850 |
| 0 | 1 | 0 | 1 | Vref x 1.930 |
| 0 | 1 | 1 | 0 | Vref x 2.020 |
| 0 | 1 | 1 | 1 | Vref x 2.090 |
| 1 | 0 | 0 | 0 | Vref x 2.165 |
| 1 | 0 | 0 | 1 | Vref x 2.245 |
| 1 | 0 | 1 | 0 | Vref x 2.335 |
| 1 | 0 | 1 | 1 | Vref x 2.400 |
| 1 | 1 | 0 | 0 | Vref x 2.500 |
| 1 | 1 | 0 | 1 | Vref x 2.570 |
| 1 | 1 | 1 | 0 | Vref x 2.645 |
| 1 | 1 | 1 | 1 | Vref x 2.725 |

*Vref is the internal reference voltage equals to 2.0V.

Power Control 4 (R0Eh) (POR = 3200h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|----|------|------|-------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | 0 | 0 | VCOMG | VDV4 | VDV3 | VDV2 | VDV1 | VDV0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| POR* | | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

*note: this POR value is for GAMAS[2:0] = 000, for POR values of all GAMAS[2:0] setting please refer to Table 5.

VcomG: When VcomG = “1”, it is possible to set output voltage of VcomL to any level, and the instruction (VDV4-0) becomes available. When VcomG = “0”, VcomL output is fixed to Hi-z level, VCIM output for VcomL power supply stops, and the instruction (VDV4-0) becomes unavailable. Set VcomG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV[4:0]: Set the alternating amplitudes of Vcom at the Vcom alternating drive. These bits amplify 0.6 to 1.23 times the VLCD63 voltage. When VcomG = “0”, the settings become invalid. External voltage at VcomR is referenced when VDH = “01111”.

$$VCOML = 0.9475 * VCOMH - VCOMA$$

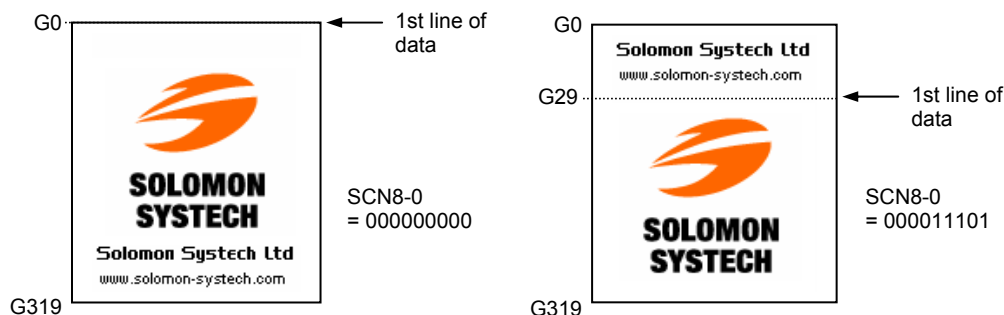
| VDV4 | VDV3 | VDV2 | VDV1 | VDV0 | Vcom Amplitude |
|------|------|------|------|------|---|
| 0 | 0 | 0 | 0 | 0 | VLCD63 x 0.60 |
| 0 | 0 | 0 | 0 | 1 | VLCD63 x 0.63 |
| 0 | 0 | 0 | 1 | 0 | VLCD63 x 0.66 |
| : | | | | | : |
| : | | | | | Step = 0.03 |
| : | | | | | : |
| 0 | 1 | 1 | 0 | 1 | VLCD63 x 0.99 |
| 0 | 1 | 1 | 1 | 0 | VLCD63 x 1.02 |
| 0 | 1 | 1 | 1 | 1 | Reference from external variable resistor |
| 1 | 0 | 0 | 0 | 0 | VLCD63 x 1.05 |
| 1 | 0 | 0 | 0 | 1 | VLCD63 x 1.08 |
| : | | | | | : |
| : | | | | | Step = 0.03 |
| : | | | | | : |
| 1 | 0 | 1 | 0 | 1 | VLCD63 x 1.20 |
| 1 | 0 | 1 | 1 | 0 | VLCD63 x 1.23 |
| 1 | 0 | 1 | 1 | 1 | Reserved |
| 1 | 1 | * | * | * | Reserved |

Note: Vcom amplitude < 5.5V

Gate Scan Position (R0Fh) (POR = 0000h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|------|------|------|------|------|------|------|------|------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SCN8 | SCN7 | SCN6 | SCN5 | SCN4 | SCN3 | SCN2 | SCN1 | SCN0 |
| POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SCN[8:0]: Set the scanning starting position of the gate driver. The valid range is from 0 to 319.



Sleep mode (R10h) (POR = 0001h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLP |
| POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

SLP: Sleep mode enable bit. In the sleep mode, the internal display operations are halted except the R-C oscillator to reduce current consumption. No change in the GDDRAM data or instructions during the sleep mode is made, although it is retained.

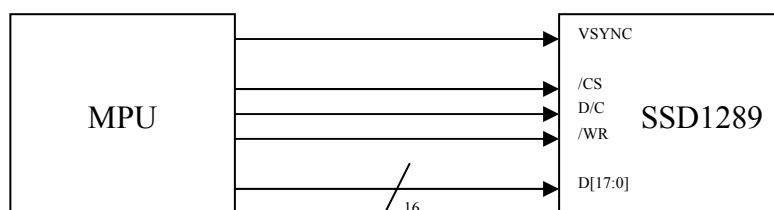
When SLP = 1, the driver enters into the sleep mode.

When SLP = 0, the driver leaves the sleep mode.

Entry Mode (R11h) (POR = 6830h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|--------|------|------|-------|-------|-------|--------|--------|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | VSMODE | DFM1 | DFM0 | TRANS | OEDef | WMode | DMode1 | DMode0 | TY1 | TY0 | ID1 | ID0 | AM | LG2 | LG1 | LG0 |
| POR | | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

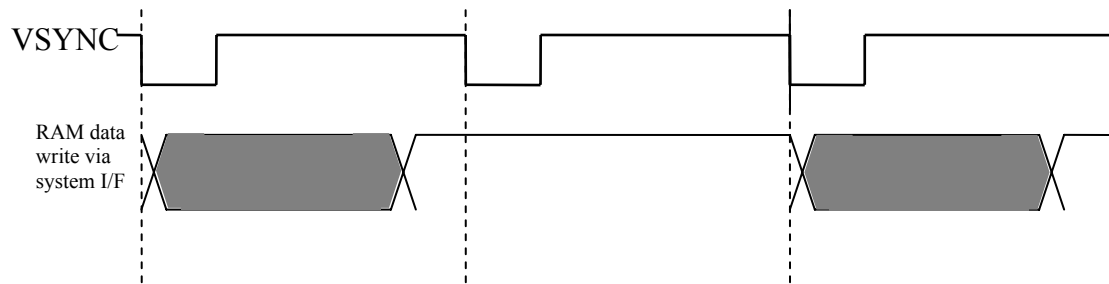
VSMODE: When VSMODE = 1 at DMode[1:0] = "00", the frame frequency will be dependent on VSYNC.



In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed (internal display operation speed + buffer), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the SSD1289 rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display.

Therefore, the SSD1289 can write data via VSYNC interface in high speed with low power consumption.



The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$Fosc[Hz] = Frame_frequency * (mux + vfp + vbp + 3) * (rtn + 16) * (div)$$

$$RAMWriteSpeed(min)[Hz] > \frac{240 * mux}{(vbp + mux - margins) * (rtn + 16) * \frac{1}{fosc}}$$

where $Fosc$ = internal oscillator frequency
 div = Division ratio determined by DIV[1:0]
 rtn = RTN[3:0]
 mux = MUX[8:0]
 vbp = VBP[7:0]
 vfp = VFT[7:0]

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

DFM[1:0]: Set the color display mode.

| DFM1 | DFM0 | Color mode |
|------|------|-----------------|
| 1 | 1 | 65k color (POR) |
| 1 | 0 | 262k color |

TRANS: When TRANS = 1, transparent display is allowed during DMode[1:0] = “1x”.

OEDef:

When OEDef = 1, OE defines the display window.
 When OEDef = 0, the display window is defined by R4Eh and R4Fh.

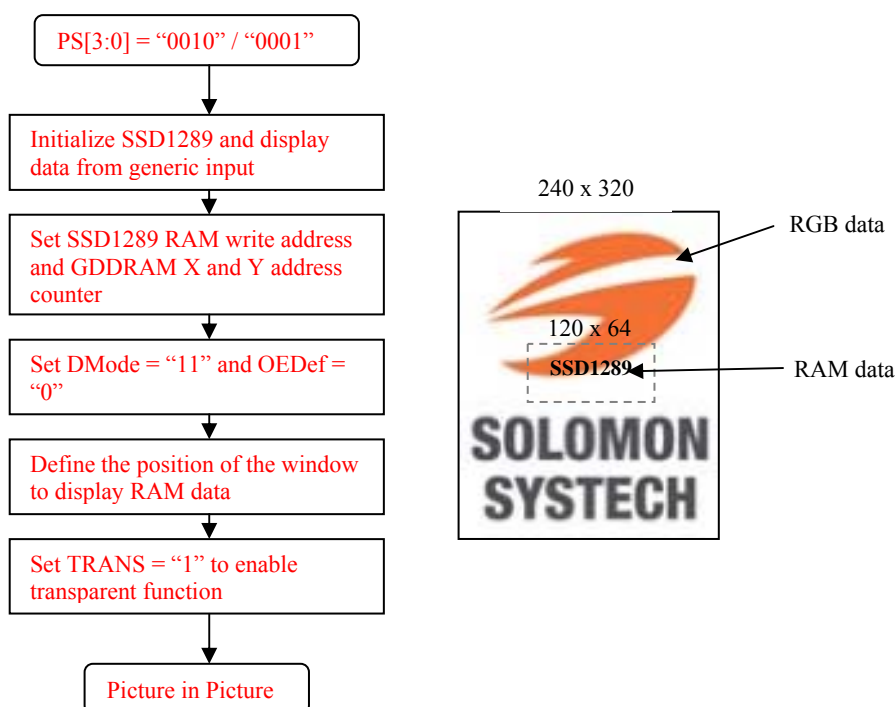
WMode: Select the source of data to write in the RAM.

| WMode | Write RAM from |
|-------|-----------------------|
| 0 | Normal data bus (POR) |
| 1 | Generic interface |

DMode[1:0]: SSD1289 allows data display from RAM data or from generic input data. When DMode[1:0] = “00”, it displays the ram content. When DMode[1:0] = “01”, it displays from generic input data.

| DMode1 | DMode0 | Display | Remark |
|--------|--------|----------------------|--|
| 0 | 0 | Ram (POR) | Frame frequency depends on Fosc (POR) |
| 0 | 1 | Generic input | Frame frequency depends on VSYNC, default DMode setting in RGB interface |
| 1 | 0 | RAM and Generic data | In this case, generic data is shown in the display window |
| 1 | 1 | RAM and Generic data | In this case, RAM data is shown in the display window |

Picture In Picture Function



TY[1:0]: In 262k color mode, 16 bit parallel interface, there are three types of methods in writing data into the ram, Type A, B and C are described as below.


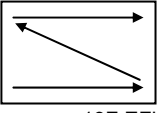
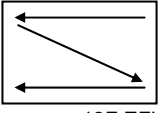
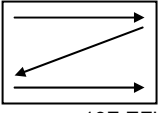
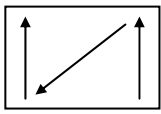
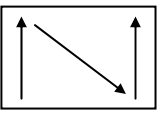
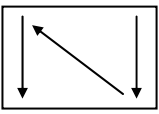
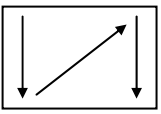
| TY1 | TY0 | Writing mode |
|-----|-----|--------------|
| 0 | 0 | Type A |
| 0 | 1 | Type B |
| 1 | 0 | Type C |

| | | | Hardware pins | | | | | | | | | | | | | | | | | |
|-----------|-------------|-----------------|---------------|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| Interface | Color mode | Cycle | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 16 bit | 262k Type A | 1 st | R5 | R4 | R3 | R2 | R1 | R0 | x | x | | G5 | G4 | G3 | G2 | G1 | G0 | x | x | |
| | | 2 nd | B5 | G4 | B3 | B2 | B1 | B0 | x | x | | R5 | R4 | R3 | R2 | R1 | R0 | x | x | |
| | | 3 rd | G5 | G4 | G3 | G2 | G1 | G0 | x | x | | B5 | G4 | B3 | B2 | B1 | B0 | x | x | |
| | 262k Type B | 1 st | R5 | R4 | R3 | R2 | R1 | R0 | x | x | | G5 | G4 | G3 | G2 | G1 | G0 | x | x | |
| | | 2 nd | x | x | x | x | x | x | x | x | | B5 | G4 | B3 | B2 | B1 | B0 | x | x | |
| | 262k Type C | 1 st | R5 | R4 | R3 | R2 | R1 | R0 | x | x | | G5 | G4 | G3 | G2 | G1 | G0 | x | x | |
| | | 2 nd | B5 | G4 | B3 | B2 | B1 | B0 | x | x | | x | x | x | x | x | x | x | x | |

Remark : x Don't care bits
 Not connected pins

ID[1:0]: The address counter is automatically incremented by 1, after data are written to the GDDRAM when ID[1:0] = “1”. The address counter is automatically decremented by 1, after data are written to the GDDRAM when ID[1:0] = “0”. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data are written to the GDDRAM is set with AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the GDDRAM. When AM = “0”, the address counter is updated in the horizontal direction. When AM = “1”, the address counter is updated in the vertical direction. When window addresses are selected, data are written to the GDDRAM area specified by the window addresses in the manner specified with ID1-0 and AM bits.

| | ID[1:0]="00" Horizontal: decrement Vertical: decrement | ID[1:0]="01" Horizontal: increment Vertical: decrement | ID[1:0]="10" Horizontal: decrement Vertical: increment | ID[1:0]="11" Horizontal: increment Vertical: increment |
|----------------------|--|--|---|--|
| AM="0" Horizontal | 00,00h  13F,EFh | 00,00h  13F,EFh | 00,00h  13F,EFh | 00,00h  13F,EFh |
| AM="1" Vertical | 00,00h  13F,EFh | 00,00h  13F,EFh | 00,00h  13F,EFh | 00,00h  13F,EFh |

LG[2:0]: Write data to the GDDRAM after comparing the write data written to the GDDRAM by the microcomputer with the values in the compare registers (CPR[5:0], CPG[5:0], CPB[5:0]) and performing a logical and arithmetic operation on them.

Generic Interface Control (R15h) (POR = 00d0h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|--------|---------|-------|-------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | INVDOT | INV DEN | INVHS | INVVS |
| POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

INVDOT: sets the signal polarity of DOTCLK pin. When INVDOT = 1, set DOTCLK is negative edge trigger.

INV DEN: sets the signal polarity of DEN pin. When INV DEN = 1, set DEN is active low.

INVHS: sets the signal polarity of HSYNC pin. When INVHS = 1, set inverse polarity of HSYNC.

INVVS: sets the signal polarity of VSYNC pin. When INVVS = 1, set inverse polarity of VSYNC.

Horizontal Porph (R16h) (POR = EF1Ch)

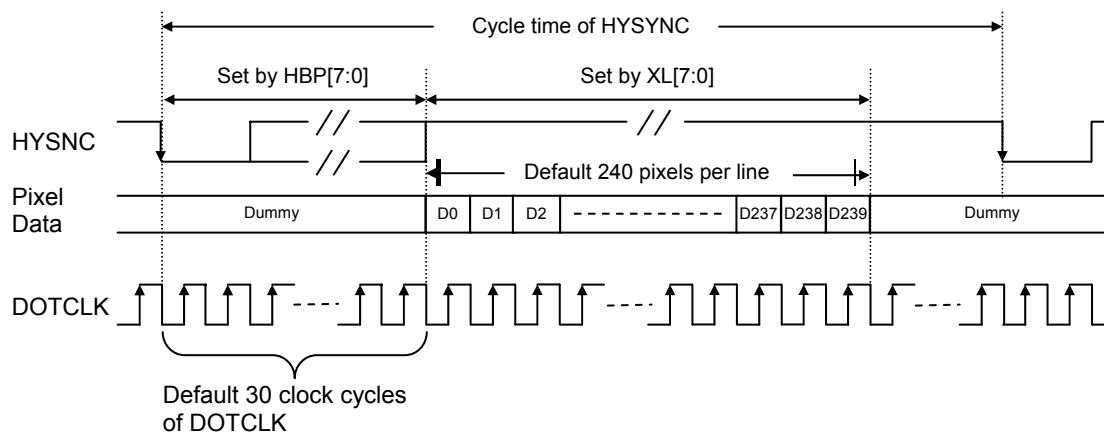
| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|------|------|------|------|------|------|------|------|
| W | 1 | XL7 | XL6 | XL5 | XL4 | XL3 | XL2 | XL1 | XL0 | HBP7 | HBP6 | HBP5 | HBP4 | HBP3 | HBP2 | HBP1 | HBP0 |

XL[7:0]: Set the number of valid pixel per line. Number of valid pixel per line is equal to **XL[7:0] + 1**

| XL7 | XL6 | XL5 | XL4 | XL3 | XL2 | XL1 | XL0 | No. of pixel per line |
|----------|-----|-----|-----|-----|-----|-----|-----|-----------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 3 |
| ⋮ | | | | | | | | ⋮ |
| Step = 1 | | | | | | | | ⋮ |
| | | | | | | | | ⋮ |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 239 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 240 (POR) |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Reserved |
| 1 | 1 | 1 | 1 | * | * | * | * | Reserved |

HBP[7:0]: Set the delay period from falling edge of HSYNC signal to first valid data. The pixel data exceed the range set by XL[7:0] and before the first valid data will be treated as dummy data.

| HBP7 | HBP6 | HBP5 | HBP4 | HBP3 | HBP2 | HBP1 | HBP0 | No. of clock cycle of DOTCLK |
|----------|------|------|------|------|------|------|------|------------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 3 |
| ⋮ | | | | | | | | ⋮ |
| Step = 1 | | | | | | | | ⋮ |
| | | | | | | | | ⋮ |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 28 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 29 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 30 (POR) |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 31 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 32 |
| ⋮ | | | | | | | | ⋮ |
| Step = 1 | | | | | | | | ⋮ |
| | | | | | | | | ⋮ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 256 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 257 |



Vertical Porph (R17h) (POR = 0103h)

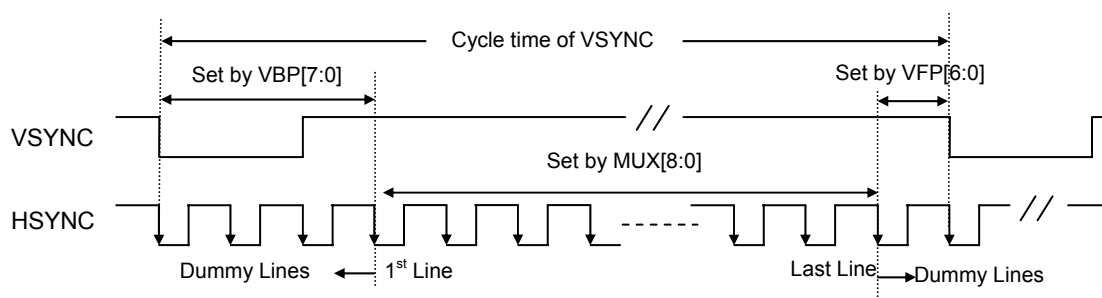
| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| W | 1 | 0 | VFP6 | VFP5 | VFP4 | VFP3 | VFP2 | VFP1 | VFP0 | VBP7 | VBP6 | VBP5 | VBP4 | VBP3 | VBP2 | VBP1 | VBP0 |
| POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

VFP[6:0]: Set the delay period from the last valid line to the falling edge of VSYNC of the next frame. The line data within this delay period will be treated as dummy line.

| VFP6 | VFP5 | VFP4 | VFP3 | VFP2 | VFP1 | VFP0 | No. of clock cycle of HSYNC |
|------|------|------|------|------|------|------|-----------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 (POR) |
| : | : | | | | | | Step = 1 |
| : | : | | | | | | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 127 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 128 |

VBP[7:0]: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line.

| VBP7 | VBP6 | VBP5 | VBP4 | VBP3 | VBP2 | VBP1 | VBP0 | No. of clock cycle of HSYNC |
|------|------|------|------|------|------|------|------|-----------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 4 (POR) |
| : | : | : | : | : | : | : | : | Step = 1 |
| : | : | : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 255 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 256 |



Power Control 5 (R1Eh) (POR = 0029h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|----|------|------|------|------|------|------|-----|-----|------|-----|------|------|------|------|------|------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | nOTP | 0 | VCm5 | VCm4 | VCm3 | VCm2 | VCm1 | VCm0 |
| POR* | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |

*note: this POR value is for GAMAS[2:0] = 000, for POR values of all GAMAS[2:0] setting please refer to Table 5.

nOTP: nOTP equals to “0” after power on reset and VcomH voltage equals to programmed OTP value. When nOTP set to “1”, setting of VCM[5:0] becomes valid and voltage of VcomH can be adjusted.

VCm[5:0]: Set the VcomH voltage if nOTP = “1”. These bits amplify the VcomH voltage 0.35 to 0.99 times the VLCD63 voltage. Default value is “101001” when power on reset.

| VCm5 | VCm4 | VCm3 | VCm2 | VCm1 | VCm0 | VcomH |
|------|------|------|------|------|------|---------------|
| 0 | 0 | 0 | 0 | 0 | 0 | VLCD63 x 0.35 |
| 0 | 0 | 0 | 0 | 0 | 1 | VLCD63 x 0.36 |
| | | | | | | ⋮ |
| | | | | | | Step = 0.01 |
| | | | | | | ⋮ |
| 1 | 1 | 1 | 1 | 1 | 0 | VLCD63 x 0.98 |
| 1 | 1 | 1 | 1 | 1 | 1 | VLCD63 x 0.99 |

Write Data to GRAM (R22h)

| R/W | DC | D[17:0] |
|-----|----|---|
| W | 1 | WD[17:0] mapping depends on the interface setting |

WD[17:0]: Transforms all the GDDRAM data into 18-bit, and writes the data. Format for transforming data into 18-bit depends on the interface used. SSD1289 selects the grayscale level according to the GDDRAM data. After writing data to GDDRAM, address is automatically updated according to AM bit and ID bit. Access to GDDRAM during stand-by mode is not available.

Read Data from GRAM (R22h)

| R/W | DC | D[17:0] |
|-----|----|---|
| R | 1 | RD[17:0] mapping depends on the interface setting |

RD[17:0]: Read 18-bit data from the GDDRAM. When the data is read to the microcomputer, the first-word read immediately after the GDDRAM address setting is latched from the GDDRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal. When bit processing, such as a logical operation, is performed, only one read can be processed since the latched data in the first word is used.

RAM write data mask (R23h – R24h) (POR = 0000h)

| Reg# | R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-----|----|------|------|------|------|------|------|-----|-----|------|------|------|------|------|------|-----|-----|
| R23h | W | 1 | WMR5 | WMR4 | WMR3 | WMR2 | WMR1 | WMR0 | 0 | 0 | WMG5 | WMG4 | WMG3 | WMG2 | WMG1 | WMG0 | 0 | 0 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R24h | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | WMB5 | WMB4 | WMB3 | WMB2 | WMB1 | WMB0 | 0 | 0 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

WMR[5:0], WMG[5:0], WMB[5:0]: In writing to the GDDRAM, these bits write-mask the data to be written to the GDDRAM by a bit unit. For example, if WMR5 = 1, the WMR5 write-mask is enabled and data RR5 will be masked and not write into the GDDRAM. WMR[5:0] mask pins RR[5:0], WMG[5:0] mask pins GG[5:0], and WMB[5:0] mask pins BB[5:0]. For writing GDDRAM methods, refer to Section 14 Interface Mapping”.

Frame Frequency Control (R25h) (POR = 8000h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | OSC3 | OSC2 | OSC1 | OSC0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| POR* | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

OSC[3:0]: Set the frame frequency by OSC[3:0]

| OSC[3:0] | Internal Oscillator Frequency (Hz) | Corresponding Frame Freq (Hz) (other registers are at POR value) |
|----------|------------------------------------|---|
| 0000 | 390K | 50 |
| 0010 | 430K | 55 |
| 0101 | 470K | 60 |
| 1000 | 510K | 65 |
| 1010 | 548K | 70 |
| 1100 | 587K | 75 |
| 1110 | 626K | 80 |

Vcom OTP (R28h – R29h)

| Reg# | R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-----|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R28h | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| R29h | W | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

When OTP is access, these registers must be set accordantly.

OTP programming sequence

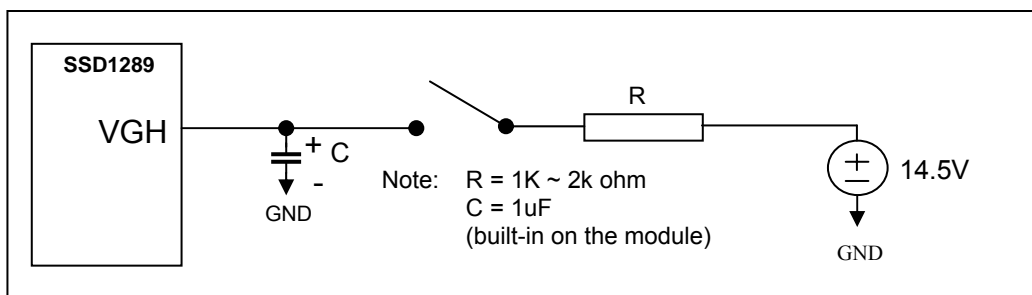
| Step | Operation | | | | | | | | |
|-------|---|-------|-------|------|--------|------|--------|------|--------|
| 1 | Power up the module at VCI = 2.7V, VDDEXT = VDDIO = 1.8V. Turn on the display as normal to 65k/262k color mode (displaying a test pattern if any). | | | | | | | | |
| 2 | Set nOTP to "1" (R1Eh) and optimizes VcomH by adjusting VCM[5:0] (R1Eh). | | | | | | | | |
| 3 | Power down the whole module. | | | | | | | | |
| 4 | Connect a supply to the module at VCI = 2.7V, VDDEXT = VDDIO = 1.8V | | | | | | | | |
| 5 | Write below commands for OTP initialization and wait for 200ms for activate the OTP : <table border="1" data-bbox="635 1352 995 1482"> <tr> <th>Index</th><th>Value</th></tr> <tr> <td>R00h</td><td>0x0001</td></tr> <tr> <td>R28h</td><td>0x0006</td></tr> <tr> <td>R29h</td><td>0x80C0</td></tr> </table> <p>Connect a 14.5V supply to VGH through a current limiting resistor, see figure below.</p> | Index | Value | R00h | 0x0001 | R28h | 0x0006 | R29h | 0x80C0 |
| Index | Value | | | | | | | | |
| R00h | 0x0001 | | | | | | | | |
| R28h | 0x0006 | | | | | | | | |
| R29h | 0x80C0 | | | | | | | | |
| 6 | Write the optimized value found in Step 2 to VCM[5:0] (R1Eh) and set nOTP to "1". | | | | | | | | |
| 7 | Fire the OTP by write HEX code "000Ah" to register R28h. | | | | | | | | |
| 8 | Wait 500ms. | | | | | | | | |
| 9 | OTP complete. Power down the whole module and remove 14.5V supply. | | | | | | | | |

Note: nOTP must set to "0" to activate the OTP effect.

Precaution:

1. All capacitors on OTP machine should be discharged completely before placing the LCD module.
2. The OTP programming voltage should not be applied when placing and removing the LCD module.
3. The OTP programming voltage should not be applied before VDDIO/VDDEXT/VCI.
4. After OTP is finished, the capacitors at VGH and VCIX2 must be discharged completely before removing the LCD module.

Figure 9-3 – OTP circuitry



Gamma Control (R30h to R3Bh)

| Reg# | R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-----|----|------|------|------|--------|--------|--------|--------|--------|-----|-----|-----|-----|--------|--------|--------|--------|
| R30h | W | 1 | 0 | 0 | 0 | 0 | 0 | PKP 12 | PKP 11 | PKP 10 | 0 | 0 | 0 | 0 | 0 | PKP 02 | PKP 01 | PKP 00 |
| R31h | W | 1 | 0 | 0 | 0 | 0 | 0 | PKP 32 | PKP 31 | PKP 30 | 0 | 0 | 0 | 0 | 0 | PKP 22 | PKP 21 | PKP 20 |
| R32h | W | 1 | 0 | 0 | 0 | 0 | 0 | PKP 52 | PKP 51 | PKP 50 | 0 | 0 | 0 | 0 | 0 | PKP 42 | PKP 41 | PKP 40 |
| R33h | W | 1 | 0 | 0 | 0 | 0 | 0 | PRP 12 | PRP 11 | PRP 10 | 0 | 0 | 0 | 0 | 0 | PRP 02 | PRP 01 | PRP 00 |
| R34h | W | 1 | 0 | 0 | 0 | 0 | 0 | PKN 12 | PKN 11 | PKN 10 | 0 | 0 | 0 | 0 | 0 | PKN 02 | PKN 01 | PKN 00 |
| R35h | W | 1 | 0 | 0 | 0 | 0 | 0 | PKN 32 | PKN 31 | PKN 30 | 0 | 0 | 0 | 0 | 0 | PKN 22 | PKN 21 | PKN 20 |
| R36h | W | 1 | 0 | 0 | 0 | 0 | 0 | PKN 52 | PKN 51 | PKN 50 | 0 | 0 | 0 | 0 | 0 | PKN 42 | PKN 41 | PKN 40 |
| R37h | W | 1 | 0 | 0 | 0 | 0 | 0 | PRN 12 | PRN 11 | PRN 10 | 0 | 0 | 0 | 0 | 0 | PRN 02 | PRN 01 | PRN 00 |
| R3Ah | W | 1 | 0 | 0 | 0 | VRP 14 | VRP 13 | VRP 12 | VRP 11 | VRP 10 | 0 | 0 | 0 | 0 | VRP 03 | VRP 02 | VRP 01 | VRP 00 |
| R3Bh | W | 1 | 0 | 0 | 0 | VRN 14 | VRN 13 | VRN 12 | VRN 11 | VRN 10 | 0 | 0 | 0 | 0 | VRN 03 | VRN 02 | VRN 01 | VRN 00 |

Note: please refer to table 5 for POR values.

PKP[52:00]: Gamma micro adjustment register for the positive polarity output

PRP[12:00]: Gradient adjustment register for the positive polarity output

VRP[14:00]: Adjustment register for amplification adjustment of the positive polarity output

PKN[52:00]: Gamma micro adjustment register for the negative polarity output

PRN[12:00]: Gradient adjustment register for the negative polarity output

VRN[14:00]: Adjustment register for the amplification adjustment of the negative polarity output.
(For details, see the Section 11 Gamma Adjustment Function).

Vertical Scroll Control (R41h-R42h) (POR = 0000h)

| Reg# | R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-----|----|------|------|------|------|------|------|-----|------|------|------|------|------|------|------|------|------|
| R41h | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VL18 | VL17 | VL16 | VL15 | VL14 | VL13 | VL12 | VL11 | VL10 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R42h | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VL28 | VL27 | VL26 | VL25 | VL24 | VL23 | VL22 | VL21 | VL20 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VL1[8:0]: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the first to 320th can be scrolled for the number of the raster-row. After 320th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL1[8:0]) is valid when VLE1 = “1” or VLE2 = “1”. The raster-row display is fixed when VLE[2:1] = “00”.

VL2[8:0]: Specify scroll length at the scroll display for vertical smooth scrolling at 2nd screen. The display-start raster-row (VL2[8:0]) is valid when VLE1 = “1” and VLE2 = “1”.

Horizontal RAM address position (R44h) (POR = EF00h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| W | 1 | HEA7 | HEA6 | HEA5 | HEA4 | HEA3 | HEA2 | HEA1 | HEA0 | HSA7 | HSA6 | HSA5 | HSA4 | HSA3 | HSA2 | HSA1 | HSA0 |
| POR | | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

HSA[7:0]/HEA[7:0]: Specify the start/end positions of the window address in the horizontal direction by an address unit. Data are written to the GDDRAM within the area determined by the addresses specified by HEA[7:0] and HSA[7:0]. These addresses must be set before the RAM write. In setting these bits, make sure that “00”h ≤ HSA[7:0] ≤ HEA[7:0] ≤ “EF”h.

Vertical RAM address position (R45h-R46h)

| Reg# | R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-----|----|------|------|------|------|------|------|-----|------|------|------|------|------|------|------|------|------|
| R45h | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VSA8 | VSA7 | VSA6 | VSA5 | VSA4 | VSA3 | VSA2 | VSA1 | VSA0 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R46h | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VEA8 | VEA7 | VEA6 | VEA5 | VEA4 | VEA3 | VEA2 | VEA1 | VEA0 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

VSA[8:0]/VEA[8:0]: Specify the start/end positions of the window address in the vertical direction by an address unit. Data are written to the GRAM within the area determined by the addresses specified by VEA[8:0] and VSA[8:0]. These addresses must be set before the RAM write. In setting these bits, make sure that “00”h ≤ VSA[8:0] ≤ VEA[8:0] ≤ “13F”h.

1st Screen driving position (R48h-R49h)

| Reg# | R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-----|----|------|------|------|------|------|------|-----|------|------|------|------|------|------|------|------|------|
| R48h | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SS18 | SS17 | SS16 | SS15 | SS14 | SS13 | SS12 | SS11 | SS10 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R49h | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SE18 | SE17 | SE16 | SE15 | SE14 | SE13 | SE12 | SE11 | SE10 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

SS1[8:0]: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the set gate driver, i.e. the first driving Gate is G0 if SS1[8:0] = 00H

SE1[8:0]: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the set gate driver. For instance, when SS1[8:0] = “07”H and SE1[8:0] = “10”H are set, the LCD driving is performed from G7 to G16, and non-selection driving is performed for G1 to G6, G17, and others. Ensure that SS1[8:0] ≤ SE1[8:0] ≤ 13FH.

2nd Screen driving position (R4Ah-R4Bh)

| Reg# | R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-----|----|------|------|------|------|------|------|-----|------|------|------|------|------|------|------|------|------|
| R4Ah | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SS28 | SS27 | SS26 | SS25 | SS24 | SS23 | SS22 | SS21 | SS20 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R4Bh | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SE28 | SE27 | SE26 | SE25 | SE24 | SE23 | SE22 | SE21 | SE20 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

SS2[8:0]: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the set gate driver. The second screen is driven when SPT = “1”.

SE2[8:0]: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the set gate driver. For instance, when SPT = “1”, SS2[8:0] = “20”H, and SE2[8:0] = “2F”H are set, the LCD driving is performed from G32 to G47. Ensure that SS1[8:0] ≤ SE1[8:0] ; SS2[8:0] ≤ SE2[8:0] ≤ 13FH.

RAM address set (R4Eh-R4Fh)

| Reg# | R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|------|-----|----|------|------|------|------|------|------|-----|------|------|------|------|------|------|------|------|------|
| R4Eh | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | XAD7 | XAD6 | XAD5 | XAD4 | XAD3 | XAD2 | XAD1 | XAD0 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R4Fh | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | YAD8 | YAD7 | YAD6 | YAD5 | YAD4 | YAD3 | YAD2 | YAD1 | YAD0 |
| | POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

XAD[7:0]: Make initial settings for the GDDRAM X address in the address counter (AC).

YAD[8:0]: Make initial settings for the GDDRAM Y address in the address counter (AC).

After GDDRAM data are written, the address counter is automatically updated according to the settings with AM, I/D bits and setting for a new GDDRAM address is not required in the address counter. Therefore, data are written consecutively without setting an address. The address counter is not automatically updated when data are read out from the GDDRAM. GDDRAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses.

Window Address Function

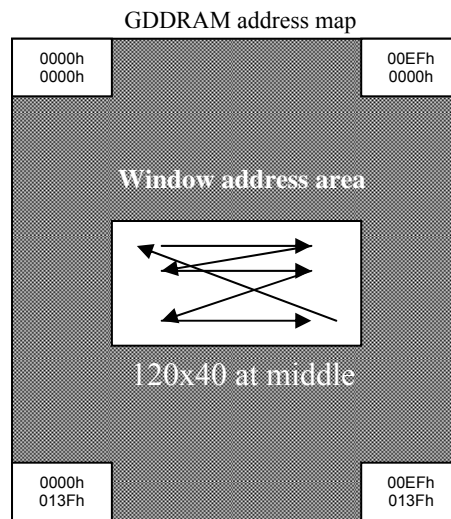
The window address function enables writing display data sequentially in a window address area made in the internal GDDRAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and ID[1:0] bits set the transition direction of RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the SSD1289 to write data including image data sequentially without taking the data wrap position into account. The window address area must be made within the GDDRAM address map area.

Condition:

$00h \leq HSA[7:0] \leq HEA[7:0] \leq EFh$

$00h \leq VSA[8:0] \leq VEA[8:0] \leq 13Fh$

AM and ID[1:0] refer to R11h



Window address setting area:

HSA[7:0] = 3Bh; HEA[7:0] = B3h

VSA[8:0] = 8Bh; VEA[8:0] = B3h

AM = "0" and ID[1:] = "11"

Partial Display Mode

The SSD1289 enables to selectively drive two screens at arbitrary positions with the screen-driving position registers (R48h to R4Bh). Only the lines required to display two screens at arbitrary positions are selectively driven to reduce the power consumption.

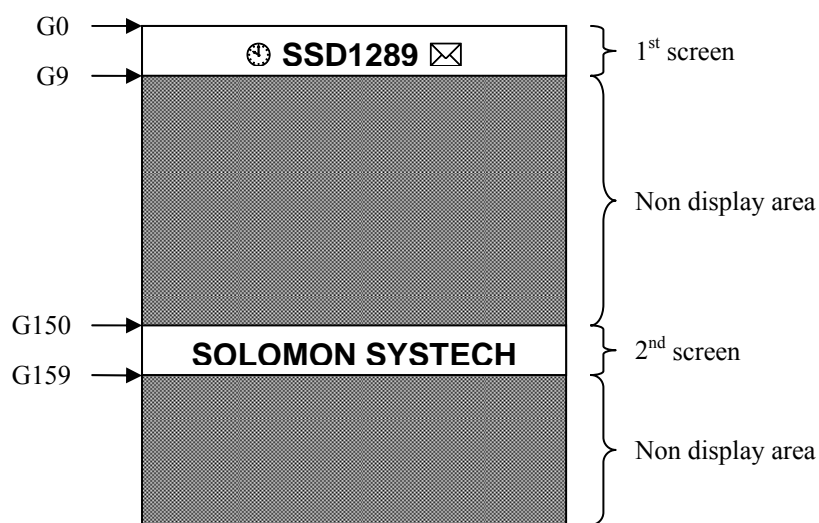
The first screen driving position registers (R48 and R49) specifies the start line (SS18-10) and the end line (SE18-10) for displaying the first screen. The second screen driving position register (R4A) specifies the start line (SS28-20) and the end line (SE28-20) for displaying the second screen. The second screen control is effective when the SPT bit is set to 1. The total number of lines driven for displaying the first and second screens must be less than the number of lines to drive the LCD.

Condition:

$SS1[8:0] \leq SE1[8:0] \leq 13FH$

$SS1[8:0] \leq SE1[8:0]$

$SS2[8:0] \leq SE2[8:0] \leq 13FH$



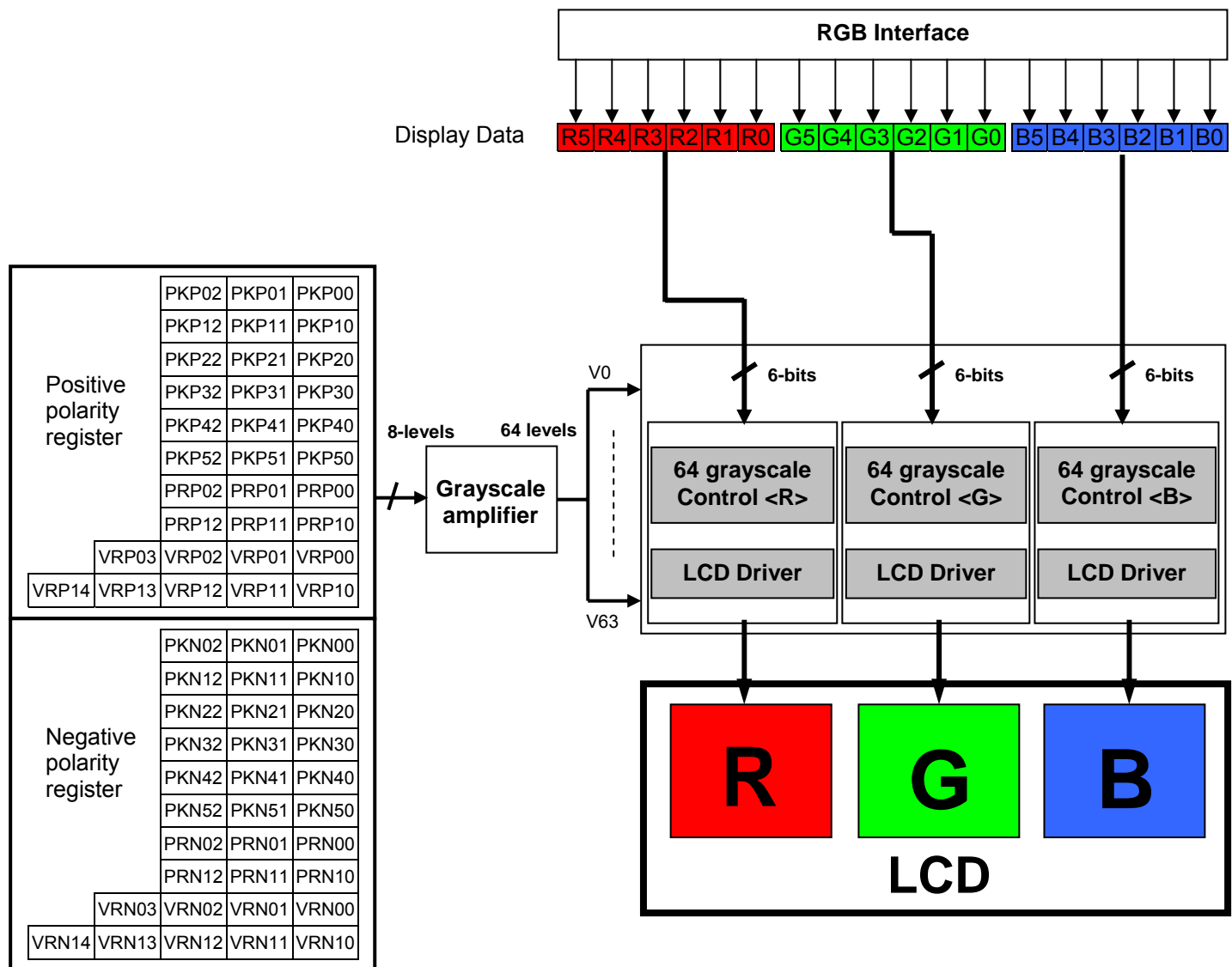
The number of driven display lines: MUX[8:0] = 13F (319+1 lines)

1st screen setting: SS[18:10] = 00h, SE[18:10] = 09h

2nd screen setting: SS[28:10] = 96h, SE[28:10] = 9Fh

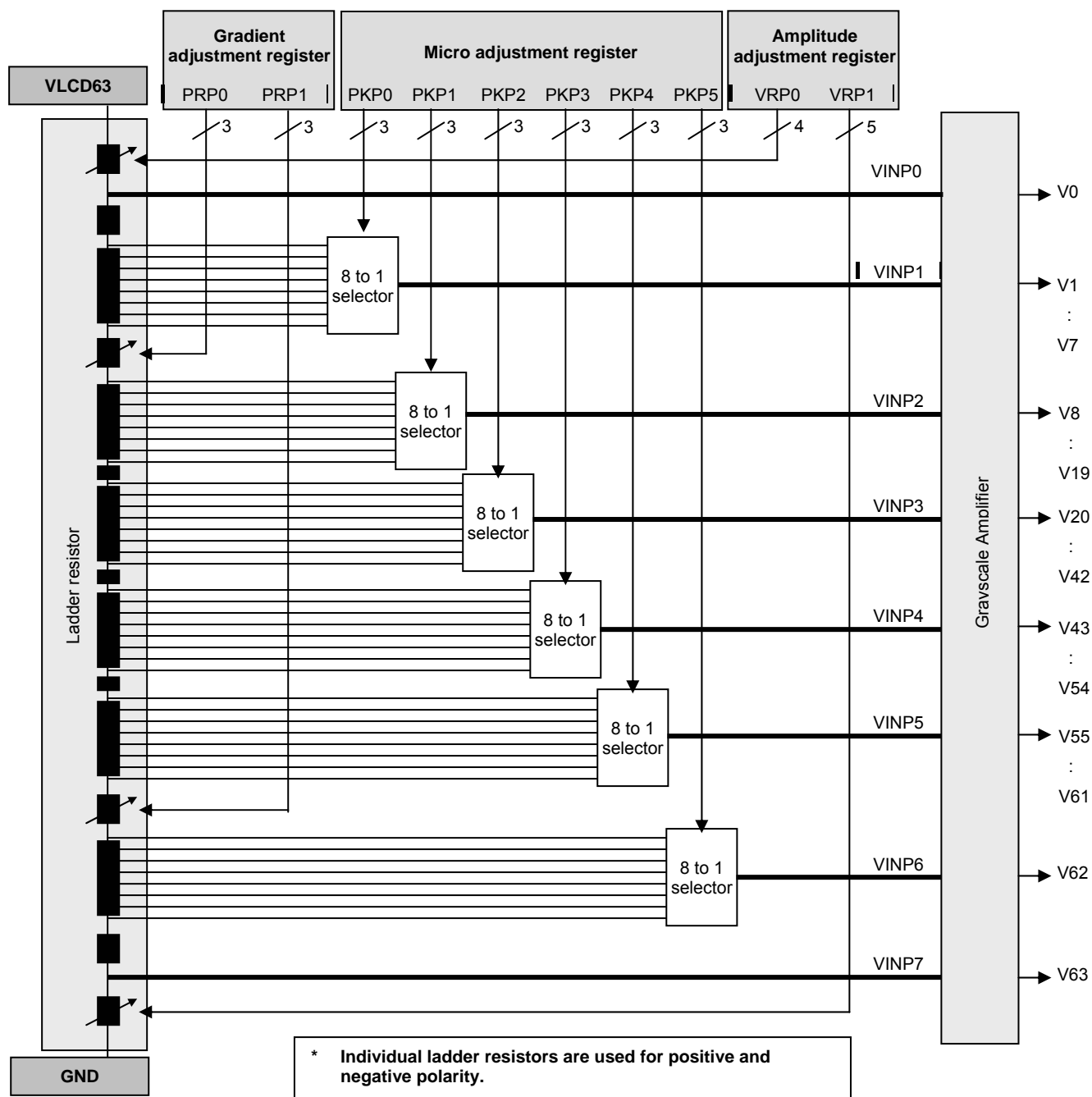
10 GAMMA ADJUSTMENT FUNCTION

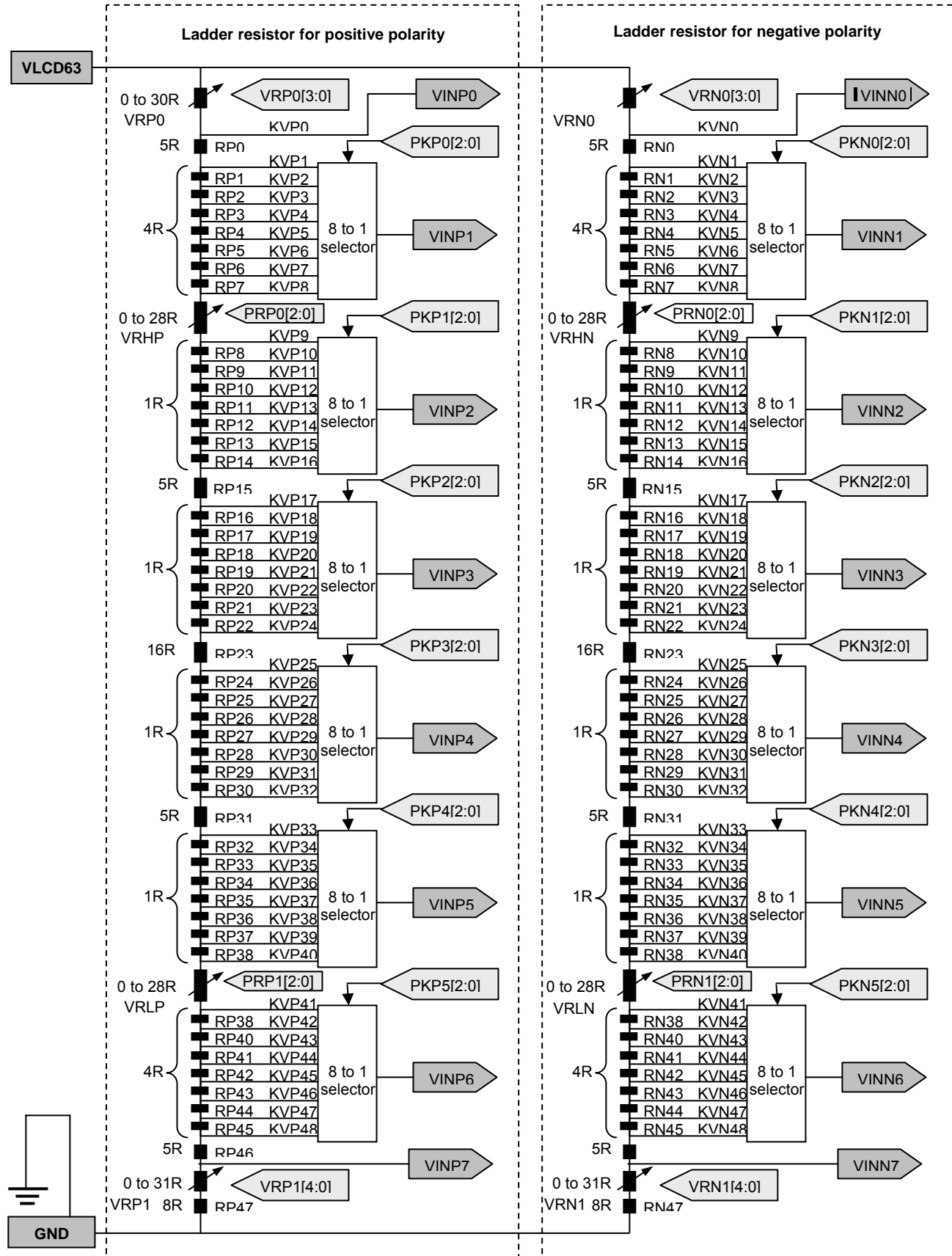
The SSD1289 incorporates gamma adjustment function for the 262,144-color display. Gamma adjustment is implemented by deciding the 8-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.



10.1 Structure of Grayscale Amplifier

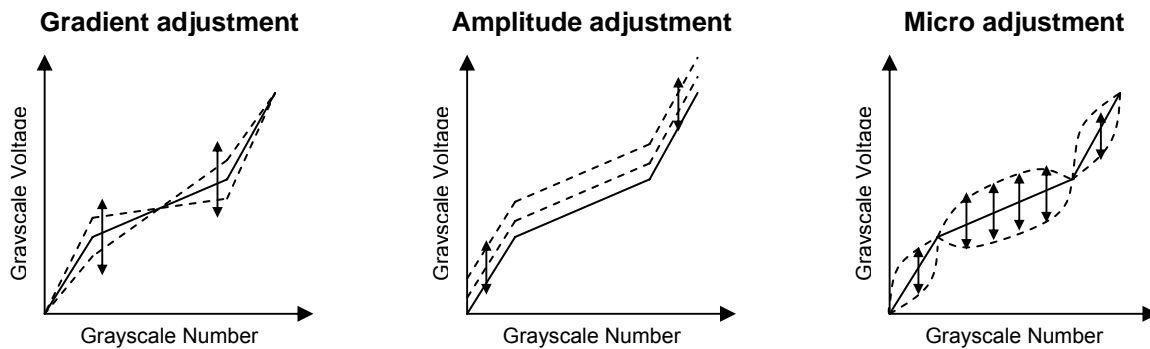
Below figure indicates the structure of the grayscale amplifier. It determines 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.





10.2 Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) Following graphics indicates the operation of each adjusting register.



10.2.1 Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 / PRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

10.2.2 Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

10.2.3 Micro adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

10.3 Ladder Resistor / 8 to 1 selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors.

Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 / PRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

| PRP(N)[0:1] | Resistance |
|-------------|------------|
| 000 | 0R |
| 001 | 4R |
| 010 | 8R |
| 011 | 12R |
| 100 | 16R |
| 101 | 20R |
| 110 | 24R |
| 111 | 28R |

| VRP(N)0 | Resistance |
|-----------|------------|
| 0000 | 0R |
| 0001 | 2R |
| 0010 | 4R |
| : | |
| Step = 2R | |
| : | |
| 1110 | 28R |
| 1111 | 30R |

| VRP(N)1 | Resistance |
|-----------|------------|
| 00000 | 0R |
| 00001 | 1R |
| 00010 | 2R |
| : | |
| Step = 1R | |
| : | |
| 11110 | 30R |
| 11111 | 31R |

8 to 1 selector

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

| Postive polarity | | | | | | | Negative polarity | | | | | | |
|----------------------|------------------|-------|-------|-------|-------|-------|----------------------|------------------|-------|-------|-------|-------|-------|
| Registor PKP[2:0] | Selected voltage | | | | | | Registor PKN[2:0] | Selected voltage | | | | | |
| | VINP1 | VINP2 | VINP3 | VINP4 | VINP5 | VINP6 | | VINN1 | VINN2 | VINN3 | VINN4 | VINN5 | VINN6 |
| 000 | KVP1 | KVP9 | KVP17 | KVP25 | KVP33 | KVP41 | 000 | KVN1 | KVN9 | KVN17 | KVN25 | KVN33 | KVN41 |
| 001 | KVP2 | KVP10 | KVP18 | KVP26 | KVP34 | KVP42 | 001 | KVN2 | KVN10 | KVN18 | KVN26 | KVN34 | KVN42 |
| 010 | KVP3 | KVP11 | KVP19 | KVP27 | KVP35 | KVP43 | 010 | KVN3 | KVN11 | KVN19 | KVN27 | KVN35 | KVN43 |
| 011 | KVP4 | KVP12 | KVP20 | KVP28 | KVP36 | KVP44 | 011 | KVN4 | KVN12 | KVN20 | KVN28 | KVN36 | KVN44 |
| 100 | KVP5 | KVP13 | KVP21 | KVP29 | KVP37 | KVP45 | 100 | KVN5 | KVN13 | KVN21 | KVN29 | KVN37 | KVN45 |
| 101 | KVP6 | KVP14 | KVP22 | KVP30 | KVP38 | KVP46 | 101 | KVN6 | KVN14 | KVN22 | KVN30 | KVN38 | KVN46 |
| 110 | KVP7 | KVP15 | KVP23 | KVP31 | KVP39 | KVP47 | 110 | KVN7 | KVN15 | KVN23 | KVN31 | KVN39 | KVN47 |
| 111 | KVP8 | KVP16 | KVP24 | KVP32 | KVP40 | KVP48 | 111 | KVN8 | KVN16 | KVN24 | KVN32 | KVN40 | KVN48 |

| Grayscale voltage | Formula | Grayscale voltage | Formula | Grayscale voltage | Formula |
|-------------------|-------------------------|-------------------|-------------------------|-------------------|-------------------------|
| V0 | VINP(N)0 | V22 | $V43+(V20-V43)*(21/23)$ | V44 | $V55+(V43-V55)*(22/24)$ |
| V1 | VINP(N)1 | V23 | $V43+(V20-V43)*(20/23)$ | V45 | $V55+(V43-V55)*(20/24)$ |
| V2 | $V8+(V1-V8)*(30/48)$ | V24 | $V43+(V20-V43)*(19/23)$ | V46 | $V55+(V43-V55)*(18/24)$ |
| V3 | $V8+(V1-V8)*(23/48)$ | V25 | $V43+(V20-V43)*(18/23)$ | V47 | $V55+(V43-V55)*(16/24)$ |
| V4 | $V8+(V1-V8)*(16/48)$ | V26 | $V43+(V20-V43)*(17/23)$ | V48 | $V55+(V43-V55)*(14/24)$ |
| V5 | $V8+(V1-V8)*(12/48)$ | V27 | $V43+(V20-V43)*(16/23)$ | V49 | $V55+(V43-V55)*(12/24)$ |
| V6 | $V8+(V1-V8)*(8/48)$ | V28 | $V43+(V20-V43)*(15/23)$ | V50 | $V55+(V43-V55)*(10/24)$ |
| V7 | $V8+(V1-V8)*(4/48)$ | V29 | $V43+(V20-V43)*(14/23)$ | V51 | $V55+(V43-V55)*(8/24)$ |
| V8 | VINP(N)2 | V30 | $V43+(V20-V43)*(13/23)$ | V52 | $V55+(V43-V55)*(6/24)$ |
| V9 | $V20+(V8-V20)*(22/24)$ | V31 | $V43+(V20-V43)*(12/23)$ | V53 | $V55+(V43-V55)*(4/24)$ |
| V10 | $V20+(V8-V20)*(20/24)$ | V32 | $V43+(V20-V43)*(11/23)$ | V54 | $V55+(V43-V55)*(2/24)$ |
| V11 | $V20+(V8-V20)*(18/24)$ | V33 | $V43+(V20-V43)*(10/23)$ | V55 | VINP(N)5 |
| V12 | $V20+(V8-V20)*(16/24)$ | V34 | $V43+(V20-V43)*(9/23)$ | V56 | $V62+(V55-V62)*(44/48)$ |
| V13 | $V20+(V8-V20)*(14/24)$ | V35 | $V43+(V20-V43)*(8/23)$ | V57 | $V62+(V55-V62)*(40/48)$ |
| V14 | $V20+(V8-V20)*(12/24)$ | V36 | $V43+(V20-V43)*(7/23)$ | V58 | $V62+(V55-V62)*(36/48)$ |
| V15 | $V20+(V8-V20)*(10/24)$ | V37 | $V43+(V20-V43)*(6/23)$ | V59 | $V62+(V55-V62)*(32/48)$ |
| V16 | $V20+(V8-V20)*(8/24)$ | V38 | $V43+(V20-V43)*(5/23)$ | V60 | $V62+(V55-V62)*(25/48)$ |
| V17 | $V20+(V8-V20)*(6/24)$ | V39 | $V43+(V20-V43)*(4/23)$ | V61 | $V62+(V55-V62)*(18/48)$ |
| V18 | $V20+(V8-V20)*(4/24)$ | V40 | $V43+(V20-V43)*(3/23)$ | V62 | VINP(N)6 |
| V19 | $V20+(V8-V20)*(2/24)$ | V41 | $V43+(V20-V43)*(2/23)$ | V63 | VINP(N)7 |
| V20 | VINP(N)3 | V42 | $V43+(V20-V43)*(1/23)$ | | |
| V21 | $V43+(V20-V43)*(22/23)$ | V43 | VINP(N)4 | | |

Reference voltage of positive polarity:

| Reference | Formula | Micr0-adjusting rgister | Reference voltage |
|-----------|--|-------------------------|-------------------|
| KVP0 | $VLCD63 - \Delta V \times VRP0 / SUMRP$ | -- | VINP0 |
| KVP1 | $VLCD63 - \Delta V \times (VRP0 + 5R) / SUMRP$ | PKP0[2:0] = "000" | VINP1 |
| KVP2 | $VLCD63 - \Delta V \times (VRP0 + 9R) / SUMRP$ | PKP0[2:0] = "001" | |
| KVP3 | $VLCD63 - \Delta V \times (VRP0 + 13R) / SUMRP$ | PKP0[2:0] = "010" | |
| KVP4 | $VLCD63 - \Delta V \times (VRP0 + 17R) / SUMRP$ | PKP0[2:0] = "011" | |
| KVP5 | $VLCD63 - \Delta V \times (VRP0 + 21R) / SUMRP$ | PKP0[2:0] = "100" | |
| KVP6 | $VLCD63 - \Delta V \times (VRP0 + 25R) / SUMRP$ | PKP0[2:0] = "101" | |
| KVP7 | $VLCD63 - \Delta V \times (VRP0 + 29R) / SUMRP$ | PKP0[2:0] = "110" | |
| KVP8 | $VLCD63 - \Delta V \times (VRP0 + 33R) / SUMRP$ | PKP0[2:0] = "111" | |
| KVP9 | $VLCD63 - \Delta V \times (VRP0 + 33R + VRHP) / SUMRP$ | PKP1[2:0] = "000" | VINP2 |
| KVP10 | $VLCD63 - \Delta V \times (VRP0 + 34R + VRHP) / SUMRP$ | PKP1[2:0] = "001" | |
| KVP11 | $VLCD63 - \Delta V \times (VRP0 + 35R + VRHP) / SUMRP$ | PKP1[2:0] = "010" | |
| KVP12 | $VLCD63 - \Delta V \times (VRP0 + 36R + VRHP) / SUMRP$ | PKP1[2:0] = "011" | |
| KVP13 | $VLCD63 - \Delta V \times (VRP0 + 37R + VRHP) / SUMRP$ | PKP1[2:0] = "100" | |
| KVP14 | $VLCD63 - \Delta V \times (VRP0 + 38R + VRHP) / SUMRP$ | PKP1[2:0] = "101" | |
| KVP15 | $VLCD63 - \Delta V \times (VRP0 + 39R + VRHP) / SUMRP$ | PKP1[2:0] = "110" | |
| KVP16 | $VLCD63 - \Delta V \times (VRP0 + 40R + VRHP) / SUMRP$ | PKP1[2:0] = "111" | |
| KVP17 | $VLCD63 - \Delta V \times (VRP0 + 45R + VRHP) / SUMRP$ | PKP2[2:0] = "000" | VINP3 |
| KVP18 | $VLCD63 - \Delta V \times (VRP0 + 46R + VRHP) / SUMRP$ | PKP2[2:0] = "001" | |
| KVP19 | $VLCD63 - \Delta V \times (VRP0 + 47R + VRHP) / SUMRP$ | PKP2[2:0] = "010" | |
| KVP20 | $VLCD63 - \Delta V \times (VRP0 + 48R + VRHP) / SUMRP$ | PKP2[2:0] = "011" | |
| KVP21 | $VLCD63 - \Delta V \times (VRP0 + 49R + VRHP) / SUMRP$ | PKP2[2:0] = "100" | |
| KVP22 | $VLCD63 - \Delta V \times (VRP0 + 50R + VRHP) / SUMRP$ | PKP2[2:0] = "101" | |
| KVP23 | $VLCD63 - \Delta V \times (VRP0 + 51R + VRHP) / SUMRP$ | PKP2[2:0] = "110" | |
| KVP24 | $VLCD63 - \Delta V \times (VRP0 + 52R + VRHP) / SUMRP$ | PKP2[2:0] = "111" | |
| KVP25 | $VLCD63 - \Delta V \times (VRP0 + 68R + VRHP) / SUMRP$ | PKP3[2:0] = "000" | VINP4 |
| KVP26 | $VLCD63 - \Delta V \times (VRP0 + 69R + VRHP) / SUMRP$ | PKP3[2:0] = "001" | |
| KVP27 | $VLCD63 - \Delta V \times (VRP0 + 70R + VRHP) / SUMRP$ | PKP3[2:0] = "010" | |
| KVP28 | $VLCD63 - \Delta V \times (VRP0 + 71R + VRHP) / SUMRP$ | PKP3[2:0] = "011" | |
| KVP29 | $VLCD63 - \Delta V \times (VRP0 + 72R + VRHP) / SUMRP$ | PKP3[2:0] = "100" | |
| KVP30 | $VLCD63 - \Delta V \times (VRP0 + 73R + VRHP) / SUMRP$ | PKP3[2:0] = "101" | |
| KVP31 | $VLCD63 - \Delta V \times (VRP0 + 74R + VRHP) / SUMRP$ | PKP3[2:0] = "110" | |
| KVP32 | $VLCD63 - \Delta V \times (VRP0 + 75R + VRHP) / SUMRP$ | PKP3[2:0] = "111" | |
| KVP33 | $VLCD63 - \Delta V \times (VRP0 + 80R + VRHP) / SUMRP$ | PKP4[2:0] = "000" | VINP5 |
| KVP34 | $VLCD63 - \Delta V \times (VRP0 + 81R + VRHP) / SUMRP$ | PKP4[2:0] = "001" | |
| KVP35 | $VLCD63 - \Delta V \times (VRP0 + 82R + VRHP) / SUMRP$ | PKP4[2:0] = "010" | |
| KVP36 | $VLCD63 - \Delta V \times (VRP0 + 83R + VRHP) / SUMRP$ | PKP4[2:0] = "011" | |
| KVP37 | $VLCD63 - \Delta V \times (VRP0 + 84R + VRHP) / SUMRP$ | PKP4[2:0] = "100" | |
| KVP38 | $VLCD63 - \Delta V \times (VRP0 + 85R + VRHP) / SUMRP$ | PKP4[2:0] = "101" | |
| KVP39 | $VLCD63 - \Delta V \times (VRP0 + 86R + VRHP) / SUMRP$ | PKP4[2:0] = "110" | |
| KVP40 | $VLCD63 - \Delta V \times (VRP0 + 87R + VRHP) / SUMRP$ | PKP4[2:0] = "111" | |
| KVP41 | $VLCD63 - \Delta V \times (VRP0 + 87R + VRHP + VRLP) / SUMRP$ | PKP5[2:0] = "000" | VINP6 |
| KVP42 | $VLCD63 - \Delta V \times (VRP0 + 91R + VRHP + VRLP) / SUMRP$ | PKP5[2:0] = "001" | |
| KVP43 | $VLCD63 - \Delta V \times (VRP0 + 95R + VRHP + VRLP) / SUMRP$ | PKP5[2:0] = "010" | |
| KVP44 | $VLCD63 - \Delta V \times (VRP0 + 99R + VRHP + VRLP) / SUMRP$ | PKP5[2:0] = "011" | |
| KVP45 | $VLCD63 - \Delta V \times (VRP0 + 103R + VRHP + VRLP) / SUMRP$ | PKP5[2:0] = "100" | |
| KVP46 | $VLCD63 - \Delta V \times (VRP0 + 107R + VRHP + VRLP) / SUMRP$ | PKP5[2:0] = "101" | |
| KVP47 | $VLCD63 - \Delta V \times (VRP0 + 111R + VRHP + VRLP) / SUMRP$ | PKP5[2:0] = "110" | |
| KVP48 | $VLCD63 - \Delta V \times (VRP0 + 115R + VRHP + VRLP) / SUMRP$ | PKP5[2:0] = "111" | |
| KVP49 | $VLCD63 - \Delta V \times (VRP0 + 120R + VRHP + VRLP) / SUMRP$ | -- | VINP7 |

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0 + VRP1

ΔV : Voltage difference between VLCD63 and of GND.

Reference voltage of negative polarity:

| Reference | Formula | Micr0-adjusting register | Reference voltage |
|-----------|--|--------------------------|-------------------|
| KVN0 | $VLCD63 - \Delta V \times VRN0 / SUMRN$ | -- | VINN0 |
| KVN1 | $VLCD63 - \Delta V \times (VRN0 + 5R) / SUMRN$ | $PKN0[2:0] = "000"$ | VINN1 |
| KVN2 | $VLCD63 - \Delta V \times (VRN0 + 9R) / SUMRN$ | $PKN0[2:0] = "001"$ | |
| KVN3 | $VLCD63 - \Delta V \times (VRN0 + 13R) / SUMRN$ | $PKN0[2:0] = "010"$ | |
| KVN4 | $VLCD63 - \Delta V \times (VRN0 + 17R) / SUMRN$ | $PKN0[2:0] = "011"$ | |
| KVN5 | $VLCD63 - \Delta V \times (VRN0 + 21R) / SUMRN$ | $PKN0[2:0] = "100"$ | |
| KVN6 | $VLCD63 - \Delta V \times (VRN0 + 25R) / SUMRN$ | $PKN0[2:0] = "101"$ | |
| KVN7 | $VLCD63 - \Delta V \times (VRN0 + 29R) / SUMRN$ | $PKN0[2:0] = "110"$ | |
| KVN8 | $VLCD63 - \Delta V \times (VRN0 + 33R) / SUMRN$ | $PKN0[2:0] = "111"$ | |
| KVN9 | $VLCD63 - \Delta V \times (VRN0 + 33R + VRHN) / SUMRN$ | $PKN1[2:0] = "000"$ | VINN2 |
| KVN10 | $VLCD63 - \Delta V \times (VRN0 + 34R + VRHN) / SUMRN$ | $PKN1[2:0] = "001"$ | |
| KVN11 | $VLCD63 - \Delta V \times (VRN0 + 35R + VRHN) / SUMRN$ | $PKN1[2:0] = "010"$ | |
| KVN12 | $VLCD63 - \Delta V \times (VRN0 + 36R + VRHN) / SUMRN$ | $PKN1[2:0] = "011"$ | |
| KVN13 | $VLCD63 - \Delta V \times (VRN0 + 37R + VRHN) / SUMRN$ | $PKN1[2:0] = "100"$ | |
| KVN14 | $VLCD63 - \Delta V \times (VRN0 + 38R + VRHN) / SUMRN$ | $PKN1[2:0] = "101"$ | |
| KVN15 | $VLCD63 - \Delta V \times (VRN0 + 39R + VRHN) / SUMRN$ | $PKN1[2:0] = "110"$ | |
| KVN16 | $VLCD63 - \Delta V \times (VRN0 + 40R + VRHN) / SUMRN$ | $PKN1[2:0] = "111"$ | |
| KVN17 | $VLCD63 - \Delta V \times (VRN0 + 45R + VRHN) / SUMRN$ | $PKN2[2:0] = "000"$ | VINN3 |
| KVN18 | $VLCD63 - \Delta V \times (VRN0 + 46R + VRHN) / SUMRN$ | $PKN2[2:0] = "001"$ | |
| KVN19 | $VLCD63 - \Delta V \times (VRN0 + 47R + VRHN) / SUMRN$ | $PKN2[2:0] = "010"$ | |
| KVN20 | $VLCD63 - \Delta V \times (VRN0 + 48R + VRHN) / SUMRN$ | $PKN2[2:0] = "011"$ | |
| KVN21 | $VLCD63 - \Delta V \times (VRN0 + 49R + VRHN) / SUMRN$ | $PKN2[2:0] = "100"$ | |
| KVN22 | $VLCD63 - \Delta V \times (VRN0 + 50R + VRHN) / SUMRN$ | $PKN2[2:0] = "101"$ | |
| KVN23 | $VLCD63 - \Delta V \times (VRN0 + 51R + VRHN) / SUMRN$ | $PKN2[2:0] = "110"$ | |
| KVN24 | $VLCD63 - \Delta V \times (VRN0 + 52R + VRHN) / SUMRN$ | $PKN2[2:0] = "111"$ | |
| KVN25 | $VLCD63 - \Delta V \times (VRN0 + 68R + VRHN) / SUMRN$ | $PKN3[2:0] = "000"$ | VINN4 |
| KVN26 | $VLCD63 - \Delta V \times (VRN0 + 69R + VRHN) / SUMRN$ | $PKN3[2:0] = "001"$ | |
| KVN27 | $VLCD63 - \Delta V \times (VRN0 + 70R + VRHN) / SUMRN$ | $PKN3[2:0] = "010"$ | |
| KVN28 | $VLCD63 - \Delta V \times (VRN0 + 71R + VRHN) / SUMRN$ | $PKN3[2:0] = "011"$ | |
| KVN29 | $VLCD63 - \Delta V \times (VRN0 + 72R + VRHN) / SUMRN$ | $PKN3[2:0] = "100"$ | |
| KVN30 | $VLCD63 - \Delta V \times (VRN0 + 73R + VRHN) / SUMRN$ | $PKN3[2:0] = "101"$ | |
| KVN31 | $VLCD63 - \Delta V \times (VRN0 + 74R + VRHN) / SUMRN$ | $PKN3[2:0] = "110"$ | |
| KVN32 | $VLCD63 - \Delta V \times (VRN0 + 75R + VRHN) / SUMRN$ | $PKN3[2:0] = "111"$ | |
| KVN33 | $VLCD63 - \Delta V \times (VRN0 + 80R + VRHN) / SUMRN$ | $PKN4[2:0] = "000"$ | VINN5 |
| KVN34 | $VLCD63 - \Delta V \times (VRN0 + 81R + VRHN) / SUMRN$ | $PKN4[2:0] = "001"$ | |
| KVN35 | $VLCD63 - \Delta V \times (VRN0 + 82R + VRHN) / SUMRN$ | $PKN4[2:0] = "010"$ | |
| KVN36 | $VLCD63 - \Delta V \times (VRN0 + 83R + VRHN) / SUMRN$ | $PKN4[2:0] = "011"$ | |
| KVN37 | $VLCD63 - \Delta V \times (VRN0 + 84R + VRHN) / SUMRN$ | $PKN4[2:0] = "100"$ | |
| KVN38 | $VLCD63 - \Delta V \times (VRN0 + 85R + VRHN) / SUMRN$ | $PKN4[2:0] = "101"$ | |
| KVN39 | $VLCD63 - \Delta V \times (VRN0 + 86R + VRHN) / SUMRN$ | $PKN4[2:0] = "110"$ | |
| KVN40 | $VLCD63 - \Delta V \times (VRN0 + 87R + VRHN) / SUMRN$ | $PKN4[2:0] = "111"$ | |
| KVN41 | $VLCD63 - \Delta V \times (VRN0 + 87R + VRHN + VRLN) / SUMRN$ | $PKN5[2:0] = "000"$ | VINN6 |
| KVN42 | $VLCD63 - \Delta V \times (VRN0 + 91R + VRHN + VRLN) / SUMRN$ | $PKN5[2:0] = "001"$ | |
| KVN43 | $VLCD63 - \Delta V \times (VRN0 + 95R + VRHN + VRLN) / SUMRN$ | $PKN5[2:0] = "010"$ | |
| KVN44 | $VLCD63 - \Delta V \times (VRN0 + 99R + VRHN + VRLN) / SUMRN$ | $PKN5[2:0] = "011"$ | |
| KVN45 | $VLCD63 - \Delta V \times (VRN0 + 103R + VRHN + VRLN) / SUMRN$ | $PKN5[2:0] = "100"$ | |
| KVN46 | $VLCD63 - \Delta V \times (VRN0 + 107R + VRHN + VRLN) / SUMRN$ | $PKN5[2:0] = "101"$ | |
| KVN47 | $VLCD63 - \Delta V \times (VRN0 + 111R + VRHN + VRLN) / SUMRN$ | $PKN5[2:0] = "110"$ | |
| KVN48 | $VLCD63 - \Delta V \times (VRN0 + 115R + VRHN + VRLN) / SUMRN$ | $PKN5[2:0] = "111"$ | |
| KVN49 | $VLCD63 - \Delta V \times (VRN0 + 120R + VRHN + VRLN) / SUMRN$ | -- | VINN7 |

SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0 + VRN1

ΔV : Voltage difference between VLCD63 and of GND.

11 MAXIMUM RATINGS

Maximum Ratings (Voltage Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|-----------|---|------------------|------|
| VDDIO | Supply Voltage | -0.3 to +4.0 | V |
| VDDEXT | | -0.3 to +4.0 | V |
| VCI | Input Voltage | VSS - 0.3 to 5.0 | V |
| I | Current Drain Per Pin Excluding V_{DDIO} and V_{SS} | 25 | mA |
| T_A | Operating Temperature | -20 to +70 | °C |
| T_{stg} | Storage Temperature | -65 to +150 | °C |

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, strong electric fields, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices. It is advised that proper precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VCI and Vout be constrained to the range $V_{SS} < V_{DDIO} \leq V_{CI} < V_{OUT}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS} , $V_{DDIO} = 1.65$ to $3.6V$, $T_A = -20$ to $70^\circ C$)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|-----------------|--|--|----------------------------------|-----|------------------|---------|
| VDDIO | Power supply pin of IO pins | Recommend Operating Voltage Possible Operating Voltage | 1.4 | - | 3.6 | V |
| VDDEXT | Auxiliary power supply pin for VDD | Recommend Operating Voltage Possible Operating Voltage | 1.4 | - | 3.6 | V |
| VCI | Booster Reference Supply Voltage Range | Recommend Operating Voltage Possible Operating Voltage | 2.5 or VDDIO whichever is higher | - | 3.6 | V |
| VGH | Gate driver High Output Voltage Booster efficiency | No panel loading; 4x or 5x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm | 88 | 90 | - | % |
| | | No panel loading; 6x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm | 82 | 84 | - | % |
| VCIX2 | VCIX2 primary booster efficiency | No panel loading, ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm | 83 | 85 | - | % |
| VGH | Gate driver High Output Voltage | | 9 | - | 15 | V |
| VGL | Gate driver Low Output Voltage | | -15 | - | -7 | V |
| VcomH | Vcom High Output Voltage | | - | - | 5 | V |
| VcomL | Vcom Low Output Voltage | | $-V_{CIM}+0.5$ | - | - | V |
| VLCD63 | Max. Source Voltage | | - | - | 5 | V |
| $\Delta VLCD63$ | Source voltage variation | | -2 | | 2 | % |
| V_{OH1} | Logic High Output Voltage | $I_{out} = -100\mu A$ | $0.9 * V_{DDIO}$ | - | VDDIO | V |
| V_{OL1} | Logic Low Output Voltage | $I_{out} = 100\mu A$ | 0 | - | $0.1 * V_{DDIO}$ | V |
| V_{IH1} | Logic High Input voltage | | $0.8 * V_{DDIO}$ | - | VDDIO | V |
| V_{IL1} | Logic Low Input voltage | | 0 | - | $0.2 * V_{DDIO}$ | V |
| I_{OH} | Logic High Output Current Source | $V_{out} = V_{DDIO} - 0.4V$ | 50 | - | - | μA |
| I_{OL} | Logic Low Output Current Drain | $V_{out} = 0.4V$ | - | - | -50 | μA |

| | | | | | | | |
|----------------------------------|---|---|------|-----|------|-----|----|
| I _{OZ} | Logic Output Tri-state Current Drain Source | | -1 | - | 1 | μA | |
| I _{IL} /I _{IH} | Logic Input Current | | -1 | - | 1 | μA | |
| C _{IN} | Logic Pins Input Capacitance | | - | 5 | 7.5 | pF | |
| f _{DOTCLK} | DOTCLK frequency | Display is ON | 1 | | 8.22 | MHz | |
| R _{SON} | Source drivers output resistance | | - | 1 | - | kΩ | |
| R _{GON} | Gate drivers output resistance | | - | 500 | - | Ω | |
| R _{CON} | Vcom output resistance | | - | 200 | - | Ω | |
| I _{dp} (262k) | Display current for 262k | Vddio=Vddext = 1.8V, Vci = 2.8V. 5x/-5x booster ratio. Full color current consumption, without panel loading | Ivdd | - | 150 | 300 | uA |
| | | Ivci | - | 2.5 | 8 | mA | |
| I _{dp} (8 color) | Display current for 8 color mode | Current consumption for 8 color partial display, without panel loading | Ivdd | - | 120 | 300 | μA |
| | | Ivci | - | 1 | 5 | mA | |
| I _{slp} | Sleep mode current | Oscillator off, no source/gate output, Ram read write halt. Send command R10-0001 (sleep mode), R00-0000 (stop osc) | Ivdd | - | 30 | 100 | μA |
| | | Ivci | - | 40 | 200 | μA | |

Remark: Ivdd = Ivddio + Ivddext

13 AC CHARACTERISTICS

Table 13-1 – Parallel 6800 Timing Characteristics ($T_A = -20$ to 70°C , $V_{DDIO} = 1.4\text{V}$ to 3.6V , $V_{DDEXT} = 1.4\text{V} - 1.95\text{V}$, $\text{REGVDD} = 'L'$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------|------------------------------------|------|-----|-----|------|
| t_{cycle} | Clock Cycle Time (write cycle) | 100 | - | - | ns |
| t_{cycle} | Clock Cycle Time (read cycle) | 1000 | - | - | ns |
| t_{AS} | Address Setup Time | 0 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Data Setup Time | 5 | - | - | ns |
| t_{DHW} | Data Hold Time | 5 | - | - | ns |
| t_{ACC} | Data Access Time | 250 | - | - | ns |
| t_{OH} | Output Hold time | 100 | - | - | ns |
| PWCS_L | Pulse width /CS low (write cycle) | 50 | - | - | ns |
| PWCS_H | Pulse width /CS high (write cycle) | 50 | - | - | ns |
| PWCS_L | Pulse width /CS low (read cycle) | 500 | - | - | ns |
| PWCS_H | Pulse width /CS high (read cycle) | 500 | - | - | ns |
| t_R | Rise time | - | - | 4 | ns |
| t_F | Fall time | - | - | 4 | ns |

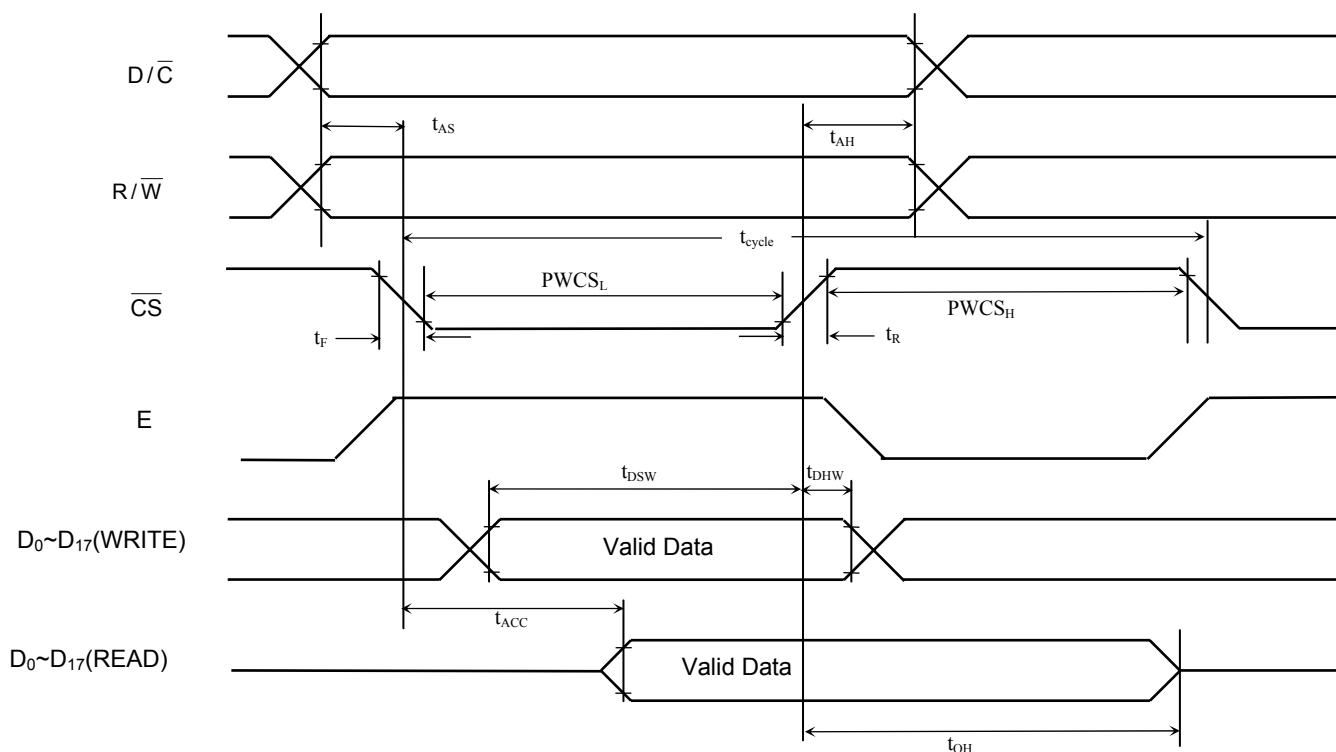


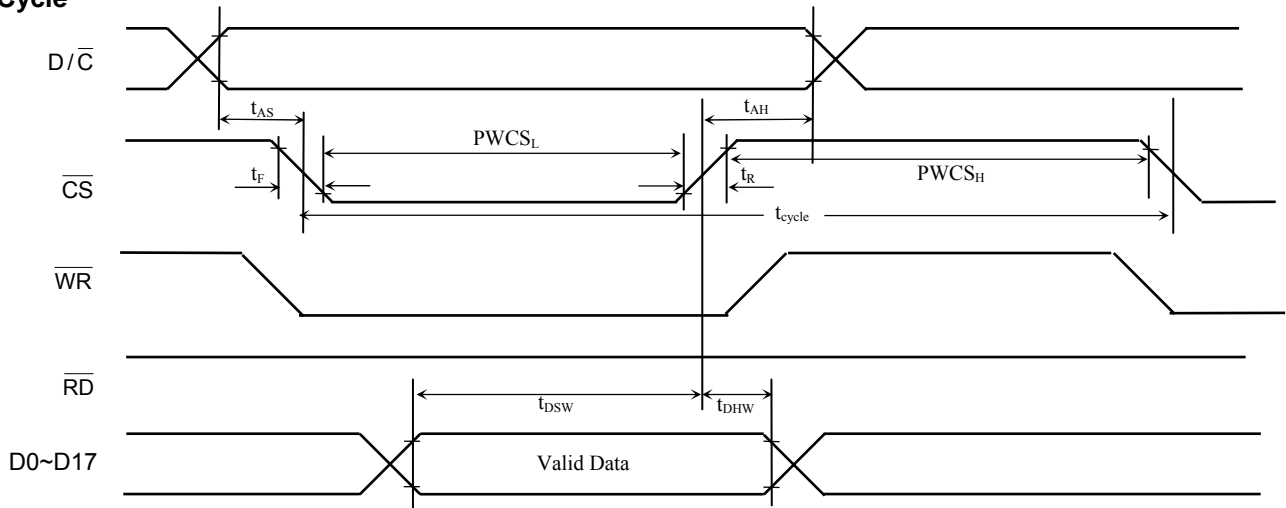
Figure 13-1 –Parallel 6800-series Interface Timing Characteristics

Table 13-2 – Parallel 8080 Timing Characteristics

($T_A = -20$ to 70°C , $V_{DDIO} = 1.65\text{V}$ to 3.6V , $V_{DDEXT} = 1.65\text{V}$ to 1.95V , $\text{REGVDD} = 'L'$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------|------------------------------------|------|-----|-----|------|
| t_{cycle} | Clock Cycle Time (write cycle) | 100 | - | - | ns |
| t_{cycle} | Clock Cycle Time (read cycle) | 1000 | - | - | ns |
| t_{AS} | Address Setup Time | 0 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Data Setup Time | 5 | - | - | ns |
| t_{DHW} | Data Hold Time | 5 | - | - | ns |
| t_{ACC} | Data Access Time | 250 | - | - | ns |
| t_{OH} | Output Hold time | 100 | - | - | ns |
| PWCS_L | Pulse Width /CS low (write cycle) | 50 | - | - | ns |
| PWCS_H | Pulse Width /CS high (write cycle) | 50 | - | - | ns |
| PWCS_L | Pulse Width /CS low (read cycle) | 500 | - | - | ns |
| PWCS_H | Pulse Width /CS high (read cycle) | 500 | - | - | ns |
| t_R | Rise time | - | - | 4 | ns |
| t_F | Fall time | - | - | 4 | ns |

Write Cycle



Read Cycle

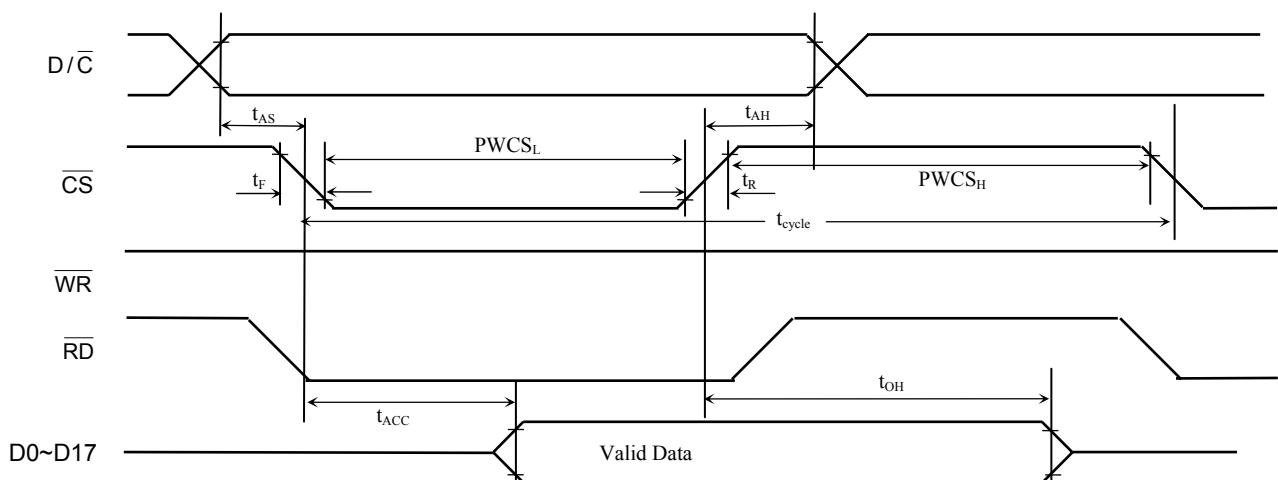


Figure 13-2 –Parallel 8080-series Interface Timing Characteristics

Table 13-3 - Serial Timing Characteristics

($T_A = -20$ to 70°C , $V_{DDIO} = 1.65\text{V}$ to 3.6V , $V_{DDEXT} = 1.65\text{V}$ to 1.95V , $\text{REGVDD} = 'L'$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------|--|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 77 | - | - | ns |
| f_{CLK} | Serial Clock Cycle Time SPI Clock tolerance = ± 2 ppm | - | - | 13 | MHz |
| t_{AS} | Register select Setup Time | 4 | - | - | ns |
| t_{AH} | Register select Hold Time | 5 | - | - | ns |
| t_{CSS} | Chip Select Setup Time | 2 | - | - | ns |
| t_{CSH} | Chip Select Hold Time | 10 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 5 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 10 | - | - | ns |
| t_{CLKL} | Clock Low Time | 38 | - | - | ns |
| t_{CLKH} | Clock High Time | 38 | - | - | ns |
| t_{R} | Rise time | - | - | 4 | ns |
| t_{F} | Fall time | - | - | 4 | ns |

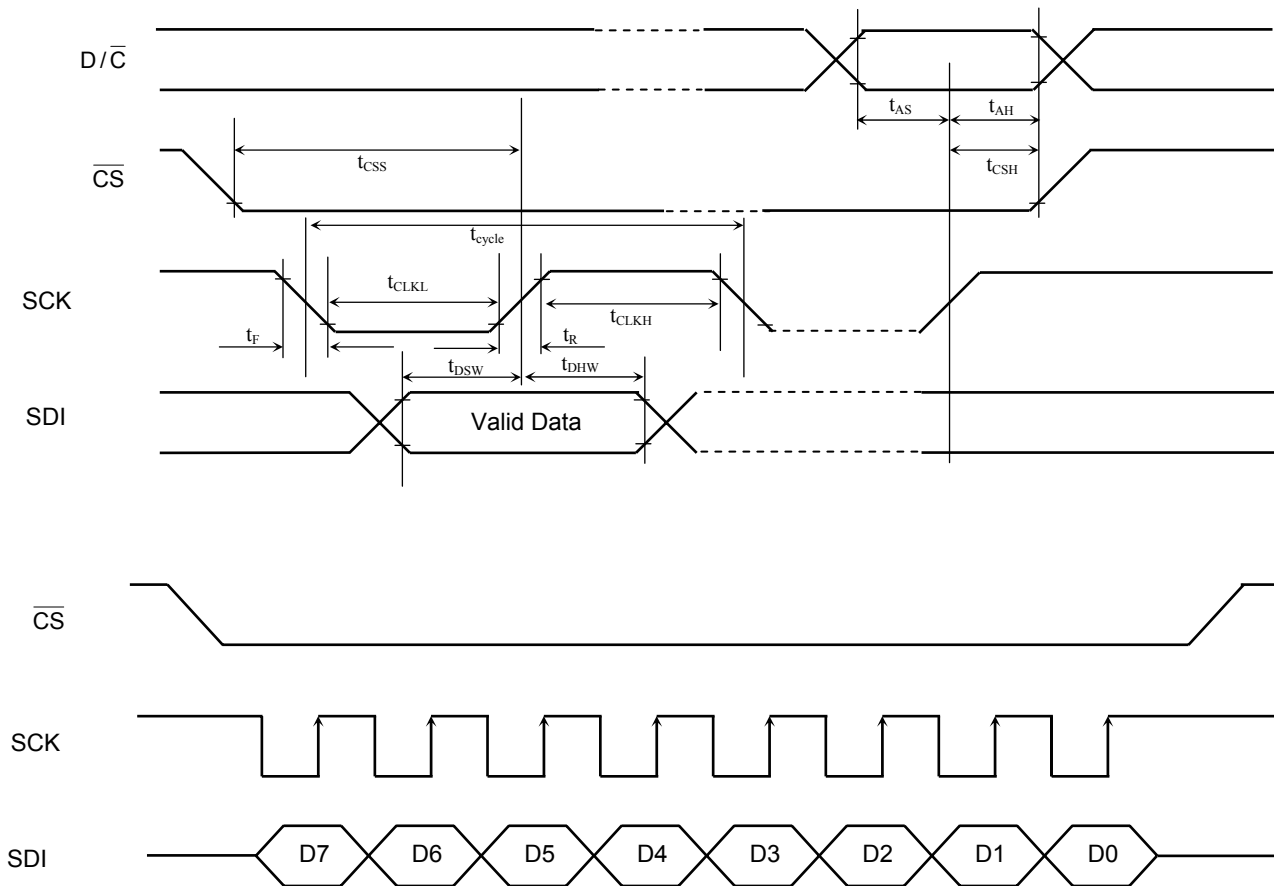
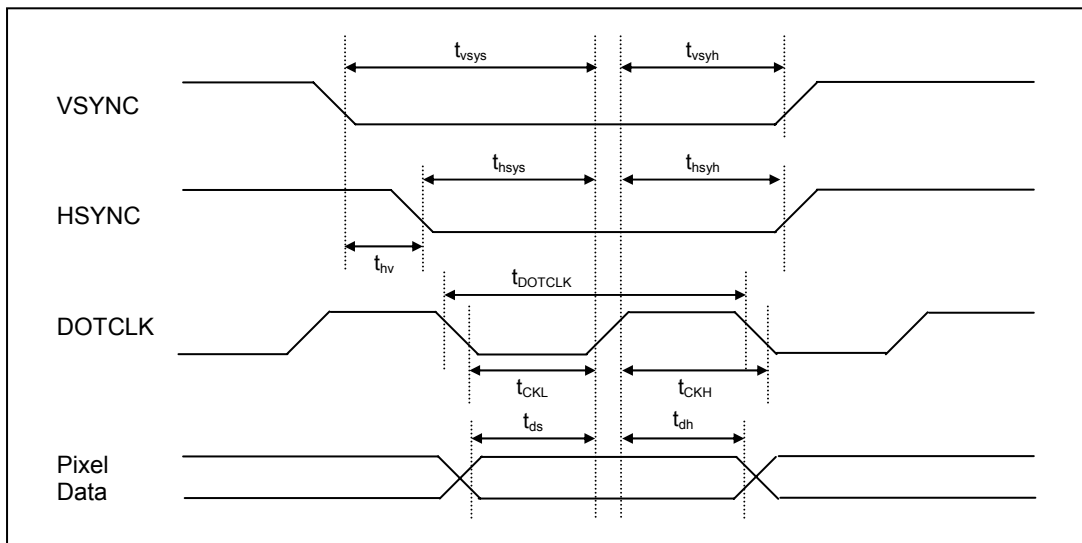


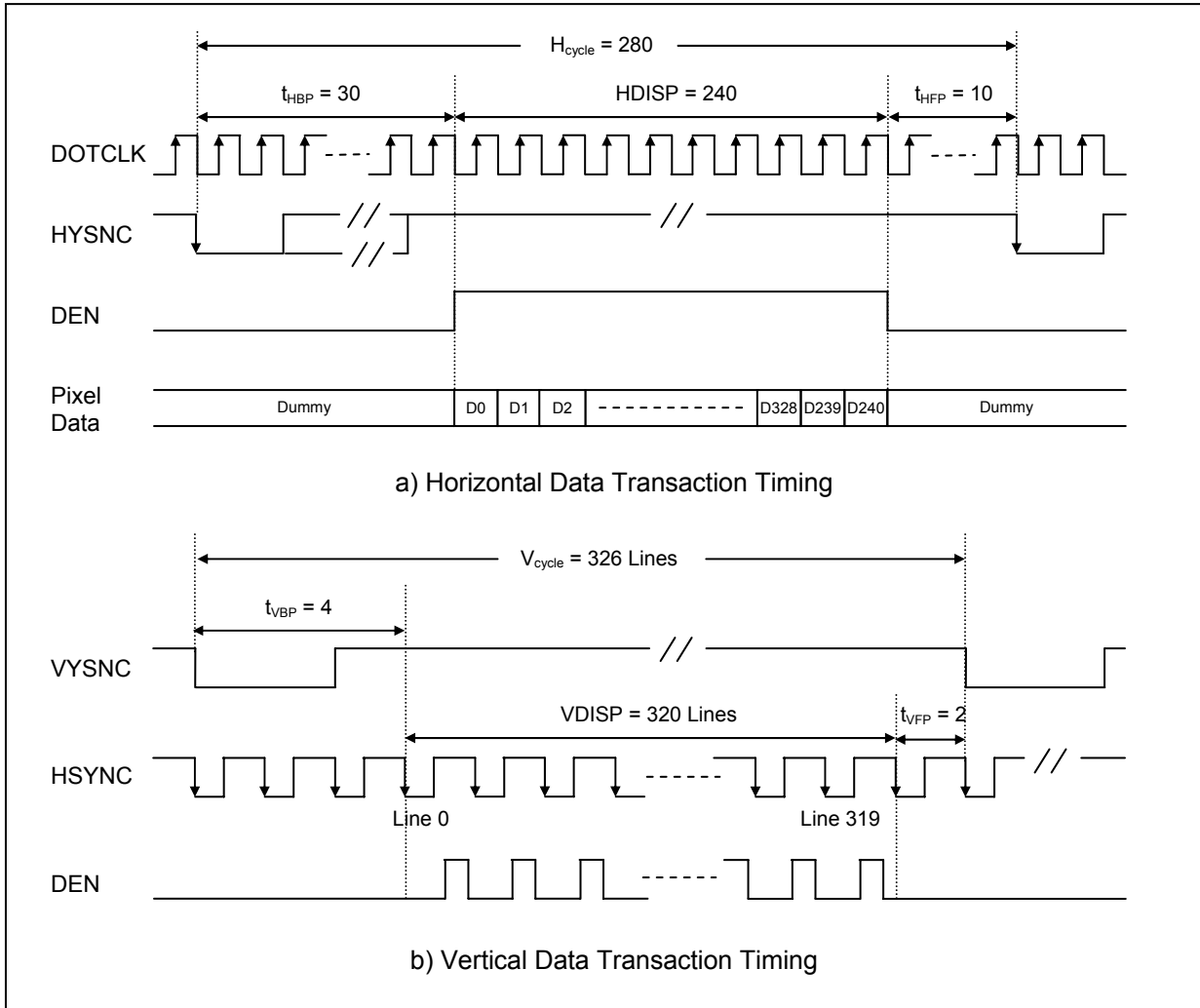
Figure 13-3 – 4 wire Serial Timing Characteristics

Figure 13-4 - Pixel Clock Timing in RGB interface mode



| Characteristics | Symbol | Min | Typ | Max | Units |
|--|--------------|-----|-----|------|--------------|
| DOTCLK Frequency | f_{DOTCLK} | - | 5.5 | 8.22 | MHz |
| DOTCLK Period | t_{DOTCLK} | 122 | 182 | - | nSec |
| Vertical Sync Setup Time | t_{vsys} | 20 | - | - | nSec |
| Vertical Sync Hold Time | t_{vsyh} | 20 | - | - | nSec |
| Horizontal Sync Setup Time | t_{hsys} | 20 | - | - | nSec |
| Horizontal Sync Hold Time | t_{hsyh} | 20 | - | - | nSec |
| Phase difference of Sync Signal Falling Edge | t_{hv} | 0 | - | 240 | t_{DOTCLK} |
| DOTCLK Low Period | t_{CKL} | 61 | - | - | nSec |
| DOTCLK High Period | t_{CKH} | 61 | - | - | nSec |
| Data Setup Time | t_{ds} | 40 | - | - | nSec |
| Data hold Time | t_{dh} | 40 | - | - | nSec |

Figure 0-5 - Pixel Clock Timing in RGB interface mode



| Characteristics | Symbol | Min | Typ | Max | Unit |
|------------------------------|-------------------------------------|-----|------|------|---------------------|
| DOTCLK Frequency | f _{DOTCLK} | - | 5.5 | 8.22 | MHz |
| DOTCLK Period | t _{DOTCLK} | 122 | 182 | - | nSec |
| Horizontal Frequency (Line) | f _H | - | 19.6 | 29.3 | kHz |
| Vertical Frequency (Refresh) | f _V | - | 60 | 90 | Hz |
| Horizontal Back Porch | t _{HBP} | - | 30 | - | t _{DOTCLK} |
| Horizontal Front Porch | t _{HFP} | - | 10 | - | t _{DOTCLK} |
| Horizontal Data Start Point | t _{HBP} | - | 30 | - | t _{DOTCLK} |
| Horizontal Blanking Period | t _{HBP} + t _{HFP} | - | 40 | - | t _{DOTCLK} |
| Horizontal Display Area | HDISP | - | 240 | - | t _{DOTCLK} |
| Horizontal Cycle | H _{cycle} | - | 280 | - | t _{DOTCLK} |
| Vertical Back Porch | t _{VBP} | - | 4 | - | Line |
| Vertical Front Porch | t _{VFP} | - | 2 | - | Line |
| Vertical Data Start Point | t _{VBP} | - | 4 | - | Line |
| Vertical Blanking Period | t _{VBP} + t _{VFP} | - | 6 | - | Line |
| Vertical Display Area | VDISP | - | 320 | - | Line |
| Vertical Cycle | V _{cycle} | - | 326 | - | Line |

14 GDDRAM ADDRESS

| | | | | | | | | | | | | | | | | | | | | |
|--------------------|-------|--------------|------|------|--------------|------|------|--------------|------|------|-----|--------------|------|------|--------------|------|------|---------------------|-----|--|
| | RL=1 | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | ... | S714 | S715 | S716 | S717 | S718 | S719 | Vertical address | | |
| | RL=0 | S719 | S718 | S717 | S716 | S715 | S714 | S713 | S712 | S711 | ... | S5 | S4 | S3 | S2 | S1 | S0 | | | |
| | BGR=0 | R | G | B | R | G | B | R | G | B | ... | R | G | B | R | G | B | | | |
| | BGR=1 | B | G | R | B | G | R | B | G | R | ... | B | G | R | B | G | R | | | |
| TB=1 | TB=0 | | | | | | | | | | | | | | | | | | | |
| G0 | G319 | 0000H,0000H | | | 0000H, 0001H | | | 0000H, 0010H | | | ... | 0000H, 00EEH | | | 0000H, 00EFH | | | 0 | | |
| G1 | G318 | 0001H,0000H | | | 0001H, 0001H | | | 0001H, 0010H | | | ... | 0001H, 00EEH | | | 0001H, 00EFH | | | 1 | | |
| G2 | G317 | 0010H,0000H | | | 0010H, 0001H | | | 0010H, 0010H | | | ... | 0010H, 00EEH | | | 0010H, 00EFH | | | 2 | | |
| G3 | G316 | 0011H,0000H | | | 0011H, 0001H | | | 0011H, 0010H | | | ... | 0011H, 00EEH | | | 0011H, 00EFH | | | 3 | | |
| G4 | G315 | 0100H,0000H | | | 0100H, 0001H | | | 0100H, 0010H | | | ... | 0100H, 00EEH | | | 0100H, 00EFH | | | 4 | | |
| . | . | . | | | . | | | . | | | . | . | | | . | | | . | | |
| . | . | . | | | . | | | . | | | . | . | | | . | | | . | | |
| . | . | . | | | . | | | . | | | . | . | | | . | | | . | | |
| G316 | G3 | 013CH, 0000H | | | 013CH, 0001H | | | 013CH, 0010H | | | ... | 013CH, 00EEH | | | 013CH, 00EFH | | | 316 | | |
| G317 | G2 | 013DH, 0000H | | | 013DH, 0001H | | | 013DH, 0010H | | | ... | 013DH, 00EEH | | | 013DH, 00EFH | | | 317 | | |
| G318 | G1 | 013EH, 0000H | | | 013EH, 0001H | | | 013EH, 0010H | | | ... | 013EH, 00EEH | | | 013EH, 00EFH | | | 318 | | |
| G319 | G0 | 013FH, 0000H | | | 013FH, 0001H | | | 013FH, 0010H | | | ... | 013FH, 00EEH | | | 013FH, 00EFH | | | 319 | | |
| Horizontal address | | 0 | | | | 1 | | | | 2 | | | | ... | 238 | | | | 239 | |

Remark : The address is in 00xxH,0yyyH format, where yyy is the vertical address and xx is the horizontal address

15 INTERFACE MAPPING

15.1 Interface Setting

Table 15-1: Interface setting and data bus setting

| PS3 | PS2 | PS1 | PS0 | Interface Mode | Data bus |
|-----|-----|-----|-----|-----------------------------------|---------------------------|
| 1 | 1 | 1 | 1 | 3-wire SPI | |
| 1 | 1 | 1 | 0 | 4-wire SPI | |
| 1 | 0 | 1 | 1 | 16-bit 6800 parallel interface | D[17:10], D[8:1] |
| 1 | 0 | 1 | 0 | 8-bit 6800 parallel interface | D[8:1] |
| 1 | 0 | 0 | 1 | 16-bit 8080 parallel interface | D[17:10], D[8:1] |
| 1 | 0 | 0 | 0 | 8-bit 8080 parallel interface | D[8:1] |
| 0 | 1 | 1 | 1 | 18-bits 6800 parallel interface | D[17:0] |
| 0 | 1 | 1 | 0 | 9-bits 6800 parallel interface | D[8:0] |
| 0 | 1 | 0 | 1 | 18-bit 8080 parallel interface | D[17:0] |
| 0 | 1 | 0 | 0 | 9-bit 8080 parallel interface | D[8:0] |
| 0 | 0 | 1 | 1 | 6-bit serial RGB interface | D[17:12] |
| 0 | 0 | 1 | 0 | 16-bit RGB interface + 4-wire SPI | D[17:11], D[11:6], D[4:0] |
| 0 | 0 | 0 | 1 | 18-bit RGB interface + 4-wire SPI | D[17:0], |

15.1.1 6800-series System Bus Interface



Table 15-2 – The Function of 6800-series parallel interface

| PS3 | PS2 | PS1 | PS0 | Interface Mode | Data bus | R/W | E | D/C | /CS | Operation |
|-----|-----|-----|-----|---------------------------------|------------------|-----|---|-----|-----|----------------------------------|
| 1 | 0 | 1 | 1 | 16-bit 6800 parallel interface | D[17:10], D[8:1] | 1 | ↓ | 0 | 0 | Read 8-bit command |
| | | | | | | 1 | ↓ | 1 | 0 | Read 8-bit parameters or status* |
| | | | | | | 0 | ↓ | 0 | 0 | Write 8-bit command |
| | | | | | | 0 | ↓ | 1 | 0 | Write 16-bit display data |
| 1 | 0 | 1 | 0 | 8-bit 6800 parallel interface | D[8:1] | 1 | ↓ | 0 | 0 | Read 8-bit command |
| | | | | | | 1 | ↓ | 1 | 0 | Read 8-bit parameters or status* |
| | | | | | | 0 | ↓ | 0 | 0 | Write 8-bit command |
| | | | | | | 0 | ↓ | 1 | 0 | Write 8-bit display data |
| 0 | 1 | 1 | 1 | 18-bits 6800 parallel interface | D[17:0] | 1 | ↓ | 0 | 0 | Read 8-bit command |
| | | | | | | 1 | ↓ | 1 | 0 | Read 8-bit parameters or status* |
| | | | | | | 0 | ↓ | 0 | 0 | Write 8-bit command |
| | | | | | | 0 | ↓ | 1 | 0 | Write 18-bit display data |
| 0 | 1 | 1 | 0 | 9-bits 6800 parallel interface | D[8:0] | 1 | ↓ | 0 | 0 | Read 8-bit command |
| | | | | | | 1 | ↓ | 1 | 0 | Read 8-bit parameters or status* |
| | | | | | | 0 | ↓ | 0 | 0 | Write 8-bit command |
| | | | | | | 0 | ↓ | 1 | 0 | Write 9-bit display data |

* A dummy read is required before the first actual display data read

15.1.2 8080-series System Bus Interface

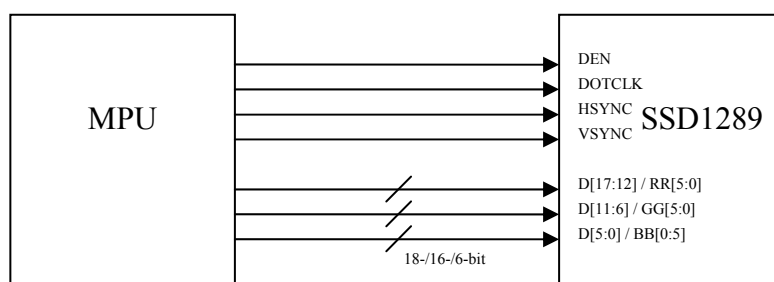


Table 15-3

| PS3 | PS2 | PS1 | PS0 | Interface Mode | Data bus | /WR | /RD | D/C | /CS | Operation |
|-----|-----|-----|-----|--------------------------------|---------------------|-----|-----|-----|-----|----------------------------------|
| 1 | 0 | 0 | 1 | 16-bit 8080 parallel interface | D[17:10], D[8:1] | 1 | 0 | 0 | 0 | Read 8-bit command |
| | | | | | | 1 | 0 | 1 | 0 | Read 8-bit parameters or status* |
| | | | | | | 0 | 1 | 0 | 0 | Write 8-bit command |
| | | | | | | 0 | 1 | 1 | 0 | Write 16-bit display data |
| 1 | 0 | 0 | 0 | 8-bit 8080 parallel interface | D[8:1] | 1 | 0 | 0 | 0 | Read 8-bit command |
| | | | | | | 1 | 0 | 1 | 0 | Read 8-bit parameters or status* |
| | | | | | | 0 | 1 | 0 | 0 | Write 8-bit command |
| | | | | | | 0 | 1 | 1 | 0 | Write 8-bit display data |
| 0 | 1 | 0 | 1 | 18-bit 8080 parallel interface | D[17:0] | 0 | 1 | 0 | 0 | Read 8-bit command |
| | | | | | | 1 | 0 | 1 | 0 | Read 8-bit parameters or status* |
| | | | | | | 0 | 1 | 0 | 0 | Write 8-bit command |
| | | | | | | 0 | 1 | 1 | 0 | Write 18-bit display data |
| 0 | 1 | 0 | 0 | 9-bit 8080 parallel interface | D[8:0] | 1 | 0 | 0 | 0 | Read 8-bit command |
| | | | | | | 1 | 0 | 1 | 0 | Read 8-bit parameters or status* |
| | | | | | | 0 | 1 | 0 | 0 | Write 8-bit command |
| | | | | | | 0 | 1 | 1 | 0 | Write 9-bit display data |

* A dummy read is required before the first actual display data read

15.1.3 Generic Bus Interface



15.2 Mapping for Writing an Instruction

| | | Hardware pins | | | | | | | | | | | | | | | | | |
|-----------|-----------------|---------------|------|------|------|------|------|-----|-----|----|------|------|------|------|------|------|-----|-----|----|
| Interface | Cycle | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 18 bits | | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | x | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 | x |
| 16 bits | | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 | |
| 9 bits | 1 st | | | | | | | | | | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | x |
| | 2 nd | | | | | | | | | | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 | x |
| 8 bits | 1 st | | | | | | | | | | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | |
| | 2 nd | | | | | | | | | | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 | |

Remark : x Don't care bits
 Not connected pins

15.3 Mapping for Writing Pixel Data

| | | | Hardware pins | | | | | | | | | | | | | | | | | |
|-----------------|-----------------|-----------------|---------------|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| Interface | Color mode | Cycle | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 18 bits | 262k | | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |
| 16 bits | 262k | 1 st | R5 | R4 | R3 | R2 | R1 | R0 | x | x | | G5 | G4 | G3 | G2 | G1 | G0 | x | x | |
| | | 2 nd | B5 | B4 | B3 | B2 | B1 | B0 | x | x | | R5 | R4 | R3 | R2 | R1 | R0 | x | x | |
| | | 3 rd | G5 | G4 | G3 | G2 | G1 | G0 | x | x | | B5 | B4 | B3 | B2 | B1 | B0 | x | x | |
| | | 1 st | R5 | R4 | R3 | R2 | R1 | R0 | x | x | | G5 | G4 | G3 | G2 | G1 | G0 | x | x | |
| | | 2 nd | x | x | x | x | x | x | x | x | | B5 | B4 | B3 | B2 | B1 | B0 | x | x | |
| | | 1 st | R5 | R4 | R3 | R2 | R1 | R0 | x | x | | G5 | G4 | G3 | G2 | G1 | G0 | x | x | |
| | 2 nd | B5 | B4 | B3 | B2 | B1 | B0 | x | x | | x | x | x | x | x | x | x | x | | |
| | 65k | | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 | |
| 9 bits | 262k | 1 st | | | | | | | | | | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 |
| | | 2 nd | | | | | | | | | | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |
| 8 bits | 262k | 1 st | | | | | | | | | | R5 | R4 | R3 | R2 | R1 | R0 | x | x | |
| | | 2 nd | | | | | | | | | | G5 | G4 | G3 | G2 | G1 | G0 | x | x | |
| | | 3 rd | | | | | | | | | | B5 | B4 | B3 | B2 | B1 | B0 | x | x | |
| | 65k | 1 st | | | | | | | | | | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | |
| 2 nd | | | | | | | | | | | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 | | |

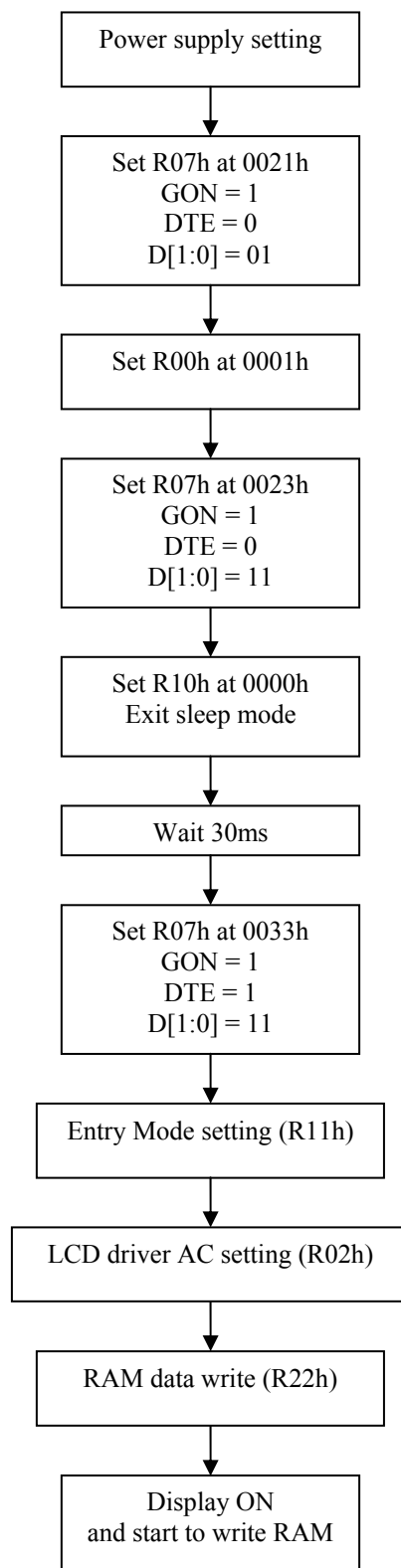
Remark : x Don't care bits
 Not connected pins

15.4 Mapping for Writing Pixel Data in generic mode

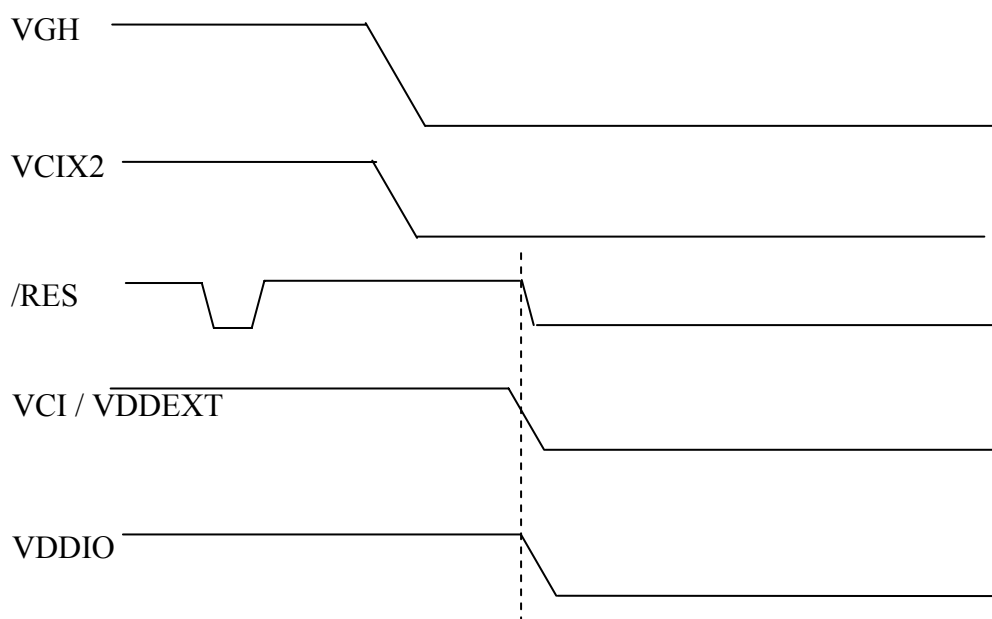
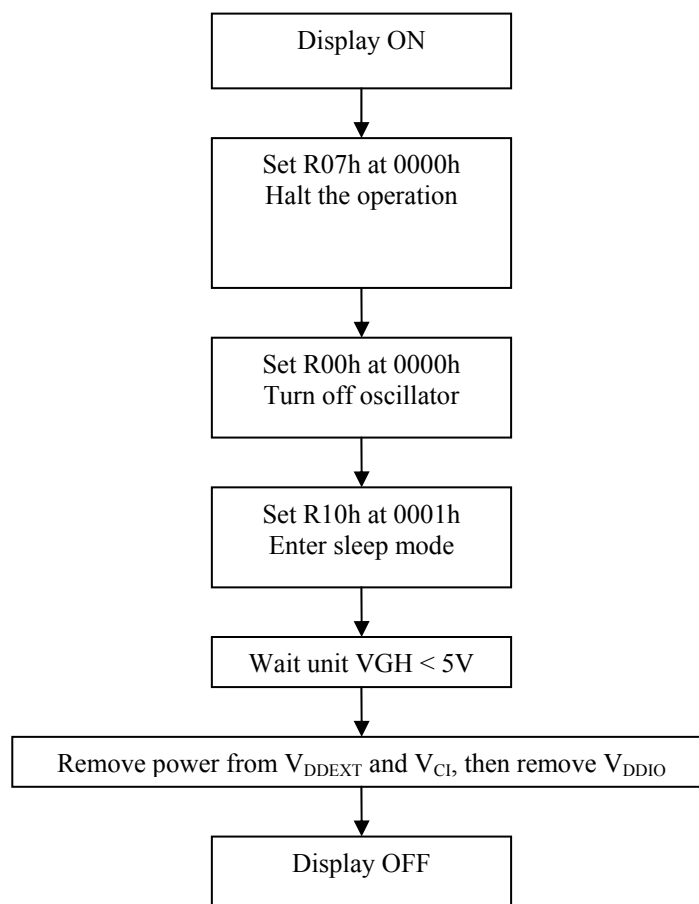
| | | Hardware pins | | | | | | | | | | | | | | | | | |
|------------|------------|---------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Interface | Color mode | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 18-bit RGB | 262k | RR5 | RR4 | RR3 | RR2 | RR1 | RR0 | GG5 | GG4 | GG3 | GG2 | GG1 | GG0 | BB0 | BB1 | BB2 | BB3 | BB4 | BB5 |
| 16-bit RGB | 65k | RR4 | RR3 | RR2 | RR1 | RR0 | | GG5 | GG4 | GG3 | GG2 | GG1 | GG0 | | BB0 | BB1 | BB2 | BB3 | BB4 |
| 6-bit RGB | 262k | RR5 | RR4 | RR3 | RR2 | RR1 | RR0 | | | | | | | | | | | | |
| | | GG5 | GG4 | GG3 | GG2 | GG1 | GG0 | | | | | | | | | | | | |
| | | BB0 | BB1 | BB2 | BB3 | BB4 | BB5 | | | | | | | | | | | | |

16 DISPLAY SETTING SEQUENCE

16.1 Display ON Sequence



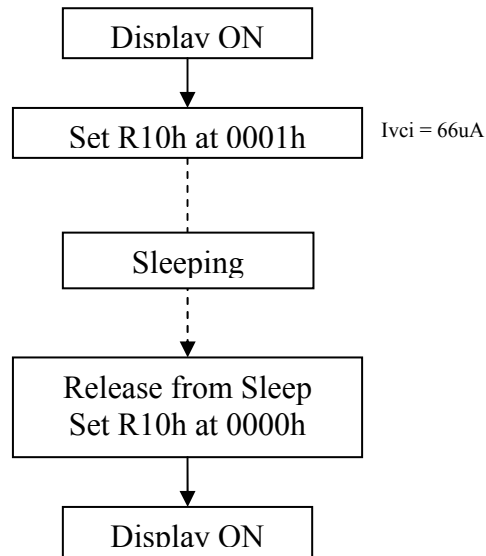
16.2 Display OFF Sequence



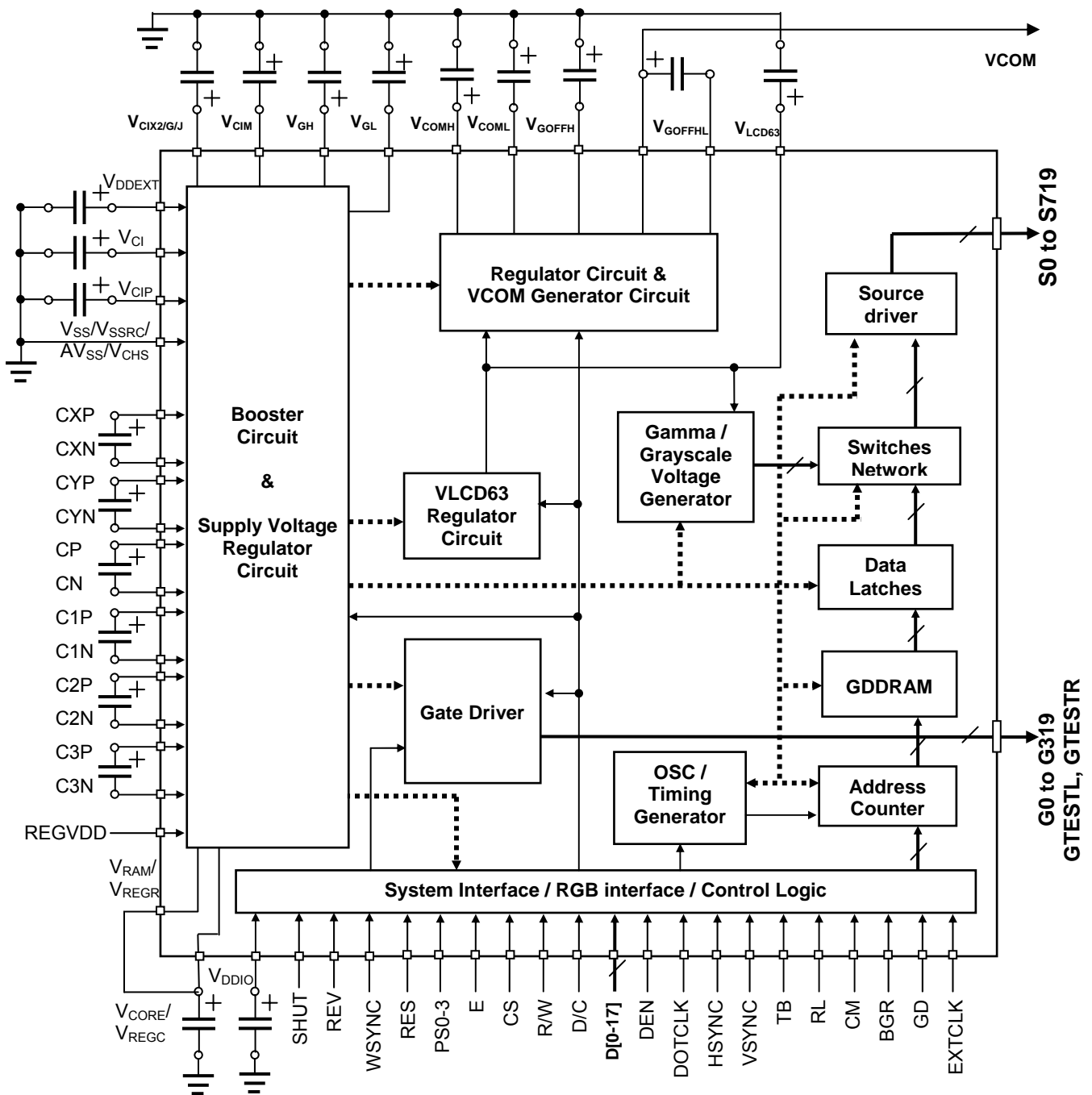
Note:

1. V_{DDIO} should be the last to fall, or VCI/V_{DDEXT}/V_{DDIO} could be power off at the same time
2. If OTP is active in the application, the OTP programming voltage should be turned off and capacitors at VGH and VCIX2 discharged before VCI/V_{DDEXT}/V_{DDIO} are turned off.

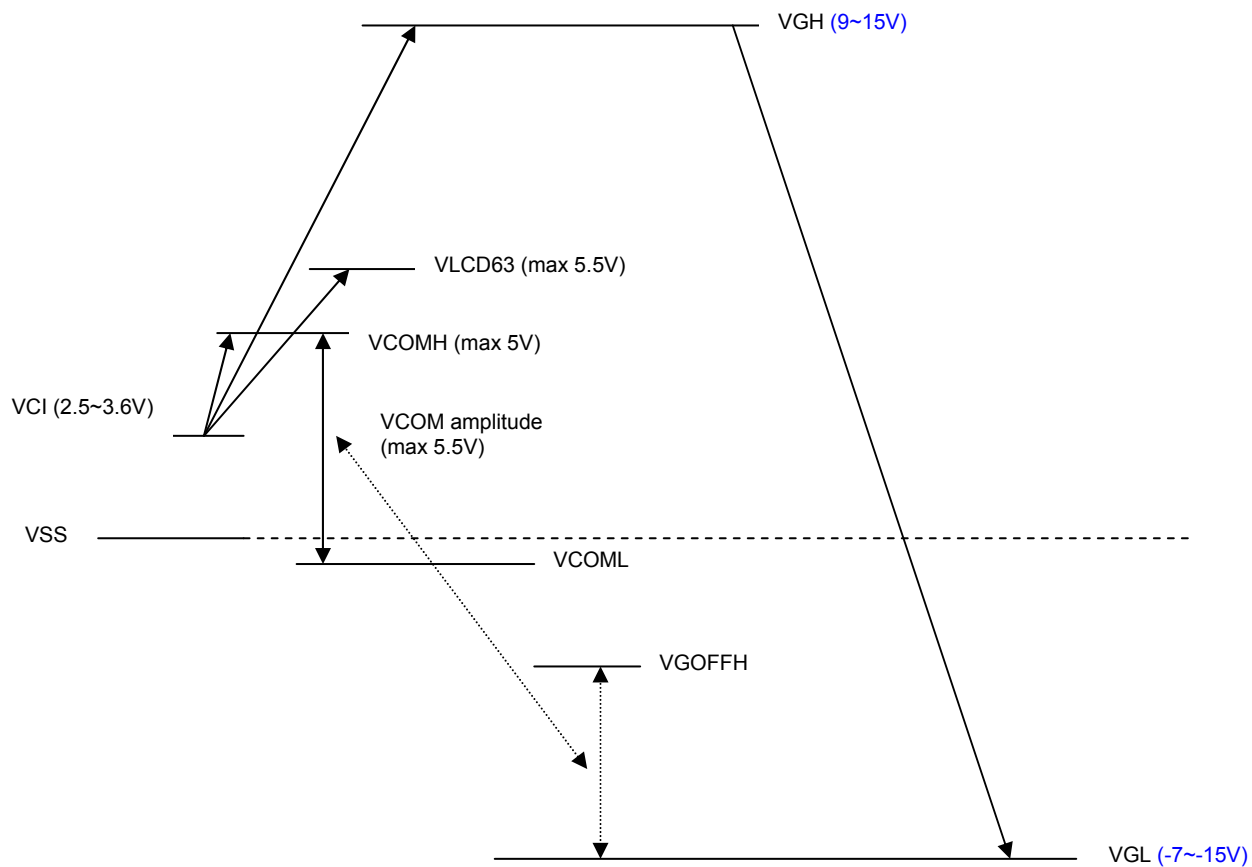
16.3 Sleep Mode Display Sequence



17 POWER SUPPLY BLOCK DIAGRAM



18 SSD1289 OUTPUT VOLTAGE RELATIONSHIP



19 APPLICATION CIRCUIT

Figure 19-1 - Booster Capacitors

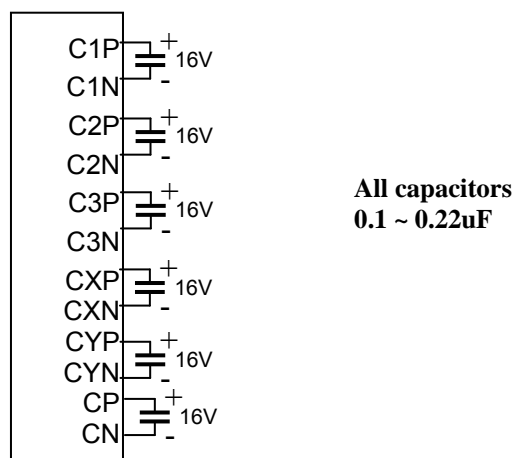
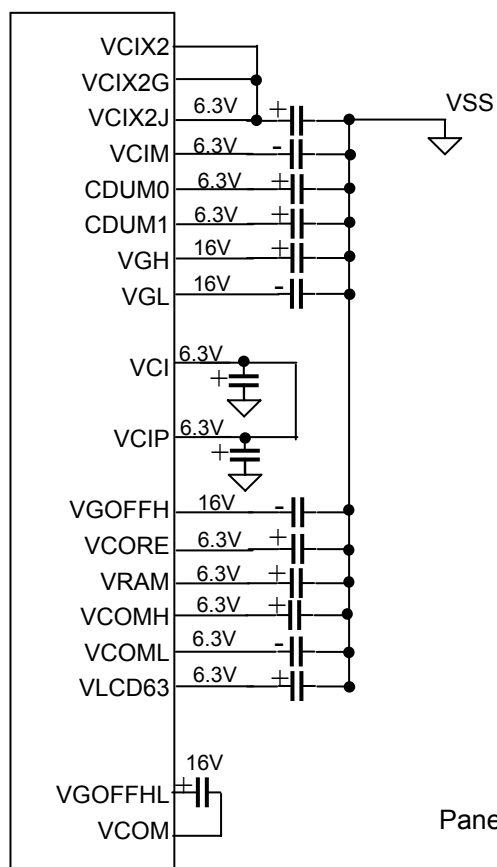


Figure 19-2 – Filtering and charge sharing capacitors



Capacitor for VCIX2 / VCIX2G / VCIX2J = 3.3uF ~ 4.7uF.
Capacitor for VCI = 4.7uF
All other capacitors 1.0uF ~ 2.2uF.
2.2uF is preferred for better display and power consumption.
Capacitors on VGOFFH, VGOFFHL are for Cs on gate application. Leave them open for Cs on COM application.
Capacitors on CDUM0 and CDUM1 are for power saving.

VCIX2 should be separated with VCIX2G/VCIX2J at ITO layout to provide noise free path.
VCI should be separated with VCIP at ITO layout to provide noise free path.
VSS should be separated with VCHS, AVSS and VSSRC at ITO layout to provide noise free path.

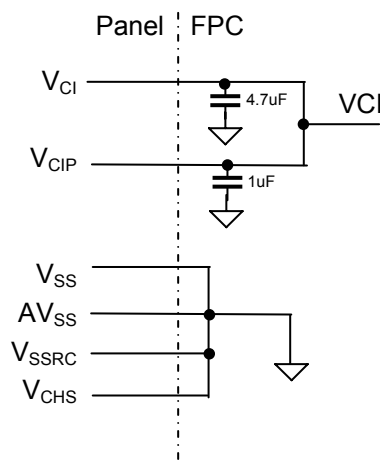
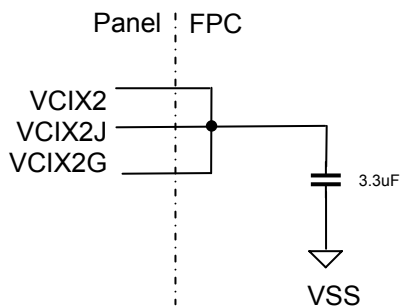


Figure 19-3 – Power supply pin connection

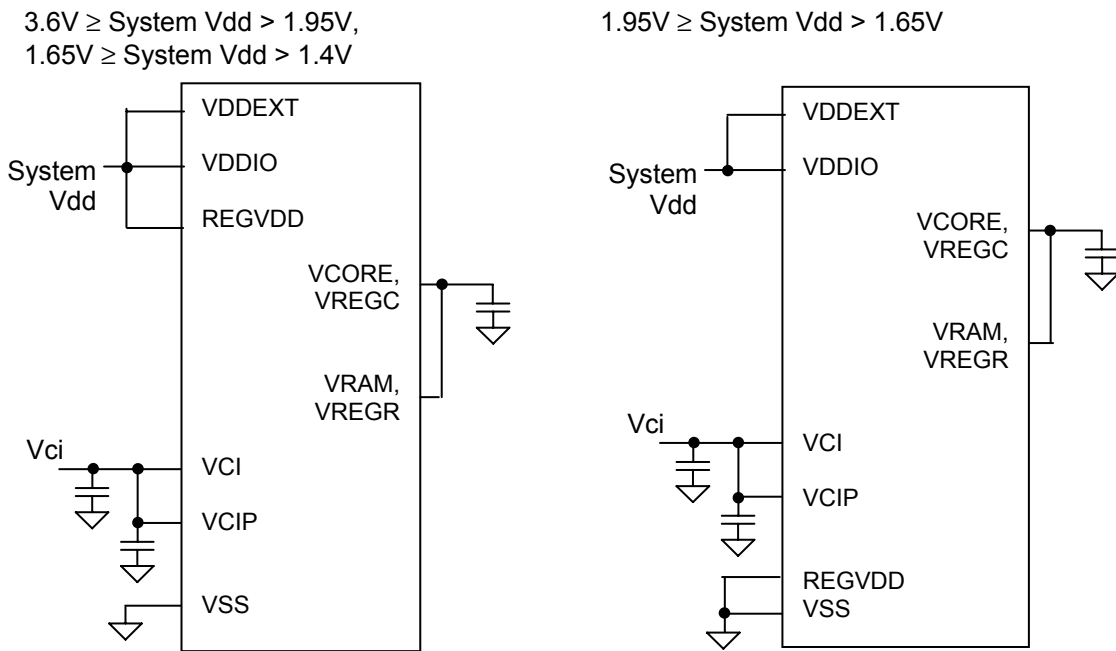


Figure 19-4 – Panel Connection Example

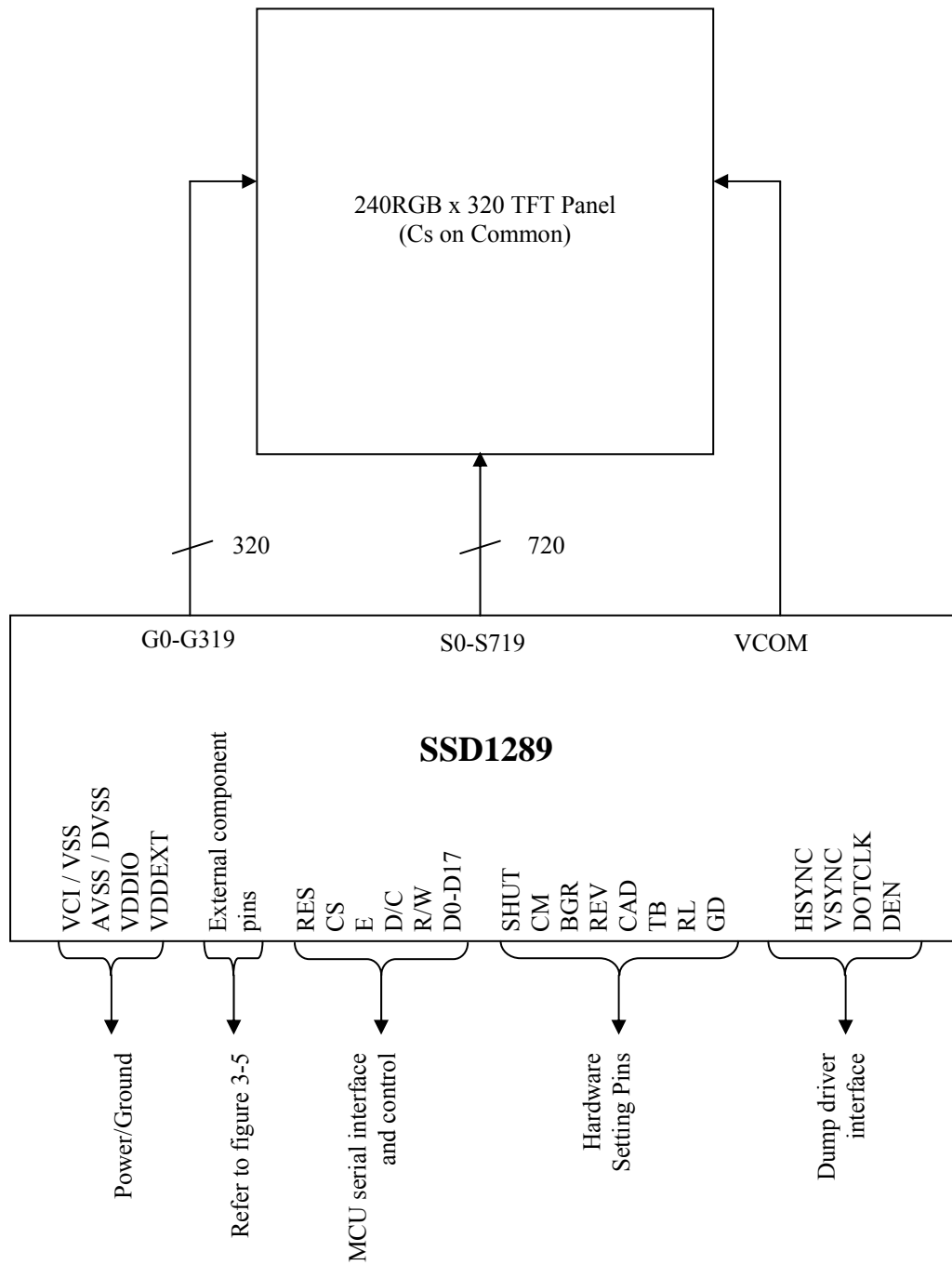
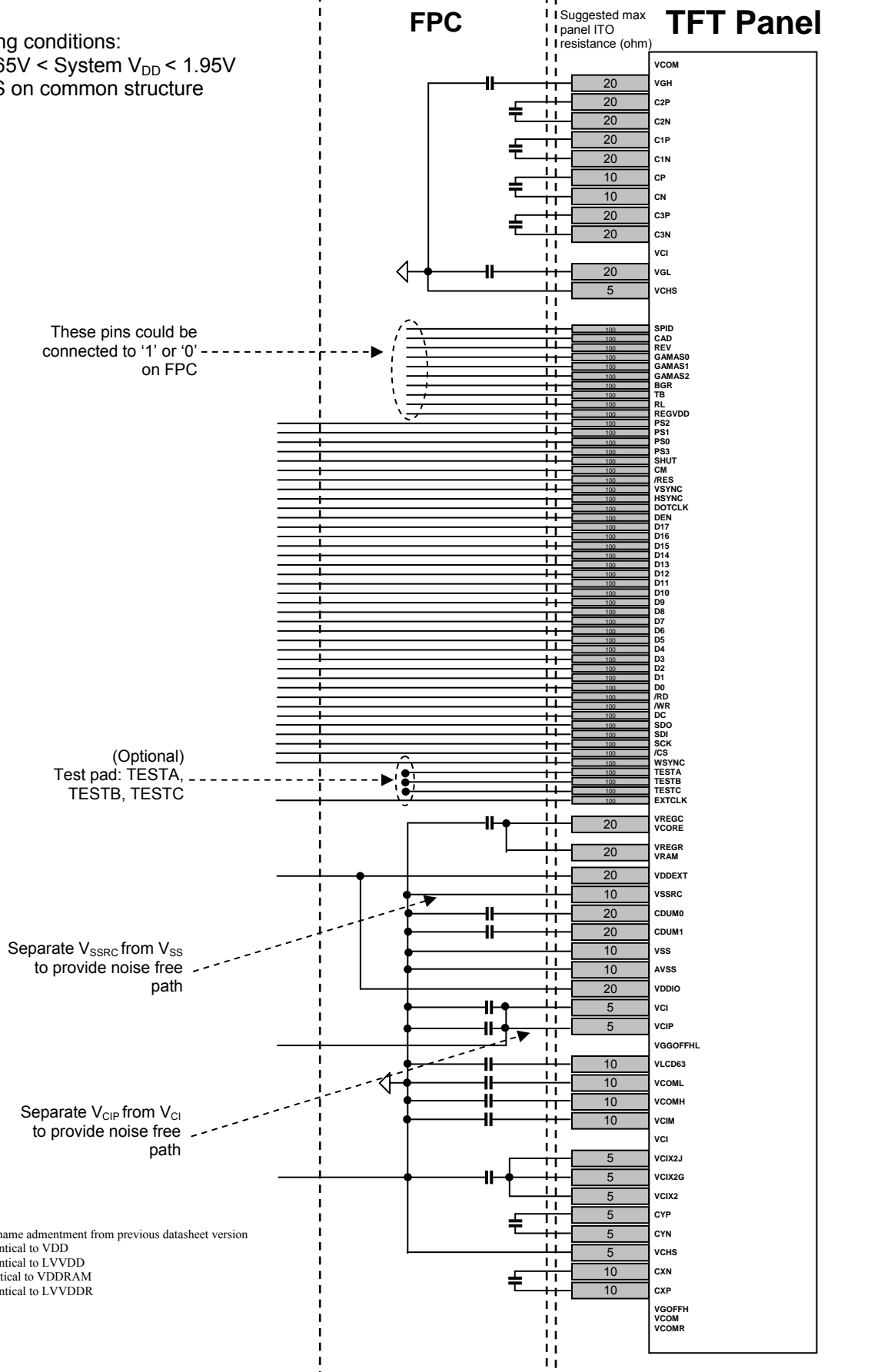


Figure 19-5 - ITO and FPC connection example

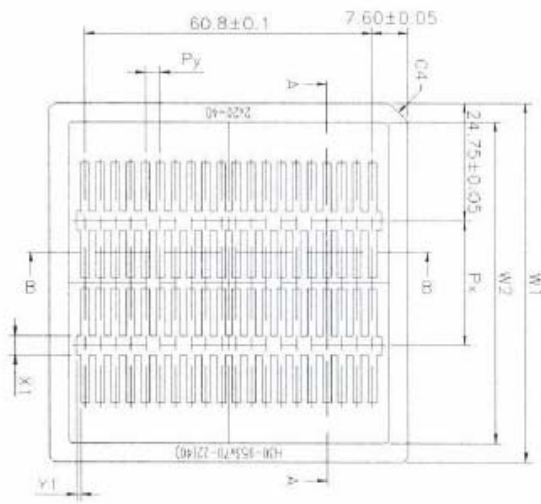
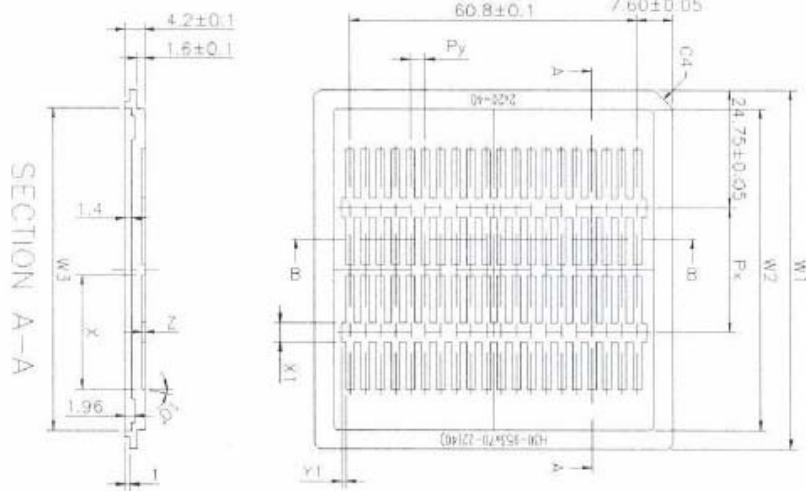
Operating conditions:

- $1.65V < \text{System } V_{DD} < 1.95V$
- CS on common structure

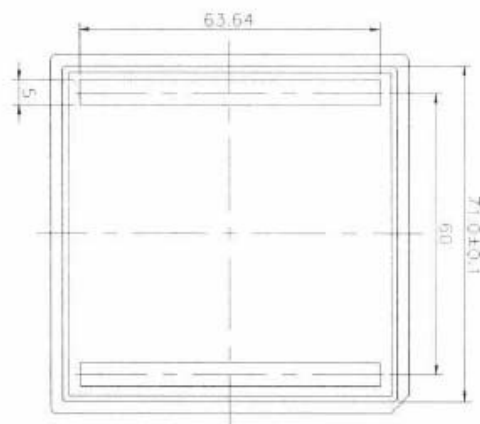


20 PACKAGE INFORMATION

20.1 DIE TRAY DIMENSIONS



SECTION B-B



| | Spec | |
|----|------------|--------|
| | mm | (mil) |
| W1 | 76.00±0.1 | (2992) |
| W2 | 68.00±0.1 | (2677) |
| W3 | 68.30±0.1 | (2689) |
| X1 | 4.00±0.1 | (157) |
| Y1 | 1.00±0.1 | (39) |
| Px | 26.50±0.05 | (1043) |
| Py | 3.20±0.05 | (126) |
| X | 24.21±0.05 | (953) |
| Y | 1.79±0.05 | (70) |
| Z | 0.56±0.05 | (22) |
| N | 40 | |

- Remark1 :
1. Depth of text : Max. 0.1mm
 2. Tray material : ABS
 3. Tray color code : Black
 4. Surface resistance : $10^9 \sim 10^{11} \Omega$
 5. Tray warpage : Max. 0.10mm
 6. Unspecified dim's tolerance : $\pm 0.15\text{mm}$
 7. Pocket size : 24.21x1.79x0.56mm

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