AXI Central DMA v2.0

***IP User Guide** (Beta Release)*

November 29, 2023

RapidSilicon

Contents

IP Summary

Introduction

The AXI Central Direct Memory Access (AXI CDMA) is a highly flexible and scalable soft IP core that is designed to provide a direct memory access (DMA) capability to System-on-Chip (SoC) designs. The AXI CDMA is optimized for memory-mapped source and destination addresses, enabling direct communication between different memory regions without the need for involvement from the processor.

Built on the widely adopted Advanced extensible Interface (AXI) bus protocol, the AXI CDMA offers a standardized interconnect architecture for on-chip and off-chip communication. By enabling fast and efficient data transfers between memory regions, the AXI CDMA reduces the load on the processor and improves the overall performance and efficiency of the system, especially for data-intensive applications. With its ease of integration, reliability, and high-performance capabilities, the AXI CDMA is an essential component of modern SoC designs and plays a critical role in enabling efficient communication between different components of the system.

Features

- Data Transfer via AXI4 Interface
- Register Access via AXI4-Lite Slave Interface
- Configurable address widths and data widths
- Register Direct Mode
- Optional realignment FIFO for unaligned transfers
- Interrupts for CDMA completion and errors

Overview

AXI Central DMA

The AXI CDMA is designed to be part of the custom embedded setup via the AXI4 Interconnect, providing convenient access to the system processor via the AXI4-Lite interface. To perform simple CDMA operations, the core can be controlled through the register interface. The core is responsible for transferring data between the designated source and destination addresses. Upon completion, the interrupt output from the AXI CDMA will trigger an interrupt in the system Interrupt Controller, freeing up the processor for other tasks shown figure 1. The CDMA is optimized for efficient data transfer between memory locations in the custom embedded setup.

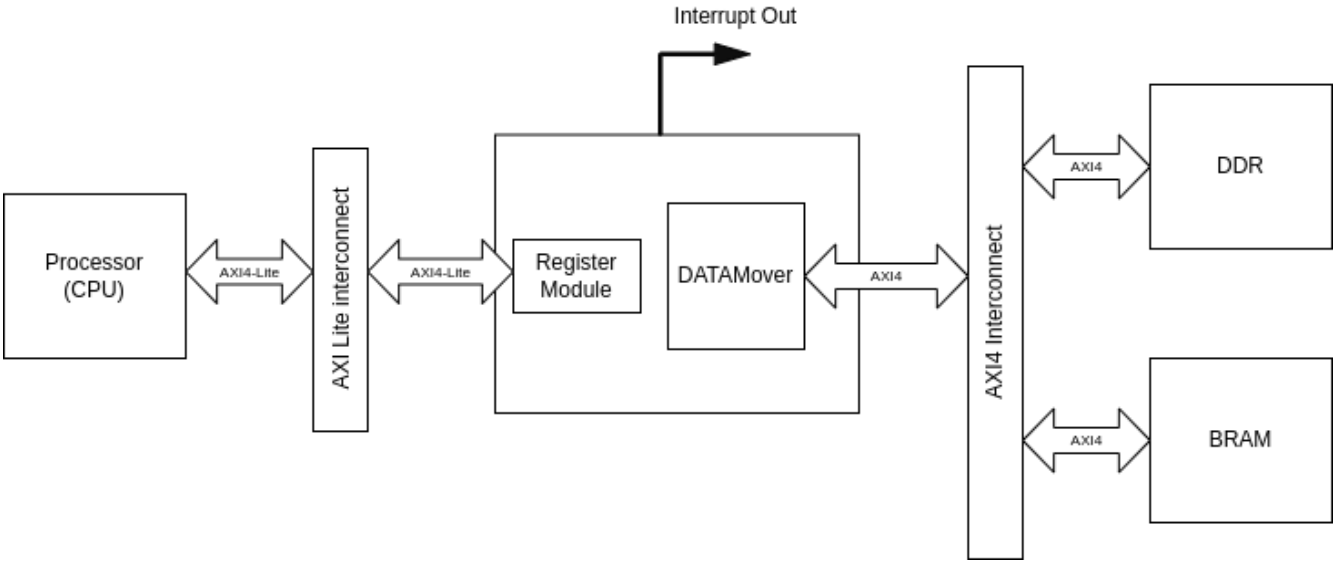


Figure 1. AXICDMA Typical configuration

Licensing

IP Specification

Overview

The figure 2 shows the detailed internal block diagram of the AXICDMA (AXI Central DMA). The AXI CDMA is a component designed to provide high-speed data transfer capabilities in an embedded processing system utilizing the AXI4 system interfaces.The core consists of multiple functional blocks, including an AXI4 Master interface for memory-mapped to memory-mapped (MM2M) transfer operations, an AXI4-Lite Slave interface for register access, and an AXI DataMover helper core for high-throughput data transfer.

The skid buffer is a component of the AXI CDMA IP core works by temporarily storing data, allowing for more time to process and transfer the information. The primary purpose of the skid buffer is to provide pipeline support, ensuring efficient and effective data transfer. The Register Module houses the control register for the AXI CDMA, which are accessible via the AXI4-Lite Slave interface. These registers provide control and monitoring for all CDMA operations and transfer requests.The AXI DataMover is responsible for the primary data transport function and offers various features, such as address boundary protection, automatic burst partitioning, and byte-level data realignment. This allows the AXI CDMA to read and write data from/to any byte offset combination, ensuring efficient and effective data transfer.

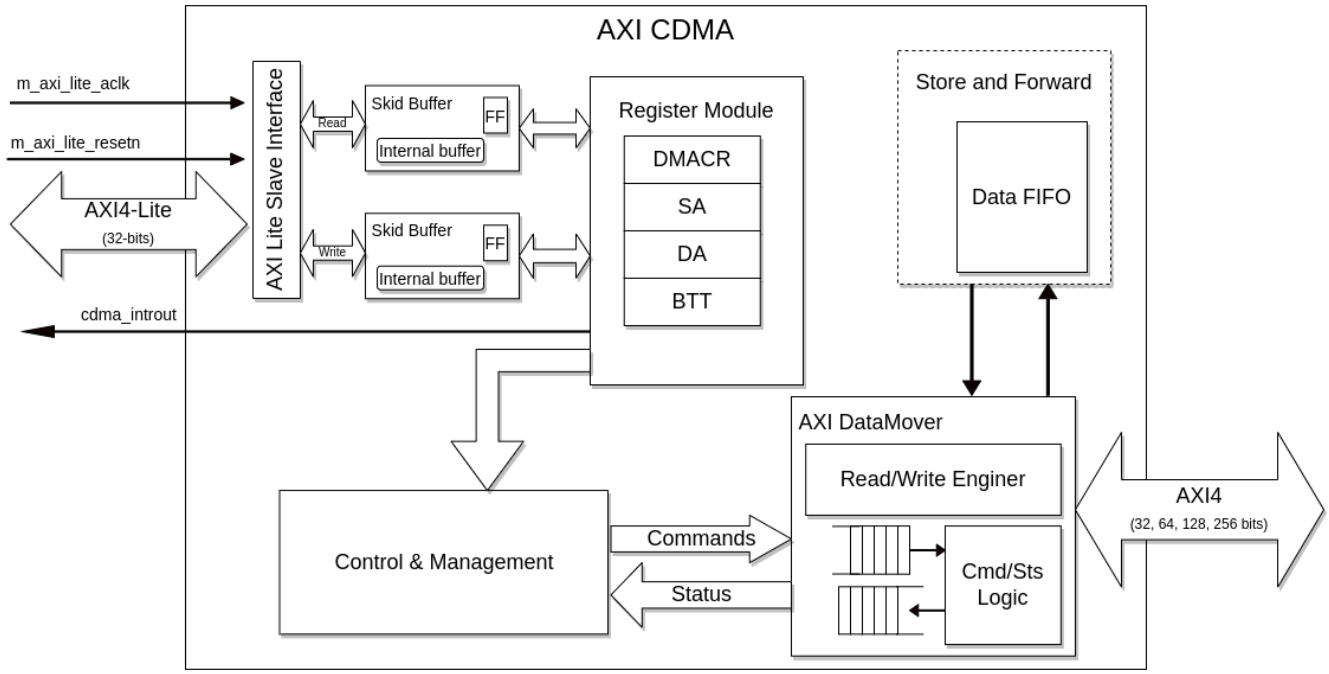


Figure 2. Top Module

The store and forward block with data FIFO is a component of the AXI CDMA IP core. It is connected with the AXI DataMover and its purpose is to temporarily store and buffer incoming data, allowing it to be processed in an efficient manner. The data FIFO serves as a buffer for the transfer of data between the DataMover and the store and forward mechanism helps to ensure a smooth and error-free flow of data within the system.

IP Support Details

The table 1 presents the specifics of IP support for the AXICDMA IP Core, including pertinent information such as synthesis, simulation and source details.

Compliance		IP Resources					Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Software Driver**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI4-lite	verilog	SDC	C++	-	-	Raptor	Verilator	Raptor

Table 1. IP Information

Ports

Table 3 lists the top Slave interface ports of AXICDMA.

Signal name	I/O	Description
AXI4-Lite Slave Interface Signals		
AXI4-Lite Clock and Reset		
S_AXI_ACLK	I	AXI4-Lite Clock
S_AXI_ARESETN	I	AXI4-Lite RESET
AXI4-Lite WRITE ADDRESS CHANNEL		
s_axil_awvalid	I	AXI4-Lite Write address valid
s_axil_awready	O	AXI4-Lite Write address ready
s_axil_awaddr	I	AXI4-Lite Write address
s_axil_awprot	I	AXI4-Lite Protection type
AXI4-Lite WRITE DATA CHANNEL		
s_axil_wvalid	I	AXI4-Lite Write valid
s_axil_wready	O	AXI4-Lite Write ready.
s_axil_wdata	I	AXI4-Lite Write data
s_axil_wstrb	I	AXI4-Lite Write strobes
AXI4-Lite WRITE RESPONSE CHANNEL		
s_axil_bvalid	O	AXI4-Lite~ Write response valid
s_axil_bready	I	AXI4-Lite Response ready
s_axil_bresp	O	AXI4-Lite Write response
AXI4-Lite READ ADDRESS CHANNEL		
s_axil_arvalid	I	AXI4-Lite Read address valid
s_axil_arready	O	AXI4-Lite Read address ready
s_axil_araddr	I	AXI4-Lite Read address
s_axil_arprot	I	AXI4-Lite Protection type
AXI4-Lite READ DATA CHANNEL		
s_axil_rvalid	I	AXI4-Lite Read valid
s_axil_rready	O	AXI4-Lite Read ready
s_axil_rresp	I	AXI4-Lite Read data
s_axil_rdata	O	AXI4-Lite Read response

Table 3. AXICDMA Slave Interface

Table 5 lists the top Master interface ports of AXICDMA.

Signal name	I/O	Description
AXI4 Master WRITE ADDRESS CHANNEL		
m_axi_awid	O	AXI4 Master Write ID
m_axi_awaddr	O	AXI4 Master Write address
m_axi_awlen	O	AXI4 Master Write busrt length
m_axi_awsize	O	AXI4 Master Write busrt size
m_axi_awbusrt	O	AXI4 Master Write busrt type
m_axi_awlock	O	AXI4 Master Write locking
m_axi_awcache	O	AXI4 Master Write cache handling
m_axi_awprot	O	AXI4 Master Write protection level
m_axi_awqos	O	AXI4 Master Write QoS setting
m_axi_awvalid	O	AXI4 Master Write address valid

m_axi_awready	I	AXI4 Master Write addresready
AXI4 Master WRITE DATA CHANNEL		
m_axi_wdata	O	AXI4 Master Write data
m_axi_wstrb	O	AXI4 Master Write data strobe
m_axi_wlast	O	AXI4 Master Write data last transfer in busrt
m_axi_wvalid	O	AXI4 Master Write data valid
m_axi_wready	I	AXI4 Master Write data ready
AXI4 Master WRITE RESPONSE CHANNEL		
m_axi_bid	I	AXI4 Master Write response ID
m_axi_bresp	I	AXI4 Master Write response
m_axi_bvalid	I	AXI4 Master Write response valid
m_axi_bready	O	AXI4 Master Write response ready
AXI4 Master READ ADDRESS CHANNEL		
m_axi_arid	O	AXI4 Master read ID
m_axi_araddr	O	AXI4 Master read address
m_axi_arlen	O	AXI4 Master read busrt length
m_axi_arsize	O	AXI4 Master read busrt size
m_axi_arbusrt	O	AXI4 Master read busrt type
m_axi_arlock	O	AXI4 Master read locking
m_axi_arcache	O	AXI4 Master read cache handling
m_axi_arprot	O	AXI4 Master read protection level
m_axi_arqos	O	AXI4 Master read QoS setting
m_axi_arvalid	O	AXI4 Master read address valid
m_axi_arready	I	AXI4 Master read addresready
AXI4 Master WRITE DATA CHANNEL		
m_axi_rid	I	AXI4 Master Read DATA ID
m_axi_rdata	I	AXI4 Master read data
m_axi_rresp	I	AXI4 Master read response
m_axi_rlast	I	AXI4 Master read data last transfer in busrt
m_axi_rvalid	I	AXI4 Master read data valid
m_axi_rready	O	AXI4 Master read data ready

Table 5. AXICDMA Master Interface

Parameters

Table 5 lists the parameters of the AXICDMA.

Parameters	Values	Default Values	Description
AXI DATA WIDTH	8-256	32	Define size of data for AXI master data channel
AXI ADDR WIDTH	8-256	32	Define size of address for AXI Master address channel
AXIL DATA WIDTH	32	32	Define the size of data for AXILite data channel
AXIL ADDR WIDTH	1-32	32	Define size of address for AXILite address channel
ID WIDTH	1-64	5	Define the of value of AXI ID

Table 5. Parameters

Registers Address Space

Table 8 lists the configuration registers of the AXICDMA.

Name	Register ID	Bits	Type	Off sets	Default Value	Description
Control Register	CTRL_ADDR	32	RW	0x00	0x00000000	Configures and controls the CDMA transfer
Reserved	UNUSED_ADDR	32		0x04	0x00000000	Not used by the CDMA controller, can be ignored
Source Address Register LSB	SRCLO_ADDR	32	RW	0x08	0x00000000	Holds the low 32-bits of the 64-bit source memory address
Source Address Register MSB	SRCHI_ADDR	32	RW	0x0C	0x00000000	Holds the high 32-bits of the 64-bit source memory address
Destination Address Register LSB	DSTLO_ADDR	32	RW	0X10	0x00000000	Holds the low 32-bits of the 64-bit destination memory address
Destination Address Register MSB	DSTHI_ADDR	32	RW	0X14	0x00000000	Holds the high 32-bits of the 64-bit destination memory address
Byte to Transfer Register LSB	LENLO_ADDR	32	RW	0X18	0x00000000	Holds the low 32-bits of the total number of data words minus the successful writes
Byte to Transfer Register MSSB	LENHI_ADDR	32	RW	0x1C	0x00000000	Holds the high 32-bits of the total number of data words minus the successful writes

Table 8. AXICDMA Registers Address Space

CSRs Description

AXICDMA Control Register (CTRL_ADDR)

This register is responsible for providing control of the AXI CDMA to software applications.

Bits		Description	Bit-field	Val-ues	Configuration
Reserved		RESERVED	[31:23]		Reserved
KEY	QoS	The QOS field is used to set the quality of service for the transfer, such as priority level, bandwidth, or latency.	[22:20]	0	set the AXI quality of service for the transfer
	PROT	The PROT field is used to set the level of protection for the transfer, such as read-only, read-write, or execute-only.	[19:16]	0	set the AXI level of protection for the transfer
Reseved		RESERVED	[15:5]		Reserved
Error		Indicates whether the transfer ended with an error.	[4]	1	Error Interrupt enabled
Abort		Indicates whether the transfer is being aborted or has been aborted.	[3]	0	transfer is not being aborted
				1	Abort a transfer that is currently in progress
Interrupt Enable		Enables or disables interrupts for the CDMA core.	[2]	0	Complete Interrupt disable
				1	Complete Interrupt Enable
Interrupt Clear		Clears any pending interrupts.	[1]	1	Clear the Interrupt
Start/Busy		When set to 1, initiates a transfer. When set to 0, stops the transfer.	[0]	0	CDMA DATA transferred
				1	CDMA DATA transferring

Control Register

[31:23]	[22:20]	[19:16]	[15:5]	4	3	2	1	0
Reserved	QoS	PROT	Reserved	Error	Abort	IRQ_EN	IRQ_CLR	Start/Busy

AXICDMA Source Address Register (SCRCLO_ADDR)

This register serves as the initial read address for data transfers performed by DMA operations.

Bits	Description	Bitfield	Values	Configuration
SCRCLO_ADDR	This register serves as the initial read address for data transfers performed by CDMA operations.	[31:0]	0	User Specifier source Address

Source Address Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Source Address																															

AXICDMA MSB 32bits Source Address Register (SCRCHI_ADDR)

This register serves as the MSB 32bits of read address for data transfers performed by DMA operations.

Bits	Description	Bitfield	Values	Configuration
SCRCHI_ADDR	This register serves as the MSB 32bits of read address for data transfers performed by CDMA operations.	[31:0]	0	User Specifier MSB 32bits source Address

MSB 32bits Source Address Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB 32bits Source Address																															

AXICDMA Destination Address Register (DSTLO_ADDR)

This register serves as the initial write address for data transfers performed by DMA operations.

Bits	Description	Bitfield	Values	Configuration
DSTLO_ADDR	This register serves as the initial write address for data transfers performed by CDMA operations.	[31:0]	0	User Specifier Destination Address

Destination Address Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Destination Address																															

AXICDMA MSB 32bits Destination Address Register (DSTHI_ADDR)

This register serves as the MSB 32bits of write destination address for data transfers performed by DMA operations.

Bits	Description	Bitfield	Values	Configuration
DSTHI_ADDR	This register serves as the MSB 32bits of write destination address for data transfers performed by CDMA operations.	[31:0]	0	User Specifier MSB 32bits Destination Address

MSB 32bits Destination Address Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB 32bits Destination Address																															

AXICDMA Bytes to Move Register (LENLO_ADDR)

This register serves the values of Bytes to Move for data transfers performed by CDMA operations.

Bits	Description	Bitfield	Values	Configuration
LENLO_ADDR	This register serves the values of Bytes to Move for data transfers performed by CDMA operations.	[31:0]	0	User Specifier No of Bytes to Transfer

Bytes to Move Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bytes to Move																															

AXICDMA MSB 32bits Bytes to Move Register (LENHI_ADDR)

This register serves the MSB 32bits values of Bytes to Move for data transfers performed by CDMA operations.

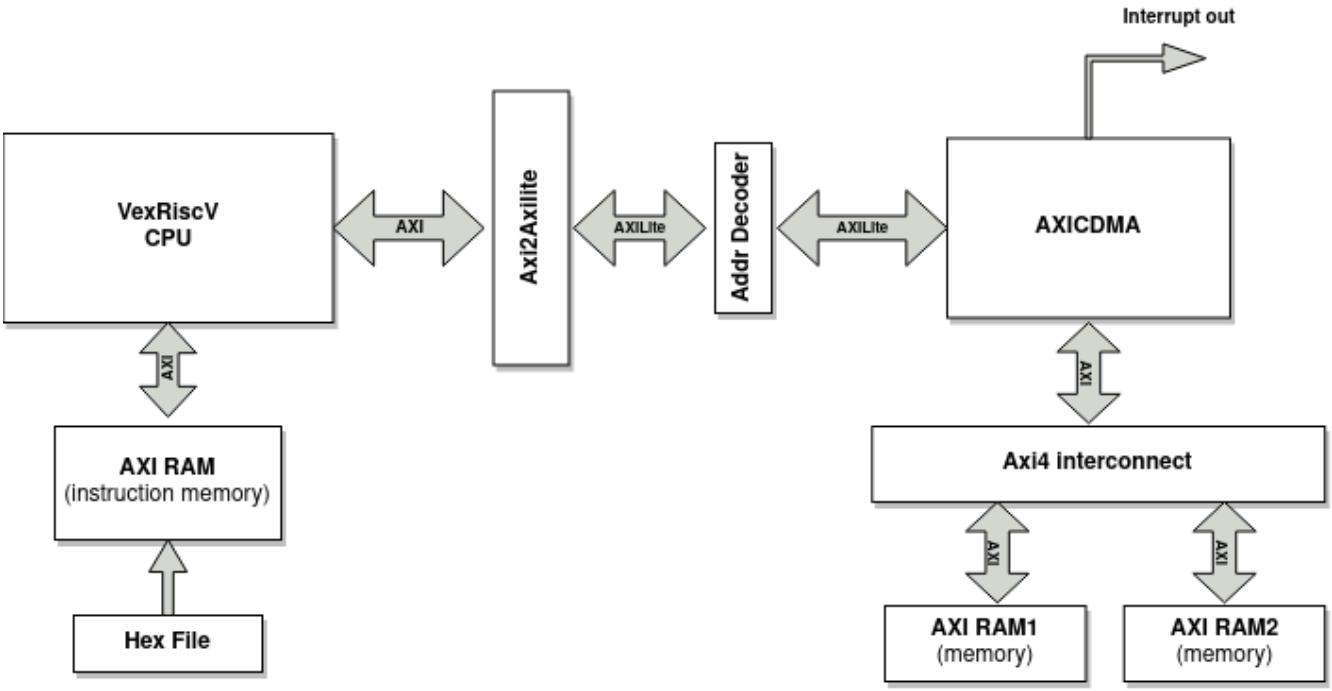
Bits	Description	Bitfield	Values	Configuration
LENHI_ADDR	This register serves MSB 32bits the values of Bytes to Move for data transfers performed by CDMA operations.	[31:0]	0	User Specifier No of MSB 32bits Bytes to Move

MSB 32bits Bytes to Move Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB 32bits Bytes to Move																															

AXICDMA Example Design

In this example design, a baremetal hex file is loaded into an AXI RAM, which is used as a substitute for a ROM. The VexRiscv CPU is capable of directly loading instructions onto its instruction bus without the need for an interconnect. The AXICDMA is connected as a peripheral to the CPU via an AXILite interconnect, which communicates with the CPU using an AXI2AXILite bridge. Additionally, the AXICDMA is connected to two different AXI BLOCK RAMs via an AXI interconnect. The AXICDMA is responsible for reading data from one AXI RAM and writing it to the other AXI RAM shown figure **??**.



AXICDMA Example Design

Design Flow

IP Customization and Generation

CDMA IP core is a part of the Raptor Design Suite Software. A customized CDMA can be generated from the Raptor's IP configurator window.

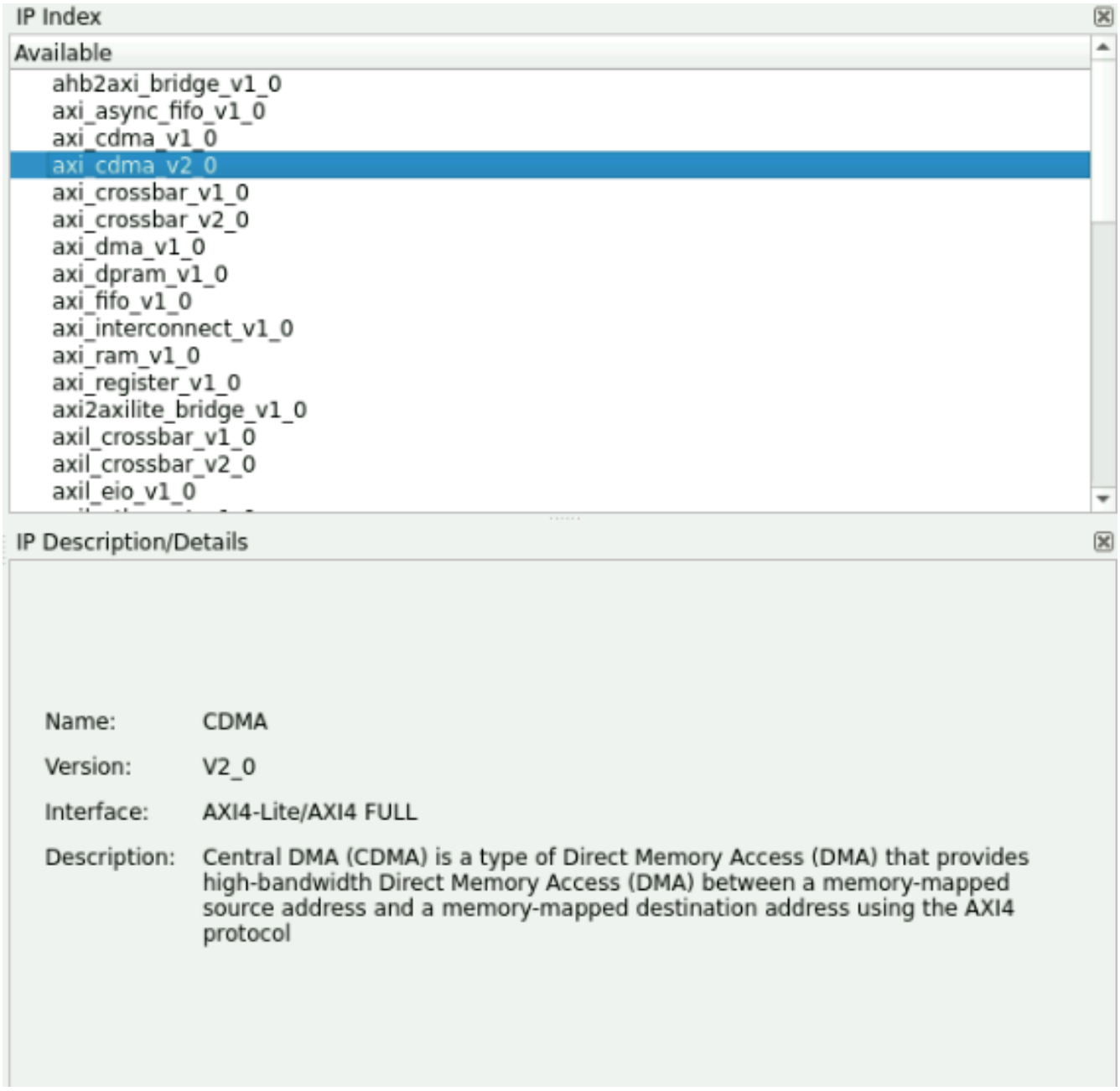


Figure 4. IP list

Parameters Customization: From the IP configuration window, the parameters of the CDMA can be configured and CDMA features can be enabled for generating a customized CDMA IP core that suits the user application requirment.

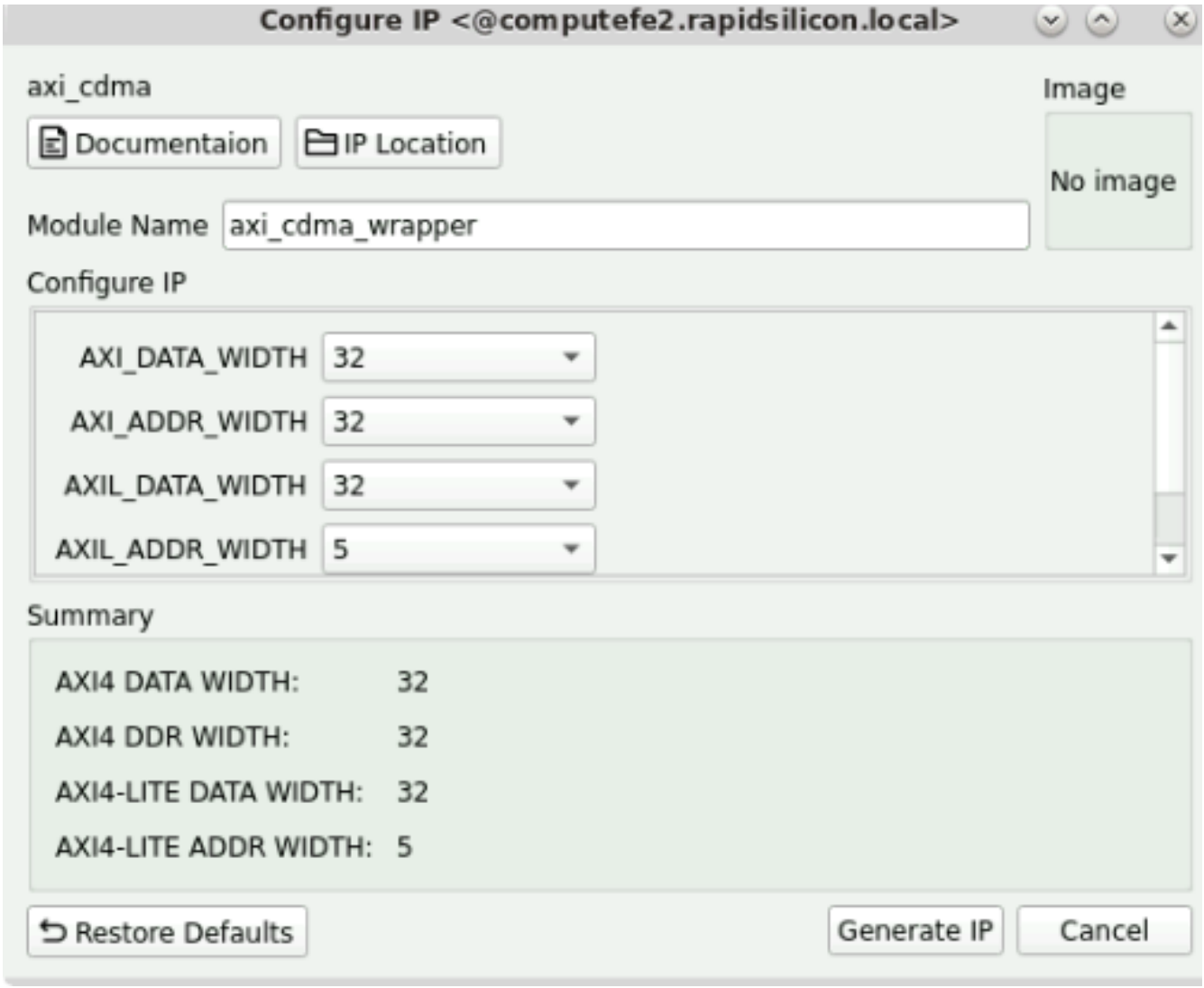


Figure 5. IP Configuration

Test Bench

There is no test bench for this IP

Revision History

Date	Version	Revisions
November 29, 2023	2.0	AXICDMA User Guide Document