

On-Chip Logic Analyzer v1.0

IP User Guide (*Beta Release*)



January 31, 2024

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IP Summary

Introduction

The On Chip Logic Analyzer (OCLA) core is a customizable logic analyzer that will be used for verification or debugging through the monitoring of internal signals within a design on field-programmable gate arrays (FPGAs).

The OCLA core boasts a variety of features commonly found in modern logic analyzers, such as edge transition triggering, multi-trigger options, and configurable parameters such as the number of probes and trace memory depth.

Additionally, the OCLA offers several modes for data capturing operations during debugging, including continuous, pre-trigger, post-trigger, and center-trigger options.

Features

- Multiple Probe Ports
- Emulated Input/Output (EIO) support
- Configurable trigger condition
- Configurable trigger mode
- Configurable data depth
- AXI probes on OCLA IP core to debug AXI IP cores in a system

Overview

On-Chip Logic Analyzer

The OCLA is an IP core that can be used to monitor and capture the behavior of signals that are connected to its "probe port." The OCLA is configured through a JTAG interface, which allows the user to set up the OCLA's modes and controls.

These signals, attached to the probe inputs, are sampled at design speeds and stored using on-chip block RAM (BRAM). The core parameters specify the number of probes, sample memory depth, debug mode and the width for each probe input. Communication with the OCLA core is conducted using JTAG interface of the FPGA.

The figure 1 shows the top-level interface diagram of the OCLA IP core.

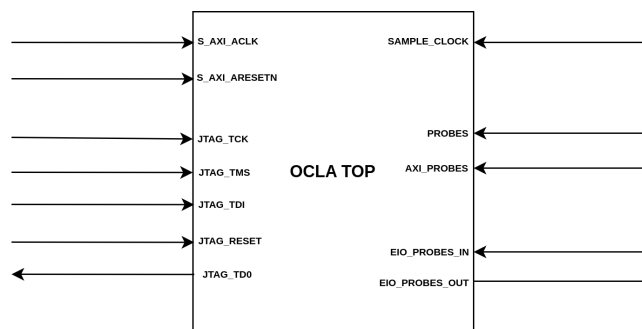


Figure 1. OCLA Top

After the design is loaded into the FPGA, use the OCLA tcl commands to set up a trigger event for the OCLA measurement. After the trigger occurs, the sample buffer is filled. You can view this data using the GTK waveform.

Licensing

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IP Specification

Overview

The OCLA IP is characterized by a modular design, comprising various modules such as the JTAG Interface, Trigger Control Unit, Sampler Buffer, Controller, and On-Chip Trace Memory modules. Furthermore, it is designed as a multi-clock system, with a sampling clock and an AXI clock.

The sampling clock is synchronized with the clock of the System/Design under test (S/DUT) and is used to sample data on the rising edge of this clock, based on the configured sampling mode of the OCLA. OCLA can be configured through the JTAG interface using tcl commands and the collected data can be subsequently read via the JTAG.

The On-Chip trace memory controller is implemented as a circular buffer based on a modified asynchronous FIFO. This design handles the clock domain crossing of the trace memory data and configuration data, ensuring efficient and accurate data transfer between the different modules.

The figure 2 presents an overview of the Debug Core in a practical use case.

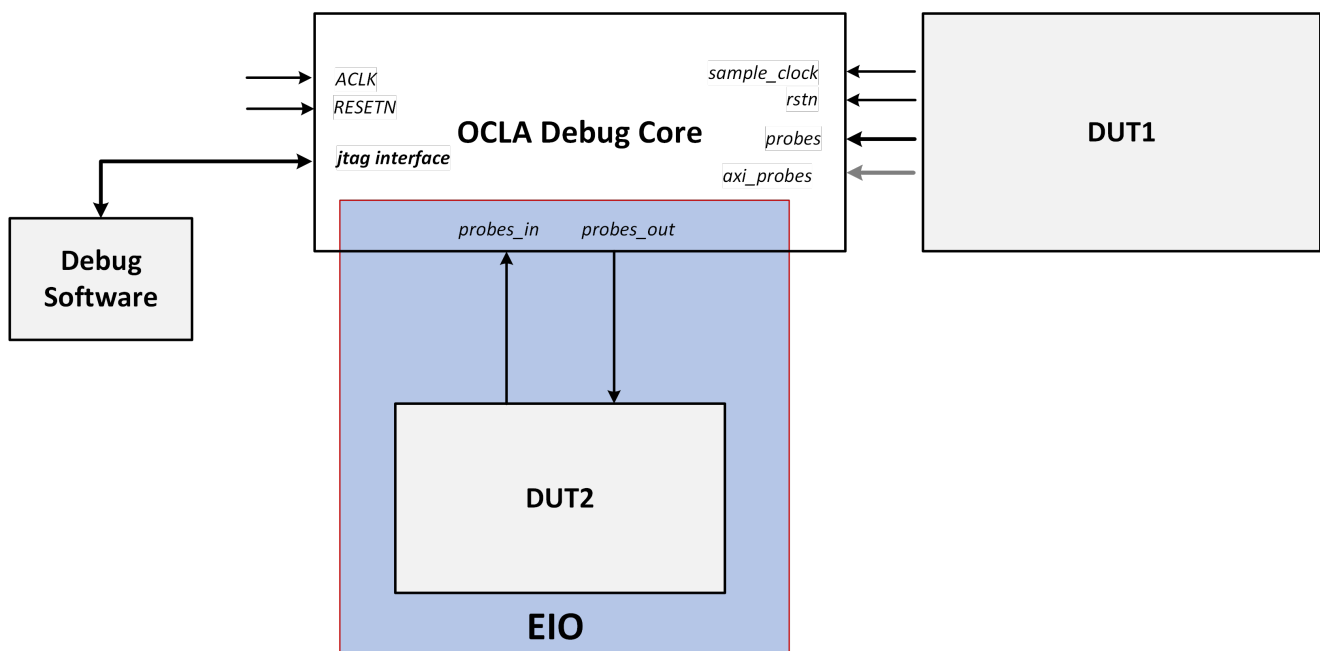


Figure 2. OCLA System Level Block Diagram

Probes

The IP supports 15 native probes, allowing users to connect signals for debugging purposes. The size of each native probe can be configured within the range of 1 to 1025. In addition to the native probes, the IP also supports AXI probes. If the IP is configured in AXI Lite or AXI Full mode, users will have access to AXI probes. These AXI probes enable users to connect to the AXI bus for debugging purposes, providing a convenient way to debug AXI bus-related issues.

EIO Capability

Using this debugging core feature, users can both monitor and actively control internal FPGA signals in real time. The number and width of the input and output ports are customizable to interface with the FPGA design. The core facilitates input and output probes, enabling the virtual driving of logic blocks and verification of their functionality.

To drive any signal within the design, the user must connect it to the probes_out port of the IP core. Similarly, to monitor any signal in real time from the Design Under Test (DUT), it needs to be connected to the probes_in port of the IP core.

MODE

The OCLA IP core can be configured in the following three modes.

- **NATIVE** In this mode the user will be allowed to set number of probes that can vary from 1 to 15. User can set the width of each probes that range from 1 to 1024. Once the IP is generated, the signals that user want to debug can be connected to these probes.
- **AXI** In this mode the user can select AXI Lite or AXI Full interface. The mode can be used if user wants to debug an AXI bus. The IP will be generated having AXI probes where user can probe their AXI bus signals that he wants to debug.
- **NATIVE_AXI** This is dual mode where user can connect custom signals as well as AXI bus. In this mode the user is allowed to select number of probes and AXI type.

Trigger

The OCLA IP core utilizes a trigger mechanism to initiate the capture of probe data samples. The trigger signal can be selected from a variety of sources, including probe input signals or axi probe signal.

OCLA also allows for the configuration of various trigger conditions on the trigger signal, such as level, edge, and value compare. The OCLA continually monitors the trigger signal, and data sampling begins when all of the trigger conditions in the active trigger pattern are satisfied.

Additionally, the OCLA features a user-configurable trigger mode setting, which determines the amount of data that should be acquired by the system prior to and following the trigger event. The acquired data is stored in a circular buffer for further analysis, which enables the system to efficiently handle large data sets and continuously update the data being captured.

OCLA supports four triggers. User can set upto 4 triggers at a time.

Trigger Conditions

Multiple options for trigger conditions are available for probe and input triggers signals. Following lists the trigger conditions:

Trigger Condition	Description
Don't Care	Default trigger condition. The channel is not used to determine the trigger event.
Low level	OCLA triggers when the probe channel is low.
High level	OCLA triggers when the probe channel is high.
Falling Edge	OCLA triggers on the falling edge the probe channel.
Rising Edge	OCLA triggers on the rising edge the probe channel.
Either Edge	OCLA triggers on either edge of the probe channel.

Value Comparison	OCLA triggers when the value of a probe channel is equal /less than / greater than some user specified value.
Boolean Trigger equations	Advance Trigger Conditions AND, OR, <, >, == etc

Table 1. Trigger Conditions

Trigger Modes

The common trigger modes are post trig, pre trig, center and countinuous.

- **Pre triggered** the stored data set will consist of data sampled after the trigger.
- **Post triggered** is the opposite and in this mode the logic analyzer stops the sampling immediately when the trigger is raised thus only storing data from before the triggering event.
- **Center triggered** is a combination putting the triggering event in the middle of the sampled data set
- **Continous trigger** mode continously samples data.

Fix number of samples

The OCLA IP core can be configured to dynamically sample a specified number of probe samples, rather than utilizing the default trace memory depth, at runtime. This allows for greater flexibility in the debugging process, as the number of probe samples can be adjusted to suit the specific requirements of runtimme debugging.

Standards

The OCLA can be configured and samples can be read via standarad JTAG interface.

IP Support Details

The table 2 presents the specifics of IP support for the OCLA IP Core, including pertinent information such as synthesis, simulation and source details.

Compliance		IP Resources					Tool Flow		
Device	Inter-face	Source Files	Con-straint File	Test-bench	Simulation Model	Software Driver	Analyze and Elaboration	Simula-tion	Synthe-sis
GEM- INI	JTAG	Systemver- ilog	SDC	-	-	-	Raptor	Third Party	Raptor

Table 2. IP Information

Resource Utilization

The table 3 presents the resources utilization of OCLA IP for the Gemini device within the Raptor Design Suite, specifically detailing the statistics of resource utilization for both the minimum and maximum configurations of the OCLA.

Configuration		Resource Utilization		
Minimum Resource	Options	Configuration	Resources	Utilized
	Number of Probe	1	LUT	263
	Trace Memory Depth	32	FLOPS	138
	Value Compare Feature	OFF	BRAM	1
	Input Triggers	0	DSP	0
Maximum Resource	Options	Configuration	Resources	Utilized
	Number of Probe	1024	LUT	1068
	Trace Memory Depth	1024	FLOPS	5466
	Value Compare Feature	ON	BRAM	29
	Input Triggers	32	DSP	0

Table 3. Resource Utilization

Ports

Table 5 lists the top interface ports of the OCLA.

Signal Name	I/O	Description
Sampling Clock and Reset		
CHs_clk	I	Clock to Sample the Probe Data. It must be same as the Design under test
RESETn	I	Reset port of OCLA and it must be same as design under test
AXI Clock and Reset		
ACLK	I	AXILite Clock
S_AXI_ARESETN	I	AXI4-Lite RESET
JTAG Interface		
JTAG_TCK	I	JTAG clock signal
JTAG_TMS	I	JTAG standard TMS
JTAG_TDI	I	JTAG standard TDI
JTAG_TDO	O	JTAG standard TDO
JTAG_TRST	I	JTAG reset signal
Emulated Input_Ouput (EIO) Ports		
eio_ip_clk	I	EIO input port clock
eio_op_clk	I	EIO output port clock
probes_in	I	EIO Input probes
probes_out	O	EIO output probes
OCLA Probes		
probes	I	OCLA Probes port in NATIVE mode
axi4_probes	I	OCLA Probes port in AXI Full mode
axiLite_probes	I	OCLA Probes port in AXI Lite mode

Table 5. OCLA Interface

Parameters

Table 5 lists the parameters of the OCLA.

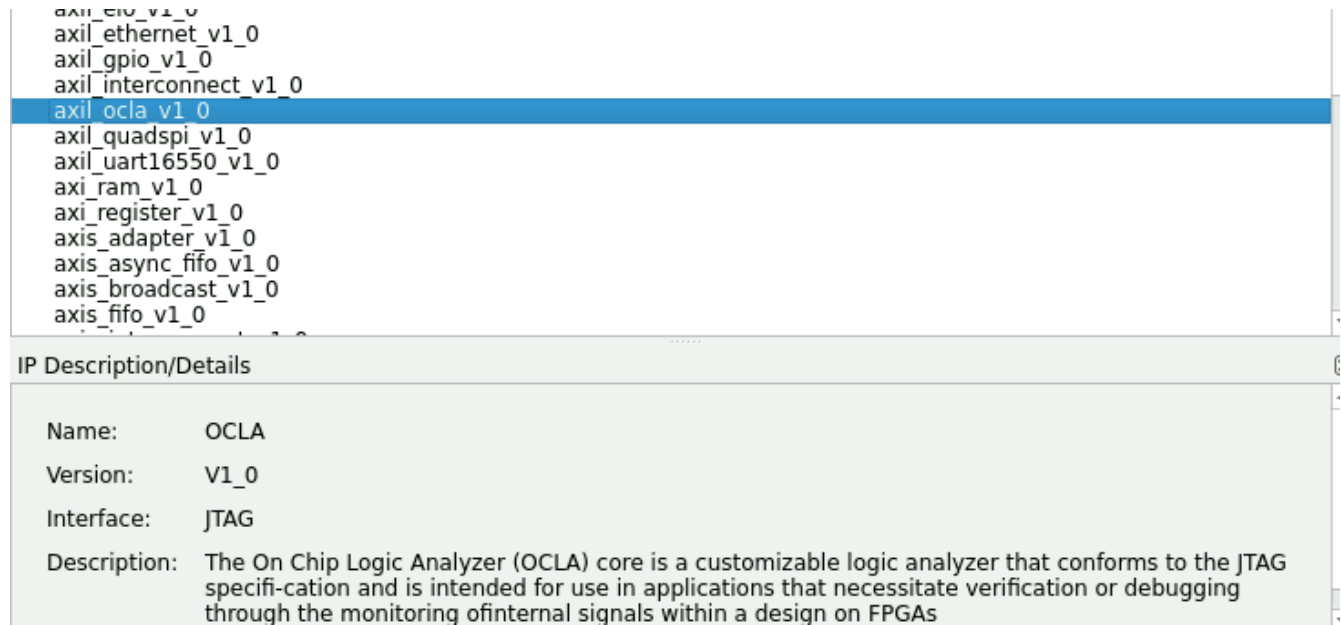
Parameters	Values	Default Value	Description
IP_TYPE	"ocla"	"ocla"	Define IP Type
IP_VERSION	32'h00000001	32'h00000001	Define IP Version.
IP_ID	Auto Generated	Auto Generated	Define IP ID which will be generated by the IP generator at run time
MODE	"NATIVE", "AXI", "NATIVE_AXI"	"NATIVE"	Define mode of OCLA
AXI_TYPE	"AXI4", "AXILite"	"AXILite"	Select AXI Type. Valid only if AXI or NATIVE_AXI mode is set
EIO_Enable	0 - 1	0	Enable EIO capability.
SAMPLING_CLK	"SINGLE", "MULTIPLE"	"SINGLE"	Set sampling clock type
NO_PROBES	1-15	1	Total Number of Probes. Valid in NATIVE and NATIVE_AXI mode only
MEM_DEPTH	32, 64, 128, 256, 512, 1024	32	Probe storage buffer depth. This number represents the maximum number of samples that can be stored at run time for each probe input.
Probe<n>_Width	1-1024	1	Define size of each probe. <n> range from 1 to 15.
INPUT_PROBE_WIDTH	1- 512	1	Input probe size for EIO IP
OUTPUT_PROBE_WIDTH	1- 512	1	Output probe size for EIO IP

Table 5. Parameters

Design Flow

IP Customization and Generation

OCLA IP core is a part of the Raptor Design Suite Software. A customized ocla can be generated from the Raptor's IP configurator window.

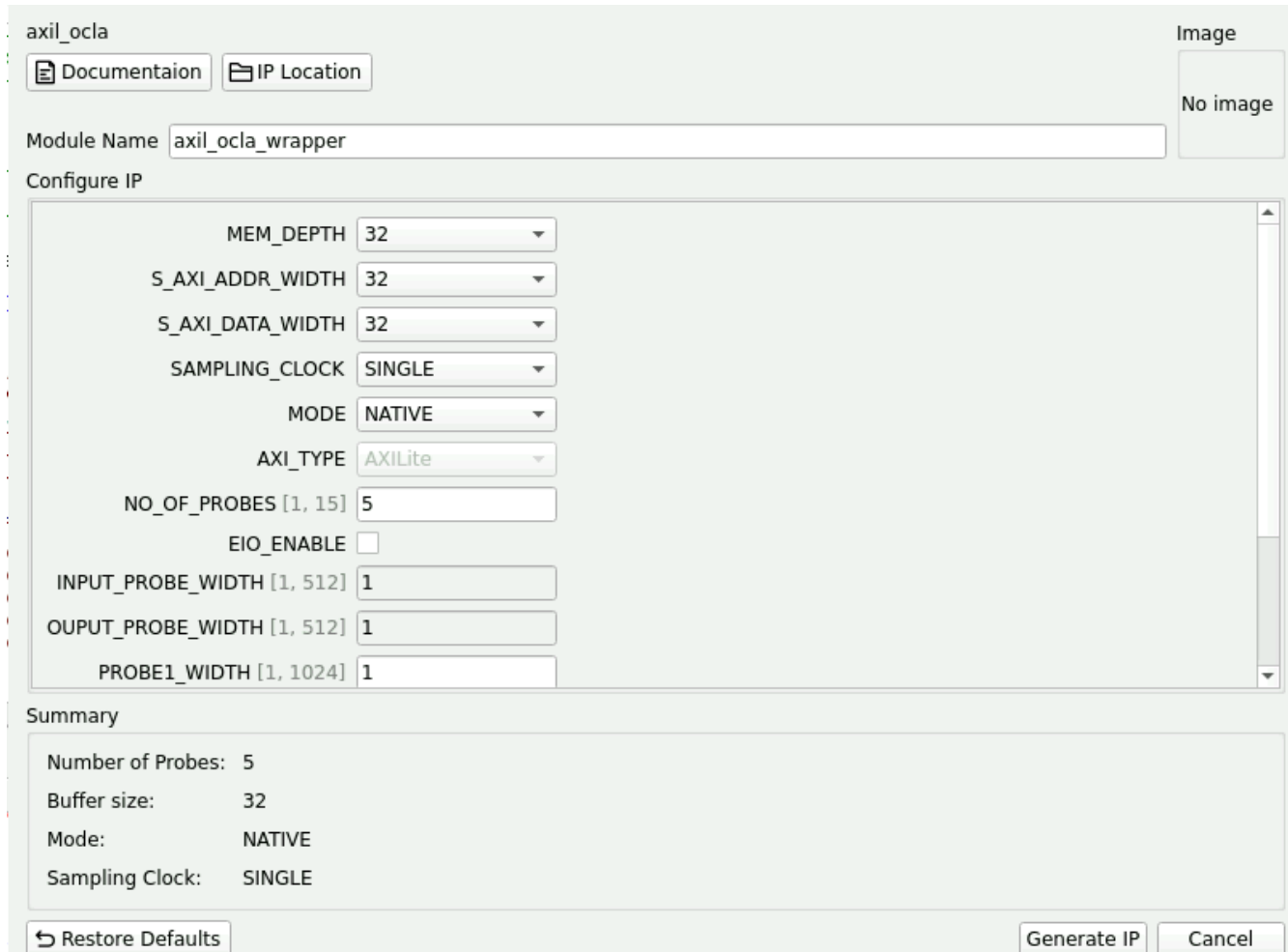


The screenshot shows the IP configurator window. The top section displays a list of IP cores, with 'axil_ocla_v1_0' selected. The bottom section, titled 'IP Description/Details', provides information about the selected OCLA core.

IP Description/Details	
Name:	OCLA
Version:	V1_0
Interface:	JTAG
Description:	The On Chip Logic Analyzer (OCLA) core is a customizable logic analyzer that conforms to the JTAG specification and is intended for use in applications that necessitate verification or debugging through the monitoring of internal signals within a design on FPGAs

Figure 3. IP list

Parameters Customization: From the IP configuration window, the parameters of the OCLA can be configured and OCLA features can be enabled for generating a customized OCLA IP core that suits the user application requirement.



The IP Configuration window for 'axil_ocla' is shown. It includes a 'Module Name' field set to 'axil_ocla_wrapper'. The 'Configure IP' section contains several parameters: MEM_DEPTH (32), S_AXI_ADDR_WIDTH (32), S_AXI_DATA_WIDTH (32), SAMPLING_CLOCK (SINGLE), MODE (NATIVE), AXI_TYPE (AXILite), NO_OF_PROBES [1, 15] (5), EIO_ENABLE (unchecked), INPUT_PROBE_WIDTH [1, 512] (1), OUTPUT_PROBE_WIDTH [1, 512] (1), and PROBE1_WIDTH [1, 1024] (1). A 'Summary' section displays: Number of Probes: 5, Buffer size: 32, Mode: NATIVE, and Sampling Clock: SINGLE. At the bottom are 'Restore Defaults', 'Generate IP', and 'Cancel' buttons. An 'Image' section on the right shows 'No image'.

Figure 4. IP Configuration

OCLA Debug Subsystem

The Generated OCLA IP Wrapper

The IP customization and generation step is followed by the availability of a top wrapper and all source files for the user. The generated top wrapper file for the OCLA comprises of two distinct clock domains, namely the sample clock and the AXI clock.

It is crucial to note that the sample clock of the OCLA should be connected to the design being monitored, while the AXI clock should be connected to the main clock if clocks are different.

The signals of the design that are intended to be sampled are connected to the probes port of the OCLA. If the OCLA is configured in AXI mode then axi ports will be available at the top wrapper of the IP core where user can connect their AXI bus that he wants to debug.

For configuring the OCLA and reading the sampled data from the system, the JTAG interface must be connected to an GPIO through which IP will communicate with the software.

OCLA Debug Subsystem

The OCLA IP core, a component used for debugging purposes, can be instantiated within a subsystem. The debug subsystem, as depicted in Figure 5, integrates the OLCA IP core within the design being monitored. The purpose of this integration is to allow for the runtime configurations of OCLA configurations through the use of the JTAG interface.

This interface serves as the primary means of controlling and configuring the OCLA IP core within the subsystem, enabling the debugging process to proceed efficiently.

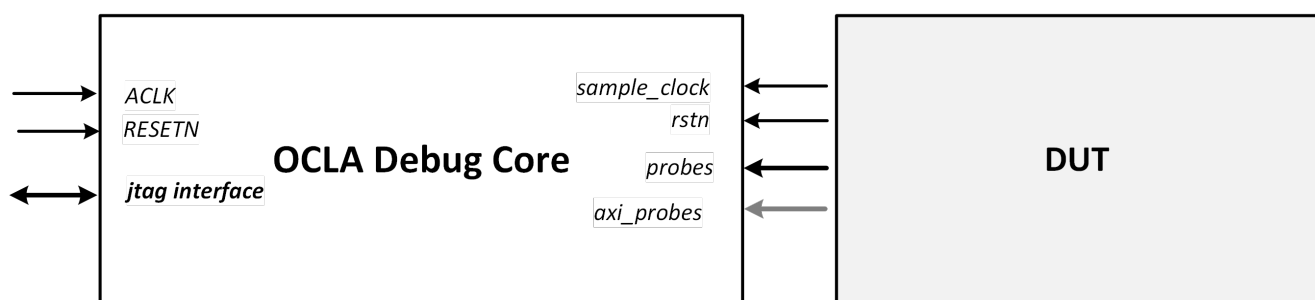


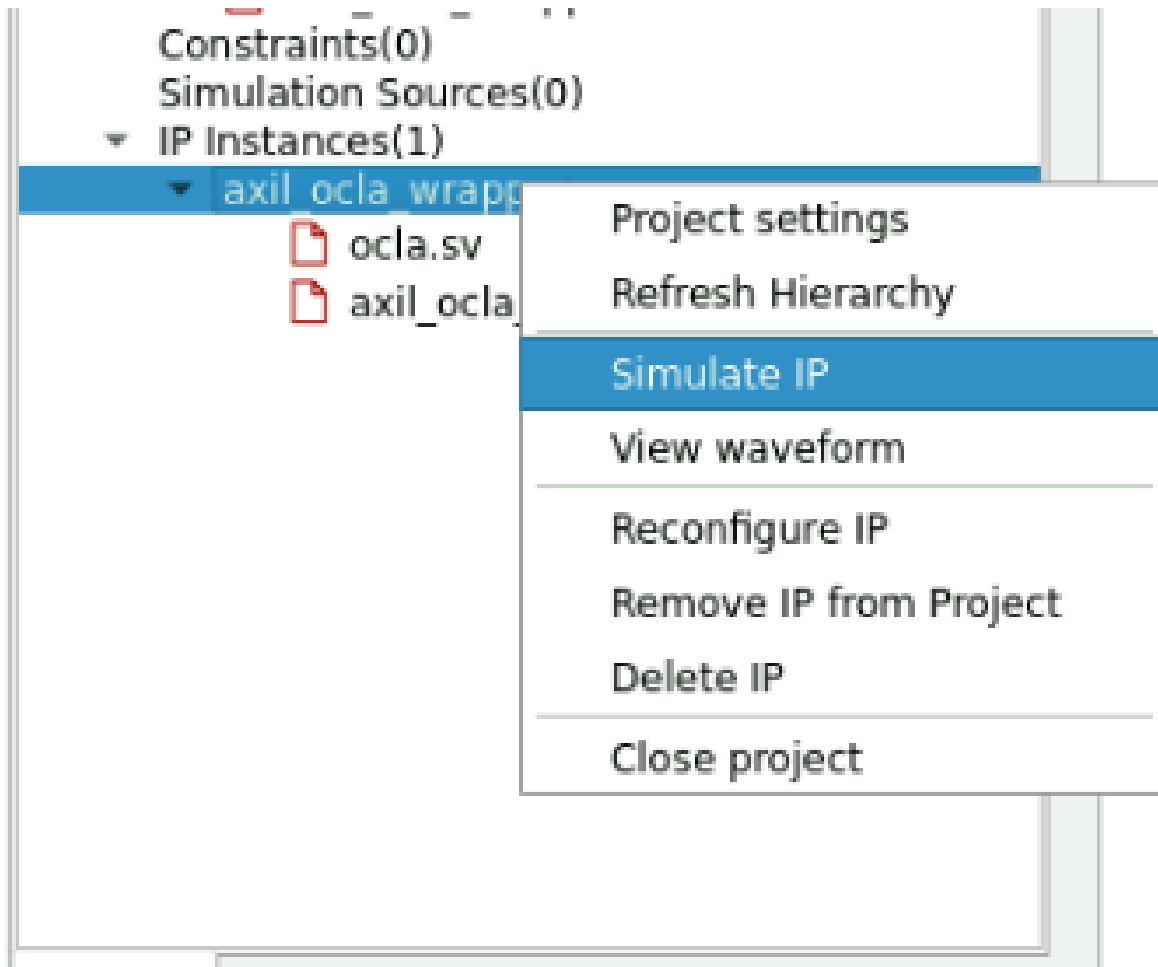
Figure 5. OCLA Debug Subsystem

Test Bench

To check the behavior of the IP Core, a verilog test-bench with basics configuration is available for simulation. Once the IP is generated then test-bench file can be found in the IP directory under sim folder.

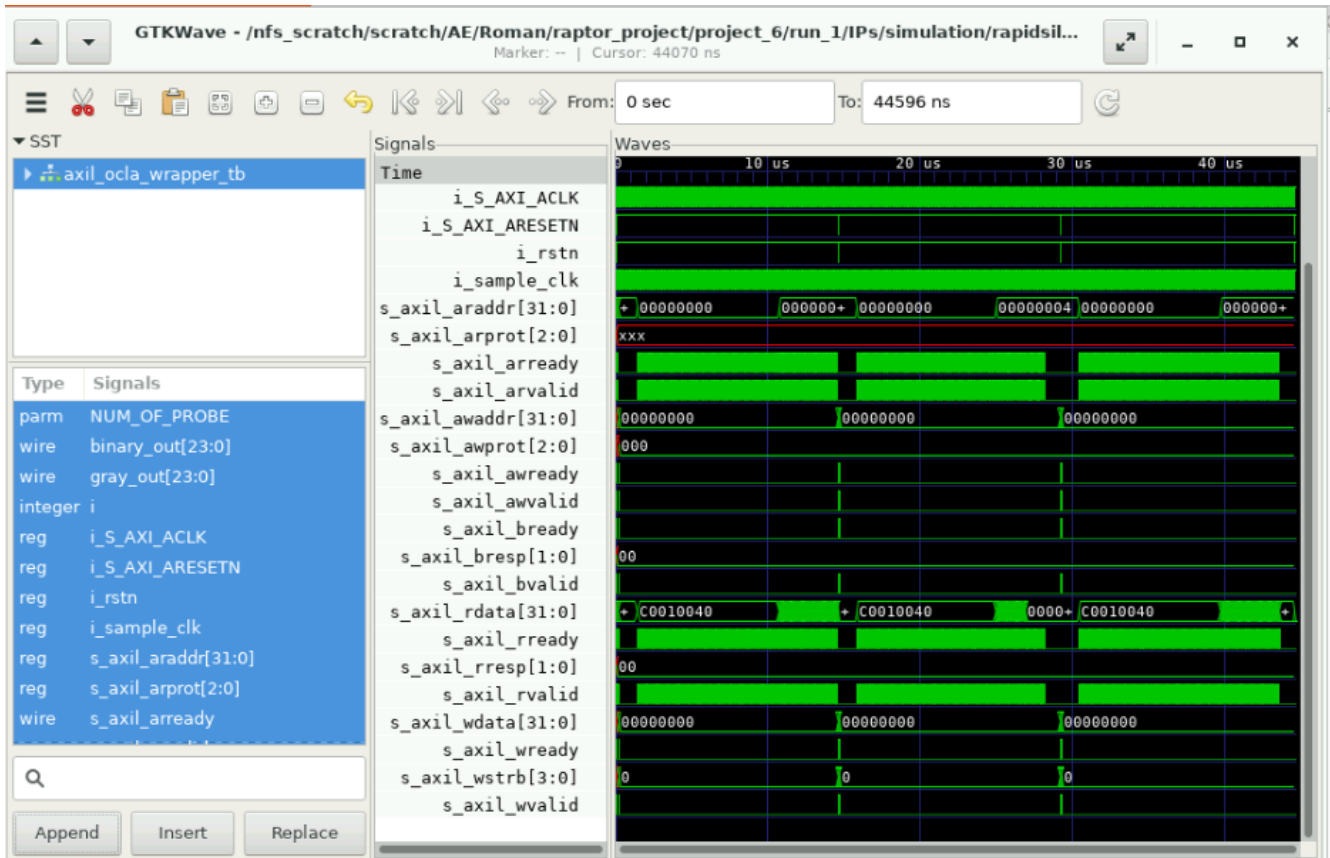
Running Simulation

1. Right click on the IP name within source tab and select Simulate IP as shown in figure below.



Running Simulation

- 2.This will run the simulation and result will dumped into vcd file.To see the waveform, again right click on the IP and select View waveform. The GTKWave will open showing the IP simulation result as shown in figure below.



Simulation Result

References

A comprehensive guide explaining how to use OCLA to debug a design can be found [here](https://www.rapidsilicon.com).

Revision History

Date	Version	Revisions
January 31, 2024	0.01	Initial version OCLA User Guide Document