AXI Lite Interconnect (Beta Release)

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Contents

IP Summary

Introduction

The AXI Lite Interconnect IP core is a module which enables communication between different AXI Lite master and slave devices in a system-on-chip (SoC) design. AXI Lite is a simplified version of the full AXI (Advanced eXtensible Interface) protocol, with a reduced number of signals and a more limited feature set, which makes it suitable for low-complexity, low-bandwidth applications. The AXI Lite Interconnect IP core acts as a central hub for the AXI Lite bus, providing connectivity and arbitration for AXI Lite master devices and AXI Lite slave devices. It supports multi-master and multi-slave configurations, allowing multiple devices to access the same memory or peripheral resources in the system.

Features

- Low latency and high bandwidth communication: AXI Lite Interconnect IP core allows multiple AXI Lite masters to communicate with multiple AXI Lite slaves through a high-bandwidth and low-latency interconnect.
- Support for multiple masters and slaves: The IP core can connect up to 16 AXI Lite masters and 16 AXI Lite slaves. This allows for a highly configurable system-on-chip design.
- Low resource utilization: The AXI Lite Interconnect IP core has low resource utilization, making it suitable for use in resource-constrained designs.
- Configurability: AXI Lite interconnect is highly configurable, allowing designers to optimize the interconnect for their specific SoC design.
- Data Width: 32, 64 bits
- Address Width: 32, 64, 128, 256 bits

Overview

AXI Lite Interconnect

The AXI Lite Interconnect IP Core is a component of the Raptor Design Suite that provides a simple, low-latency interconnect between multiple AXI Lite master and slave peripherals. The AXI Lite protocol is a simplified version of the full AXI protocol, which is used in more complex systems. The AXI Lite Interconnect IP Core provides a way to connect multiple AXI Lite interfaces together without the need for a full AXI protocol implementation. It is often used in small embedded systems, where a limited number of peripherals need to be connected together. It is designed to be lightweight and efficient, with minimal overhead and low latency. It can be used with a variety of AXI Lite-compatible peripherals, including memory controllers, UARTs, SPI controllers, and GPIO controllers.

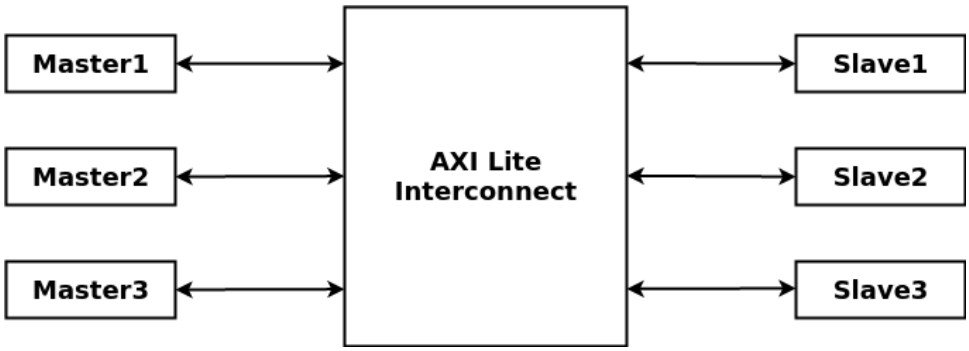

Figure 1: AXI Lite Interconnect Block Diagram

IP Specification

The AXI Lite Interconnect IP is a configurable and scalable IP block that provides connectivity between AXI Lite slave devices and AXI memory-mapped master devices. It supports the AXI4-Lite protocol, which is a simplified version of the AXI4 protocol. The AXI4-Lite protocol provides a simple, low-latency, and low-complexity interface for peripheral devices. It supports up to 16 AXI4-Lite slave devices and up to 16 AXI4-Lite master devices. It is highly configurable, allowing users to customize various parameters such as the number of ports. The figure 2 shows the top level diagram of AXI Lite Interconnect.

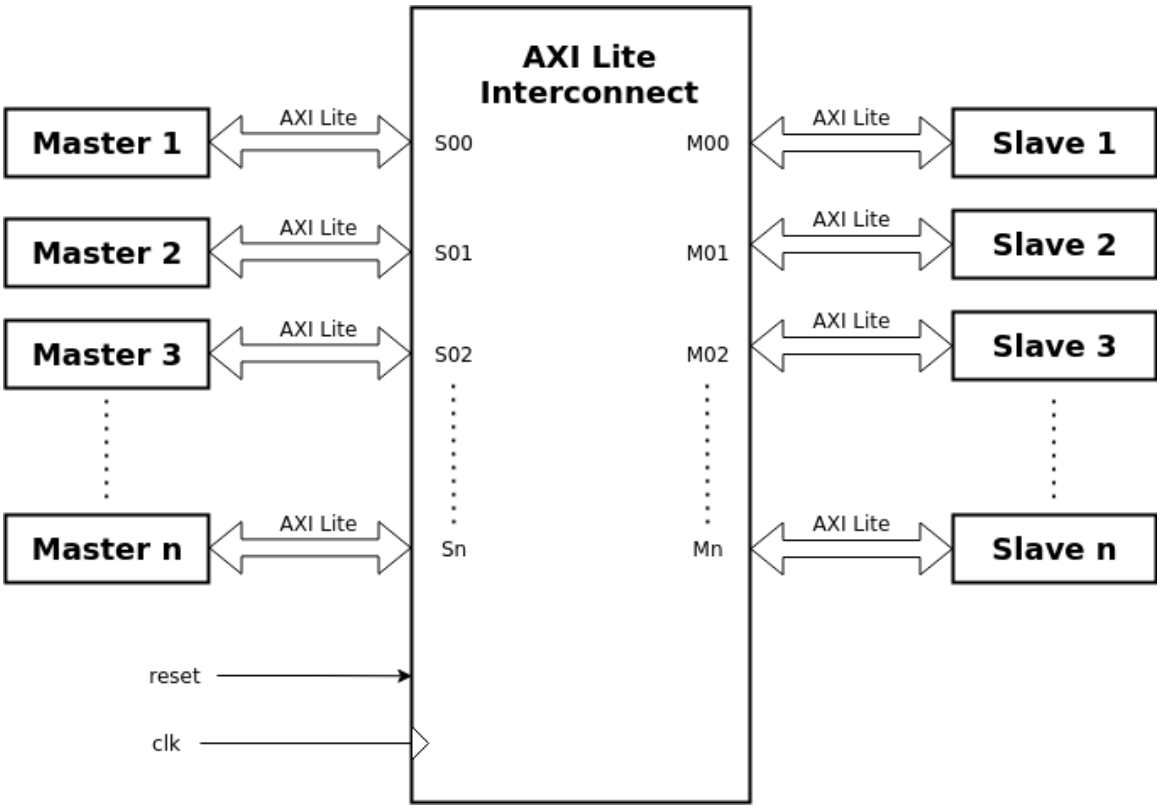

Figure 2: Top Module

Standards

The AXI Lite Master and Slave interfaces are compliant with the AMBA® AXI Protocol Specification.

IP Support Details

The Table 1 gives the support details for AXI Lite Interconnect.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI-Lite	Verilog	-	Cocotb	-	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2, remaining parameters have been kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
	Configuration		**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	S_COUNT	1	BRAMS	3
	M_COUNT	1	REGISTERS	91
	DATA_WIDTH	32	LUTS	104
	ADDR_WIDTH	32	-	-
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	S_COUNT	16	BRAMS	3
	M_COUNT	16	REGISTERS	570
	DATA_WIDTH	64	LUTS	4569
	ADDR_WIDTH	256	-	-

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the AXI Lite Interconnect.

Signal Name	I/O	Description
clk	I	Clock Signal for Interconnect
rst	I	Active Low Reset Signal
Slave Write Address Channel		
s<x>_axi_awaddr	I	Write address
s<x>_axi_awprot	I	Protection type
s<x>_axi_awvalid	I	Write address valid
s<x>_axi_awready	O	Write address ready
Slave Write Data Channel		
s<x>_axi_wdata	I	Write data
s<x>_axi_wstrb	I	Write strobe
s<x>_axi_wvalid	I	Write valid
s<x>_axi_wready	O	Write ready
Slave Write Response Channel		
s<x>_axi_bresp	O	Write response
s<x>_axi_bvalid	O	Write response valid
s<x>_axi_bready	I	Write response ready
Slave Read Address Channel		
s<x>_axi_araddr	I	Read address
s<x>_axi_arprot	I	Protection type
s<x>_axi_arvalid	I	Read address valid
s<x>_axi_arready	O	Read address ready
Slave Read Data Channel		
s<x>_axi_rdata	O	Read data
s<x>_axi_rresp	O	Read response
s<x>_axi_rvalid	O	Read valid
s<x>_axi_rready	I	Read ready
Master Write Address Channel		
m<x>_axi_awaddr	O	Write address
m<x>_axi_awprot	O	Protection type
m<x>_axi_awvalid	O	Write address valid
m<x>_axi_awready	I	Write address ready
Master Write Data Channel		
m<x>_axi_wdata	O	Write data
m<x>_axi_wstrb	O	Write strobe
m<x>_axi_wvalid	O	Write valid
m<x>_axi_wready	I	Write ready
Master Write Response Channel		
m<x>_axi_bresp	I	Write response
m<x>_axi_bvalid	I	Write response valid

Signal Name	I/O	Description
m<x>_axi_bready	O	Write response ready
Master Read Address Channel		
m<x>_axi_araddr	O	Read address
m<x>_axi_arprot	O	Protection type
m<x>_axi_arvalid	O	Read address valid
m<x>_axi_arready	I	Read address ready
Master Read Data Channel		
m<x>_axi_rdata	I	Read data
m<x>_axi_rresp	I	Read response
m<x>_axi_rvalid	I	Read valid
m<x>_axi_rready	O	Read ready

Table 3: Port List

Parameters

Table 4 lists the parameters of the AXI Lite Interconnect.

Parameter	Values	Default Value	Description
S_COUNT	1-16	4	No. of Slave Interfaces
M_COUNT	1-16	4	No. of Master Interfaces
DATA_WIDTH	32, 64	32	Data Width of Interconnect
ADDR_WIDTH	32, 64, 128, 256	32	Address Width of Interconnect

Table 4: Parameters

Design Flow

IP Customization and Generation

AXI Lite Interconnect IP core is a part of the Raptor Design Suite Software. A customized interconnect can be generated from the Raptor's IP configuration window as shown in figure 3.

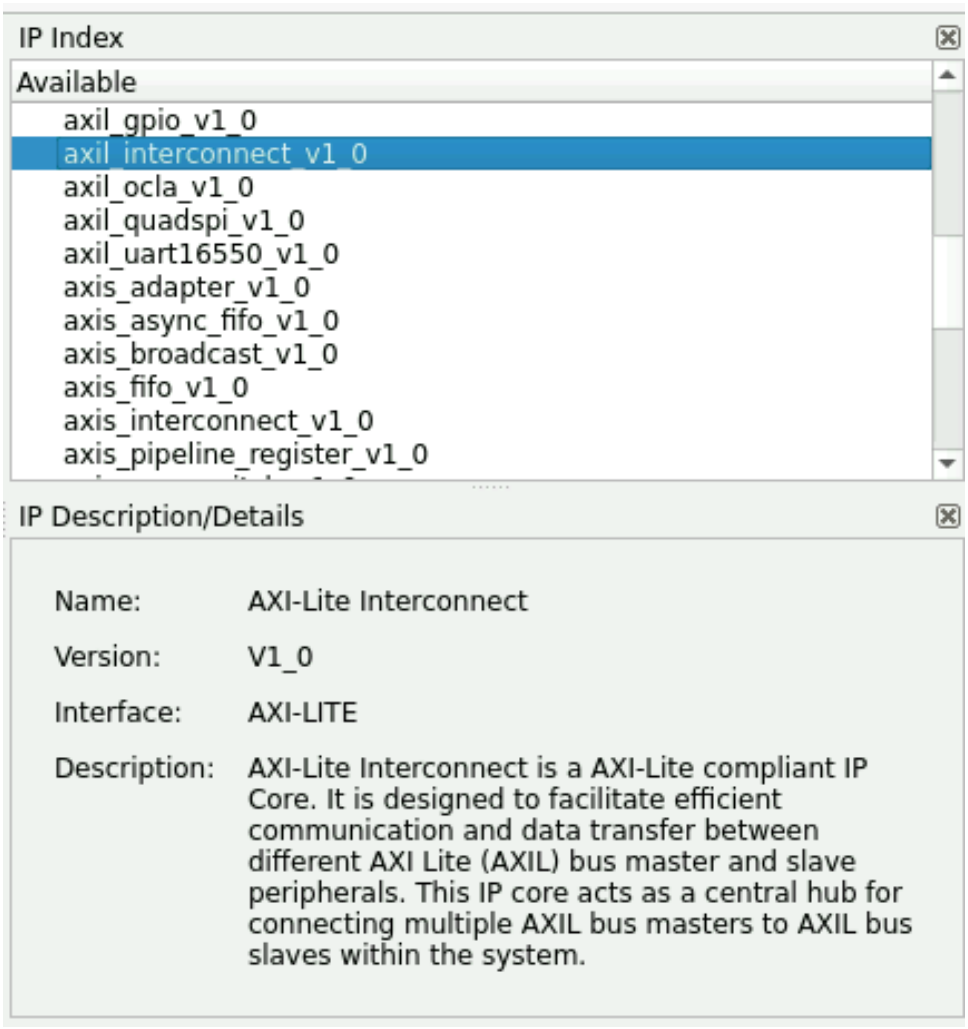

Figure 3: IP List

Parameters Customization

From the IP configuration window, the parameters of the AXI Lite Interconnect can be configured and it's features can be enabled for generating a customized IP core that suits the user application requirements. All parameters are shown in Figure 4. In Figure 4, the module name specifies the name of both the Verilog file and the top-level IP name that will be generated based on above configured parameters. The Output Dir is a directory option that allows the user to specify where they want the generated IP to be saved.

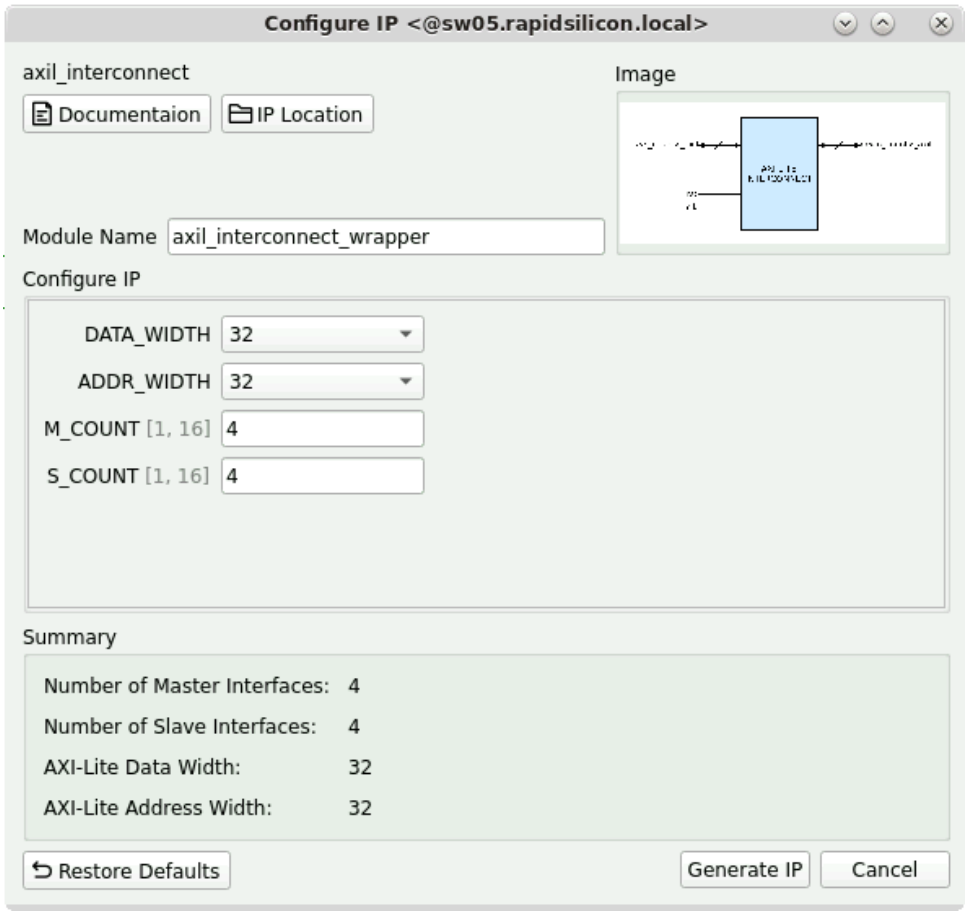

Figure 4: IP Configuration

Test Bench

The AXI Lite interconnect IP Core is provided with a testbench which is based upon Coco tb verification environment. For simulation, right click on generated IP Instance and then click "Simulate IP" as shown in Figure 5.

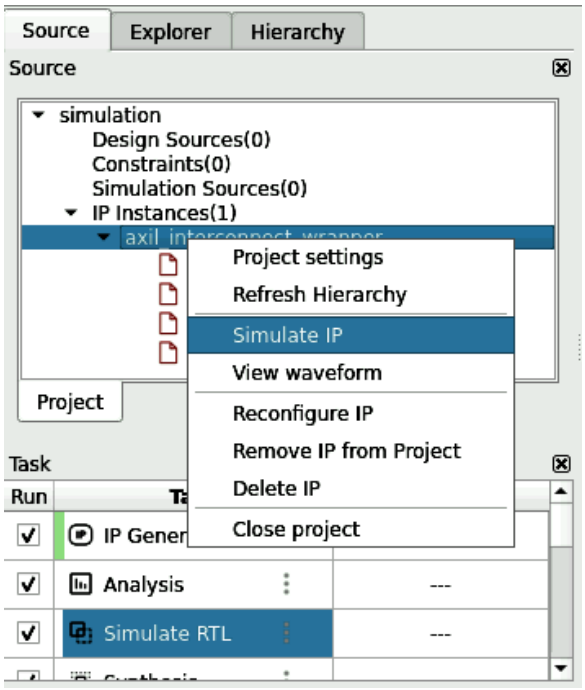

Figure 5: Simulate IP

In this test, four masters ad four slaves are connected to interconnect. Interconnect assigns address space to each slave. Each master communicate with each slave. The input data is generated using a test data generator module. Input data is routed from master to slave through interconnect. After running the simulation, you'll get pass/ fail status on console. The status of test is shown in Figure 6.

```
** test_axil_interconnect.run_test_write_009    PASS        5140.00          0.57       8989.05  **
** test_axil_interconnect.run_test_write_010    PASS        5140.00          0.57       8962.88  **
** test_axil_interconnect.run_test_write_011    PASS        5140.00          0.55       9298.45  **
** test_axil_interconnect.run_test_write_012    PASS        5140.00          0.57       8990.32  **
** test_axil_interconnect.run_test_write_013    PASS        7090.00          0.85       8323.00  **
** test_axil_interconnect.run_test_write_014    PASS        7090.00          0.84       8421.18  **
** test_axil_interconnect.run_test_write_015    PASS        7090.00          0.85       8386.09  **
** test_axil_interconnect.run_test_write_016    PASS        7090.00          0.85       8390.35  **
** test_axil_interconnect.run_test_read_001     PASS        4070.00          0.43       9402.16  **
** test_axil_interconnect.run_test_read_002     PASS        4070.00          0.40      10062.10  **
** test_axil_interconnect.run_test_read_003     PASS        4070.00          0.42       9585.29  **
** test_axil_interconnect.run_test_read_004     PASS        4070.00          0.40      10118.14  **
** test_axil_interconnect.run_test_read_005     PASS        5130.00          0.57       8922.04  **
** test_axil_interconnect.run_test_read_006     PASS        5130.00          0.58       8896.55  **
** test_axil_interconnect.run_test_read_007     PASS        5130.00          0.55       9279.00  **
** test_axil_interconnect.run_test_read_008     PASS        5130.00          0.57       8949.83  **
** test_axil_interconnect.run_test_read_009     PASS        5140.00          0.58       8884.73  **
** test_axil_interconnect.run_test_read_010     PASS        5140.00          0.57       8989.29  **
** test_axil_interconnect.run_test_read_011     PASS        5140.00          0.55       9312.99  **
** test_axil_interconnect.run_test_read_012     PASS        5140.00          0.57       8992.07  **
** test_axil_interconnect.run_test_read_013     PASS        7090.00          0.84       8428.27  **
** test_axil_interconnect.run_test_read_014     PASS        7090.00          0.84       8437.13  **
** test_axil_interconnect.run_test_read_015     PASS        7090.00          0.84       8404.02  **
** test_axil_interconnect.run_test_read_016     PASS        7090.00          0.84       8411.95  **
** test_axil_interconnect.run_stress_test_001   PASS      188960.00         17.45      10826.36  **
*************************************************************************************************
** TESTS=33 PASS=33 FAIL=0 SKIP=0                        360390.03         38.05       9472.13  **
*************************************************************************************************
```

Figure 6: Simulation Results

You can view waveform of the results. To view waveform, right click on generated IP Instance and then click "View waveform" as shown in Figure 7.

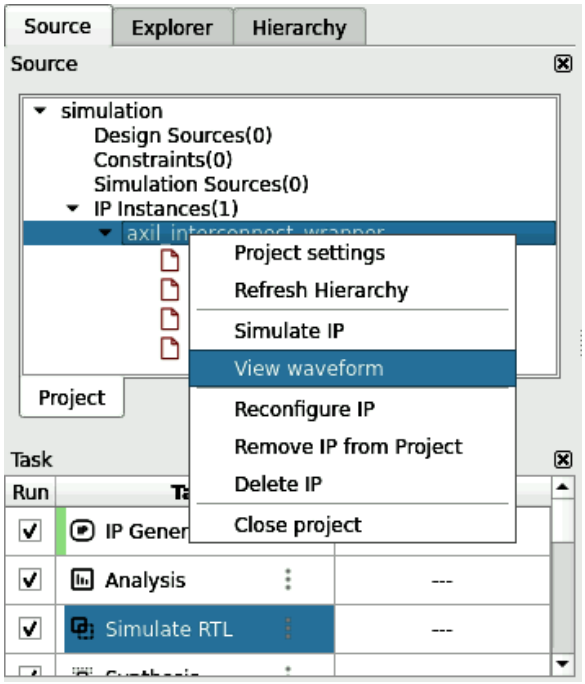

Figure 7: View Waveform

Revision History

Date	Version	Revisions
November 20, 2023	0.1	Initial version AXI Lite Interconnect User Guide