

# Boot Clock IP V1.0

---

*IP User Guide(Beta Release)*



November 29, 2023

# Contents

Licensing .....	3
<b>IP Specification</b>	<b>4</b>
<b>Overview</b>	<b>4</b>
Boot Clock IP .....	4
IP Support Details .....	5
Resource Utilization .....	5
Port List .....	6
Parameters .....	6
<b>Design Flow</b>	<b>7</b>
IP Customization and Generation .....	7
Synthesis and PnR .....	8
<b>Test Bench</b>	<b>9</b>
<b>Release</b>	<b>10</b>
Revision History .....	10



## **Licensing**

**COPYRIGHT TEXT:**

---

Copyright (c) 2022 RapidSilicon

Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions: The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software.

THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE.

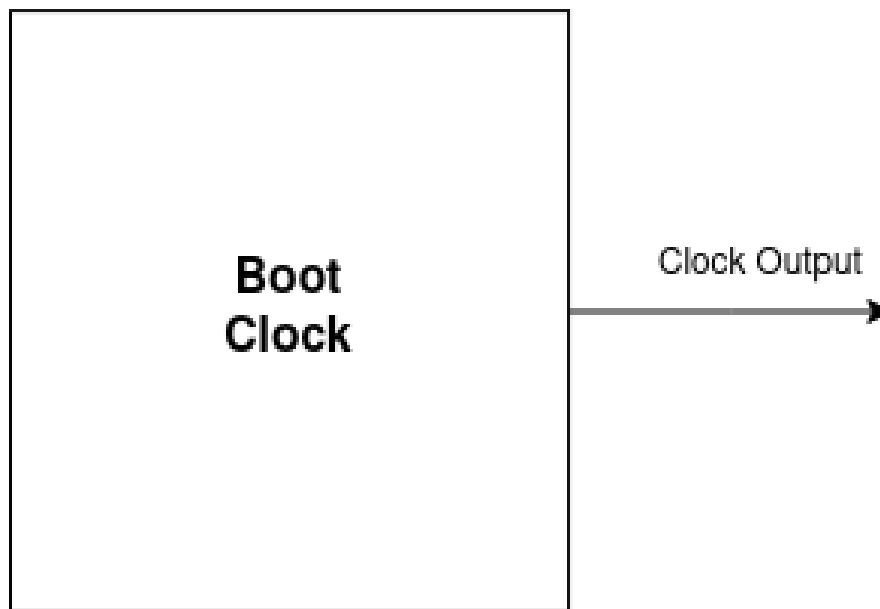
---

# IP Specification

## Overview

### Boot Clock IP

Boot Clock is added as an oscillator IP in IP Catalog. This IP module is designed to generate an initial clock signal upon system power-up or reset, contributing to the proper configuration and activation of essential components within the device. The oscillator functionality embedded in the boot clock IP ensures the delivery of a precise and consistent clock signal, allowing for the orderly execution of boot code, initialization routines, and subsequent system operations.



**Figure 1.** Boot Clock IP Block

### Features:

- Generates parameterizable frequency generation for peripherals and interconnects

## IP Support Details

Compliance		IP Resources					Tool Flow		
Device	Interface	Source Files	Constraint File	Testbench	Simulation Model	Software Driver	Analyze and Elaboration	Simulation	Synthesis
GEMINI	AXI4-lite	Verilog	-	<verilog	-	-	Raptor	Raptor	Raptor

## Resource Utilization

Please note that the utilization and timing figures provided in this section for the Processor Boot clock IP core should be considered as estimates, as they are based on its usage in conjunction with other design modules in the FPGA. Once integrated with other designs in the system, the FPGA resource utilization and core timing may differ from the reported results.

## Ports

Table 2 lists the top interface ports of the Boot Clock Core.

Signal Name	I/O	Description
O	O	Output clock generated

Boot Clock Interface

## Parameters

Table 3 lists the parameters of the Boot Clock Core.

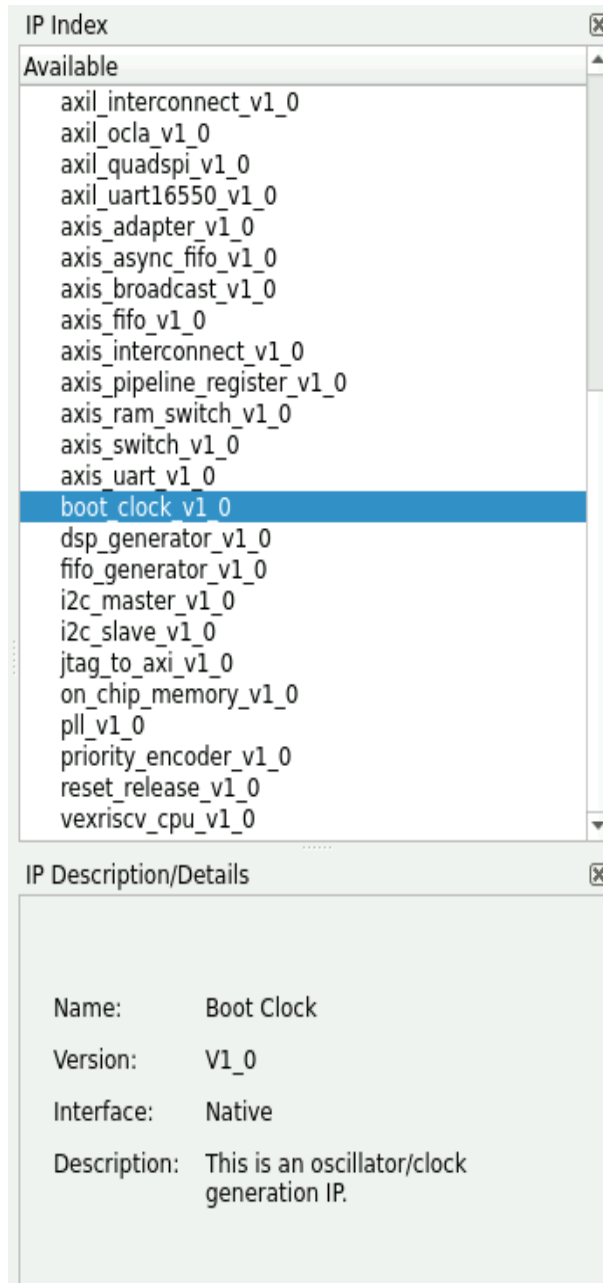
Parameter	Values	Default Value	Description
Period	25	25	Period of clock.

Parameters

# Design Flow

## IP Customization and Generation

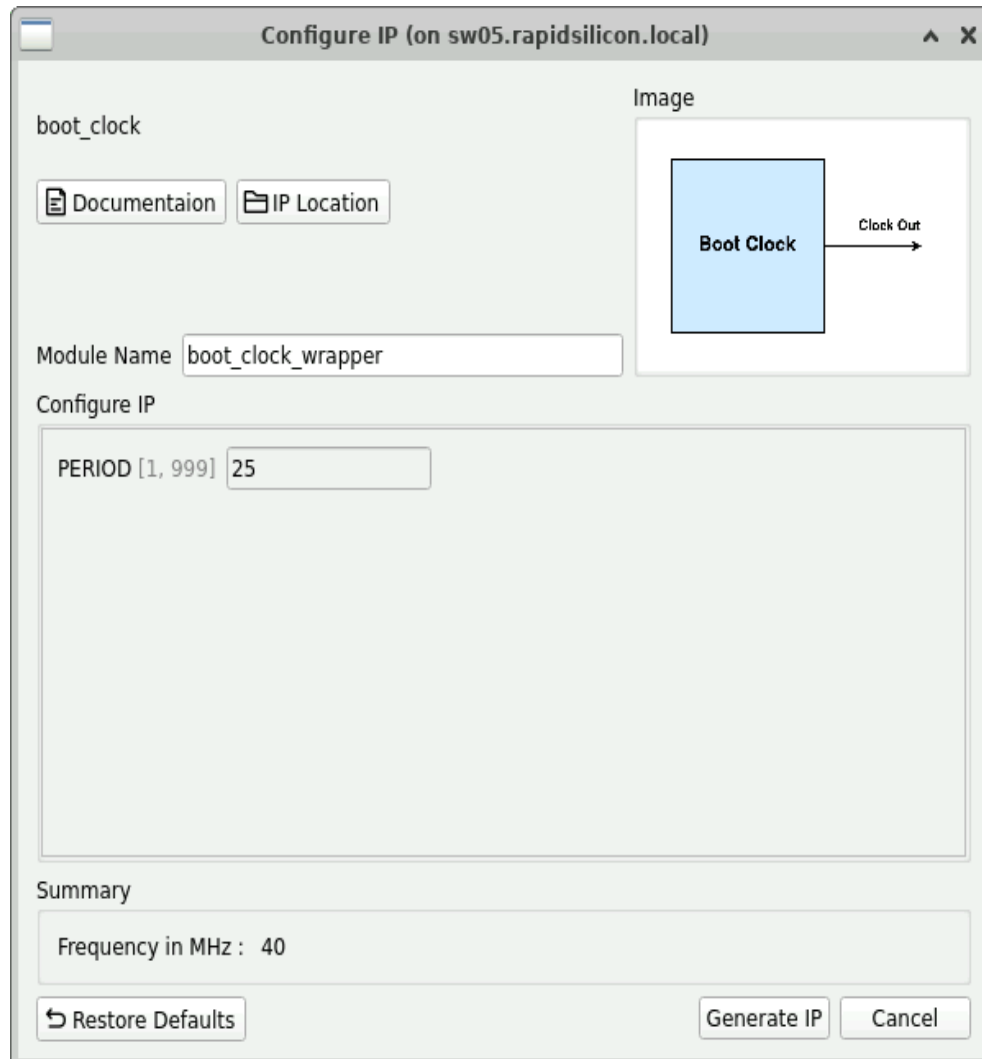
Boot Clock IP core is a part of the Raptor Design Suite Software. A customized Boot Clock can be generated from the Raptor's IP configurator window.



IP list



**Parameters Customization:** From the IP configuration window, the parameters of the Boot Clock IP can be configured and Boot Clock IP features can be enabled for generating a customized Boot Clock IP core that suits the user application requirement.



IP Configuration

## Synthesis and PnR

Raptor Suite is armed with tools for Synthesis along with Post and Route capabilities and the generated post-synthesis and post-route and place netlists can be viewed and analyzed from within the Raptor. The generated bitstream can then be uploaded on an FPGA device to be utilized in hardware application.

# Test Bench

Simulation currently not supported in Raptor.

# Revision History

+

Date	Version	Revisions
November 29, 2023	0.01	Initial version Boot Clock IP User Guide