On Chip Memory Generator (Beta Release)

Version 0.1

February 12, 2024

Copyright

Trademarks

Disclaimers

Contents

IP Summary

Introduction

The On Chip Memory IP Core is a pre-designed and pre-verified memory block that can be easily integrated into FPGA and ASIC designs. It is based on the Block Random Access Memory (BRAM) technology and provides a large amount of memory resources for storing data that is frequently accessed or changed. On Chip Memory IP Core is customizable in terms of data width and depth, allowing designers to choose the best option for their specific design requirements.

Features

- On Chip Memory can be configured as Single Port RAM, Simple Dual Port RAM or True Dual Port RAM.
- Support to have multiple read and write ports, allowing multiple operations to occur simultaneously.
- Support configurable width and depth at design time, allowing for flexibility in memory size.
- Support symmetric and asymmetric read/write widths.
- Support independent clocking on each Port.
- Support to access 1 to 128 bit wide memory in symmetric mode and 9, 18, 36, 72, 144, 288 and 576 bit wide memory in asymmetric mode.
- Support depths from 2 to 32768 in symmetric mode and 1024, 2048, 4096, 8192, 16384 and 32768 in asymmetric mode.
- Support mapping feature on Block RAM or Distributed RAM (LUTs).

Overview

On Chip Memory Generator

On Chip Memory Generator is an IP Core that can generate the RTL (register-transfer level) code for on-chip memory components. This generator can be used to create custom memory components with specific parameters, such as size, bit-width, and number of ports, without the need for manual RTL coding. The Figure 1 shows the block diagram of On Chip Memory Generator.

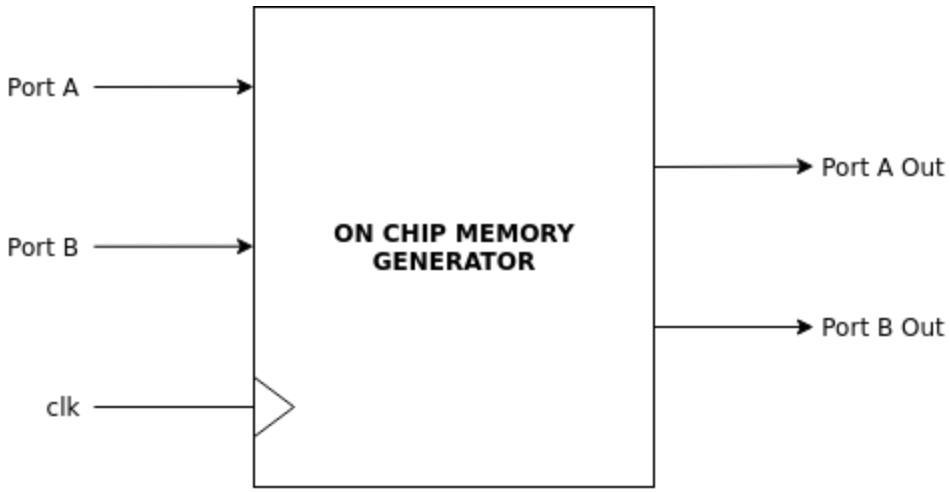

Figure 1: OCM Generator Block Diagram

IP Specification

On-Chip Memory Generator supports data widths from 1 to 128 in symmetric mode and 9, 18, 36, 72, 144, 288 and 576 bits in asymmetric, and write depth from 2 to 32768 in symmetric and 1024, 2048, 4096, 8192, 16384 and 32768 in asymmetric mode provides a flexible and scalable memory solution. The IP core supports separate clocks for two ports, allowing for independent control of each port's read and write operations. It also offers three different memory types: Single Port, Simple Dual Port, and True Dual Port. Single Port provides access to the memory through a single clock and data port, Simple Dual Port provides basic two-port functionality with independent clock, and True Dual Port provides two independent ports with separate clocks for maximum flexibility and performance. This IP core is a versatile and high-performance solution for embedded systems and integrated circuits with memory requirements. The Figure 2 shows the top level diagram of On Chip Memory.

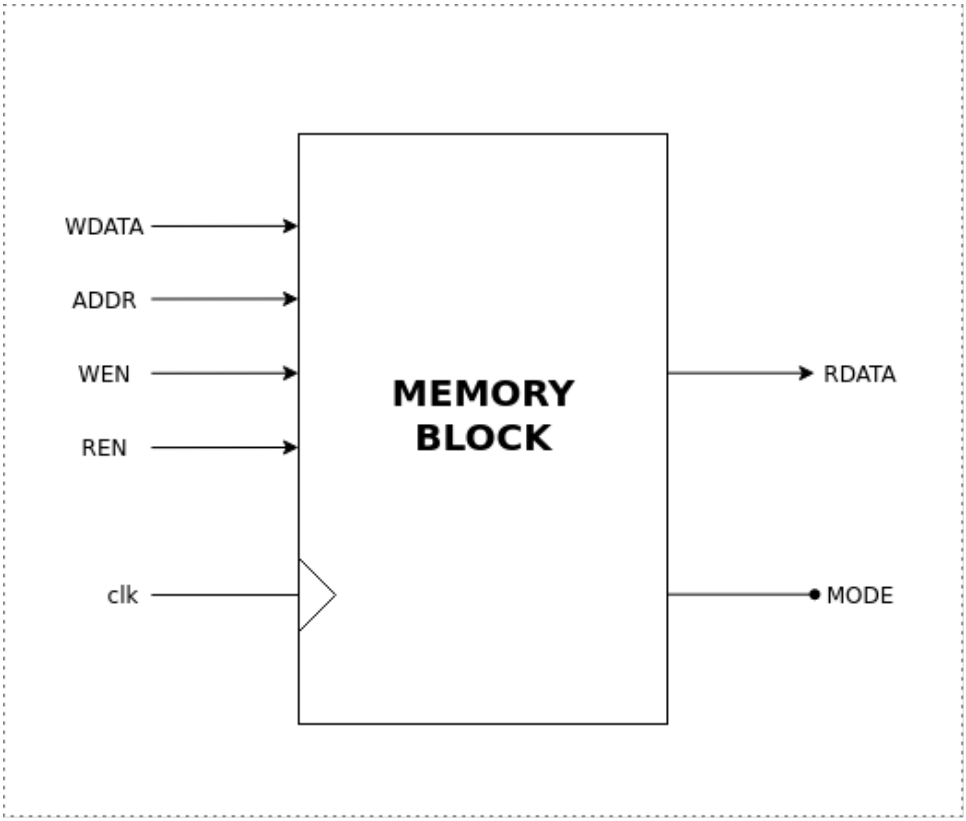

Figure 2: Top Module

Memory Types

Three types of memories are supported by On Chip Memory Generator. These are:

- **Single Port RAM:**
  A Single-Port RAM is a type of Random Access Memory that has only one port for reading and writing data. It allows only one operation (read or write) at a time, thus making it less flexible compared to a dual-port RAM which has two ports allowing for both read and write operations to occur simultaneously. Single-port RAM is commonly used in applications where cost and/or chip area are a concern, as they are simpler to implement and consume less resources compared to a dual-port RAM. It is shown in Figure 3.

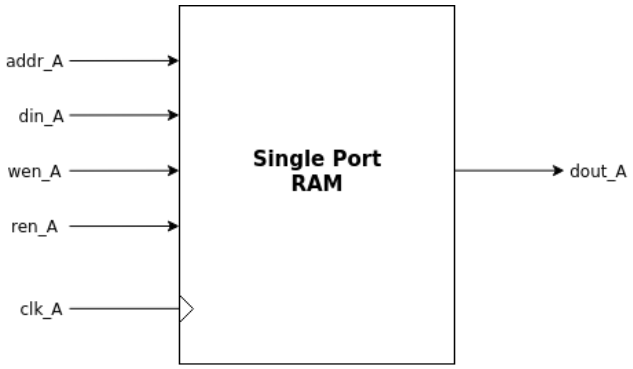

Figure 3: Single Port RAM

- **Simple Dual Port RAM:**
  A Simple Dual-Port RAM is a type of Random Access Memory that has two independent ports, allowing for simultaneous read and write operations. This makes it more flexible compared to a single-port RAM, as it can handle multiple access requests at the same time. It is commonly used in applications where multiple processors or systems need to access shared memory simultaneously. It is shown in Figure 4.

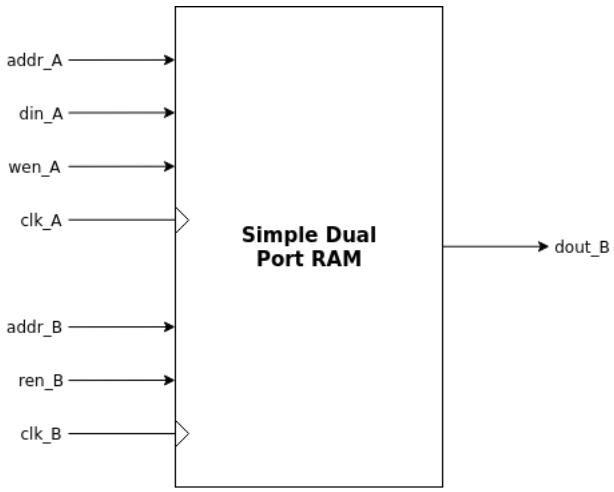

Figure 4: Simple Dual Port RAM

- **True Dual Port RAM:**
  A True Dual-Port RAM is a type of Random Access Memory that has two completely

independent ports, allowing for truly simultaneous and non-interfering read and write operations. Unlike a simple dual-port RAM, which may share certain elements such as data buses or address decoders, a true dual-port RAM has completely separate components for each port, allowing for truly independent and parallel access to the memory. True dual-port RAMs are commonly used in applications where the highest level of parallelism is required, such as in high-speed communication systems, real-time video processing, and other high-performance applications. It is shown in Figure 5.

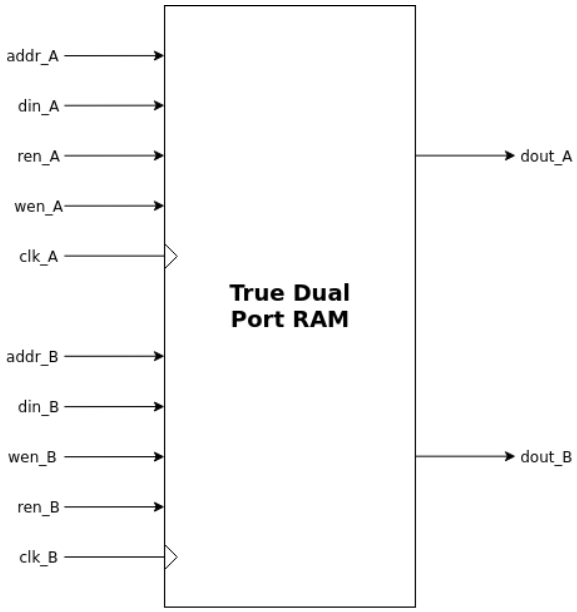

Figure 5: True Dual Port RAM

Common Clock Versus Uncommon Clock

A common clock refers to a clock signal that is shared among all the memory blocks in the device. In contrast, an uncommon clock refers to a clock signal that is unique to each memory block.

- The use of a common clock in memory blocks has several advantages. First, it simplifies the design and implementation of the memory blocks as there is only one clock signal to manage. Second, it ensures that all the memory blocks are synchronized, which is critical for high-speed data transfer and avoiding errors. However, the disadvantage of using a common clock is that it may limit the flexibility of the design, as all the memory blocks must operate at the same clock frequency.

- The use of an uncommon clock in memory blocks allows for more flexibility in the design, as each memory block can operate at a different clock frequency. This can be useful in designs that require multiple memory blocks with different timing requirements. However, the disadvantage of using an uncommon clock is that it increases the complexity of the design, as each clock signal must be managed independently, and timing issues may arise.
  Overall, the choice between using a common clock or an uncommon clock in memories using On Chip Memory Generator depends on the specific requirements of the design. If the design requires all memory blocks to operate at the same frequency, a

common clock may be the best choice. However, if the design requires flexibility in timing requirements, an uncommon clock may be more appropriate.

Block RAM Versus Distributed RAM

Two types of memory blocks that can be generated with On Chip Memory Generator are Block RAM and Distributed RAM. Block RAM is a large, rectangular array of memory cells optimized for high-speed access, while Distributed RAM is a flexible set of smaller, distributed memory cells that are suitable for storing small amounts of data. The choice between these two types of memory blocks depends on the specific requirements of the design.

IP Support Details

The Table 1 gives the support details for On Chip Memory.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	-	Verilog	-	Verilog	TDP_RAM36K	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2, remaining parameters have been kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	MEMORY_TYPE	Single_Port	BRAMS	1
	WRITE_WIDTH_A	36	LUTS	0
	WRITE_DEPTH_A	1024	REGISTERS	0
	BRAM	TRUE	-	-
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	MEMORY_TYPE	True_Dual_Port	BRAMS	128
	WRITE_WIDTH_A	576	LUTS	0
	WRITE_DEPTH_A	8192	REGISTERS	0
	BRAM	TRUE	-	-

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the On Chip Memory.

Signal Name	Input/Output	Description
clk	Input	Clock for Synchronization of two Ports
Port A		
clk_A	Input	Clock for Port A
addr_A	Input	Address Width of Port A
din_A	Input	Input Data of Port A
wen_A	Input	Write Enable to Port A
ren_A	Input	Read Enable to Port A
dout_A	Output	Output Data of Port A
Port B		
clk_B	Input	Clock for Port B
addr_B	Input	Address Width of Port B
din_B	Input	Input Data of Port B
wen_B	Input	Write Enable to Port B
ren_B	Input	Read Enable to Port B
dout_B	Output	Output Data of Port B

Table 3: Ports

Parameters

Table 4 lists the parameters of the On Chip Memory.

Parameter	Values	Default Value	Description
MEMORY_TYPE	Single Port, Simple Dual Port, True Dual Port	Single Port	Desired Memory Type
DATA_WIDTH	1 to 128	32	Data Width of Memory
WRITE_DEPTH	2 to 32768	1024	Depth of Memory
WRITE_WIDTH_A	9,18,36,72,144, 288,576	36	Write Data Width of Port A
READ_WIDTH_A	9,18,36,72,144, 288,576	36	Read Data Width of Port A
WRITE_WIDTH_B	9,18,36,72,144, 288,576	36	Write Data Width of Port B
READ_WIDTH_B	9,18,36,72,144, 288,576	36	Read Data Width of Port B
WRITE_DEPTH_A	1024,2048,4096, 8192,16384,32768	1024	Write Depth of Port A
ASYMMETRIC	True/False	False	Symmetric vs Asymmetric Ports
COMMON_CLK	True/False	False	Common Clock for Port Synchronization
BRAM	True/False	True	Block RAM vs Distributed RAM Mapping

Table 4: Parameters

Design Flow

IP Customization and Generation

On Chip Memory Generator is a part of the Raptor Design Suite Software. A customized memory can be generated from the Raptor's IP configuration window as shown in Figure 6.

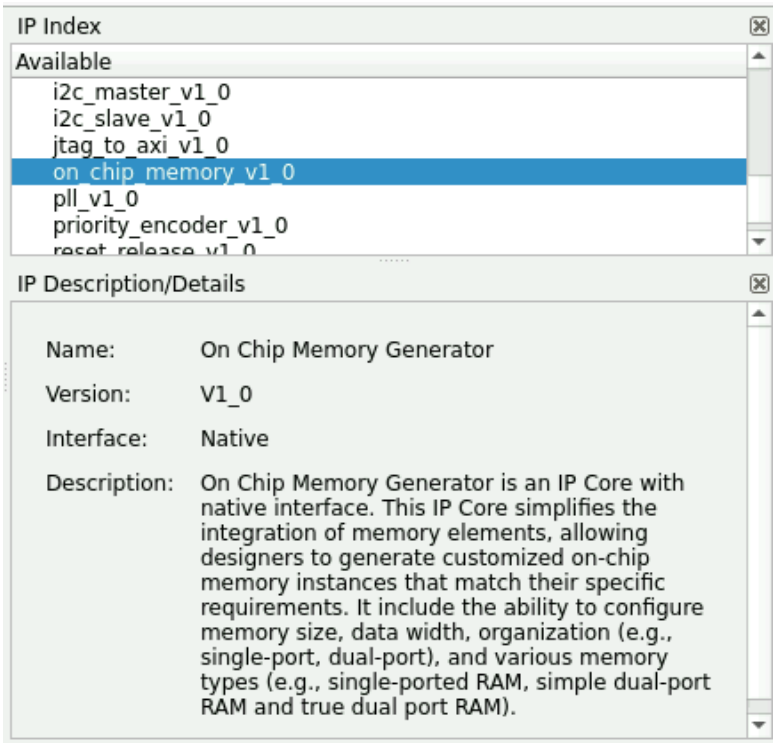

Figure 6: IP List

Parameters Customization

From the IP configuration window, the parameters of the On Chip Memory can be configured and its features can be enabled for generating a customized On Chip Memory IP core that suits the user application requirements. All parameters are shown in Figure 7. In Figure 7, the module name specifies the name of both the Verilog file and the top-level IP name that will be generated based on above configured parameters. The Output Dir is a directory option that allows the user to specify where they want the generated IP to be saved.

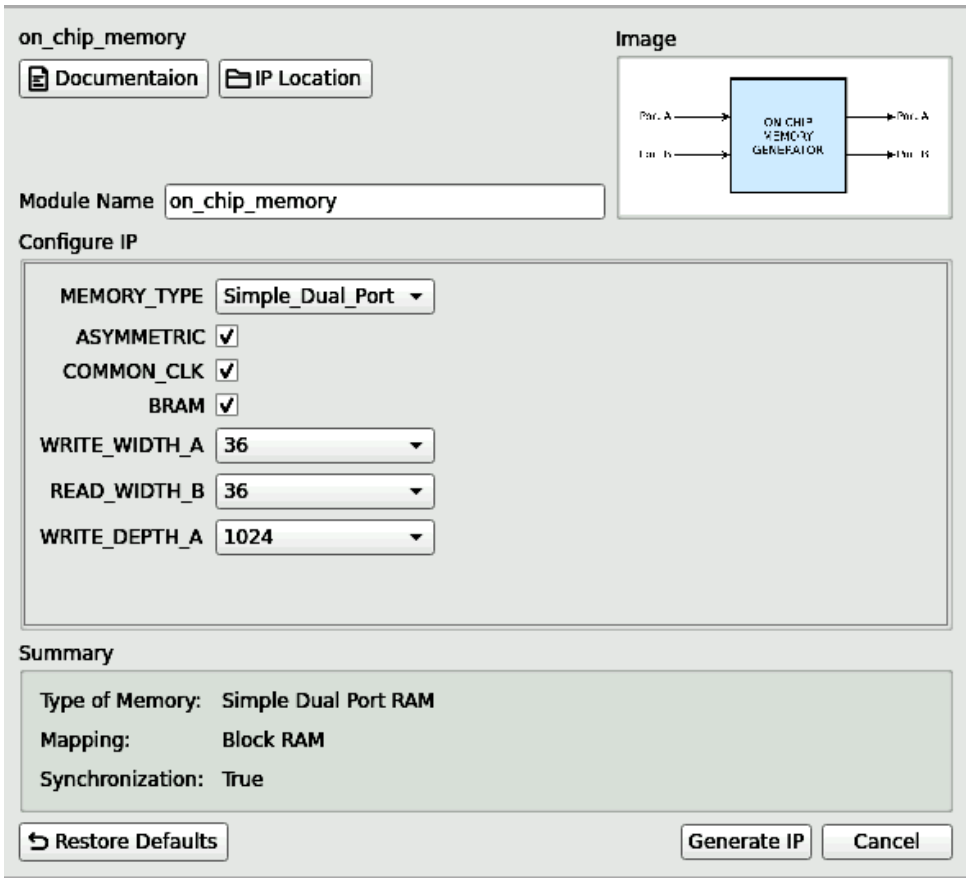

Figure 7: IP Configuration

Synthesis and PR

Raptor Design Suite is armed with tools for Synthesis along with Post and Route capabilities and the generated post-synthesis and post-route and place net-lists can be viewed and analyzed from within the Raptor. The generated bit-stream can then be uploaded on an FPGA device to be utilized in hardware applications.

Testbench

Test

The testbench attached with On Chip Memory Generator is Single Port RAM 1024x32 test. It is basically a comparison between the behavioural RTL and the generated RTL. This test provides 1024 random inputs to addr_A and din_A of both the RTLs and in the end, it compares all the outputs. If all the outputs match, then test will be passed otherwise it'll be failed. The results of this test are attached below in Figure 8.

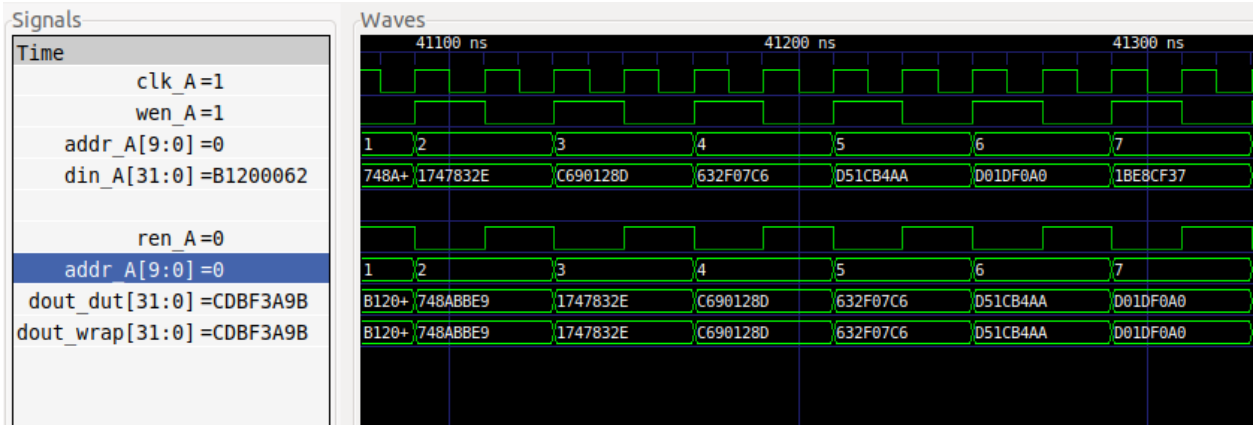

Figure 8: Test Results

Simulation

To run simulation, go to Simulate IP option as shown in Figure 9.

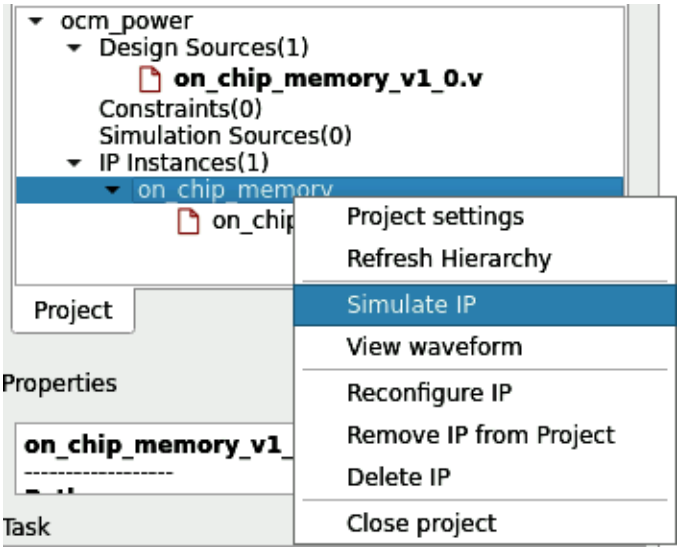

Figure 9: Simulate IP

Waveform

To view waveform, go to View waveform option as shown in Figure 10.

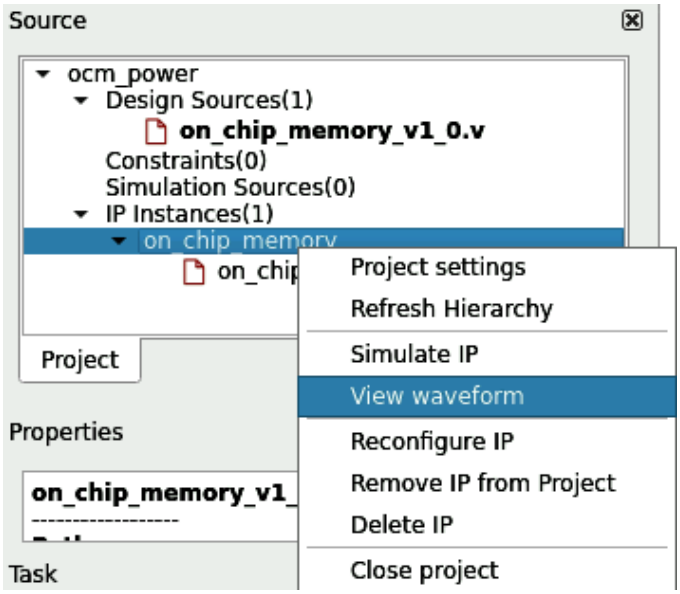

Figure 10: View Waveform

Revision History

Date	Version	Revisions
February 12, 2024	0.1	Initial version On Chip Memory Generator User Guide