PLL
(Beta Release)

Version 1.0

November 26, 2023

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IP Summary

Introduction

A PLL (Phase-Locked Loop) IP core is a fundamental building block in digital integrated circuit design, particularly in applications requiring precise clock generation and synchronization. This IP core plays a critical role in generating stable and phase-locked clock signals, making it an essential component in various digital systems, including microprocessors, communication devices, and data converters.

Features

- Upto 4 divided clock outputs
- Fast clock range 800 - 3200 MHz
- Input reference clock freq between 5 - 1200 MHz

Overview

PLL

The PLL IP core functions as a frequency synthesizer, producing one or more output clock signals that are phase-locked and synchronized to a reference clock source. This synchronization ensures that the output clocks maintain specific frequency and phase relationships, meeting the timing requirements of the entire system.

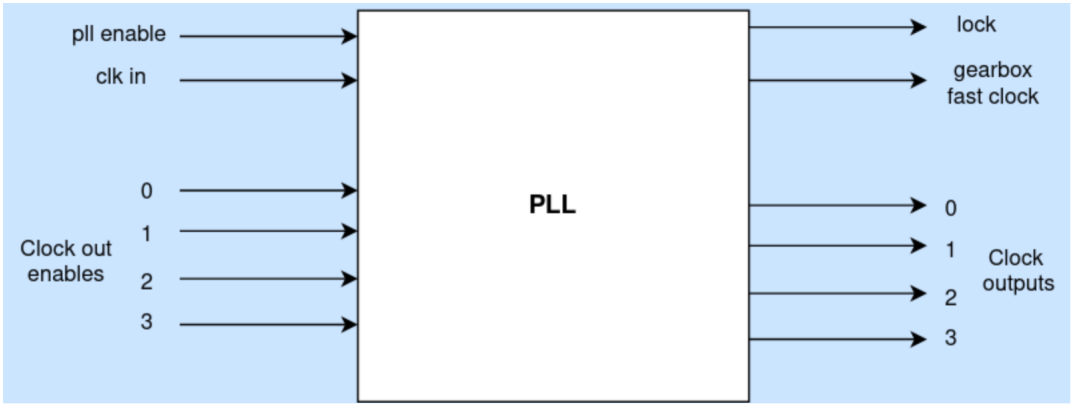

Figure 1: PLL Block Diagram

IP Specification

The working principle of a PLL (Phase-Locked Loop) IP core revolves around maintaining a stable phase and frequency relationship between its reference clock input and one or more output clock signals. It achieves this by continuously comparing the phases of the reference clock and an internally generated feedback signal using a phase detector. Any phase or frequency difference detected results in an error signal, which is converted into a control current by a charge pump. This current, after passing through a loop filter, provides a precise control voltage to a Voltage-Controlled Oscillator (VCO). The VCO generates an output clock signal whose frequency is directly proportional to this control voltage. By adjusting the VCO's frequency in response to the error signal, the PLL ensures that the output clock(s) remain locked to the reference clock, thus achieving phase-locked and synchronized clock signals suitable for various digital system applications.

IP Support Details

The Table 1 gives the support details for PLL.

Compliance		IP Resources					Tool Flow		
Device	Interface	Source Files	Constraint File	Testbench	Simulation Model	Software Driver	Analyze and Elaboration	Simulation	Synthesis
GEMINI	Native	Verilog	SDC	Verilog	verilog	Icarus	Raptor	Raptor	Raptor

Table 1: IP Details

Parameters

Table 2 lists the parameters of the PLL.

Parameter	Values	Default Value	Description
Divide clocks	8 / 16 / 32	16	Address Width for PLL
Clock_out_1	8 / 16 / 32 / 64	32	Output clocks
Fast Clock freq	800 - 3200 MHz	Desired fast clock fre-quency	5 - 1200 MHz
Reference clock PLL		Reference Clock	
ADDRESS WIDTH	8 / 16 / 32	16	Address Width for PLL
Enable input divider	True / False	Divide clock by 2 PLL	

Table 2: Parameters

Port List

Table **??**switch-intrtab:axis_switch-intrs the top interface ports of the PLL.

Signal Name	I/O	Description
AXI Clock and Reset		
PLL_EN	I	PLL Enable

CLK_IN	I	Clock Input
PLL Signals		
CLK_OUT0_EN	I	Enable CLK_OUT0
CLK_OUT1_EN	I	Enable CLK_OUT1
CLK_OUT2_EN	I	Enable CLK_OUT2
CLK_OUT3_EN	I	Enable CLK_OUT3
CLK_OUT0	O	CLK_OUT0 output
CLK_OUT1	O	CLK_OUT1 output
CLK_OUT2	O	CLK_OUT2 output
CLK_OUT3	O	CLK_OUT3 output
GEARBOX_FAST_CLK	I	Gearbox fast clock output
LOCK	I	PLL lock signal

Table 3: PLL Interface

Resource Utilization

The parameters for computing the maximum and minimum resource utilization are given in Table 4, remaining parameters have been kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minumum Resource	**Options**	**Configuration**	**Resource**	**Utilized**
	ADDR WIDTH	8	LUTs	677
	DATA WIDTH	8	Registers	557
Maximum Resource	**Options**	**Configuration**	**Resource**	**Utilized**
	ADDR WIDTH	32	LUTs	814
	DATA WIDTH	64	Registers	636

Table 4: Resource Utilization

IP Customization and Generation

PLL IP core is a part of the Raptor Design Suite Software. A customized PLL can be generated from the Raptor's IP configurator window as shown in Figure 2.

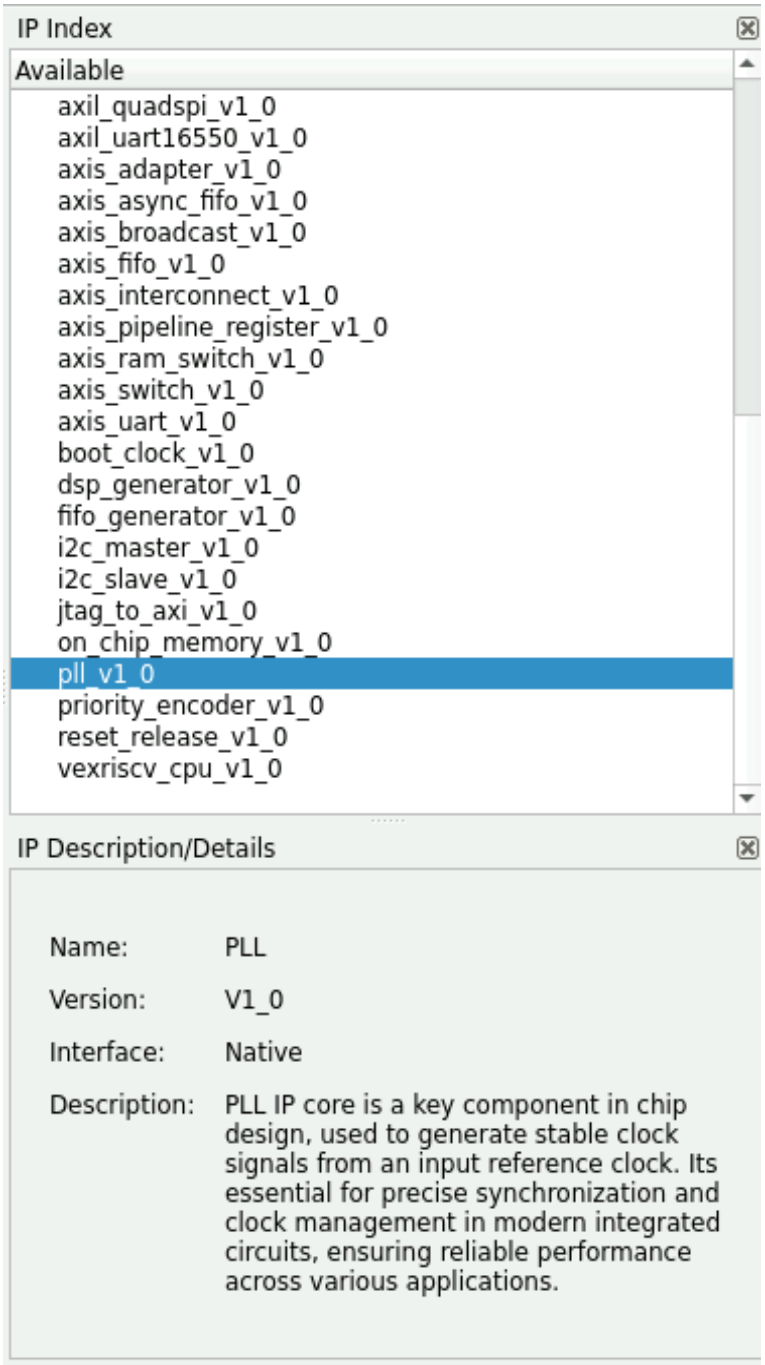

Figure 2: IP list

Parameters Customization

From the IP configuration window, the parameters of the PLL can be configured and PLL features can be enabled for generating a customized PLL IP core that suits the user application requirement as shown in Figure 3. After IP Customization, all the source files are made available to the user with a top wrapper that instantiates a parameterized instance of the PLL.

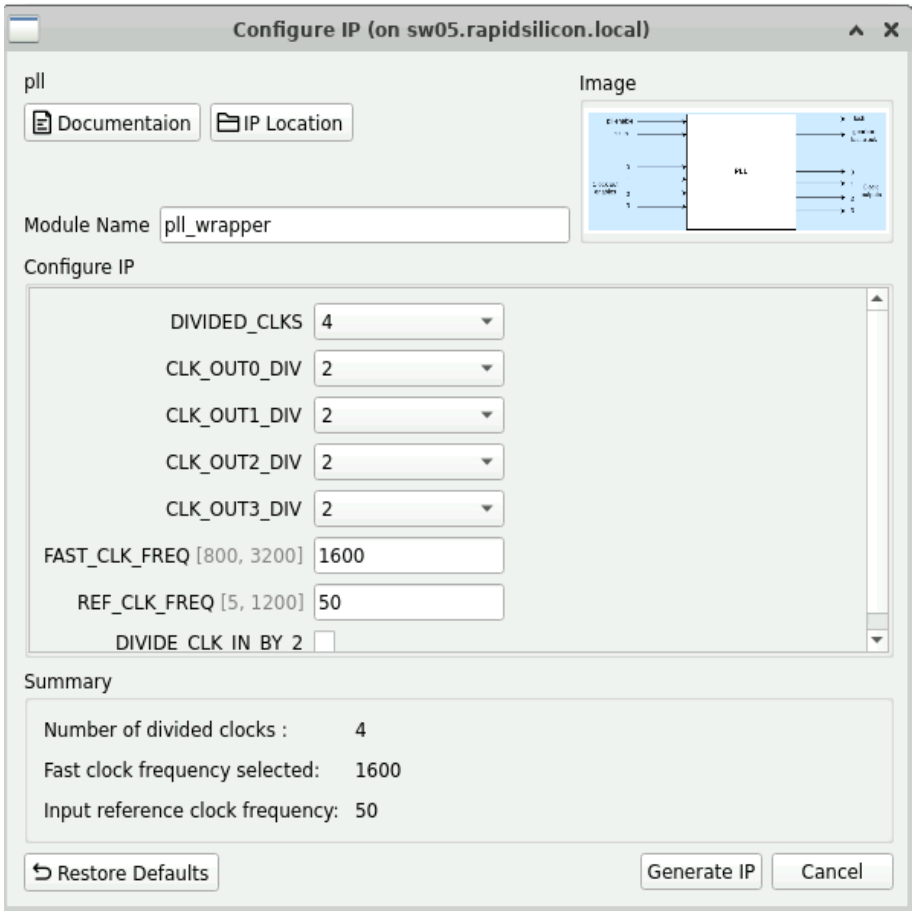

Figure 3: IP Configuration

Test Bench Simulation

Currently, no testbench added in Raptor for PLL.

Release

Release History

Date	Version	Revisions
November 26, 2023	0.01	Initial version PLL User Guide Document