AXI-Stream FIFO (Beta Release)

Version 1.0

November 26, 2023

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Contents

IP Summary

Introduction

An AXI Stream FIFO is a commonly used module in digital design that acts as a data mover between two AXI Stream interfaces. It provides a buffer to store a stream of data items coming from the input interface, and allows them to be read out in the same order from the output interface. The FIFO also have various options and configurations to control its behavior, such as the depth of the buffer, the type of synchronization mechanism used, and the way overflow or underflow situations are handled.

The AXI Stream interface is a widely used standard for streaming data in digital systems, particularly in the context of FPGA and ASIC designs. It consists of two unidirectional channels, a data channel and a control channel, both of which have a fixed format and timing. The data channel carries a continuous stream of data items, each of which can have a fixed or variable width, and the control channel includes a few signals that indicate the start and end of a transfer, as well as any error or flow control conditions.

Features

- The FIFO supports data transfer widths of 8, 16, 32, upto 1024 bits.
- The FIFO can be configured with a depth of up to 2^{15} words.
- The FIFO includes a parameterizable flag that indicates when the FIFO is empty or full.
- The FIFO includes a parameterizable flag that indicates when an error condition has occurred, such as a data overrun or underrun.
- The FIFO supports AXI4-Stream interfaces.

Overview

AXIS FIFO

An AXI streaming FIFO is an IP that allows for the transfer of large, continuous data streams between two components of a larger digital system that uses the AXI streaming protocol. The AXI streaming FIFO is designed specifically for data streams that consist of a large number of continuous data elements, such as video or audio signals, which are transferred in a continuous, sequential manner. This IP provides a buffering mechanism that ensures the reliable transfer of data between the write-side and read-side interfaces. An AXI streaming FIFO can be used in a wide range of digital systems, including multimedia systems, network switches, and digital signal processing (DSP) systems, where efficient and reliable data transfer is essential for proper system operation. A block diagram for the AXIS FIFO IP is shown in Figure 1.

The module has several status signals to indicate the state of the FIFO. The status_overflow signal is used to indicate when the FIFO has overflowed. The status_bad_frame signal is used to indicate when a frame marked as bad has been detected. The status_good_frame signal is used to indicate when a good frame has been detected. The status_full signal is used to indicate when the FIFO is full. The status_empty signal is used to indicate when the FIFO is empty.

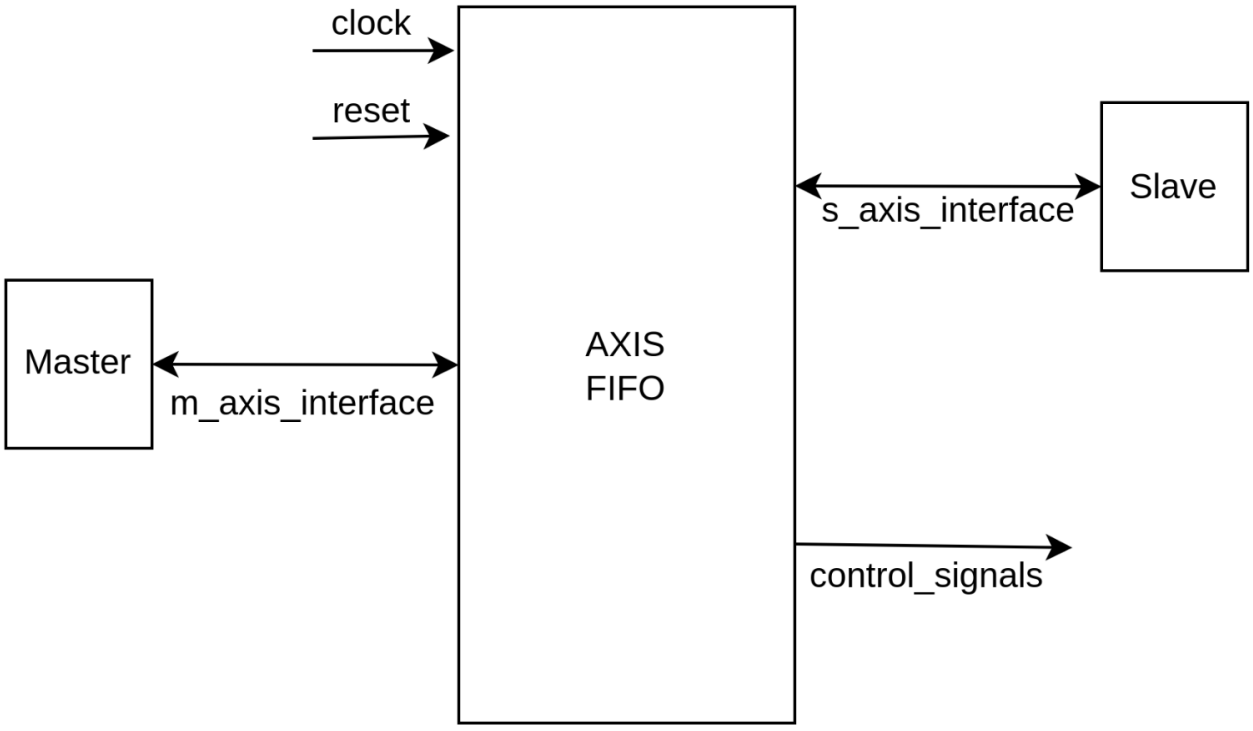

Figure 1: AXIS FIFO Block Diagram

Standards

The AXI4-Lite interface is compliant with the AMBA® AXI Protocol Specification.

IP Support Details

The Table 1 gives the support details for AXIS FIFO.

Compliance		IP Resources					Tool Flow	
Device	Interface	Source Files	Constraint File	Testbench	Simulation Model	Analyze and Elaboration	Simulation	Synthesis
GEMINI	AXI-Streaming	Verilog	-	Python	CocoTb	Raptor(Surelog)	Raptor(Icarus)	Raptor

Table 1: IP Details

Parameters

Table 2 lists the parameters of the AXIS FIFO.

Parameter	Values	Default Value	Description
DEPTH	16,32,..,32768	4096	FIFO DEPTH
DATA WIDTH	8,16,32,...,1024	8	Width of AXI stream interfaces in bits
LAST ENABLE	0 / 1	1	Propagate tlast signal
ID ENABLE	0 / 1	1	Propagate tid signal
ID WIDTH	1-8	8	tid signal width
DEST ENABLE	0 / 1	1	Propagate tdest signal
DEST WIDTH	1 - 8	8	tdest signal width
USER ENABLE	0 / 1	1	Propagate tuser signal
PIPELINE OUTPUT	0-32	2	number of output pipeline registers
FRAME FIFO	0 / 1	1	Frame FIFO mode - operate on frames instead of cycles, when set, m_axis_tvalid will not be deasserted within a frame
USER BAD FRAME VALUE	0 / 1	1	tuser value for bad frame marker
USER BAD FRAME MASK	0 / 1	1	tuser mask for bad frame marker
DROP BAD FRAME	0 / 1	1	Drop frames marked bad
DROP WHEN FULL	0 / 1	1	Drop incoming frames when full

Table 2: Parameters

Port List

Table 3 lists the top interface ports of the AXIS FIFO.

Signal Name	I/O	Description
AXI Clock and Reset		
clk	I	AXI4-Stream Clock
rst	I	AXI4-Stream RESET
AXI Slave Interface		
s_axis_tdata	I	AXI4-Stream data
s_axis_tkeep	I	AXI4-Stream keep data qualifier
s_axis_tvalid	I	AXI4-Stream valid transfer
s_axis_tready	O	AXI4-Stream transfer ready
s_axis_tlast	I	AXI4-Stream boundary of transfer packet
s_axis_tid	I	AXI4-Stream data stream identifier
s_axis_tdest	I	AXI4-Stream data routing information
s_axis_tuser	I	AXI4-Stream user defined sideband information
AXI Master Interface		
m_axis_tdata	O	AXI4-Stream data
m_axis_tkeep	O	AXI4-Stream keep data qualifier
m_axis_tvalid	O	AXI4-Stream valid transfer
m_axis_tready	I	AXI4-Stream transfer ready
m_axis_tlast	O	AXI4-Stream boundary of transfer packet
m_axis_tid	O	AXI4-Stream data stream identifier
m_axis_tdest	O	AXI4-Stream data routing information
Status Signals		
status_overflow	O	Status signal for FIFO overflow condition
status_bad_frame	O	Status signal to flag a bad frame
status_good_frame	O	Status signal to highlight a good frame
status_full	O	Status signal to highlight FIFO full condition
status_empty	O	Status signal to highlight FIFO empty condition

Table 3: AXIS FIFO Interface

Resource Utilization

The parameters for computing the maximum and minimum resource utilization are given in Table 4, remaining parameters have been kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilized**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	DEPTH	8	LUTs	175
	DATA WIDTH	8		
	ID WIDTH	1	Registers	204
	DEST WIDTH	0		
	USER WIDTH	1	BRAM	1
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	DEPTH	32768	LUTs	103778
	DATA WIDTH	4096		
	ID WIDTH	32	Registers	310644
	DEST WIDTH	32		
	USER WIDTH	32	BRAM	132

Table 4: Resource Utilization

Design Flow

IP Customization and Generation

AXIS FIFO IP core is a part of the Raptor Design Suite Software. A customized AXIS FIFO can be generated from the Raptor's IP configurator window as shown in Figure 2.

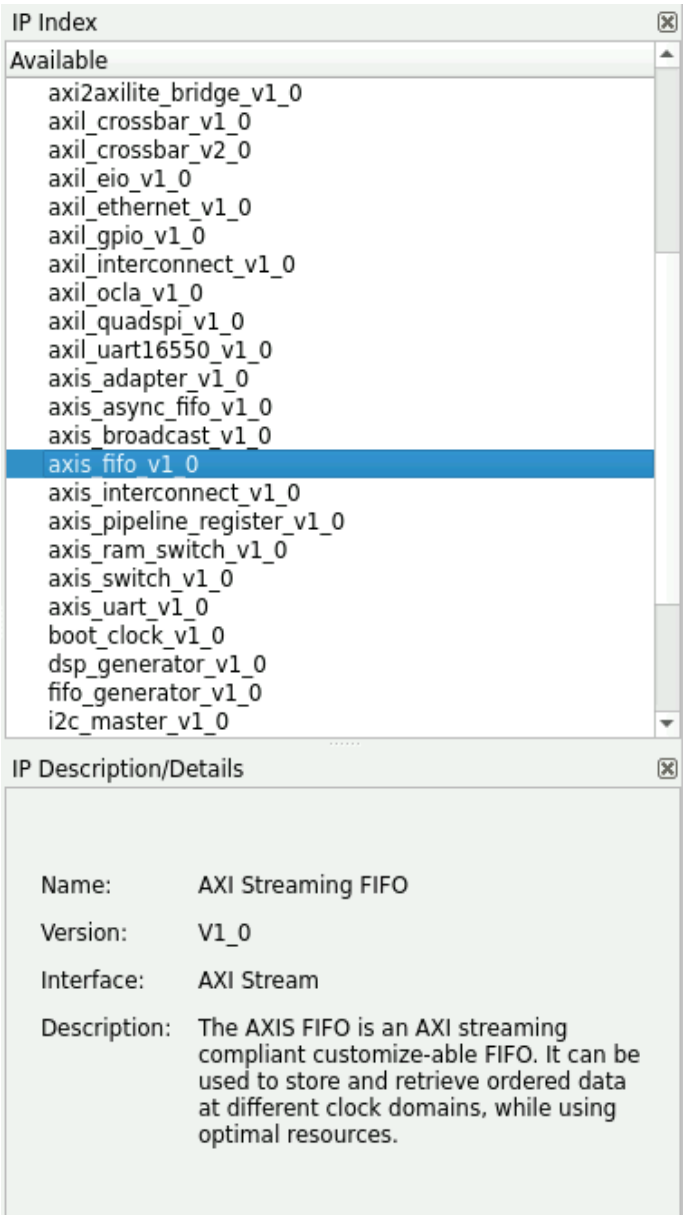

Figure 2: IP list

Parameters Customization

From the IP configuration window, the parameters of AXIS FIFO can be configured and IP features can be enabled for generating a customized AXIS FIFO IP core that suits the user application requirement as shown in Figure 3. After IP Customization, all the source files are made available to the user with a top wrapper that instantiates a parameterized instance of the AXIS FIFO.

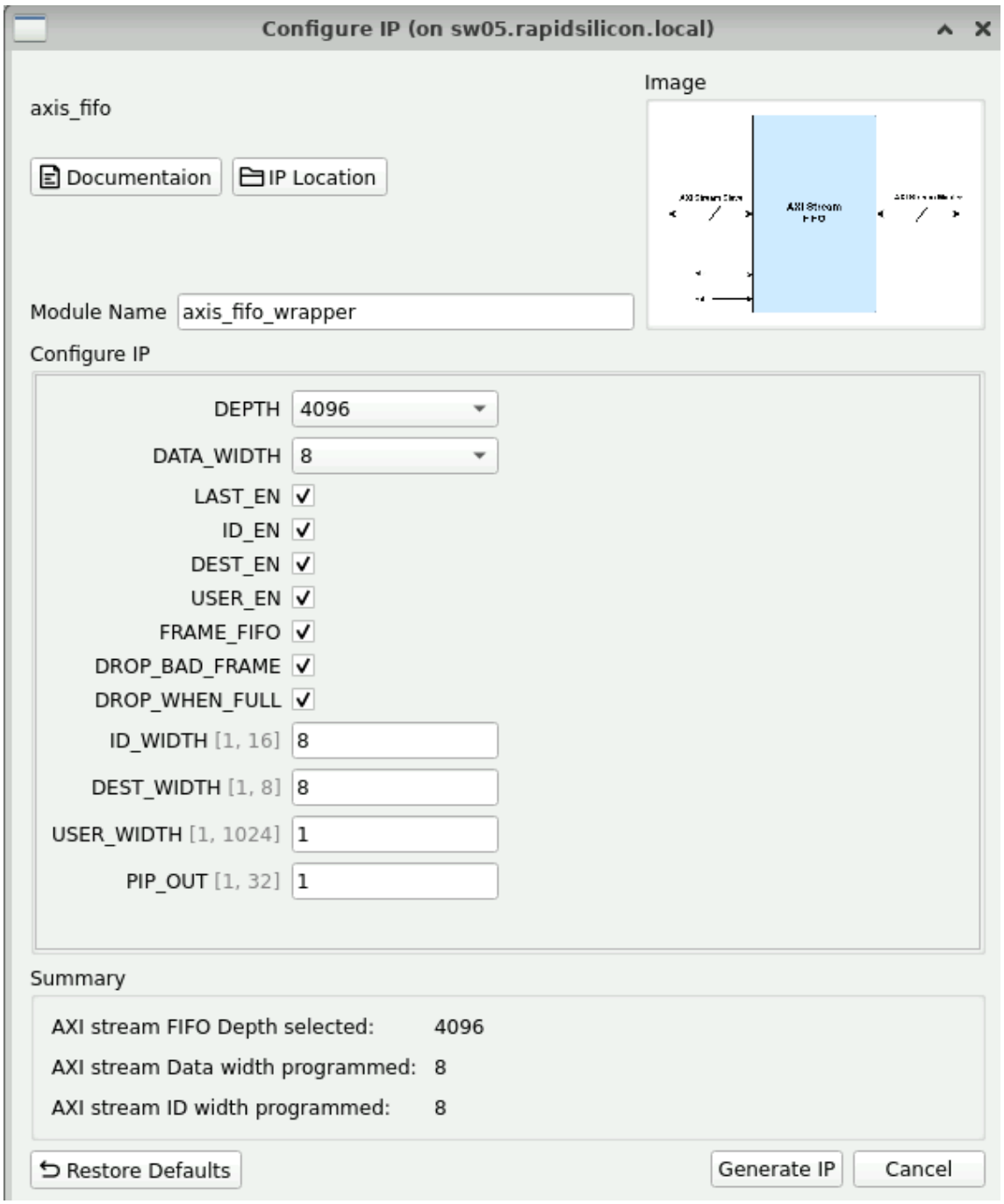

Figure 3: IP Configuration

Synthesis and PR

Raptor Suite is armed with tools for Synthesis along with Post and Route capabilities and the generated post-synthesis and post-route and place net-lists can be viewed and analyzed from within the Raptor. The generated bit-stream can then be uploaded on an FPGA device to be utilized in hardware applications.

Test Bench Simulation

The AXIS FIFO simulation is based on Cocotb. It has a complete environment that extensively tests AXIS FIFO as a DUT. It has 25 tests in total, 12 write tests, 12 read tests and a stress test. The simulation can be run from Raptor IP Catalog. The simulation can be easily run by clicking the "Simulate IP" button as shown in figure 4. The waveforms are also dumped for in-depth analysis of the whole operation which can be seen by clicking the "View Waveform" button.

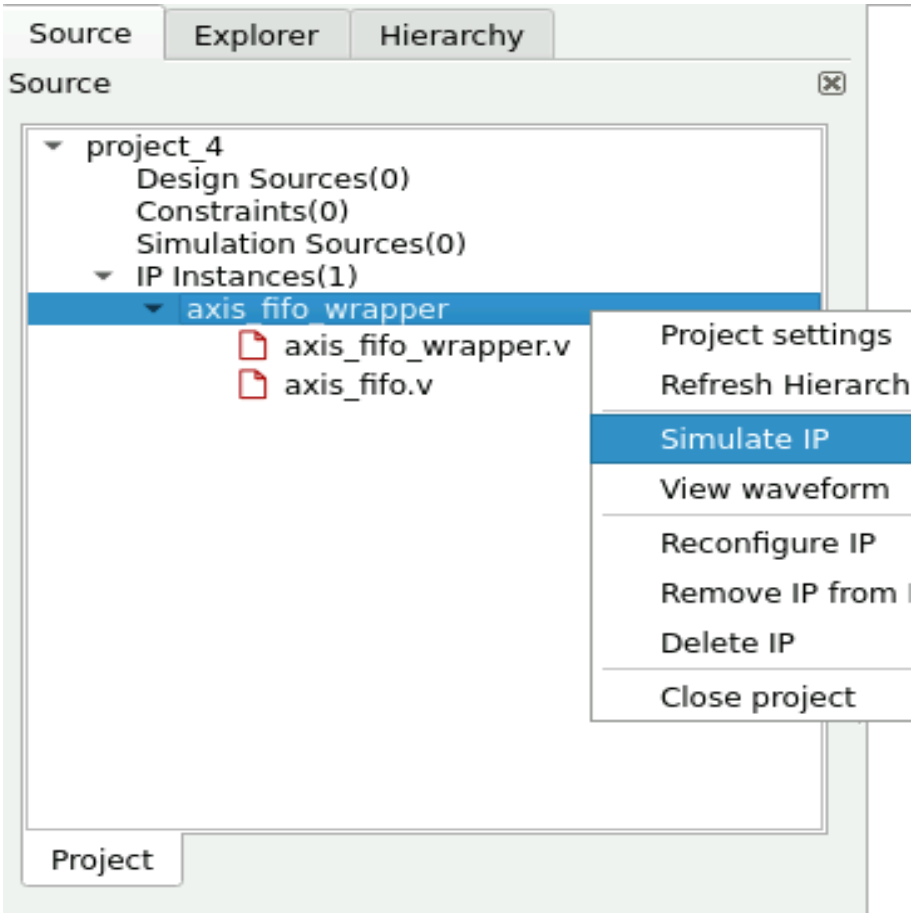

Figure 4: Simulate IP Window

The simulation results are also displayed in the console window a glimpse of which can be seen in figure 5.

```
**************************************************************************************************************
** TEST                                          STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
**************************************************************************************************************
** test_axis_fifo.run_test_001                   PASS       11060.00           0.25      44705.01  **
** test_axis_fifo.run_test_002                   PASS       28330.00           0.55      51090.30  **
** test_axis_fifo.run_test_003                   PASS       26700.00           0.55      48503.75  **
** test_axis_fifo.run_test_004                   PASS       43970.00           0.86      51037.01  **
** test_axis_fifo.run_test_tuser_assert_001      PASS         720.00           0.02      43945.04  **
** test_axis_fifo.run_test_init_sink_pause_001   PASS        1040.00           0.02      45559.35  **
** test_axis_fifo.run_test_init_sink_pause_reset_001 PASS     1420.00           0.03      47986.30  **
** test_axis_fifo.run_test_overflow_001          PASS       41040.00           0.87      47278.11  **
** test_axis_fifo.run_stress_test_001            PASS       11300.00           0.29      39140.09  **
** test_axis_fifo.run_stress_test_002            PASS       47490.00           0.94      50390.67  **
** test_axis_fifo.run_stress_test_003            PASS       45490.00           0.92      49510.92  **
** test_axis_fifo.run_stress_test_004            PASS       44730.00           0.92      48432.79  **
**************************************************************************************************************
** TESTS=12 PASS=12 FAIL=0 SKIP=0                          303290.01          10.32      29385.10  **
**************************************************************************************************************
```

Figure 5: Simulation Results

Release

Release History

Date	Version	Revisions
November 26, 2023	1.0	Initial version AXIS FIFO User Guide Document