AXI4 Interconnect (Beta Release)

Version 0.1

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Contents

IP Summary

Introduction

The AXI4 (Advanced eXtensible Interface 4) interconnect is a widely-used, industry-standard protocol for connecting intellectual property (IP) blocks in a system-on-chip (SoC) design. The AXI4 interconnect supports high-bandwidth, low-latency communication between IP blocks, and provides a range of features and functionality to optimize system performance and reduce design complexity. It includes separate read and write channels for data and control information, support for burst transfers and out-of-order transaction processing, and features to support cache coherency and multi-master configurations. The AXI4 interconnect is widely used in a range of applications, including mobile devices, networking equipment, and high-performance computing systems. It provides a standardized interface that allows IP blocks from different vendors to be easily integrated into a single SoC design, reducing development time and cost.

Features

- High performance: AXI4 interconnect is designed for high performance with a high-bandwidth, low-latency interface that can handle large amounts of data.
- Scalability: The AXI4 interconnect is highly scalable, supporting a large number of masters and slaves. This makes it suitable for complex SoC designs.
- Burst transfers: The AXI4 interconnect supports burst transfers, which allows for more efficient data transfer by reducing the number of transactions required.
- Configurability: AXI4 interconnect is highly configurable, allowing designers to optimize the interconnect for their specific SoC design.
- Address and data interleaving: AXI4 interconnect supports address and data interleaving, which allows for faster data transfers by overlapping address and data phases.
- Master Count: 16
- Slave Count: 16
- Data Width: 8, 16, 32, 64, 128, 256 bits
- Address Width: 32, 64, 128 bits
- User Width (per channel): Up to 1024 bits
- ID Width: Up to 8 bits

Overview

AXI4 Interconnect

AXI Interconnect IP core is a component used in system-on-chip (SoC) designs to connect multiple AXI masters and slaves. It acts as a central hub or router that interconnects the AXI components in a system and provides a common communication protocol for them. This IP core supports the AXI protocol. It includes multiple AXI slave and master ports, enabling it to connect multiple AXI components within a system. It uses arbitration and routing logic to manage the data transfers between the AXI components connected to its ports. It also supports various routing schemes, such as round-robin and fixed priority. The block diagram of AXI4 Interconnect is given in figure 1.

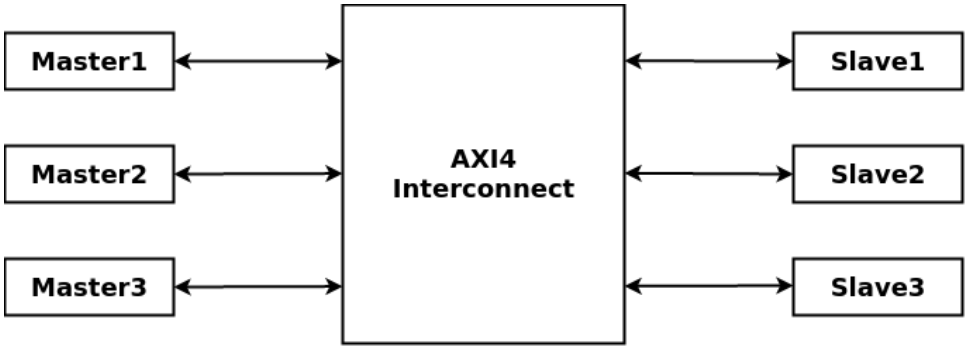

Figure 1: AXI4 Interconnect Block Diagram

IP Specification

The AXI4 Interconnect IP specification provides a standardized approach for connecting different components of a system-on-chip, such as processors, memories, DMA controllers, and other IP blocks, through a common bus architecture. It provides a set of rules and protocols for data transfer, flow control, arbitration, and other aspects of communication between the components. It supports multiple masters and multiple slaves, and can be configured to support different data widths, burst sizes, and transfer modes. It also supports various QoS (Quality of Service) levels and power management features to optimize system performance and energy efficiency. The figure 2 shows the top level diagram of AXI4 Interconnect.

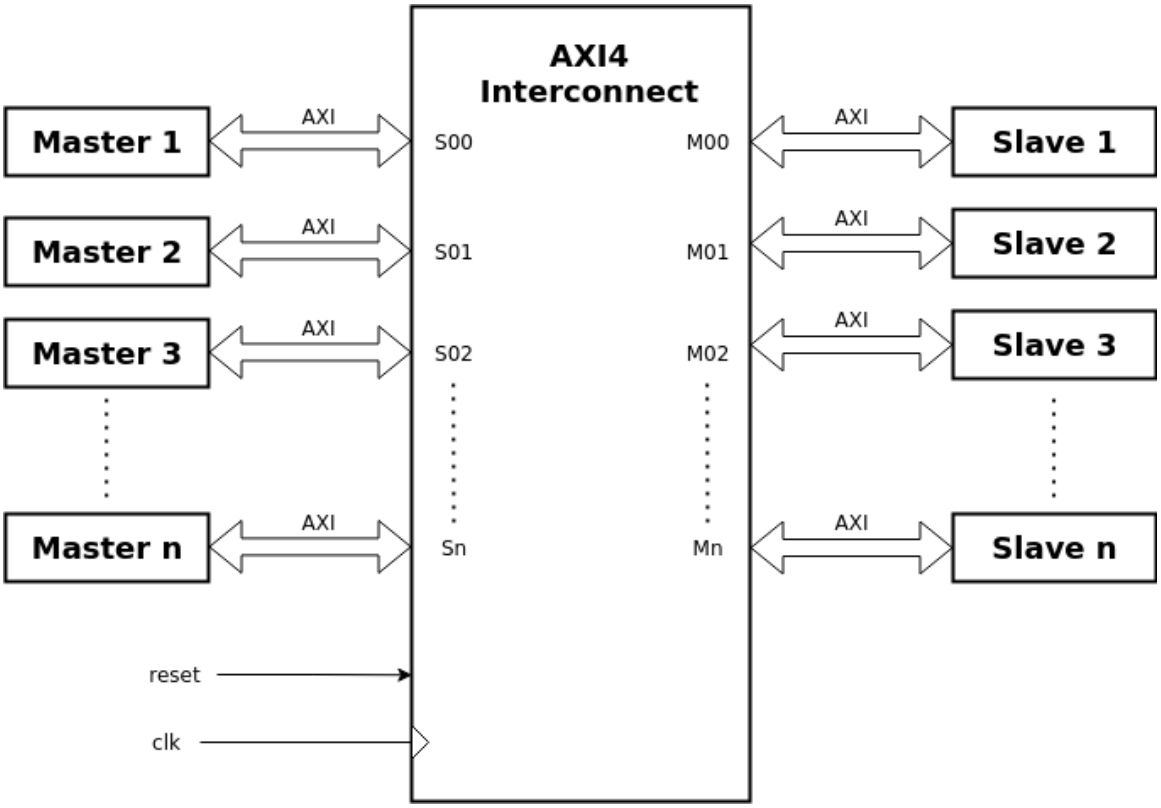

Figure 2: Top Module

Address Decoding

The block diagram in Figure 3 depicts the Address Decoder responsible for assigning address space to each Master Interface and maintaining an address table. When a transaction occurs on the Address Write or Address Read channels of the Slave Interface, the AXI4 Interconnect core must determine which Master Interface is the intended target by decoding the address. The address decoder ensures that there is no overlapping of addresses and that all addresses are aligned. It follows certain rules while assigning address space to each master interface. If the address received on the Slave Interface does not match any of the address ranges being decoded by the Address Decoder, the transaction is trapped and handled by a decoded error module. In such situations, the interconnect generates a protocol compliant response indicating that there is no available slave within this address range.

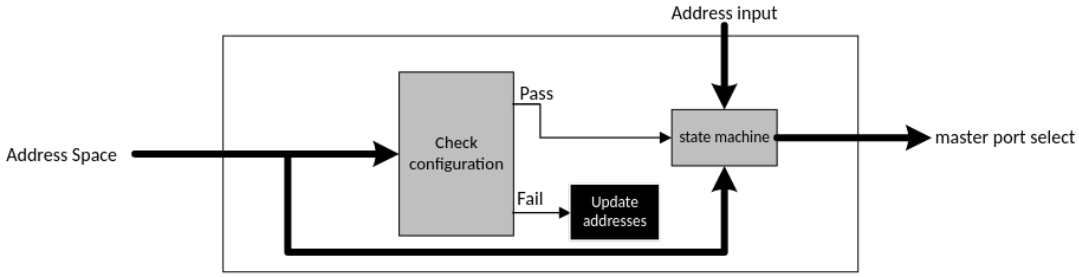

Figure 3: Address Decoding

Arbitration

The AXI4 Interconnect core has arbiters for both write and read channel instances, which are responsible for address and response arbitration. The priority encoder sets the relative priority for each transaction, and arbitration among different transactions is decided using round-robin methodology. In a write transaction, both AWVALID and AWREADY signals must be high for the transaction to start, and the transaction is considered complete when a BVALID/BREADY handshake is completed. The counter increments upon the start of a transaction and decrements upon its completion, enabling the calculation of the total number of write transactions in flight. In a read transaction, both ARVALID and ARREADY signals go high when the transaction starts, while transactions are considered complete when an RVALID/RREADY handshake completes with RLAST asserted. The Interconnect counts the total number of read transactions in flight based on these signals. Transactions that target a master interface that has reached its issuing limit are disqualified from arbitration, and their request is not forwarded to the arbiter.

Standards

The AXI4 Master and Slave interfaces are compliant with the AMBA® AXI Protocol Specification.

IP Support Details

The Table 1 gives the support details for AXI4 Interconnect.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI4	Verilog	-	Cocotb	-	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2, remaining parameters have been kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	S_COUNT	1	BRAMS	0
	M_COUNT	1	REGISTERS	152
	DATA_WIDTH	8	LUTS	173
	ADDR_WIDTH	32	-	-
Maximum Resources	**Options**	**Configuration**	**Resources**	**Utilized**
	S_COUNT	16	BRAMS	3
	M_COUNT	16	REGISTERS	1521
	DATA_WIDTH	256	LUTS	6212
	ADDR_WIDTH	128	-	-

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the AXI4 Interconnect and 'x' represents the number of interface.

Signal Name	I/O	Description
clk	I	Clock Signal for Interconnect
rst	I	Active High Synchronous Reset Signal
Slave Write Address Channel		
s<x>_axi_awid	I	Write address ID
s<x>_axi_awaddr	I	Write address
s<x>_axi_awlen	I	Burst length
s<x>_axi_awsize	I	Burst size
s<x>_axi_awburst	I	Burst type
s<x>_axi_awlock	I	Lock type
s<x>_axi_awcache	I	Memory type
s<x>_axi_awprot	I	Protection type
s<x>_axi_awvalid	I	Write address valid
s<x>_axi_awready	O	Write address ready
Slave Write Data Channel		
s<x>_axi_wdata	I	Write data
s<x>_axi_wstrb	I	Write strobe
s<x>_axi_wlast	I	Write last
s<x>_axi_wvalid	I	Write valid
s<x>_axi_wready	O	Write ready
Slave Write Response Channel		
s<x>_axi_bid	O	Response ID tag
s<x>_axi_bresp	O	Write response
s<x>_axi_bvalid	O	Write response valid
s<x>_axi_bready	I	Write response ready
Slave Read Address Channel		
s<x>_axi_arid	I	Read address ID
s<x>_axi_araddr	I	Read address
s<x>_axi_arlen	I	Burst length
s<x>_axi_arsize	I	Burst size
s<x>_axi_arburst	I	Burst type
s<x>_axi_arlock	I	Lock type
s<x>_axi_arcache	I	Memory type
s<x>_axi_arprot	I	Protection type
s<x>_axi_arvalid	I	Read address valid
s<x>_axi_arready	O	Read address ready
Slave Read Data Channel		
s<x>_axi_rid	O	Read ID tag
s<x>_axi_rdata	O	Read data

Signal Name	I/O	Description
s<x>_axi_rresp	O	Read response
s<x>_axi_rlast	O	Read last
s<x>_axi_rvalid	O	Read valid
s<x>_axi_rready	I	Read ready
Master Write Address Channel		
m<x>_axi_awid	O	Write address ID
m<x>_axi_awaddr	O	Write address
m<x>_axi_awlen	O	Burst length
m<x>_axi_awsize	O	Burst size
m<x>_axi_awburst	O	Burst type
m<x>_axi_awlock	O	Lock type
m<x>_axi_awcache	O	Memory type
m<x>_axi_awprot	O	Protection type
m<x>_axi_awvalid	O	Write address valid
m<x>_axi_awready	I	Write address ready
Master Write Data Channel		
m<x>_axi_wdata	O	Write data
m<x>_axi_wstrb	O	Write strobe
m<x>_axi_wlast	O	Write last
m<x>_axi_wvalid	O	Write valid
m<x>_axi_wready	I	Write ready
Master Write Response Channel		
m<x>_axi_bid	I	Response ID tag
m<x>_axi_bresp	I	Write response
m<x>_axi_bvalid	I	Write response valid
m<x>_axi_bready	O	Write response ready
Master Read Address Channel		
m<x>_axi_arid	O	Read address ID
m<x>_axi_araddr	O	Read address
m<x>_axi_arlen	O	Burst length
m<x>_axi_arsize	O	Burst size
m<x>_axi_arburst	O	Burst type
m<x>_axi_arlock	O	Lock type
m<x>_axi_arcache	O	Memory type
m<x>_axi_arprot	O	Protection type
m<x>_axi_arvalid	O	Read address valid
m<x>_axi_arready	I	Read address ready
Master Read Data Channel		
m<x>_axi_rid	I	Read ID tag
m<x>_axi_rdata	I	Read data
m<x>_axi_rresp	I	Read response
m<x>_axi_rlast	I	Read last

Signal Name	I/O	Description
m<x>_axi_rvalid	I	Read valid
m<x>_axi_rready	O	Read ready

Table 3: Port List

Parameters

Table 4 lists the parameters of the AXI4 Interconnect.

Parameter	Values	Default Value	Description
S_COUNT	1-16	4	No. of Slaves connected to Interconnect
M_COUNT	1-16	4	No. of Masters connected to Interconnect
DATA_WIDTH	8, 16, 32, 64, 128, 256	32	Data Width of Interconnect
ADDR_WIDTH	32, 64, 128	32	Address Width of Interconnect
ID_WIDTH	1-1024	1	ID field of Interconnect
AW_USER_EN	True/False	True	User Enable Field for AW Channel
W_USER_EN	True/False	True	User Enable Field for W Channel
B_USER_EN	True/False	True	User Enable Field for B Channel
AR_USER_EN	True/False	True	User Enable Field for AR Channel
R_USER_EN	True/False	True	User Enable Field for R Channel
AW_USER_WIDTH	1-1024	1	User Field for AW Channel
W_USER_WIDTH	1-1024	1	User Field for W Channel
B_USER_WIDTH	1-1024	1	User Field for B Channel
AR_USER_WIDTH	1-1024	1	User Field for AR Channel
R_USER_WIDTH	1-1024	1	User Field for R Channel

Table 4: Parameters

Design Flow

IP Customization and Generation

AXI4 Interconnect IP core is a part of the Raptor Design Suite Software. A customized interconnect can be generated from the Raptor's IP configuration window as shown in figure 4.

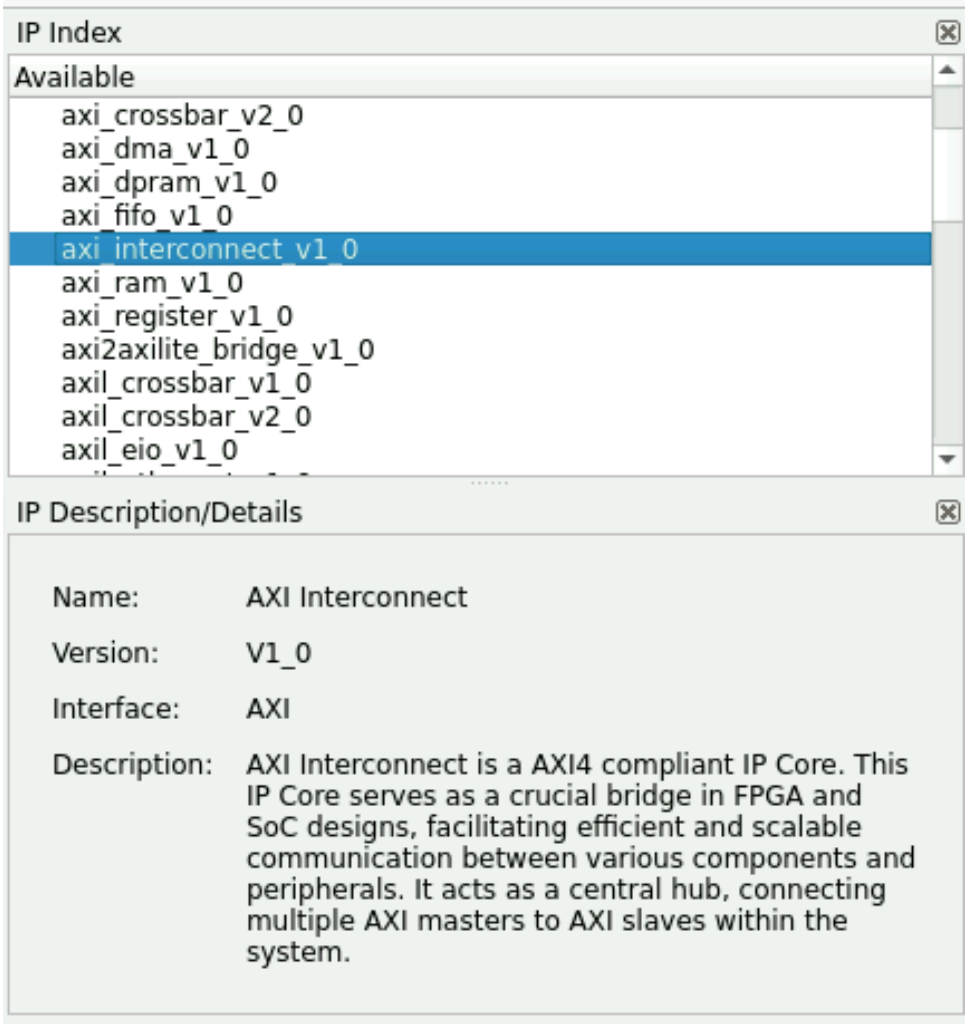

Figure 4: IP List

Parameters Customization

From the IP configuration window, the parameters of the AXI4 Interconnect can be configured and it's features can be enabled for generating a customized IP core that suits the user application requirements. All parameters are shown in Figure 5. In Figure 5, the module name specifies the name of both the Verilog file and the top-level IP name that will be generated based on above configured parameters. The Output Dir is a directory option that allows the user to specify where they want the generated IP to be saved.

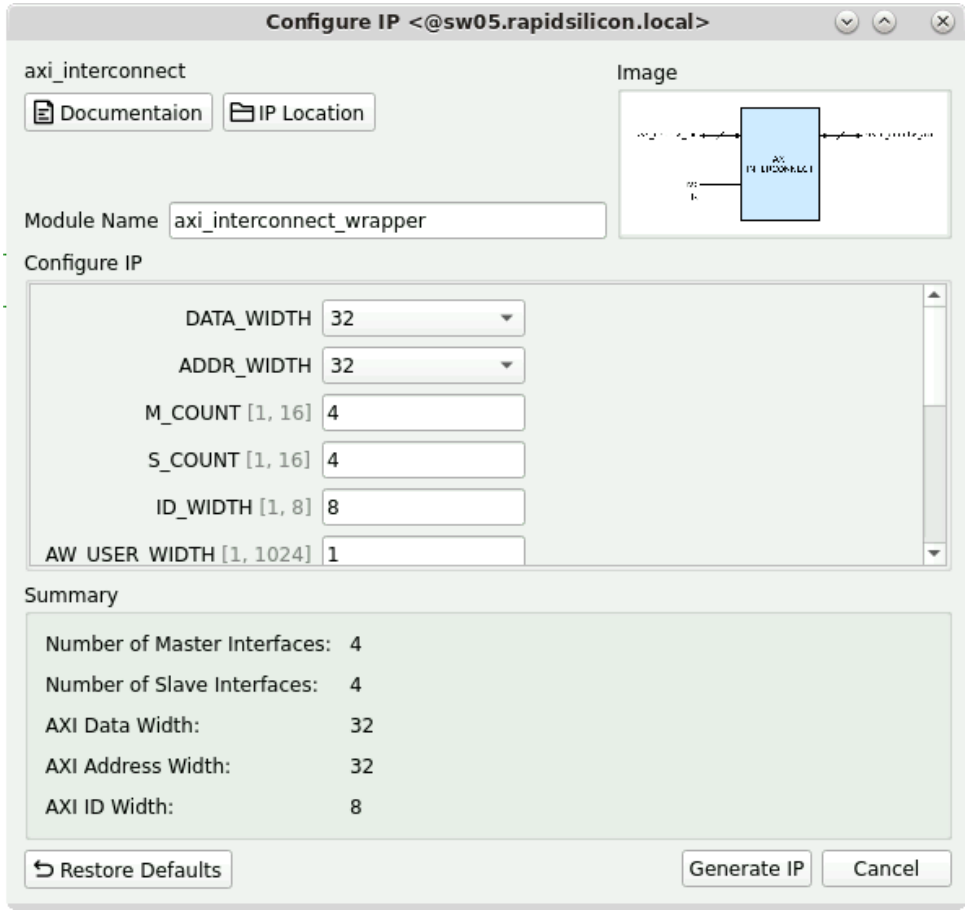

Figure 5: IP Configuration

Test Bench

The AXI4 interconnect IP Core is provided with a testbench which is based upon Cocotb verification environment. For simulation, right click on generated IP Instance and then click "Simulate IP" as shown in Figure 6.

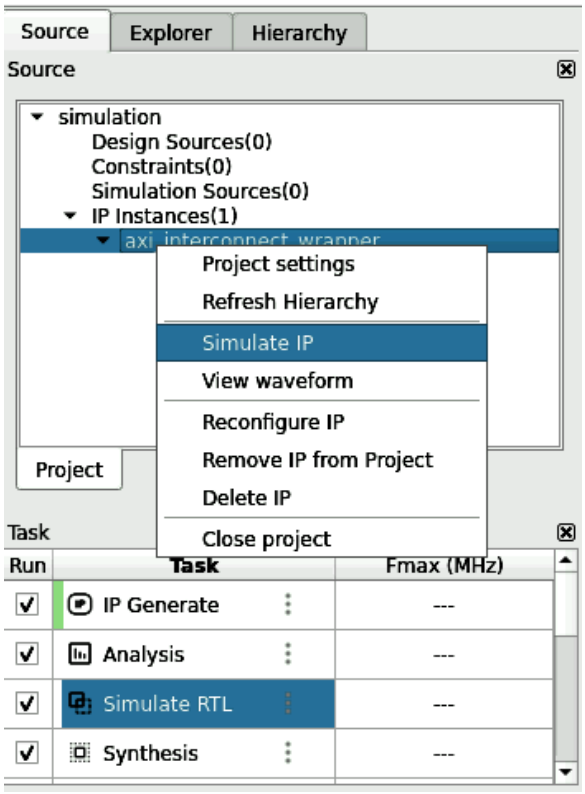

Figure 6: Simulate IP

In this test, four masters ad four slaves are connected to interconnect. Interconnect assigns fixed address space to each slave. Each master communicate with each slave. The input data is generated using a test data generator module. Input data is routed from master to slave through interconnect. After running the simulation, you'll get pass/ fail status on console. The status of test is shown in Figure 7.

```
** test_axi_interconnect.run_test_write_010    PASS       91420.00          9.78       9348.02  **
** test_axi_interconnect.run_test_write_011    PASS       91420.00          9.64       9480.31  **
** test_axi_interconnect.run_test_write_012    PASS       91420.00          9.70       9425.12  **
** test_axi_interconnect.run_test_write_013    PASS       95850.00         11.19       8562.70  **
** test_axi_interconnect.run_test_write_014    PASS       95850.00         11.11       8628.90  **
** test_axi_interconnect.run_test_write_015    PASS       95850.00         11.12       8617.64  **
** test_axi_interconnect.run_test_write_016    PASS       95850.00         11.13       8612.59  **
** test_axi_interconnect.run_test_read_001     PASS       28220.00          3.01       9385.29  **
** test_axi_interconnect.run_test_read_002     PASS       28220.00          3.01       9372.98  **
** test_axi_interconnect.run_test_read_003     PASS       28220.00          3.01       9378.30  **
** test_axi_interconnect.run_test_read_004     PASS       28220.00          3.02       9334.54  **
** test_axi_interconnect.run_test_read_005     PASS       92290.00          9.79       9427.66  **
** test_axi_interconnect.run_test_read_006     PASS       92290.00          9.85       9373.13  **
** test_axi_interconnect.run_test_read_007     PASS       92290.00          9.88       9336.93  **
** test_axi_interconnect.run_test_read_008     PASS       92290.00          9.82       9398.33  **
** test_axi_interconnect.run_test_read_009     PASS       92300.00          9.74       9477.86  **
** test_axi_interconnect.run_test_read_010     PASS       92300.00          9.80       9423.12  **
** test_axi_interconnect.run_test_read_011     PASS       92300.00          9.83       9388.08  **
** test_axi_interconnect.run_test_read_012     PASS       92300.00          9.81       9405.05  **
** test_axi_interconnect.run_test_read_013     PASS       95850.00         11.28       8494.54  **
** test_axi_interconnect.run_test_read_014     PASS       95850.00         11.29       8489.60  **
** test_axi_interconnect.run_test_read_015     PASS       95850.00         11.31       8473.20  **
** test_axi_interconnect.run_test_read_016     PASS       95850.00         11.22       8539.83  **
** test_axi_interconnect.run_stress_test_001   PASS      361340.00         35.86      10076.48  **
**************************************************************************************************
** TESTS=33 PASS=33 FAIL=0 SKIP=0                    2827090.03        307.29       9200.19  **
**************************************************************************************************
```

Figure 7: Simulation Results

You can view waveform of the results. To view waveform, right click on generated IP Instance and then click "View waveform" as shown in Figure 8.

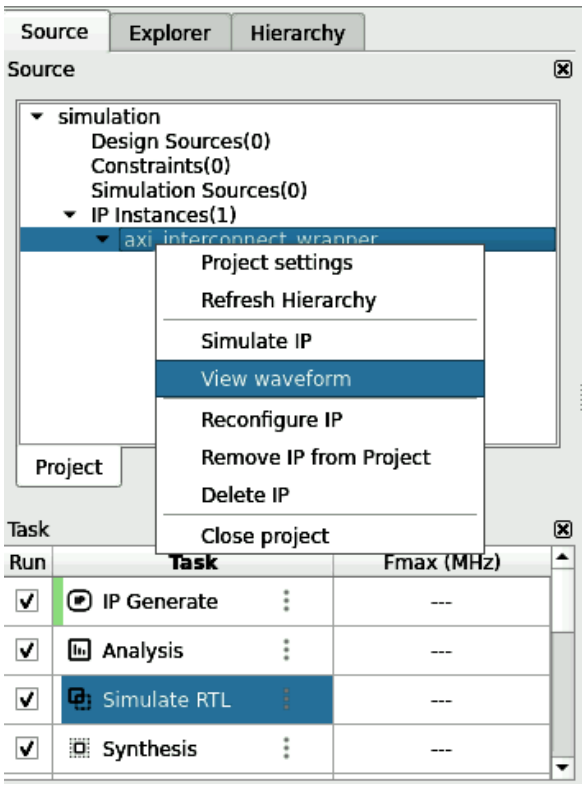

Figure 8: View Waveform

Revision History

Date	Version	Revisions
November 20, 2023	0.1	Initial version AXI4 Interconnect User Guide