Boot Clock IP V1.0

IP User Guide(Beta Release)

November 29, 2023

RapidSilicon

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Licensing

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IP Specification

Overview

Boot Clock IP

Boot Clock is added as an oscillator IP in IP Catalog.This IP module is designed to generate an initial clock signal upon system power-up or reset, contributing to the proper configuration and activation of essential components within the device. The oscillator functionality embedded in the boot clock IP ensures the delivery of a precise and consistent clock signal, allowing for the orderly execution of boot code, initialization routines, and subsequent system operations.

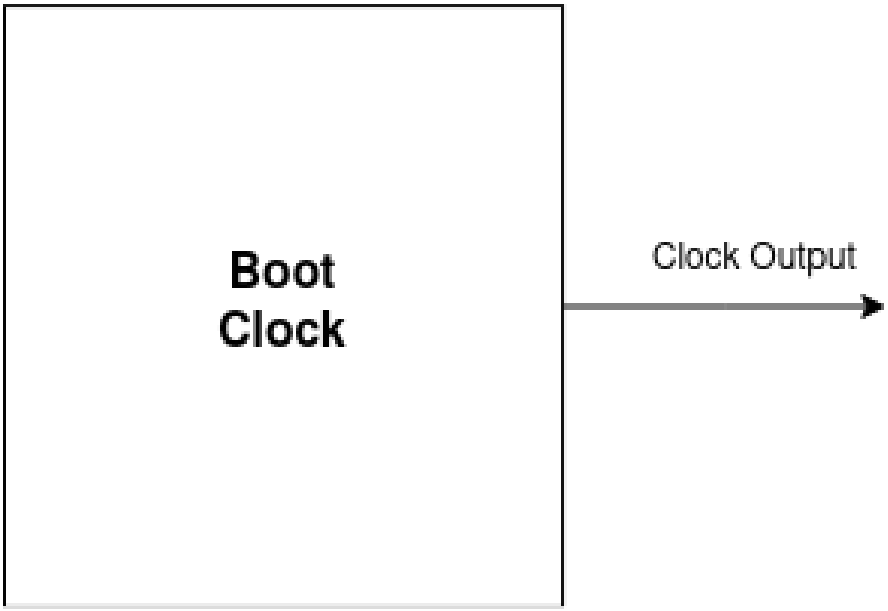


Figure 1. Boot Clock IP Block

Features:

- Generates parameterizable frequency
  generation for peripherals and interconnects

IP Support Details

Compliance		IP Resources					Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Software Driver**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI4-lite	Verilog	-	<verilog	-	-	Raptor	Raptor	Raptor

Resource Utilization

Please note that the utilization and timing figures provided in this section for the Processor Boot clock IP core should be considered as estimates, as they are based on its usage in conjunction with other design modules in the FPGA. Once integrated with other designs in the system, the FPGA resource utilization and core timing may differ from the reported results.

Ports

Table 2 lists the top interface ports of the Boot Clock Core.

Signal Name	I/O	Description
O	O	Output clock generated

Boot Clock Interface

Parameters

Table 3 lists the parameters of the Boot Clock Core.

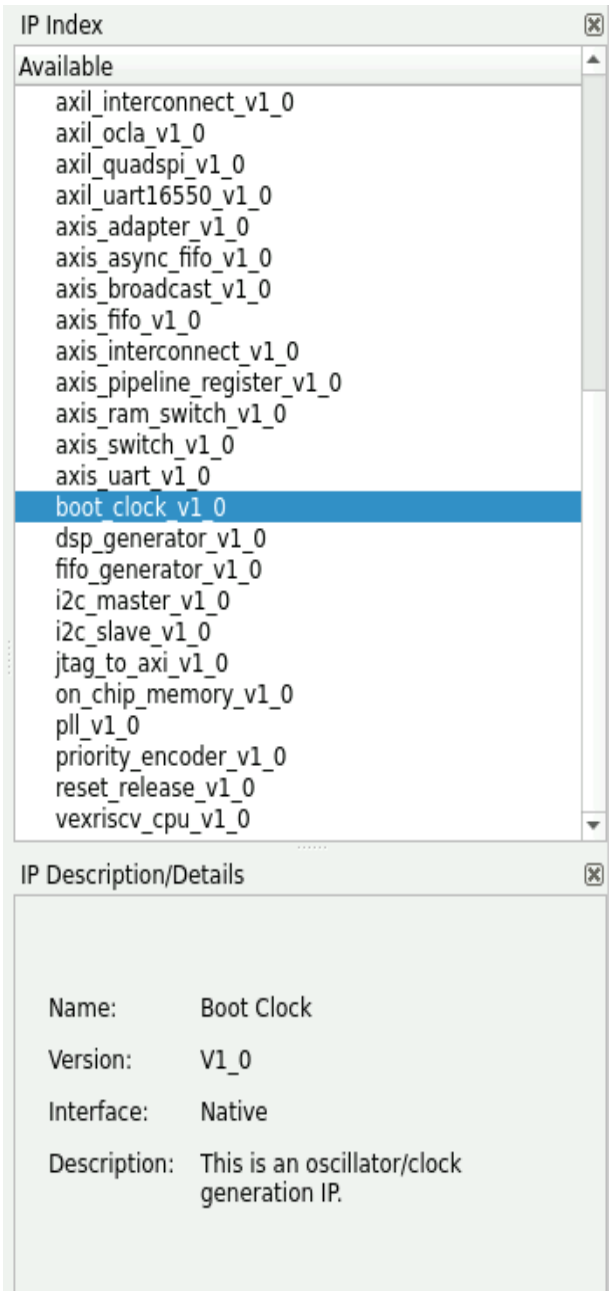
Parameter	Values	Default Value	Description
Period	25	25	Period of clock.

Parameters

Design Flow

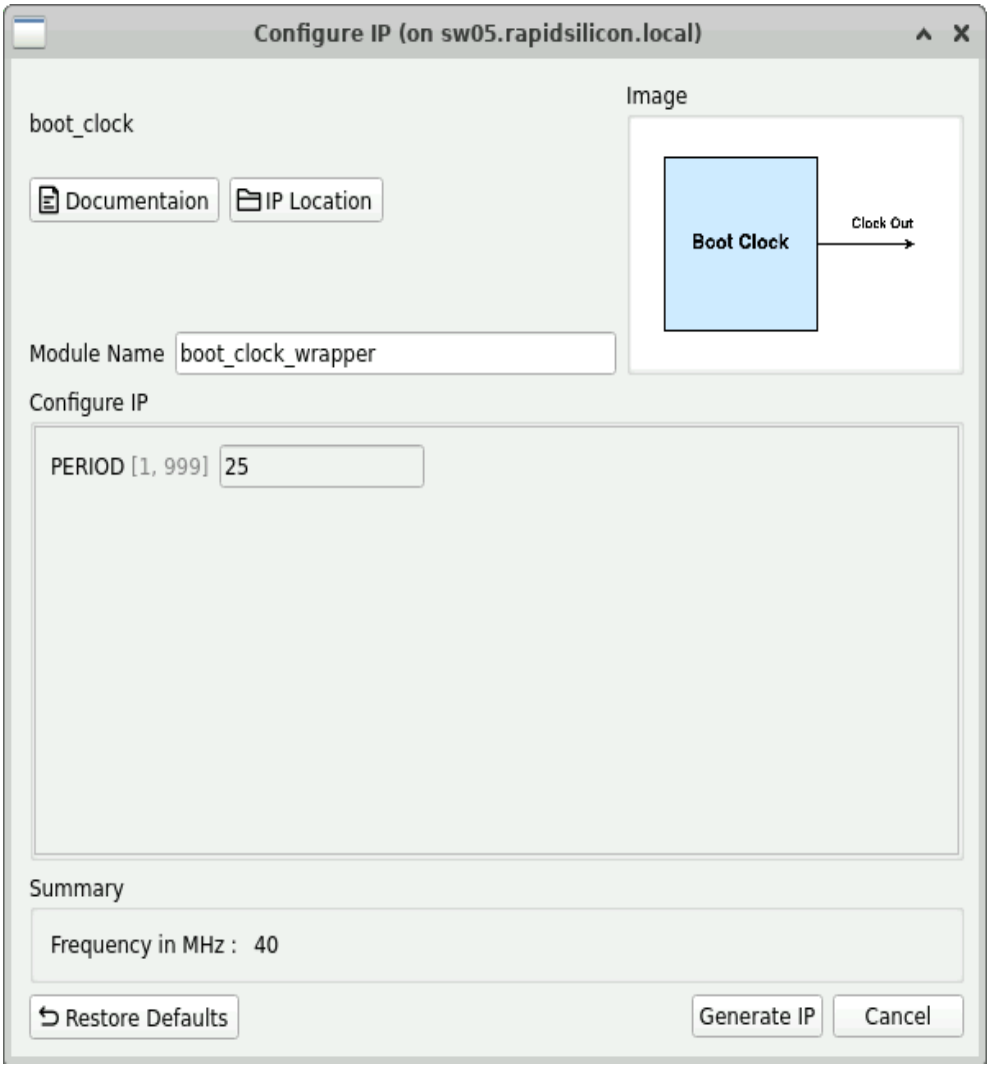
IP Customization and Generation

Boot Clock IP core is a part of the Raptor Design Suite Software. A customized Boot Clock can be generated from the Raptor's IP configurator window.



IP list

Parameters Customization: From the IP configuration window, the parameters of the Boot Clock IP can be configured and Boot Clock IP features can be enabled for generating a customized Boot Clock IP core that suits the user application requirement.



IP Configuration

Synthesis and PnR

Raptor Suite is armed with tools for Synthesis along with Post and Route capabilities and the generated post-synthesis and post-route and place netlists can be viewed and analyzed from within the Raptor. The generated bitstream can then be uploaded on an FPGA device to be utilized in hardware application.

Test Bench

Simulation currently not supported in Raptor.

Revision History

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Date	Version	Revisions
November 29, 2023	0.01	Initial version Boot Clock IP User Guide