AXI4 Lite Cross-bar v2.0

***IP User Guide** (Beta Release)*

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Contents

IP Summary

Introduction

The AXI4 Lite Crossbar is AXI4 compliance IP core that connects one or more AXI memory mapped master devices to more memory mapped slave devices. Each connected master could be a core that originates AXI transication while each connected slave could be the final target of AXI transactions or a slave interface of a downstream AXI Crossbar Lite core being cascaded.
This core support multiple clock feature, where different masters and slaves running on different clocks can communicate with each other.

Features

- Address width: Up to 256 bits
- Data width: 8, 16, 32, 64, 128, 256 bits
- Multi clock support
- Support Concurrent transactions

Overview

AXI4 Lite Crossbar

The IP has Slave and Master interfaces through which different masters and slaves devices communicate with each other. The Slave Interface of AXI4 Lite Crossbar core can be configured to comprise 1-4 Slave Interface slots to accept transactions from up to 4 connected master devices. The Master interface can be configured to comprise 1-4 Master Interface slots to issue transactions to up to 4 connected slave devices . All master and slave connected through this core can operate on different frequencies while the IP is responsible for clock conversion between these interfaces. The figure 1 shows the crossbar IP connecting multiple masters and slaves.

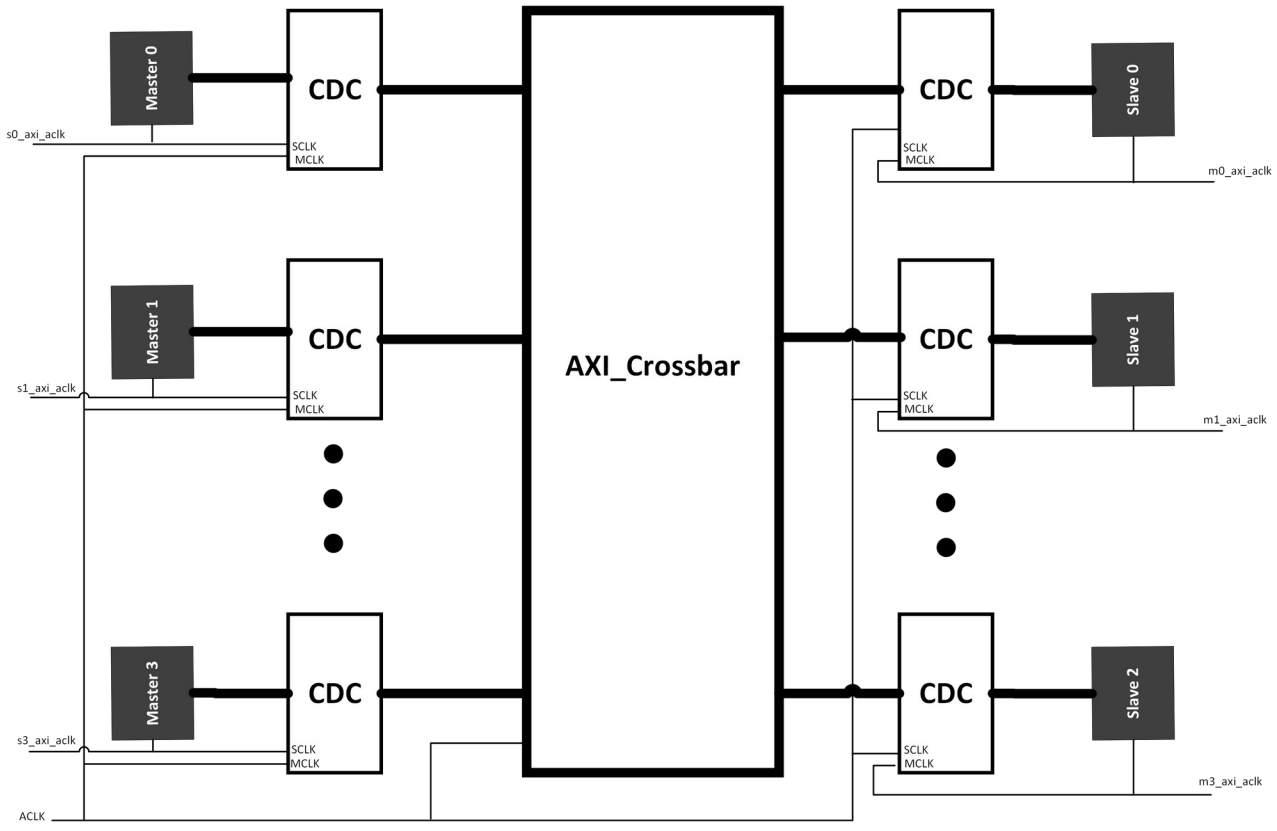


Figure 1. AXI4 Lite Crossbar connecting multiples Masters and Slaves

Licensing

IP Specification

Overview

The figure 2 shows the top level block diagram of AXI4 Lite Crossbar. Where multiple masters and slaves are connected. A maximum of 4 masters and 4 slaves can be connected with one crossbar instance. Each interface has its own CDC(Clock Domain Crossing) block for multi clock support. Inside the top the write and read channels has separate instance. All the write channels are connected with AXI Crossbar Lite Write instance while all read channels are connected with AXI Crossbar Lite Read instance. Both the write and read instance consists of a single, vectored AXI Slave Interface, plus a single, vectored AXI Master Interface. Each vectored interface can be configured to connect between 1 and 4 master/slave devices. The pathways connecting to all the master interfaces of the CDC block are merged together to connect to the vectored slave Interface of the write and read instance. The pathways connecting to all the slave interfaces of the CDC block are merged together to connect to the vectored master Interface of the write and read instance.
For each signal comprising a vectored AXI interface on the write and read instance, its natural width is multiplied by the number of devices to which it is connected.

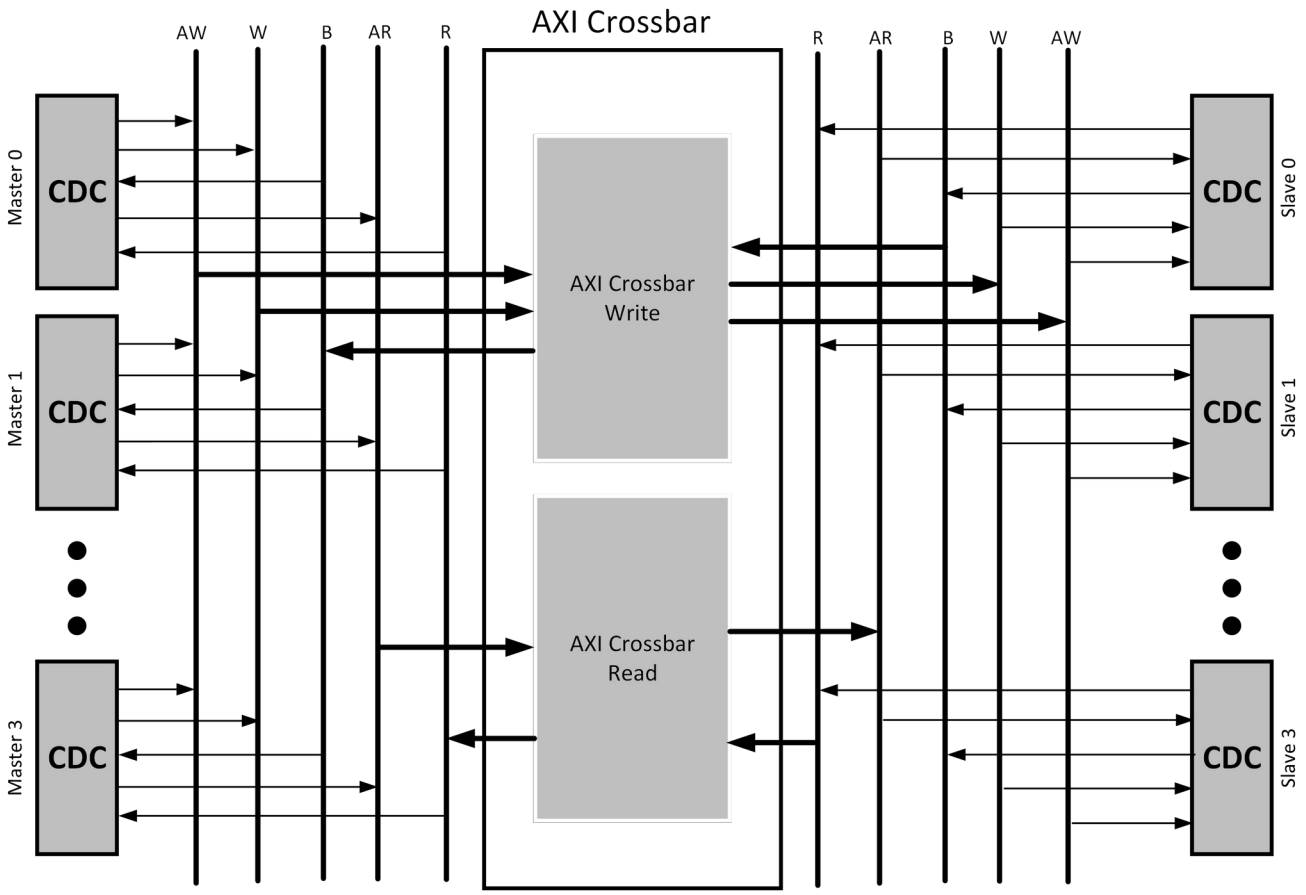


Figure 2. Top Module

Apart from CDC the core has sub modules including address decoder, priority encoder and arbiter. These modules are responsible for address decoding, setting priorities for transactions and arbitration.

Address Decoder

The figure 3 shows the block diagram of Address Decoder. The AXI4 Lite Crossbar core must determine which Master Interface is the target of each transaction by decoding the address of each Address Write channel and Address Read channel transaction from the Slave Interface slot. So the address decoder assign address space to each Master Interfcae and maintain a table called address table. The address decoder also check the address space configuration to make sure that there is no overlapping of addresses and all addresses are alligned. This address table is then used by the address decoder during address decoding. The address decoder follows certian rules while assigning address space to each master interface.
Whenever a transaction address receive on the Slave Interface does not match any of the ranges being decoded by the Address deocer, the transcation is trapped and handled by a decoded error module. In such conditios the Crossbar generates a protocol compliant response back to the master which originate the transaction with the response code (DECERR), which means that their is no slave available among this address range.

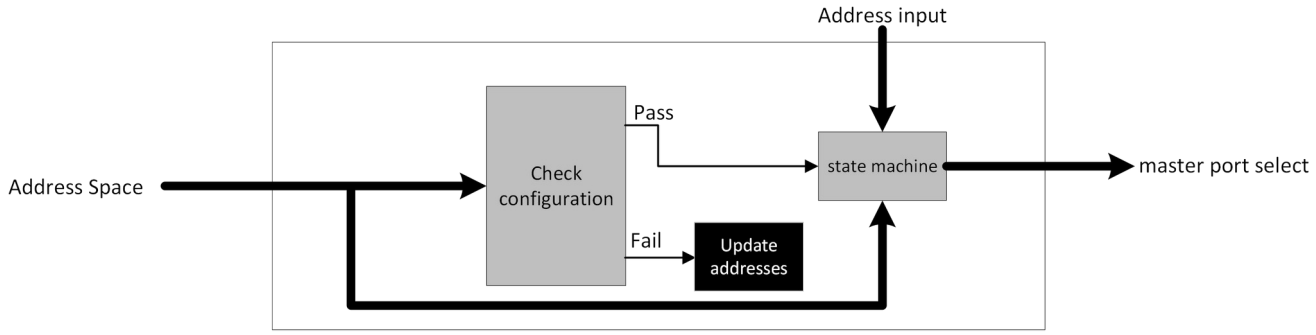


Figure 3. Address Decoder

Clock Domain Crossing

The AXI4 Lite Crossbar top wrapper has one main clock ACLK while each master and slave interface has its own clock signals as shown in figure 1. As each CDC has two clocks, one is master clock and one is slave clock as shown in figure 4. The CDC block at slave interface shares master clock with Crossbar Lite core while the CDC slave clock will be shared with master device. Similarly CDC block at master interface shares slave clock with Crossbar core while the CDC master clock will be shared with slave device. This feature allow that all the masters and slaves connected through the core can operate on different frequencies.
The CDC block is basically based on asynchronous FIFO, which has two seperate clock domain for write and read operations. Each cahnnel has its seperate FIFO instance. All the channel signals are passing through the CDC FIFO, which has two gray coded counters, one for pushing the FIFO in one clock domain while one is for popping from the FIFO in the other clock domain. The handshaking signals (VALID, READY) are used for status, writing to and reading form the FIFO. The figure 4 shows the block diagram of Clock Domain Crossing module.

Standards

The AXI4 Lite Master and Slave interfaces are compliant with the AMBA® AXI Protocol Specification.

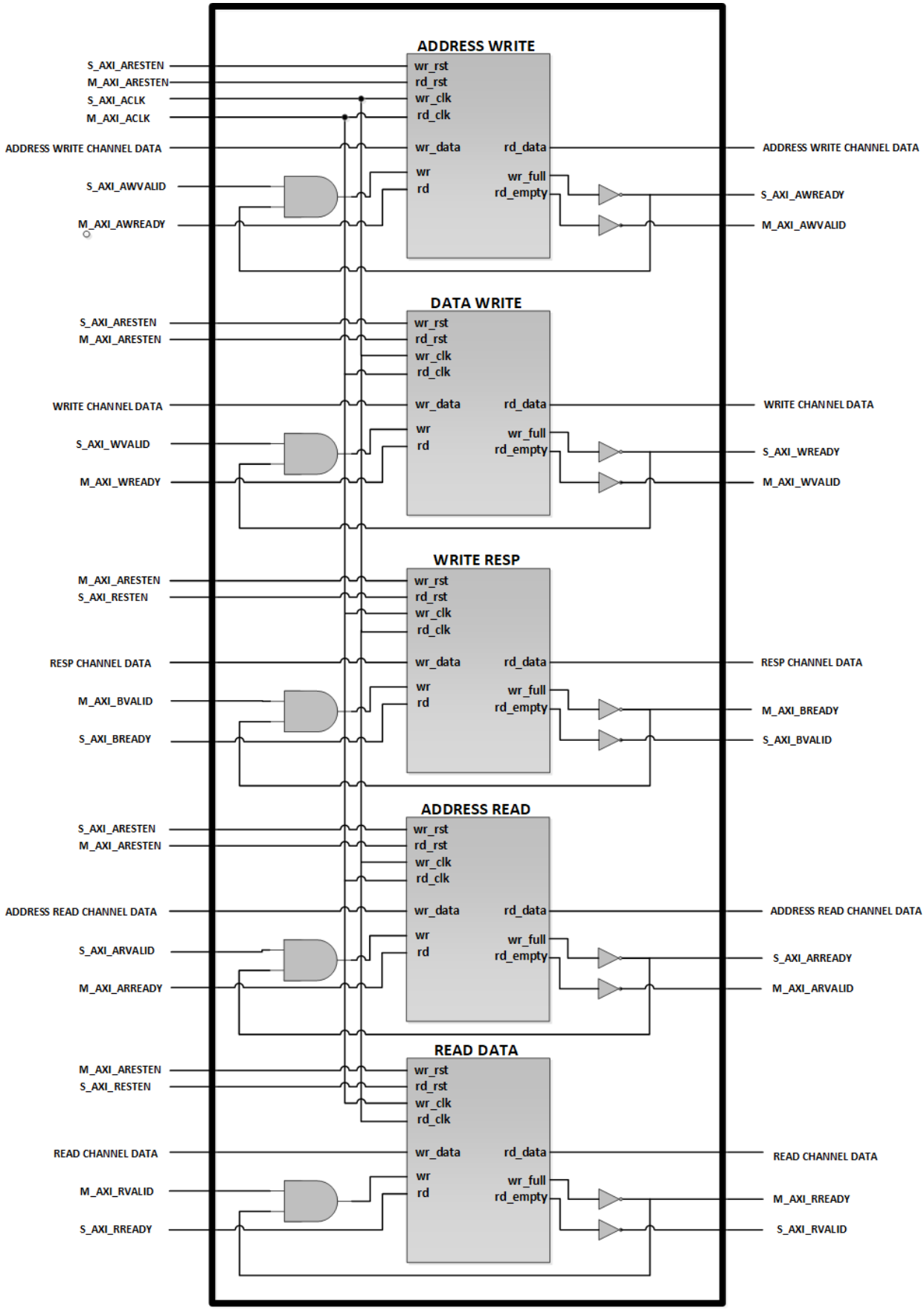


Figure 4. CDC Block Diagram

IP Support Details

Compliance		IP Resources					Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Software Driver**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI4 Lite	Verilog	SDC	Cocotb	-	-	Raptor	Raptor	Raptor

Resource Utilization

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	Number of slave Interface	1	LUT	775
			DFF	734
	Number of master Interface	1	BRAM	0
	BRAM Enable	No	DSP	0
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	Number of slave Interface	4	LUT	3209
			DFF	5709
	Number of master Interface	4	BRAM	0
	BRAM Enable	No	DSP	0

Ports

Table 2 lists the top Slave Interface ports of the AXI4 Lite Crossbar.

Signal Name	I/O	Description
AXI Clock and Reset		
ACLK	I	AXI4 Source Clock
ARESET	I	AXI4 Active High RESET
AXI WRITE ADDRESS CHANNEL		
s<nn>_axi_awaddr	I	Write address
s<nn>_axi_awprot	I	Write protection level
s<nn>_axi_awvalid	I	Write address valid
s<nn>_axi_awready	O	Write address ready (from slave)
AXI WRITE DATA CHANNEL		
s<nn>_axi_wdata	I	Write data
s<nn>_axi_wstrb	I	Write data strobe (byte select)
s<nn>_axi_wvalid	I	Write data valid
s<nn>_axi_wready	O	Write data ready (from slave)
AXI WRITE RESPONSE CHANNEL		
s<nn>_axi_bresp	O	Write response
s<nn>_axi_bvalid	O	Write response valid
s<nn>_axi_bready	I	Write response ready (from master)
AXI READ ADDRESS CHANNEL		
s<nn>_axi_araddr	I	Read address
s<nn>_axi_arprot	I	Read protection level
s<nn>_axi_arvalid	I	Read address valid
s<nn>_axi_arready	O	Read address ready (from slave)
AXI READ DATA CHANNEL		
s<nn>_axi_rdata	O	Read data
s<nn>_axi_rresp	O	Read response
s<nn>_axi_rvalid	O	Read response valid
s<nn>_axi_rready	I	Read response ready (from master)

Table 2: Crossbar Slave

Interface NOTE: The <nn> shows the number of slave interface.

Table 4 lists the top Master Interface ports of the AXI4 Lite Crossbar.

Signal Name	I/O	Description
AXI WRITE ADDRESS CHANNEL		
m<nn>_axi_awaddr	O	Write address
m<nn>_axi_awprot	O	Write protection level
m<nn>_axi_awvalid	O	Write address valid
m<nn>_axi_awready	I	Write address ready
AXI WRITE DATA CHANNEL		
m<nn>_axi_wdata	O	Write data
m<nn>_axi_wstrb	O	Write data strobe (byte select)

m<nn>_axi_wvalid	O	Write data valid
m<nn>_axi_wready	I	Write data ready
AXI WRITE RESPONSE CHANNEL		
m<nn>_axi_bresp	I	Write response
m<nn>_axi_bvalid	I	Write response valid
m<nn>_axi_bready	O	Write response ready
AXI READ ADDRESS CHANNEL		
m<nn>_axi_araddr	O	Read address
m<nn>_axi_arprot	O	Read protection level
m<nn>_axi_arvalid	O	Read address valid
m<nn>_axi_arready	I	Read address ready
AXI READ DATA CHANNEL		
m<nn>_axi_rdata	I	Read data
m<nn>_axi_rresp	I	Read response
m<nn>_axi_rvalid	I	Read response valid
m<nn>_axi_rready	O	Read response ready (from master)

Table 4: Crossbar Master Interface

NOTE: The <nn> shows the number of master interface.

Parameters

The AXI4 Lite Crossbar has set of parametes which are available to user. These parameters include data width, address width, master count, slave count and BRAM. Data width and address width define the size of data and address bus respectively. User can select from 8 up to 256bits data size, wheres address can be configured either 32 bits or 64 bits. The M Count and S Count parameters enable the total number of master and slave interfaces. The BRAM option is enabled by default. This parameter basically controll the type of memory used by the CDC block. Table 5 lists the parameters of the AXI4 Lite Crossbar.

Parameter	Values	Default Value	Description
Data Width	8-256	32	Define size of data for Data channel
Address Width	32, 64, 128,256	32	Define size of address for Address channel
M Count	2,3,4	4	Total number of master ports.
S Count	2,3,4	4	Total number of slave ports.
BRAM	1,0	1	Set to 1 to use BRAM. Set to 0 to use Distributed RAM

Table 5: Parameters List

Maximum Performance

This section summarize the estimated maximum performance for AXI4 Lite Crossbar with different number of master and slave interfaces. These frequencies are measured after running the design on Raptor in standalone mode. Table 6 shows the maximum performance results.

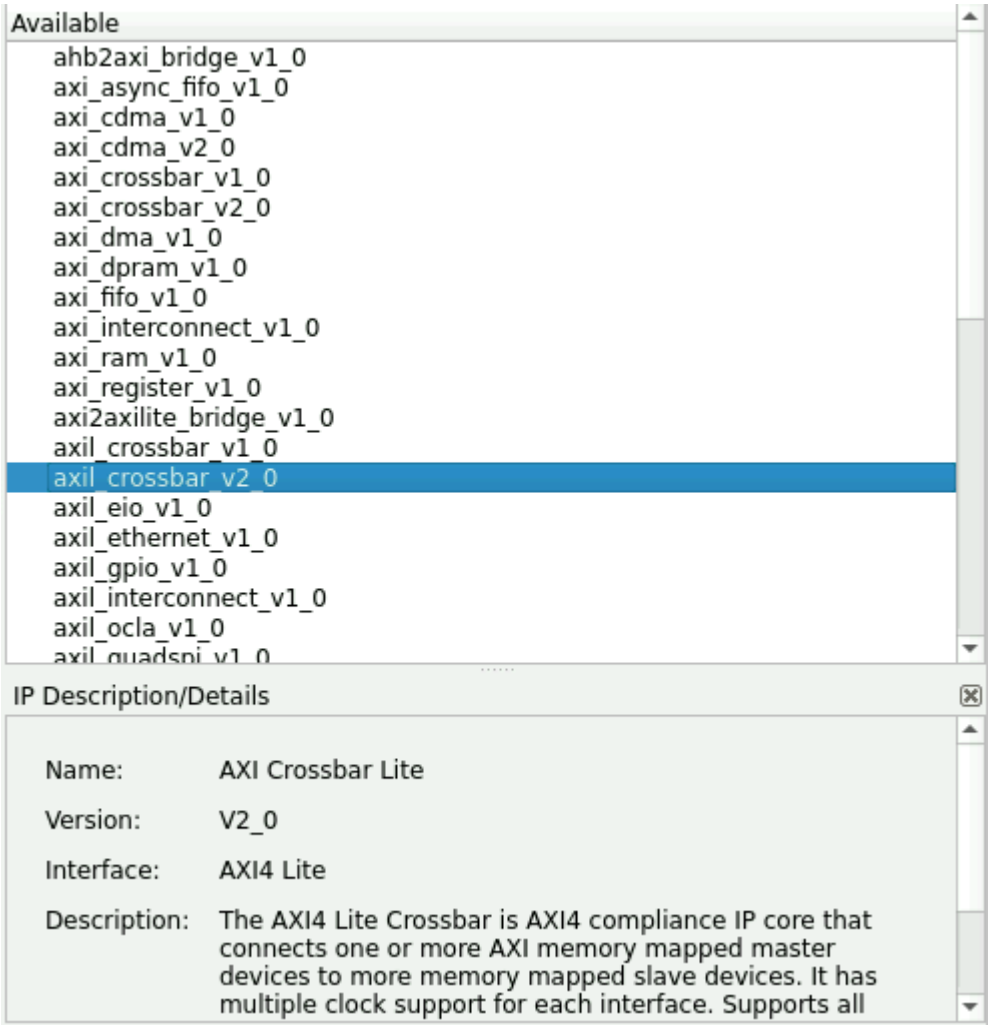
Number of Slave Interface	Number of Master Interface		
	2	3	4
1	250 MHz	—	—
2	200 MHz	—	—
3	197 MHz	180 MHz	—
4	197MHz	—	170 MHz

Table 6: AXI4 Crossbar Lite Performance (MHz) on GEMINI

Design Flow

IP Customization and Generation

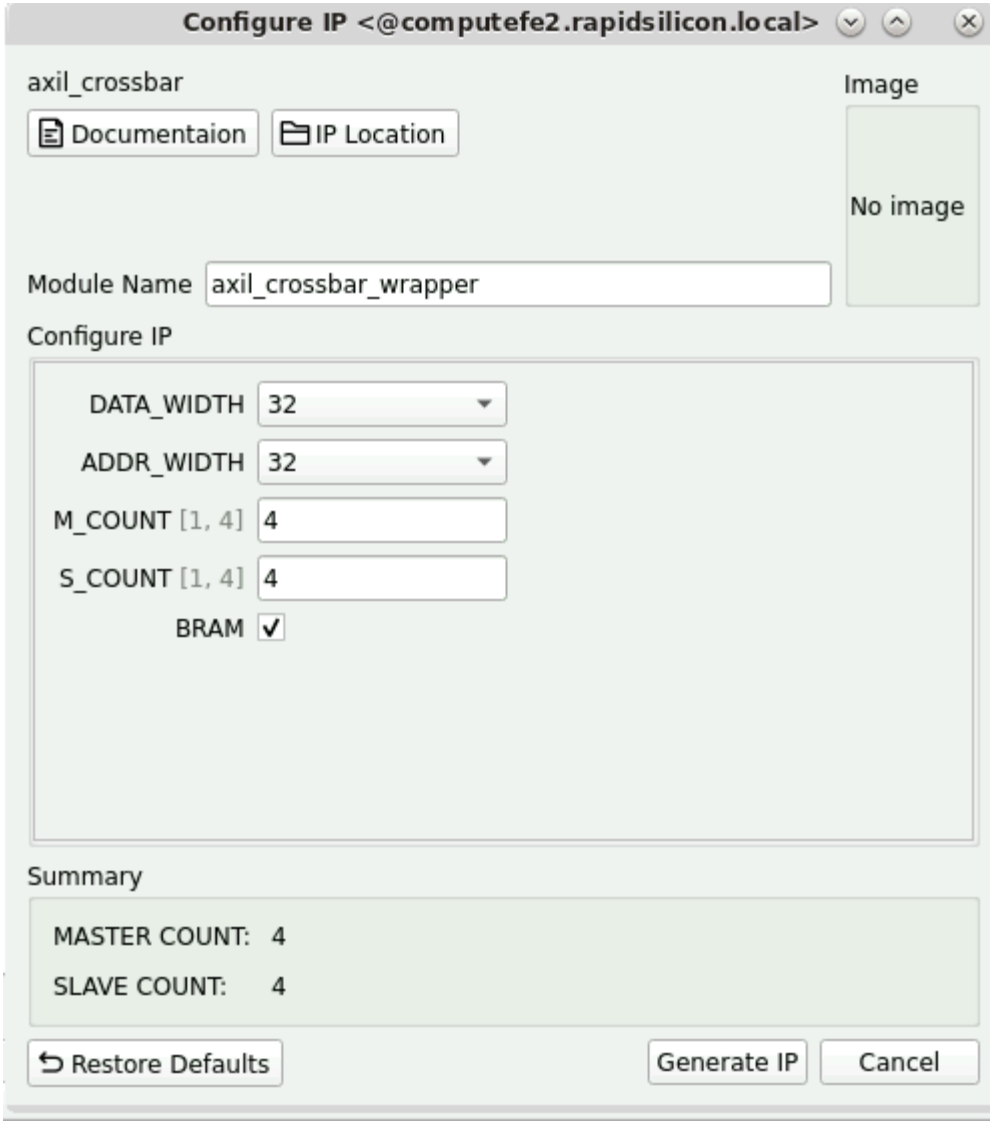
AXI4 Lite Crossbar IP is a part of the Raptor Design Suite Software. A customized IP can be generated from the Raptor's IP configurator window. First enable IP Configurator and then select the axil_crossbar_v2_0 IP from the IP list.



IP list

Single click on the IP will show details of the IP as shown in above figure.

Parameters Customization: Double click on the IP will open the IP configurator window as shown in figure below. From the IP configuration window, the parameters of the IP can be configured and AXI4 Lite Crossbar features can be enabled for generating a customized IP core that suits the user application requirement.



IP Configuration

Once all fields are configured, select Generate IP.

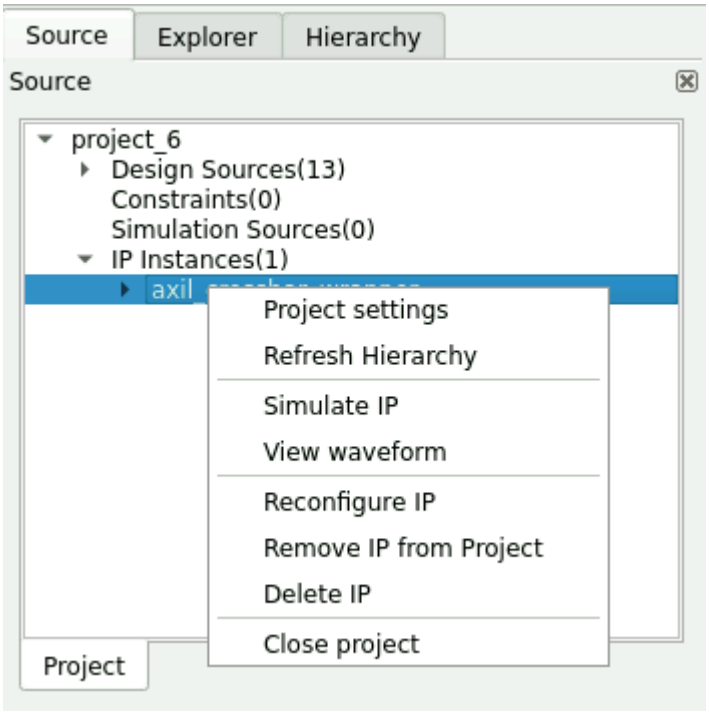
After the IP customization and generation step, a top wrapper plus all source files are made available to the user. Now user can add all the source files to project to use it at system level.

Test Bench

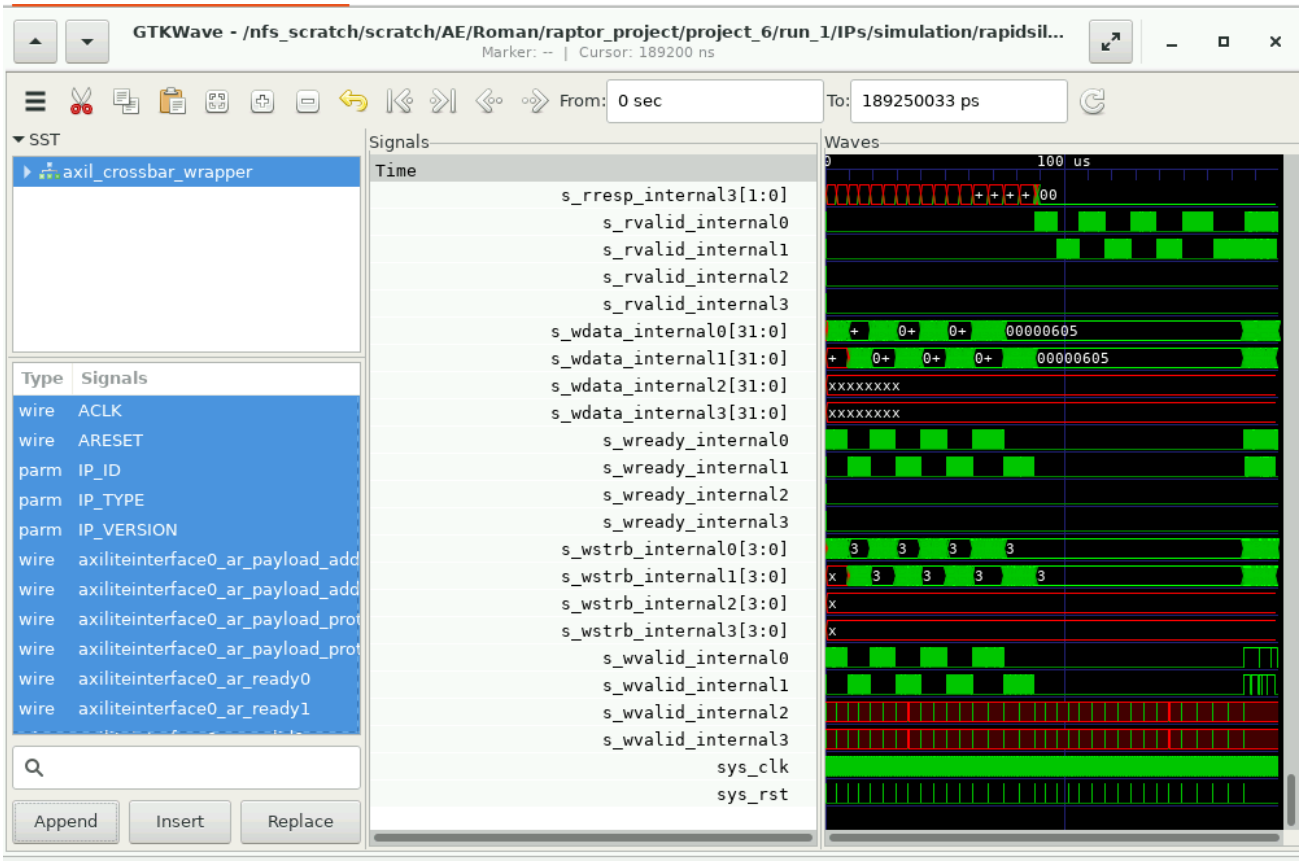
To check the behavior of the IP Core, a cocotb test-bench with basics configuration is available for simulation. Once the IP is generated then test-bench file can be found in the IP directory under sim folder.

Follow the steps below to simulate the IP:

1. Right click on the IP name within source tab and select Simulate IP as shown in figure below.



2. This will run the simulation and result will dumped into vcd file.
3. To see the waveform, again right click on the IP and select View waveform. The GTKWave will open
4. showing the IP simulation result as shown in figure below.


GTKWave - /nfs_scratch/scratch/AE/Roman/raptor_project/project_6/run_1/IPs/simulation/rapidsil...
Marker: -- | Cursor: 189200 ns
From: 0 sec
To: 189250033 ps
SST
axil_crossbar_wrapper
Type Signals
wire ACLK
wire ARESET
parm IP_ID
parm IP_TYPE
parm IP_VERSION
wire axiliteinterface0_ar_payload_add
wire axiliteinterface0_ar_payload_add
wire axiliteinterface0_ar_payload_prot
wire axiliteinterface0_ar_payload_prot
wire axiliteinterface0_ar_ready0
wire axiliteinterface0_ar_ready1
Append
Insert
Replace
Signals
Time
s_rresp_internal3[1:0]
s_rvalid_internal0
s_rvalid_internal1
s_rvalid_internal2
s_rvalid_internal3
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s_wdata_internal2[31:0]
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s_wvalid_internal2
s_wvalid_internal3
sys_clk
sys_rst
Waves
100 us
00000605
00000605
xxxxxxxx
xxxxxxxx

Revision History

Date	Version	Revisions
November 20, 2023	0.01	Initial version of AXI4 Lite Crossbar User Guide Document