Temperature Sensor v1.0

***IP User Guide** (Beta Release)*

January 31, 2024

RapidSilicon

Contents

Licensing

IP Summary

Introduction

FPGAs performs high computational tasks due to which the internal temperature of FPGAs rises. So it is very important to monitor the physical operating conditions like temperature. This IP allow user to read the internal temperature of the fabric. The temperature value is updated after some interval. The temperature sensor IP is compliant with industry standard AXI bus protocol. So user can integrate it easily with the system to monitor the temperature.

Features

- AXI Lite bus support
- Configurable Data width
- Configurable Address width

Overview

Temperature Sensor

This IP allow user to read the temperature of FPGAs. The IP support the AXI Lite interface which make it easy for user to integrate the IP within the design. The IP has buffer that store the temperature reading at a specified interval. Once the data become available in the buffer, the IP assert the ready signal of the Read channel high which indicate that data is available for reading. Then user can read the buffer values through an AXI transition .

The figure 1 shows the top-level interface diagram of the Temperature Sensor IP core.

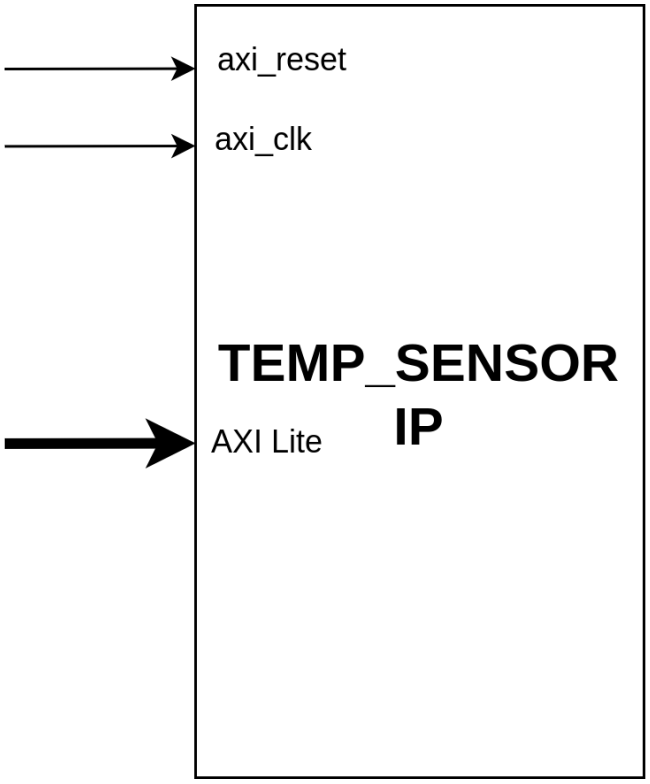


Figure 1. Temperature Sensor IP

IP Specification

The figure 2 presents block diagram of Temperature Sensor IP. The Soc_FPGA_TEMPERATURE block sense the temperature and store it in buffer as shown in figure below. On the other side user can read the buffer via AXI transication. Once the data is availble in the buffer, it notify the master that valid data is availble now.

Master cannot preform write transication to the IP and can perform read operation only.

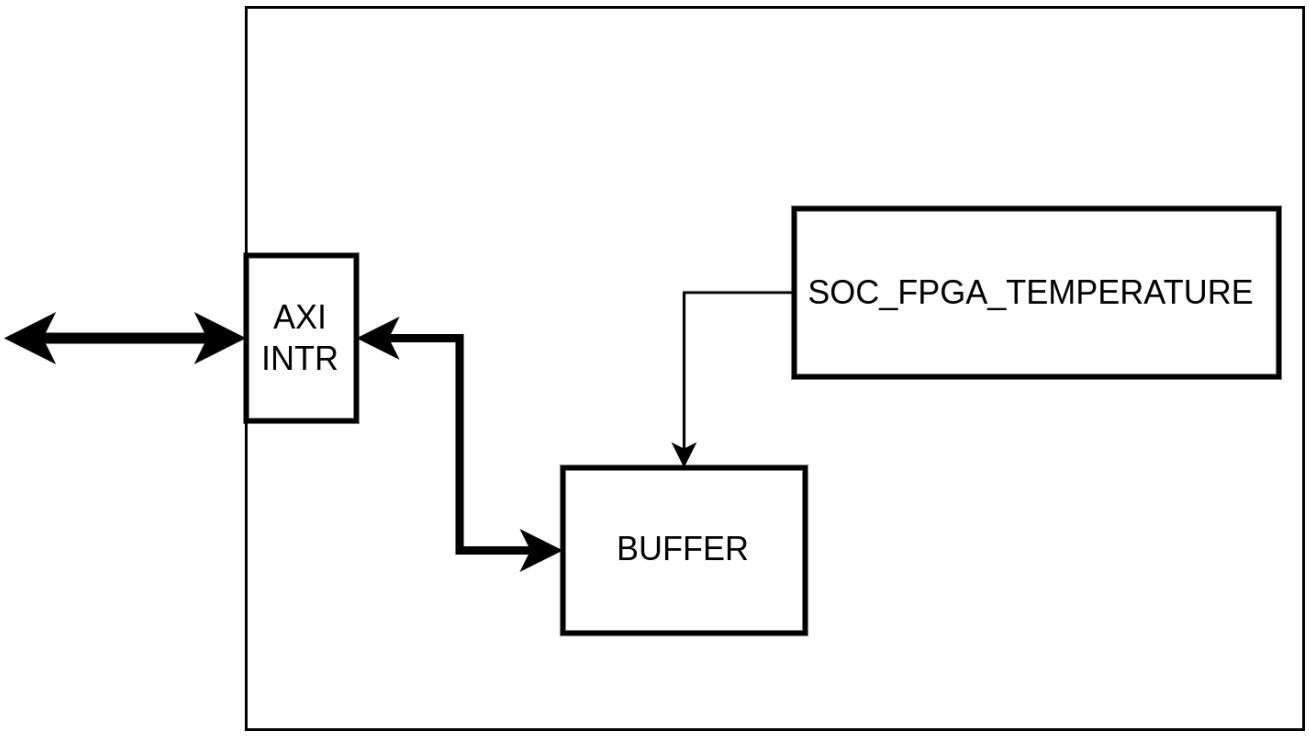


Figure 2. Temperature Sensor Block Diagram

Standards

The temperature values can be read via standarad AXI Lite interface.

IP Support Details

The table 1 presents the specifics of IP support for the Temperature Sensor IP Core, including pertinent information such as synthesis, simulation and source details.

Compliance		IP Resources					Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Software Driver**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
VIRGO	AXI Lite	Verilog	SDC	Supported	Supported	-	Raptor	Third Party	Raptor

Table 1. IP Information

Resource Utilization

The table 2 presents the resources utilization of temperature sensor IP for the VIRGO device within the Raptor Design Suite.

Resource Utillization		
Resource	Resources	Utillized
	LUTs	90
	FLOPS	113
	BRAM	0
	SOC_FPGA_TEMPERATURE	1

Table 2. Resource Utillization

Ports

Table 4 lists the top interface ports of the OCLA.

Signal Name	I/O	Description
Clock and Reset		
clk	I	AXI Clock.
rstn	I	System reset
Address Read Channel		
s_axil_arvalid	I	AXI4-Lite Read address valid
s_axil_arready	O	AXI4-Lite Read address ready
s_axil_araddr	I	AXI4-Lite Read address
s_axil_arprot	I	AXI4-Lite Protection type
Data Read Channel		
s_axil_rvalid	O	AXI4-Lite Read valid
s_axil_rready	I	AXI4-Lite Read ready
s_axil_rresp	O	AXI4-Lite Read response
s_axil_rdata	O	AXI4-Lite Read data

Table 4. IP Interface

Parameters

Table 4 lists the parameters of the OCLA.

Parameters	Values	Default Value	Description
IP_TYPE	"ocla"	"ocla"	Define IP Type
IP_VERSION	32'h00000001	32'h00000001	Define IP Version.
IP_ID	Auto Generated	Auto Generated	Define IP ID which will be generated by the IP generator at run time
DATA_WIDTH	8,16,32,64	32	Data Width for AXI bus

Table 4. Parameters

Registers Address Space

Table 6 lists the configuration registers of the Temperature Sensor IP.

Name	Register ID	Bits	Type	Off sets	Default Value	Description
IP Type Register	IP TYPE	32	RO	0x00	"TMPS"	This register hold the IP Type "TMPS"
IP Verison Register	IP VERSION	32	RO	0x04	"0x00000001"	This register hold the IP Version
IP ID Register	IP ID	32	RO	0x08	"0x03881734"	This register hold the IP ID
Sensor Data Register	TSDR	32	R	0x14	0x00000000	Temperature Sensor Data

Configuration Registers

Design Flow

IP Customization and Generation

Temperature Sensor IP core is a part of the Raptor Design Suite Software. A customized IP can be generated from the Raptor's IP configurator window.

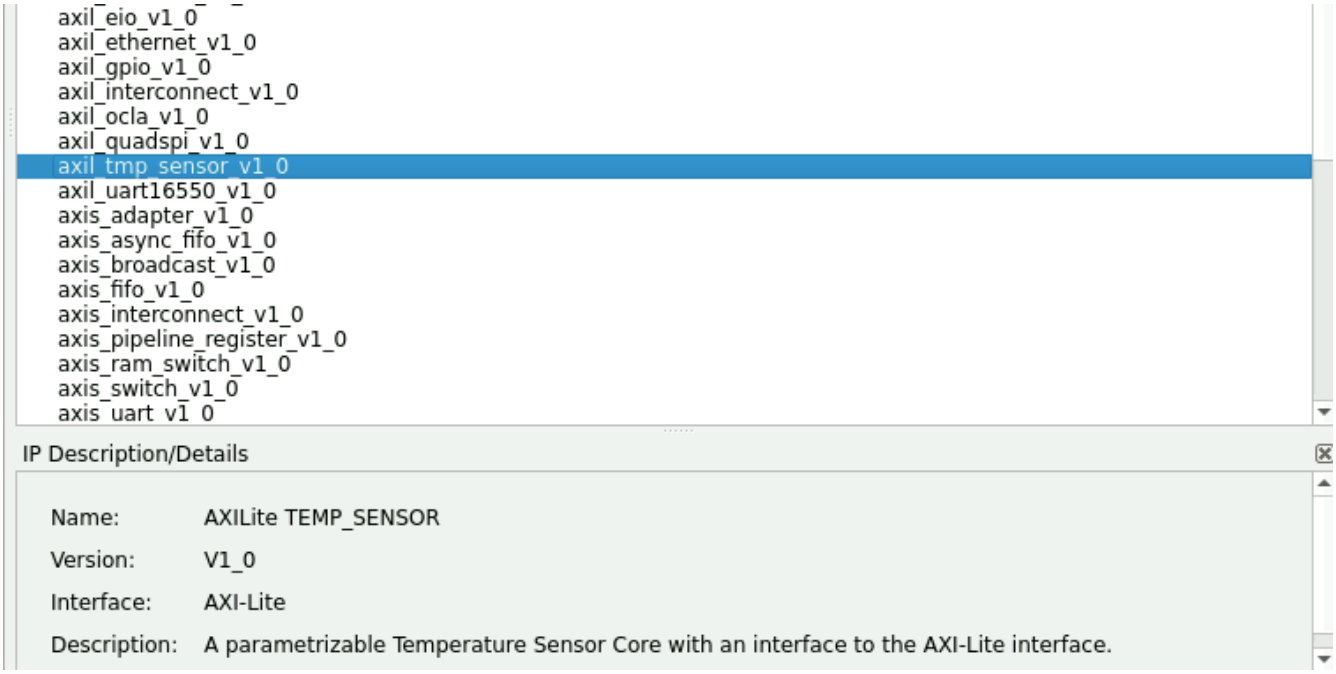


Figure 3. IP list

Parameters Customization: From the IP configuration window, the parameters of the IP can be configured for generating a customized IP core that suits the user application requirment.

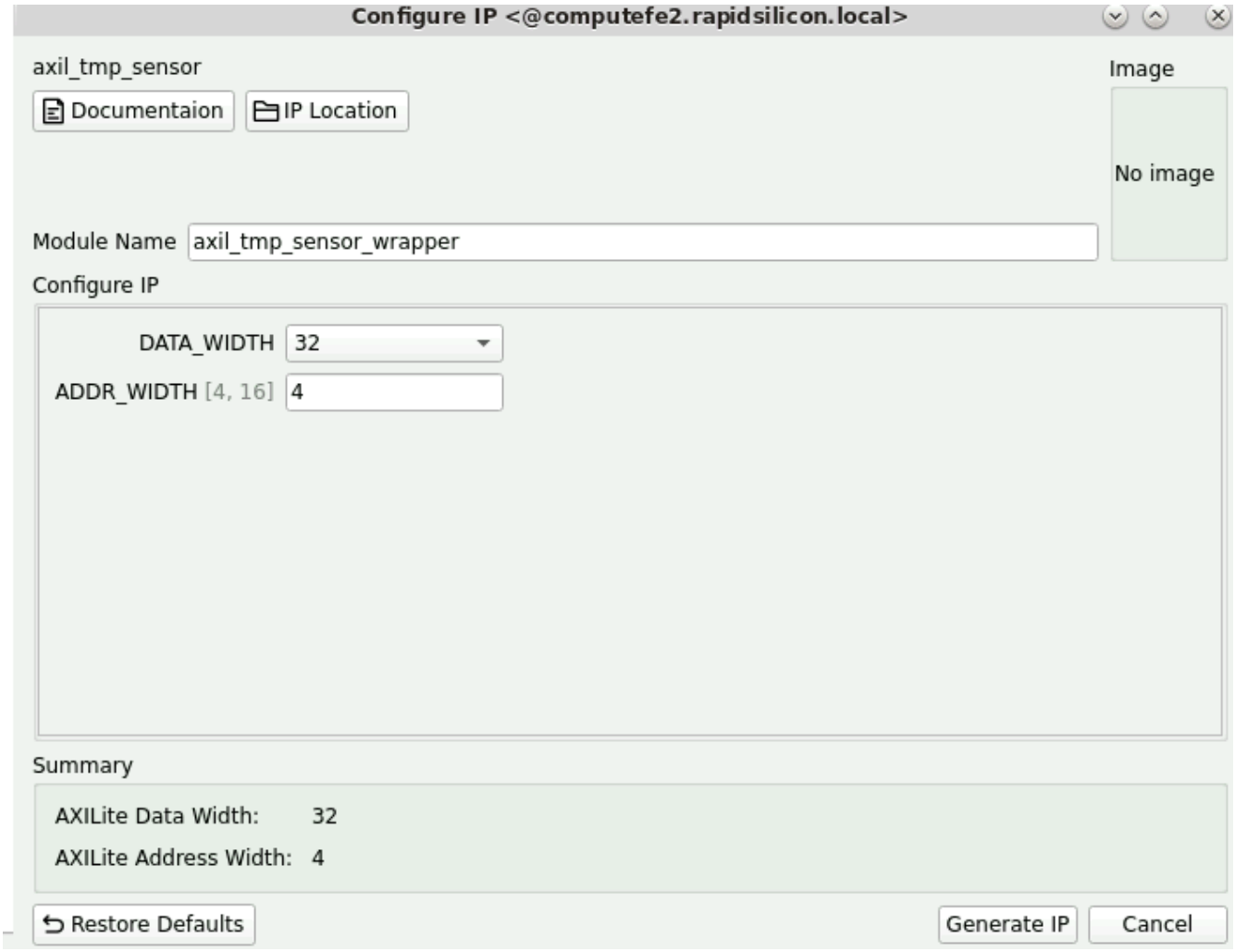


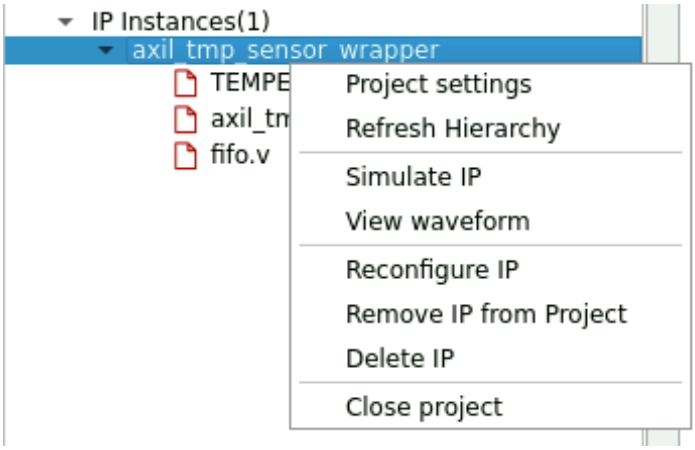
Figure 4. IP Configuration

Test Bench

To check the behavior of the IP Core, a verilog test-bench with basics configuration is available for simulation. Once the IP is generated then test-bench file can be found in the IP directory under sim folder.

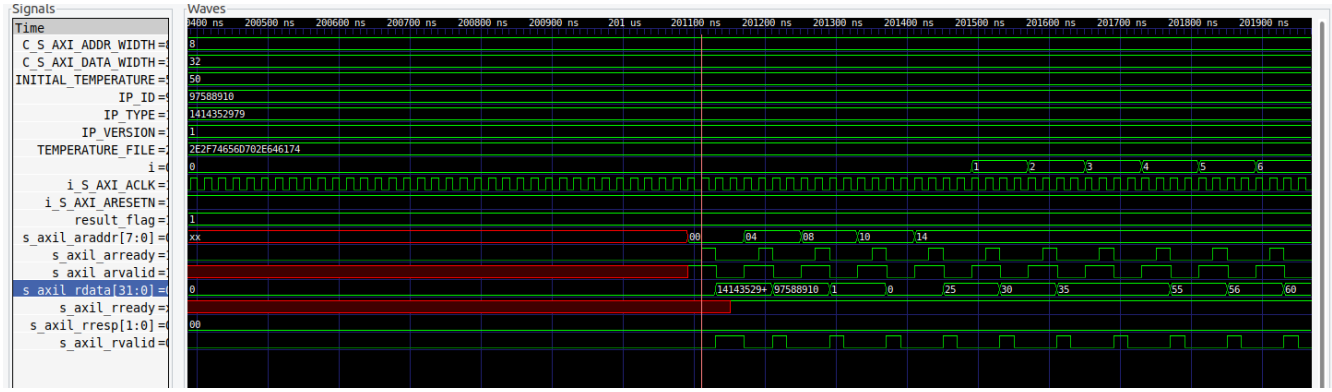
Running Simulation

1. Right click on the IP name within source tab and select Simulate IP as shown in figure below.



Running Simulation

2.This will run the simulation and result will dumped into vcd file.To see the waveform, again right click on the IP and select View waveform. The GTKWave will open showing the IP simulation result as shown in figure below.



Simulation Result

Revision History

Date	Version	Revisions
January 31, 2024	0.01	Initial version Temperature Sensor User Guide Document