**Behaviral Code**

Port ( a : in STD\_LOGIC\_VECTOR (3 downto 0);

b : in STD\_LOGIC\_VECTOR (3 downto 0);

Sel : in STD\_LOGIC\_VECTOR (3 downto 0);

Y : out STD\_LOGIC\_VECTOR (3 downto 0));

process(a,b,Sel)

begin

case Sel is

when "0010"=> Y<=a and b;

when "0011"=> Y<=a nand b;

when "0100"=> Y<=a xor b;

when "0101"=> Y<=a xnor b;

when "0110"=> Y<=a or b;

when "0111"=> Y<=a;

when "1000"=> Y<=b;

when others => Y<="0000";

end case;

end process;

**Testbench code**

-- hold reset state for 100 ns.

wait for 100 ns;

--wait for <clock>\_period\*10;

-- insert stimulus here

a<="1011";

b<="1001";

Sel<="0000";--Result of Addition

wait for 100 ns;

Sel<="0001";--Result of Subtraction

wait for 100 ns;

Sel<="0010";--Result of and

wait for 100 ns;

Sel<="0011";--Result of xor

wait for 100 ns;

Sel<="0100";--Result of xnor

wait for 100 ns;

Sel<="0101";--Result of or

wait for 100 ns;

Sel<="0111";--Value of a

wait for 100 ns;

Sel<="1000";--Value of b

wait for 100 ns;

wait for 100 ns;