A REPORT ON ANALOG ASSIGNMENT

Submitted in partial fulfillment of the course

Analog & Digital VLSI Design

By

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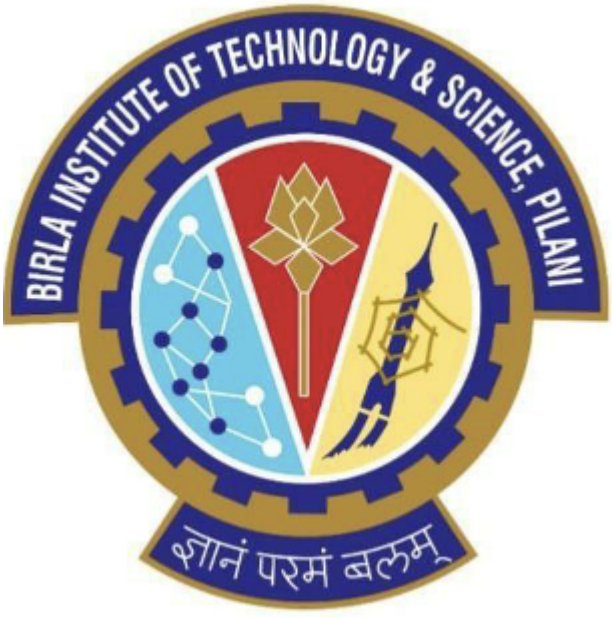

ABSTRACT

Title: Design a CMOS OPAMP

Project No.: 15

Key Words: Amplifiers, Spice, Gain, Phase, ICMR, OCMR, MOSFET Transistors,Resistor, Capacitor, etc

Project Areas: Software simulation of CMOS OPAMP

Abstract: We design the circuit diagram for the telescopic opamp along with the biassing circuit in LTSpice software. We have assigned W/L values to each of the transistors such that all of them are in saturation and give the required gain.

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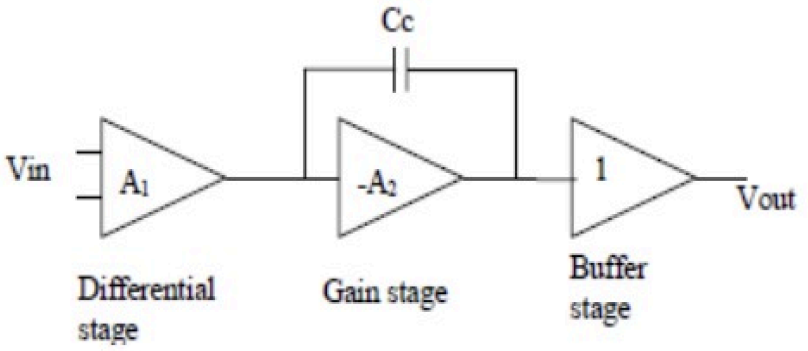
OVERVIEW

The report is based on the making of a CMOS opamp.
As per the problem statement, we have designed the circuit in LT SPICE software.Various simulations were run to get the desired results. We tweak the circuit little by little in order to obtain various other parameters, like ICMR, Gain, etc.

Problem Statement 15:

Design a CMOS OPAMP.

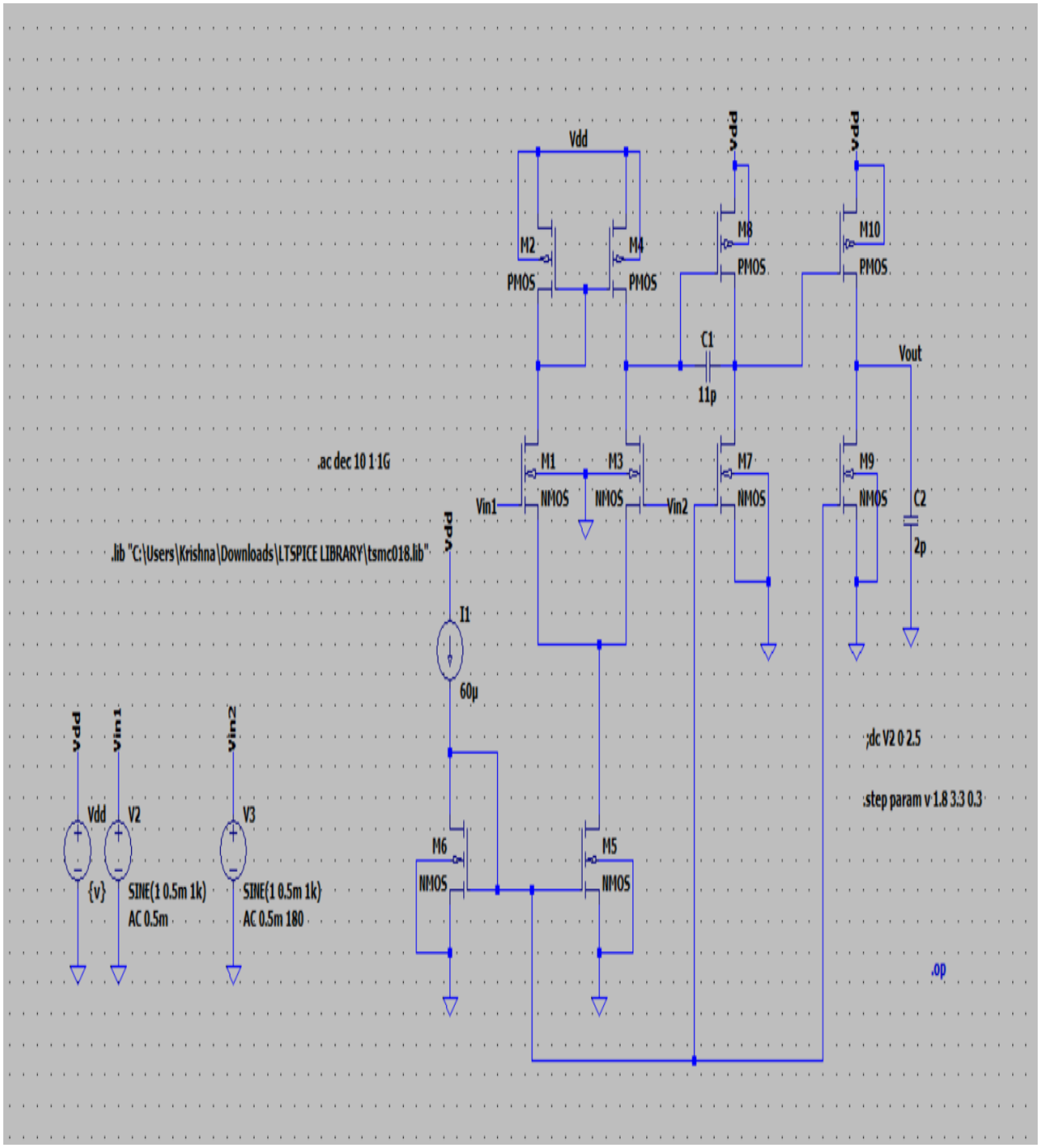


a) Analog schematic for the above model
b) Analysis of all equations of your design, with a systematic derivation of all transistors W/L ratios and spectre simulation of circuit for the following specifications.
   i) 3dB Frequency ≈ 100 KHz
   ii) Phase margin ≈ 60^0
   iii) Output swing ≥ 1V
c) Use STB Analysis to find the closed loop gain and phase margin for your OPAMP.
d) Calculate and plot the following parameters for your OPAMP: DC gain, Bode plot for AC gain and phase, CMRR plot, ICMR plot, PSRR plot, slew rate, settling time, output voltage swing (dc + Transient), power consumption, and input and output offset voltage.

SUMMARY OF RESULTS

S.No.	Quantity	Value	Required Specification
1.	DC gain	15.71	-
2.	Phase Margin	60°	~60°
3.	Power Consumed	0.42 mW	-
4.	Input DC offset	1V	-
5.	Output DC offset	1.95V	-
6.	CMRR	69.74 dB	-
7.	ICMR	2.3V	-
8.	PSRR	61.20 dB	-
9.	Slew Rate	90.07V/us	-
10.	Settling Time	50ns	-
11.	Output Voltage Swing	15.72mV	>= 1V
12.	3-db frequency	100.19 kHz	~100 kHz

CIRCUIT DIAGRAM



NETLIST

```
* E:\3-1\ADVD\Draft1.asc
Vdd Vdd 0 2.5
V2 Vin1 0 SINE(1 0.5m 1k 0.5m) AC 0.5m
V3 Vin2 0 SINE(1 0.5m 1k 0.5m) AC 0.5m 180
M3 N001 Vin2 N005 0 NMOS l=0.36u w=2.448u
M1 N002 Vin1 N005 0 NMOS l=0.36u w=0.36u
M7 N003 N004 0 0 NMOS l=0.36u w=9u
M2 Vdd N002 N002 Vdd PMOS l=0.36u w=0.72u
M4 Vdd N002 N001 Vdd PMOS l=0.36u w=4.896u
M8 Vdd N001 N003 Vdd PMOS l=0.36u w=16.56u
M10 Vdd N003 Vout Vdd PMOS l=0.36u w=28.8u
M9 Vout N004 0 0 NMOS l=0.36u w=27.72u
M6 N004 N004 0 0 NMOS l=0.36u w=10.44u
M5 N005 N004 0 0 NMOS l=0.36u w=10.44u
I1 Vdd N004 60µ
C1 N003 N001 11p
C2 Vout 0 2p
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\91928\AppData\Local\LTspice\lib\cmp\standard.mos
.lib E:\3-1\ADVD\tsmc018.lib
.backanno
.end
```

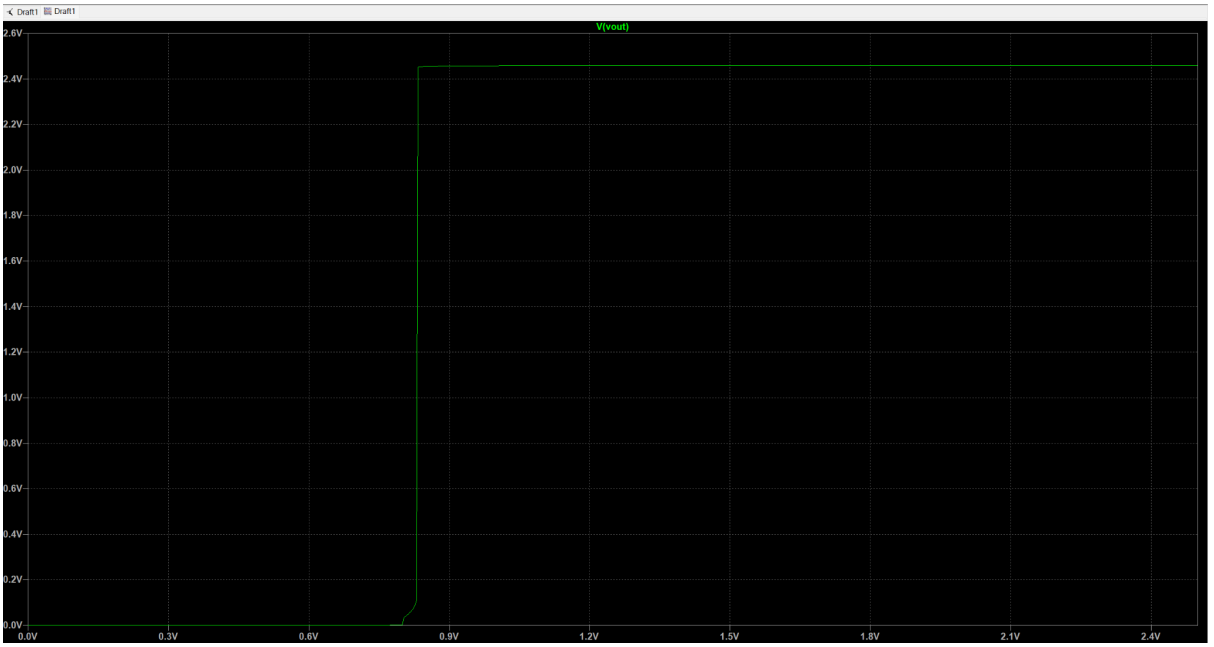
Table for W/L values for the respective MOS

M1	**1**
M2	**1**
M3	**6.8**
M4	**6.8**
M5	**29**
M6	**29**
M7	**25**
M8	**46**
M9	**77**
M10	**80**

PLOTS

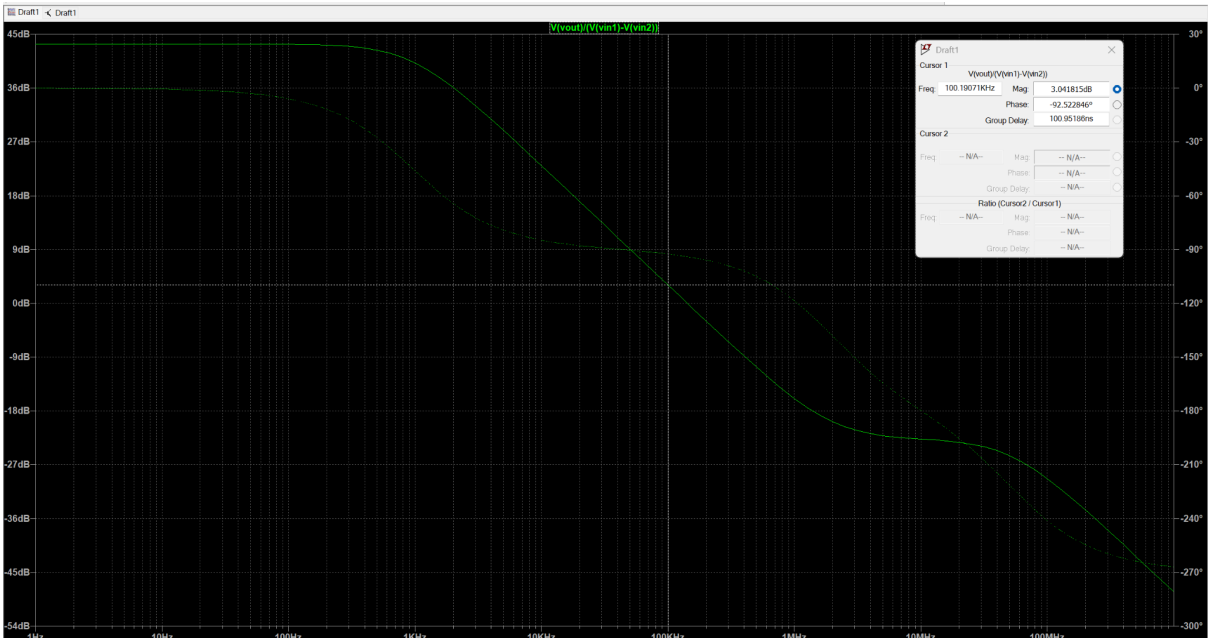
1. **DC Gain:**

   DC Gain = 15.71



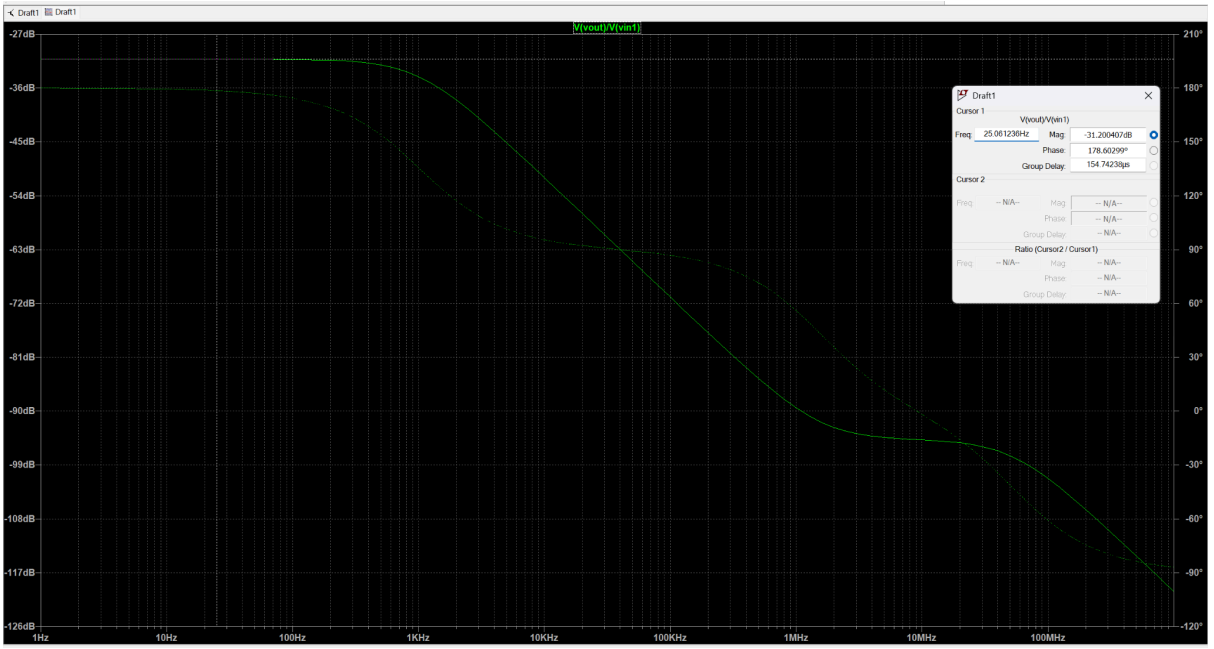
2. **Bode plot for AC gain and phase:**

   AC gain = 38.86 dB Phase margin = 60°

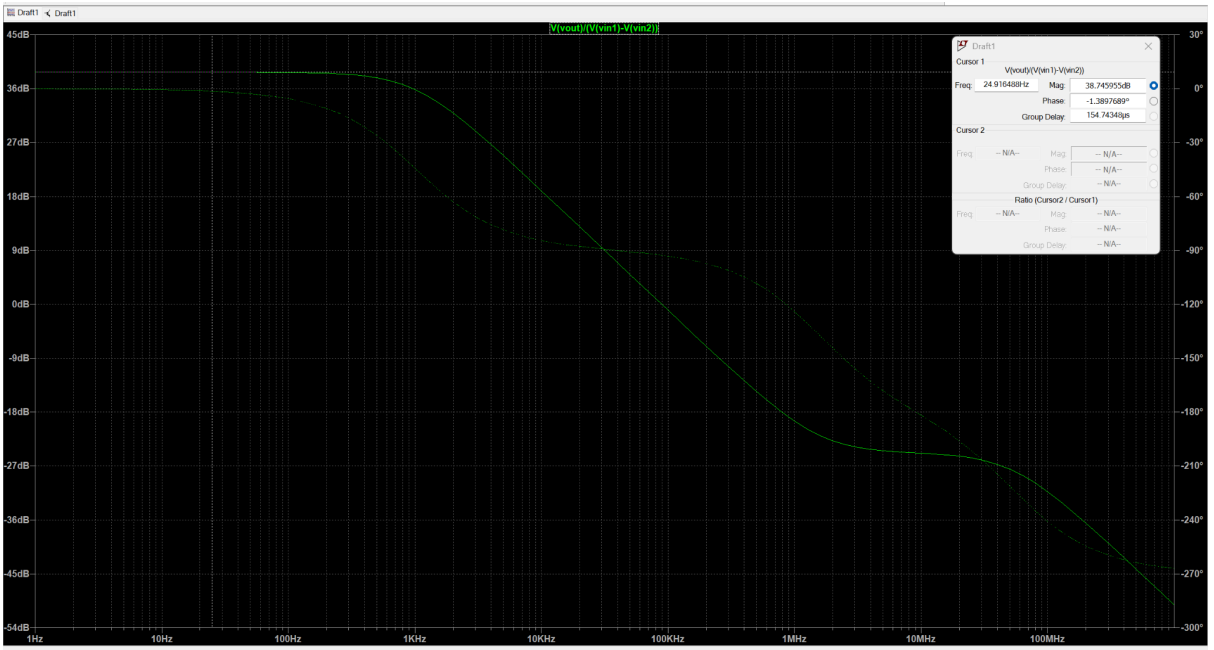


3. **CMRR Plot:**

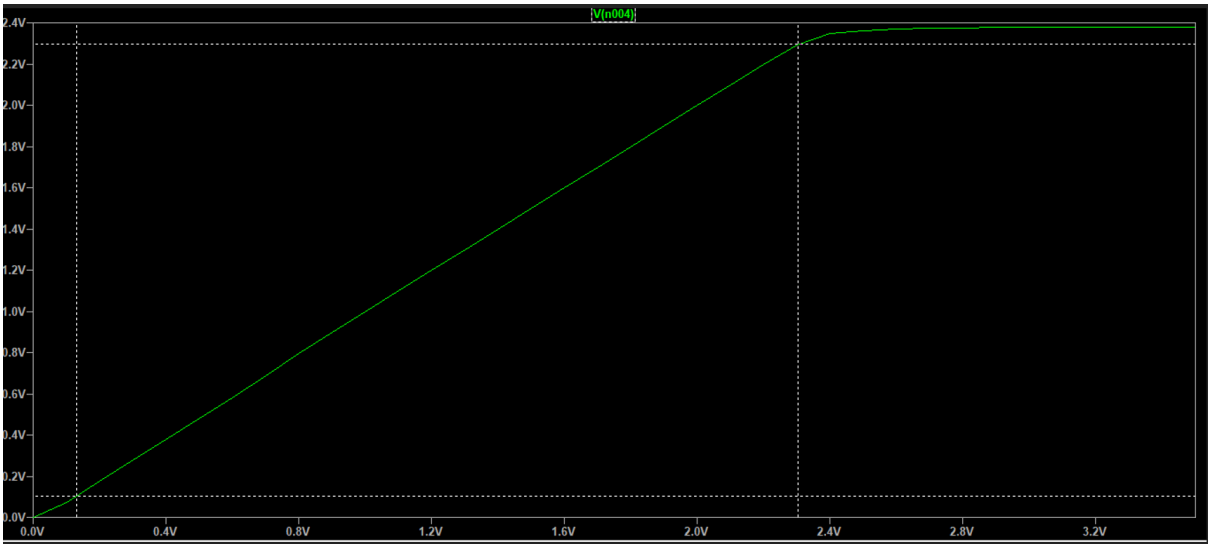
   Common Mode AC Gain plot: Adm/Acm= 38.74-(-31)dB = 69.74dB



Differential Mode AC Gain plot:

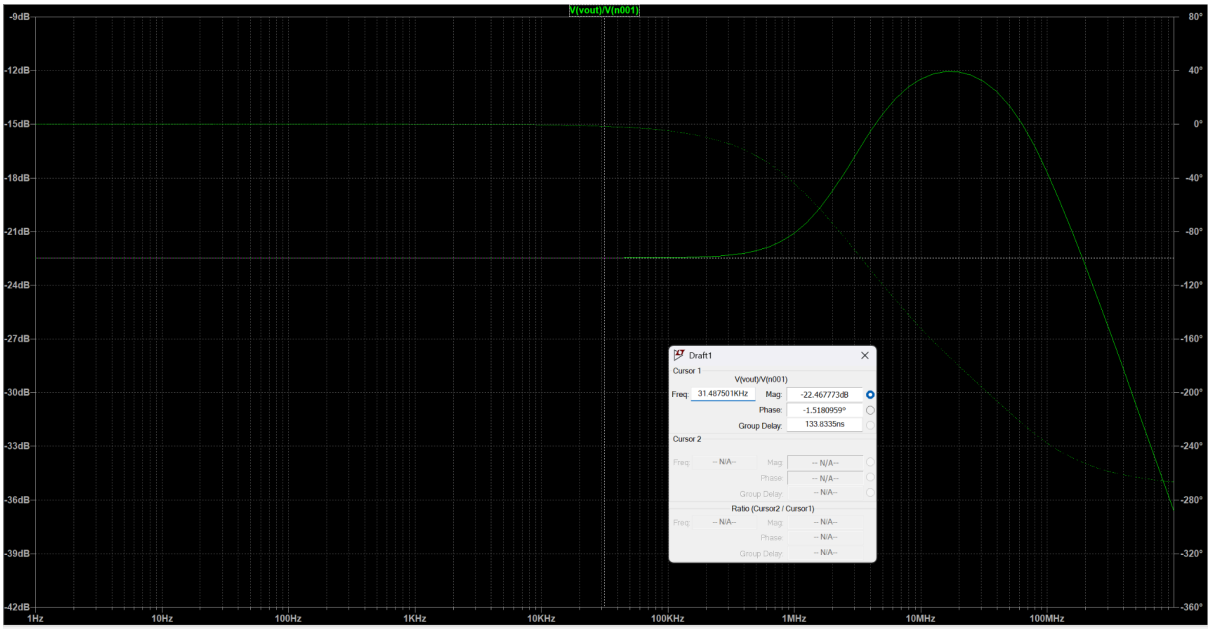


4. ICMR Plot:



5. PSRR Plot:

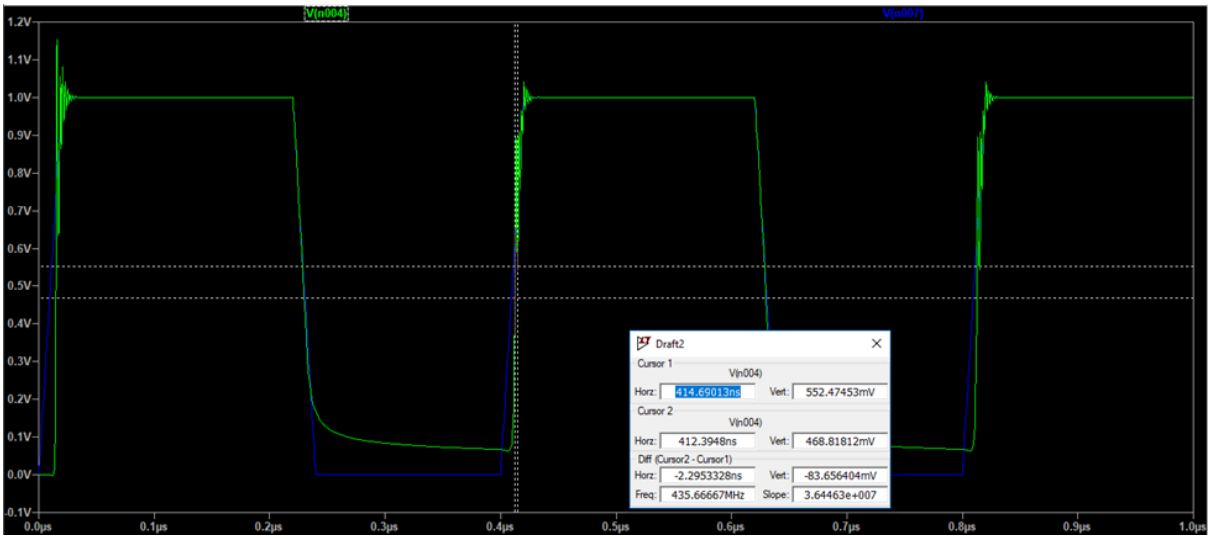
PSRR(in dB)= Adm-Avdd= 38.74-(-22.46)=61.20 dB



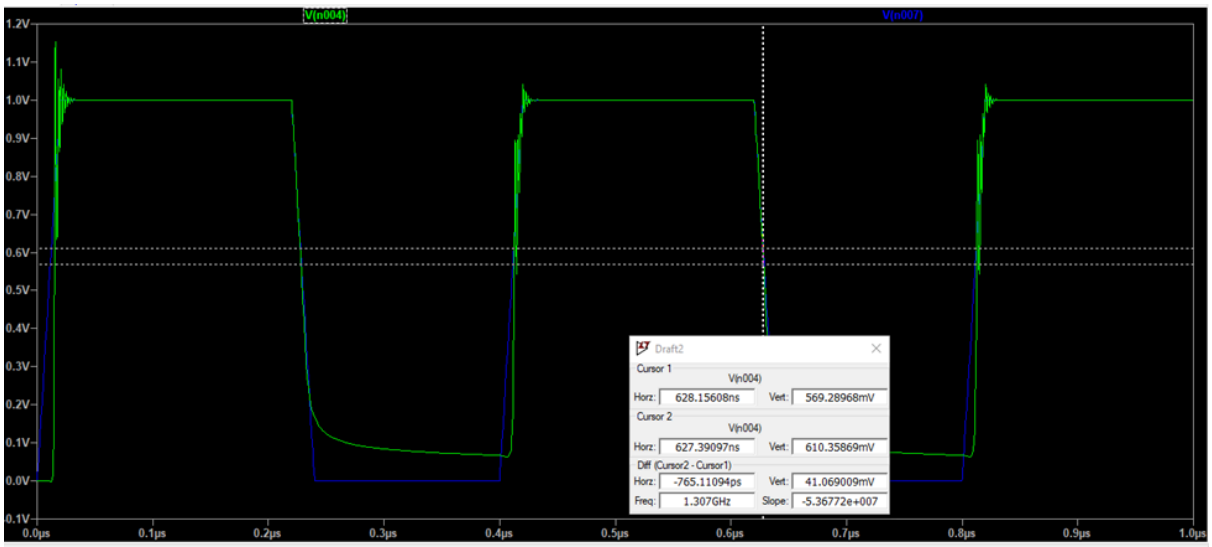
6. **Slew Rate:**

Slew rate of an Op amp is defined as the maximum rate of change of output for the small change in input. Generally SR is determined from the slope of output waveform during rise or fall of the output when the input is applied. So, we have a positive SR and a negative SR

Positive Slew Rate = 36.4 V/microsec

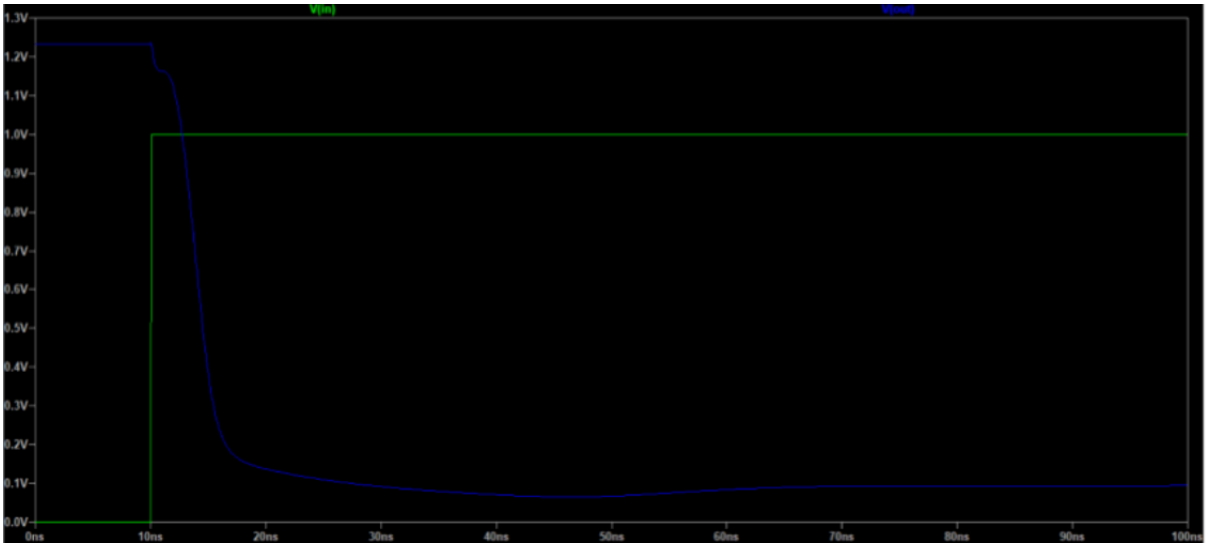


Negative Slew Rate = -53.67 V/microsec



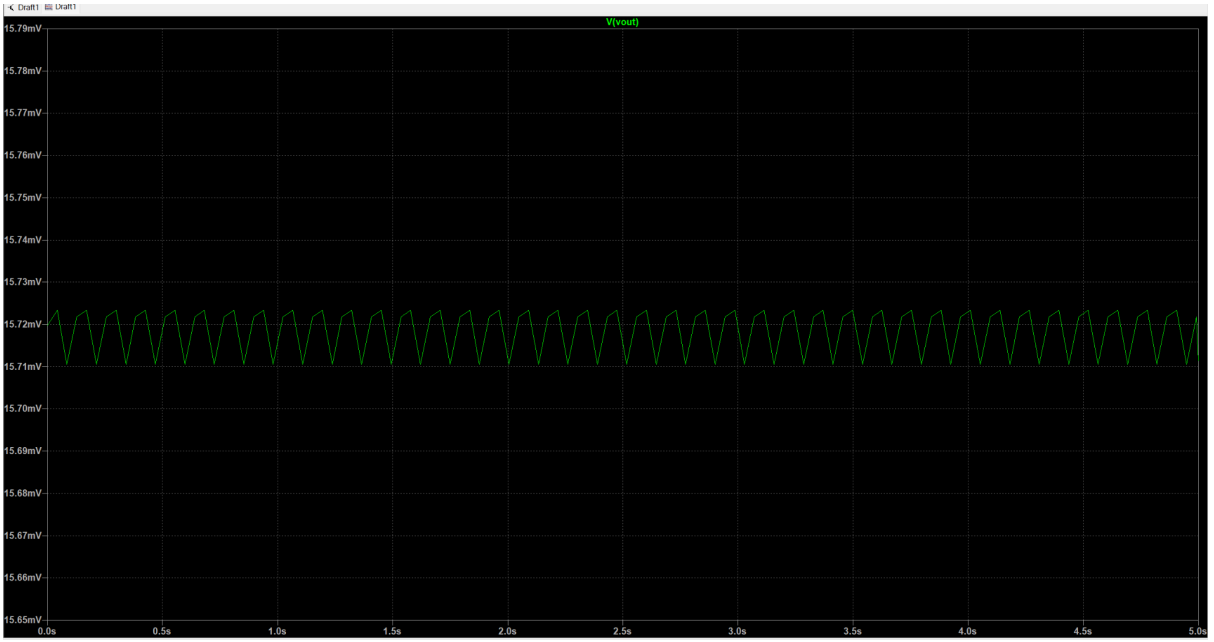
7. **Settling Time:**

Here we apply step input at 10ns and corresponding to that our output stabilizes at around 60ns. So our settling time is around
60ns – 10ns =50ns.



8. **Output voltage swing (dc +Transient):**

Output voltage swing= 15.42 mV

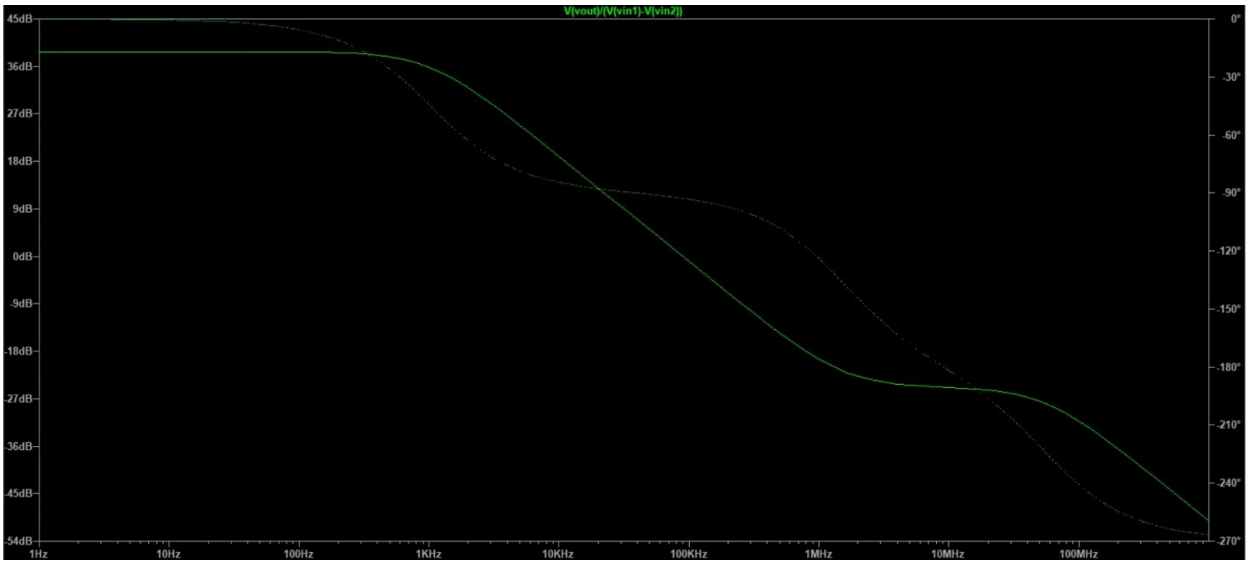


9. **Power Consumption:**

Power= 2.5x(60+5.87+39.93+51.72+10.82)uW

=(2.5 x 0.168) mW = 0.42 mW

<u>Using STB analysis we obtain the following graph:</u>



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