C028AD10b5M

10-bit 5MS/s asynchronous SAR ADC

Rev. 1.3 — 18 March 2021 Preliminary data sheet

1. General description

The C028AD10b5M IP is designed in the TSMC CLN28HPCP process.

The IP is an asynchronous clocked SAR ADC, which can convert either DC coupled 10-bit single-ended or 11-bit differential analog input signals at a maximum sampling rate of 5MS/s. The format of the digital output code is plain binary.

The IP consist of a main SAR ADC, a low-dropout regulator (LDO) and a differential analog test bus (ATB). The LDO generates a separate reference and analog supply voltage of 0.9V from an external 1.5V.

Typical application areas are:

- Voltage monitoring
- Data acquisition

The IP makes use of overrange and therefore needs two extra conversion cycles to convert the analog input to a digital word. The overrange is implemented to compensate settling behavior of the internal LDO reference output. The conversion cycles are internally clocked which removes the need of a >100MHz clock. Metastable states of the comparator which can cause loss of function in asynchronous ADCs are observable via the *timeout* output signal.

The digital output bits becomes asynchronous available when the ready signal becomes high. The resolution of the digital output data is 10-bit in single ended mode and 11-bit in differential mode. A divide by 2 mode is available to double the analog input voltage range in both single-ended and differential input modes.

All digital in- and outputs have levelshifters to the separate digital domain which can be connected to the system's digital core. These levelshifters can be disabled and put in a defined state by setting *enable_levelshifter* low. All digital inputs and outputs are protected by CDM clamps.

2. Features and benefits

2.1 Functional features

- 5MS/s conversion speed
- 1.425V-1.98V analog supply voltage range
- Selectable two differential or four single-ended input channels
- Internal reference generation by LDO
- Internally asynchronous clocked
- Power down mode with minimal power dissipation
- Metastability detection
- Deep Nwell isolation for substrate noise rejection
- DFM NXP CARM compliant

2.2 Re-use features

- Hardness: *Hard*
- Target process: *CLN28HPCP*
- CoReUse level: *3*
- CTAG type: *CTAG.AMS*

3. Integration requirements

3.1 Clock signal

Like any other sampled circuit, the SNR of the C028AD10b5M depends on the jitter of the *clk* signal. A common formula, Equation 1, can be used to estimate the SNR of a sampled signal due to clock jitter. This textbook formula assumes sinusoidal input with maximum amplitude and results in worst-case degradation.

$$SNR_{jitter} = 20log\left(\frac{1}{2\pi f_{in} t_j}\right) \quad (1)$$

where f_{in} is the input BW of the ADC and t_j the rms jitter of the *clk* signal.

With the formula below, Equation 2, the impact of jitter on the total SNR of the clocked ADC can be calculated

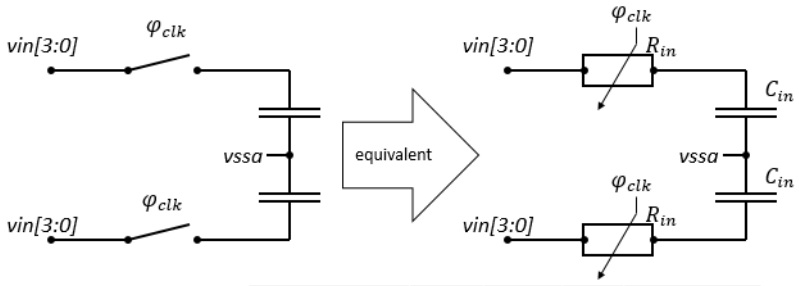
$$SNR_{tot} = (-20)log\sqrt{(10^{-(SNR_{adc}/20)})^2 + (10^{-(SNR_{jittter}/20)})^2} \quad (2)$$

Example: f_{in} = 200 kHz, t_j = 300 ps, SNR_{adc}= 60 dB, SNR_{jitter}= 68.5 dB.
The total SNR_{tot} of the clocked ADC is 59.4 dB.

3.2 Input circuit

The input stage of the C028AD10b5M is a T&H stage. The switches are bootstrapped to reduce distortion during sampling and the sample capacitor is the top-plate of the internal DAC of the SAR ADC.
The input circuit is DC-coupled, therefore the common mode voltage of the differential input is limited to a certain range. Below this range the comparator can no longer take a decision which results in loss-of-function of the C028AD10b5M. If this ever happens, it will be detected and the *timeout* output will be set to 1 for that sample.

Figure 1, shows the T&H circuit. On the left the functional circuit is shown and on the right the electrical equivalent. Basically during the sampling phase, the switches are closed and the input has a low impedance. When the switches open the input has a high impedance. During the sampling phase sufficient time should be given to the C028AD10b5M to guarantee less than $V_{LSB}/2$ settling error. During power down mode, the input circuit is considered open and therefore has a high impedance.



power_enable	φ_{clk}	R_{in}	C_{in}	Z_{in}
1	0	R_{on}	C_{in}	$R_{on} * C_{in}$
1	1	R_{off}	C_{in}	$R_{off} * C_{in}$
0	X	R_{off}	C_{in}	$R_{off} * C_{in}$

Fig 1. T&H stage of the C028AD10b5M. (L) functional circuit, (R) electrical equivalent

If the inputs of the ADC are connected to bond pads, the added inductance of the bondwire might cause overshoot and additional settling errors as the input circuit is now a RLC circuit.

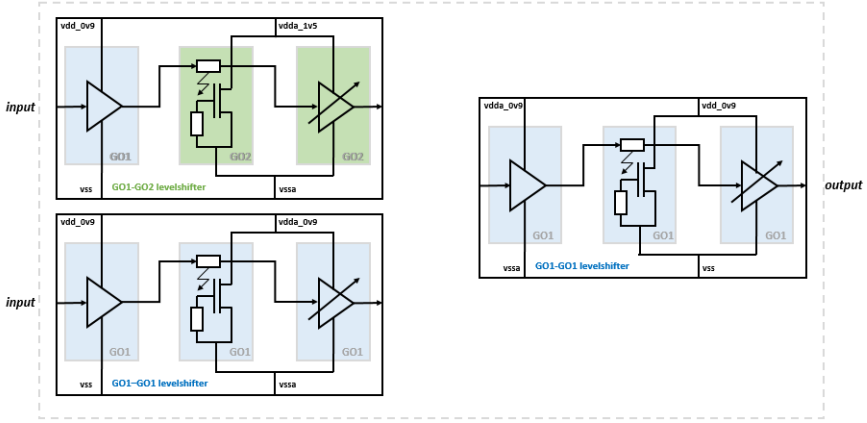
3.3 ESD protection

The C028AD10b5M contains CDM clamps in all the levelshifter circuits, which are connected to all digital inputs and outputs, as ESD protection

All analog in and outputs do not contain any ESD protection, so *vin[3:0], vneg_se, vref, ldo_bypass, atb_outp and atb_outn* pins have no ESD protection.

Figure 2, shows all ESD protections implemented in levelshifter circuits which are connected to digital inputs and outputs.

Fig 2. ESD protections of the C028AD10b5M



3.4 Bandgap reference voltage

The C028AD10b5M does not include a bandgap reference circuit. Therefore a bandgap reference circuit with a typical voltage output of 0.7V is required and needs to be connected to the *vref* input pin. The internal reference *vref_0v9* and analog supply *vdda_0v9* are derived from this reference by the LDO.

The gain and bandwidth from the *vref* input pin to the internal LDO outputs are respectively 1.3x and 1MHz. The worst case current that is drawn from the *vref* pin is about 1nA. So, with a 1MΩ bandgap output impedance the expected drop in the LDO reference input and outputs are respectively about 1mV and 1.3mV.

The *vssa* and referenced ground of the bandgap circuit should be connected together as shown in Figure 3. To keep the grounds as good as possible matched, star connection of the grounds is not advised.

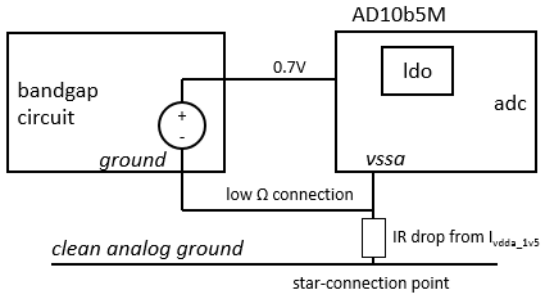


Fig 3. bandgap circuit connection to C028AD10b5M diagram

3.5 Enable_levelshifter

The IP has an *enable_levelshifter* input pin (active high) which needs to be controlled from the *vdda_1v5* voltage domain. This input controls the output of all levelshifters. When this input is set to high, the output of the levelshifters are enabled. When this input is set to low, the output of the levelshifters are forced to “0”.

The *enable_levelshifter* signal is typically used to put the C028AD10b5M in a defined state (power down) when *vdd_0v9* is not yet available or not stable enough.

3.6 SoC integration

For information on how to integrate analog IP, see Ref. 1.

3.7 Design review

It is strongly recommended to involve AMSIP in both top level **schematic** and **layout** design reviews to avoid poor performance due to wrong sharing of pins and/or routing.

The following design reviews are suggested:

schematic review: use of pad cells and sharing of pins by multiple analog and/or digital circuits.

Floor plan review: placement of analog blocks w.r.t. each other and the pad ring, orientation of analog blocks.

Final Place & Route review: cross talk issues for sensitive analog nets, interconnect resistances.

4. Ordering information

Information on how to order this IP-block can be found, see Ref. 1

5. Block diagram

The block diagram of the C028AD10b5M is shown in Figure 4.

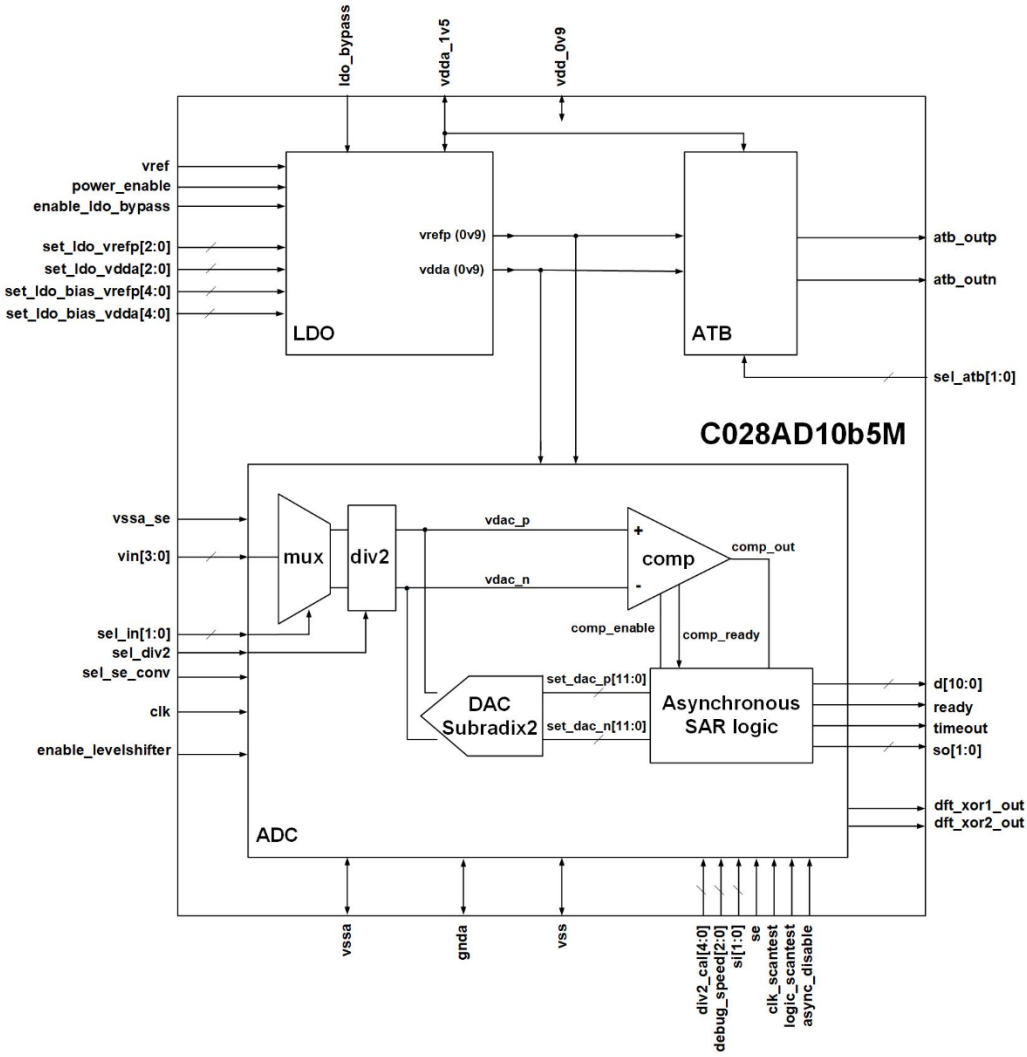


Fig 4. Block diagram of C028AD10b5M IP

6. Pinning information

6.1 Pin description

Table 1. Pin description

Symbol	Type[1]	Description
Supplies		
vdda_1v5	P	Analog supply [1.5V domain]
vdd_0v9	P	Interface supply [0.9V domain]
vssa	G	Analog ground [1.5V domain]
vss	G	Interface ground [0.9V domain]
gnda	G	substrate connection
Digital interface		
clk	I	ADC sample clock[2] (Conversion starts at rising edge of *clk*)
sel_se_conv	I	ADC single ended conversion mode[2]
sel_div2	I	ADC in div2 mode[2]
sel_in[1:0]	I	ADC input selection[2]
debug_speed[2:0]	I	ADC delay internal conversion loop[2][4] [Default setting = 1d]
si[1:0]	I	ADC scan input[2]
se	I	ADC scan enable[2]
clk_scantest	I	ADC clock signal for scantest[2]
logic_scantest	I	ADC test mode input[2]
async_disable	I	ADC test mode input, disables asynchronous reset[2]
so[1:0]	O	ADC scan output
d[10:0]	O	ADC 11-bit parallel output code (*d[10]* = MSB)
timeout	O	ADC conversion timeout signal/flag
ready	O	ADC conversion finished, output data is delayed (T_{skew}=) available
power_enable	I	Power enable selection[2]
enable_levelshifter	I	Enables all levelshifter outputs[3]
enable_ldo_bypass	I	LDO bypass selection[2]
set_ldo_vrefp[2:0]	I	Settings LDO output voltage *ref_out*[2][4] [0.825 V- 1.0 V] with 25mV step size [Default setting= 3d to give output= 0.9V]
set_ldo_vdda[2:0]	I	Settings LDO output voltage *vdd_out*[2][4] [0.825 V- 1.0 V] with 25mV step size [Default setting= 4d to give output= 0.925V]
set_ldo_bias_vrefp[4:0]	I	Settings LDO bias current *ref_out*[2][4] [Default setting= 10d]
set_ldo_bias_vdda[4:0]	I	Settings LDO bias current *vdd_out*[2][4] [Default setting= 10d]

Table 1. Pin description *...continued*

Symbol	Type[1]	Description
sel_atb[1:0]	I	Selection control signals for analog testbus[2] [Default setting= 0d, to disable the ATB switch]
div2_cal[4:0]	I	Division ratio calibration bits, ADC in divide by 2 mode[2][4] [1.89 - 2.09] with 6.25m step size [Default setting= 16d to give division factor= 1.99]
dft_xor1_out	O	DfT XOR chain 1 output (GO1) power domain
dft_xor2_out	O	DfT XOR chain 2 output (GO2) power domain
Analog interface		
vin[3:0]	AI	ADC analog inputs
vneg_se	AI	ADC negative input for single-ended conversion mode
vref	AI	LDO voltage reference input of 0.7 V (referred to *vssa*)
ldo_bypass	AI/O	LDO bypass voltage (used for overvoltage test)
atb_outp	AO	Analog testbus positive output
atb_outn	AO	Analog testbus negative output

[1] P = power; G = ground; I = digital input; O = digital output;
AI = analog input; AO = analog output; AI/O = analog in/output

[2] Signal is active high and it should be controlled from the *vdd_0v9* voltage domain

[3] Signal is active high and it should be controlled from the *vdd_1v5* voltage domain

[4] Pins should be set according to their default values to guarantee specified performance

7. Software interface

Not applicable for the C028AD10b5M.

8. Functional description

8.1 Basic functions

The C028AD10b5M is a Nyquist ADC which converts one DC-coupled differential or single-ended analog input signal respectively to a plain binary 11-bit and 10-bit digital word at a maximum conversion speed of 5 MS/s. The internal ADC reference and supply voltages are generated by a single dedicated LDO, which contain sufficient decoupling capacitance to handle the generated spiky current load from the internal SAR ADC.

8.2 Main blocks

The C028AD10b5M consists of three main blocks: SAR ADC, LDO and ATB. Additionally a digital interface block is present which buffers, levelshifts and protects the digital in- and outputs.

8.2.1 Digital interface

The digital inputs consists of levelshifters between the *vdd_0v9* domain and the internally generated *vdda_0v9* and *vdda_1v5* supplies.

The digital outputs consists of levelshifters between the internally generated *vdda_0v9* and *vdd_0v9* domains.

Each levelshifter in the digital interface includes CDM clamps.

8.2.2 LDO

The LDO generates a programmable 0.9V reference and supply voltages to the SAR ADC. This LDO needs a single external reference voltage of 0.7V. Bias currents are generated internally. The sampling and switching during the conversion cycles of the DAC generates high frequency current consumption spikes which can cause distortion on the reference signal and therefore distortion on the output of the ADC. The LDO reference output *ref_out* contains about 16pF decoupling capacitance to smoothen this distortion to acceptable level which enables the 10-bit performance of this ADC. The LDO supply output *vdd_0v9* is used to supply current to the fast-switching SAR logic and levelshifter circuits, which is decoupled with about 30pF decoupling capacitance.

8.2.3 SAR ADC

The internal structure of the SAR ADC is fully-differential, which make use of two DACs one for decoding the positive and other for negative inputs of the ADC. Fully-differential structure is chosen in order to provide both differential and single-ended input conversion modes. To allow input voltages up to 1.5V, the ADC also supports a divide by 2 mode which is done by capacitive division.

The SAR ADC consists of the following main sub-blocks: Input multiplexer, capacitive divider, Charge-redistribution sub-radix2 DAC, Strong Arm comparator and asynchronous SAR logic.

8.2.3.1 Input multiplexer

The input multiplexer is used to multiplex and sample the (multiple) analog inputs to the internal DAC circuit. It supports 2 differential inputs in differential mode and in single ended mode these inputs are configured as 4 single ended inputs. In single ended mode the negative input is connected to the *vneg_se* pin. Together with the internal DAC sub-circuit it also supports the T&H and divide by two functions.

8.2.3.2 CR-SR2-DAC

The differential (Charge-Redistribution- Sub-Radix2) DAC of the SAR ADC consist of a main DAC and a charge sharing capacitor to divide the sampled input voltage in the divide by 2 mode. A sub radix2 architecture is chosen to create overrange, which is realized by distributing the 10 binary weights into 12 conversion cycles i.s.o 10 cycles. The DAC acts as a sampling capacitor and a voltage reference generator during the SAR conversion cycles.

8.2.3.3 Comparator

The comparator decides whether the positive DAC output is bigger than the negative DAC output during the SAR conversion cycles.

8.2.3.4 Asynchronous SAR logic

The asynchronous SAR logic starts the conversion cycle at the rising edge of *clk*. It triggers the comparator and decides upon the settings of the CR-DAC. After 12 conversion cycles in single ended mode and 13 conversion cycles in differential mode, it sets the output register and resets the DAC for the next conversion.

8.3 Modes of operation

The C028AD10b5M has six modes of operation: operational differential input mode, operational single-ended input mode, operational divide by 2 mode, power down mode, sleep mode and LDO bypass mode.

The IP has input control pins for debug, calibration and control purposes, which it has to be set to their default values as given in Table 2. Changing these settings no longer guarantees correct functionality and are considered as debug options.

The settings of the remaining input control pins depends on the mode of operation, which will be listed in the concerning sections.

Table 2. default settings for all the modes

Pin name	setting	comments
set_ldo_vrefp[2:0]	011	
set_ldo_vdda[2:0]	100	
set_ldo_bias_vrefp[4:0]	01010	
set_ldo_bias_vdda[4:0]	01010	
sel_atb[1:0]	00	
debug_speed[2:0]	001	
div2_cal[4:0]	10000	
si[1:0]	00	
se	0	
clk_scantest	0	
logic_scantest	0	
async_disable	0	

8.3.1 Operational differential input mode

In differential input mode the analog inputs *vin[3:0]* are configured as 2 differential analog input pairs. In this mode the ADC is fully functional and its converting differential analog signals to a 11-bit digital code. When *clk* is low it is sampling and when *clk* is set high it starts the conversion cycle until it is finished. When the SAR ADC is finished it resets its internal states and waits for the next conversion which starts at the falling edge of *clk*. The settings for differential input mode are given in Table 3.

Table 3. differential input mode settings

Pin name	setting	comments
clk	1/0	50kHz - 5MHz
enable_levelshifter	1	equal to V_{vdda_1v5}
enable_ldo_bypass	0	
power_enable	1	
sel_se_conv	0	
sel_div2	0	
sel_in[1:0]	Dont care	

8.3.1.1 Analog input selection

The ADC input selection pins *sel_in[3:0]* allows to select one of the two differential analog inputs (see Table 4 & Figure 5). If there are unused inputs, it's advised to connect these to the *vssa* pin.

Table 4. Analog input selection in differential input mode

sel_in[1:0]	selected positive input pin	selected negative input pin
00	vin[0]	vin[1]
01	vin[0]	vin[1]
10	vin[2]	vin[3]
11	vin[2]	vin[3]

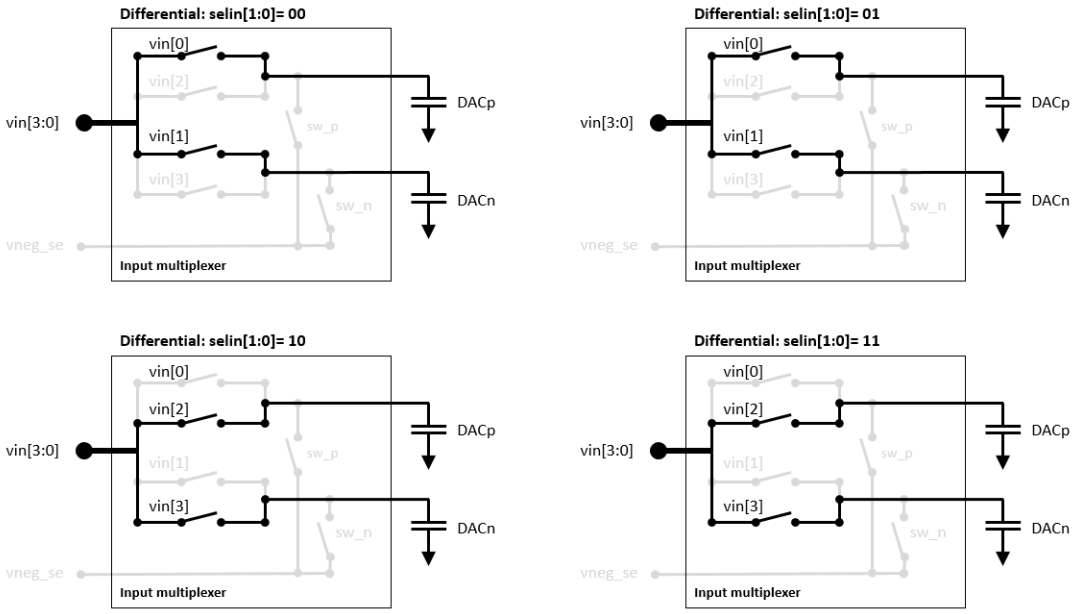


Fig 5. Analog input selection in differential input mode

8.3.2 Operational single-ended input

In single-ended input mode the analog inputs *vin[3:0]* are configured as 4 single-ended analog inputs. In this mode the ADC is fully functional and its converting single-ended analog signals to 10-bit digital code. The digital output code d[10:0] is in single ended mode LSB aligned. Which means that, in single ended mode, the MS-bit (d[10]) is always set to “0”. This to have a correct 10-bit digital output code on the available ADC 11-bit parallel output bits.

When clk is low it is sampling and when clk is set high it starts the conversion cycle until it is finished. When the SAR ADC is finished it resets its internal states and waits for the next conversion which starts at the falling edge of clk.

When *clk* is low the negative input of the comparator is connected to the *vneg_se* pin, which is meant as a reference for the conversion. Therefore it is advised to connect it to the ground connection of the applied input signal. In absence of such a ground connection, the *vneg_se* pin should be connected to the *vssa* pin of the IP. When *clk* is high the negative input of the comparator is disconnected from the *vneg_se* pin. After that a reference voltage is internally generated for the negative input of the comparator. This is done by making use of the existing capacitors in the DAC.

The settings for single-ended input mode are given in Table 5.

Table 5. single-ended input mode settings

Pin name	setting	comments
clk	1/0	50kHz - 5MHz
enable_levelshifter	1	equal to V_{vdda_1v5}
enable_ldo_bypass	0	
power_enable	1	
sel_se_conv	1	
sel_div2	0	
sel_in[1:0]	Dont care	

8.3.2.1 Analog input selection

The ADC input selection pins *sel_in[3:0]* allows to select one of the four single-ended analog inputs (see Table 6 & Figure 6). In single ended mode the negative input is internally connected to the *vneg_se* pin, which is the ground for the internal reference. In case of can be connected to the *vssa* pin. If there are unused inputs, it's advised to connect these to the *vssa* pin.

Table 6. Analog input selection in single-ended input mode

sel_in[1:0]	selected positive input pin
00	vin[0]
01	vin[1]
10	vin[2]
11	vin[3]

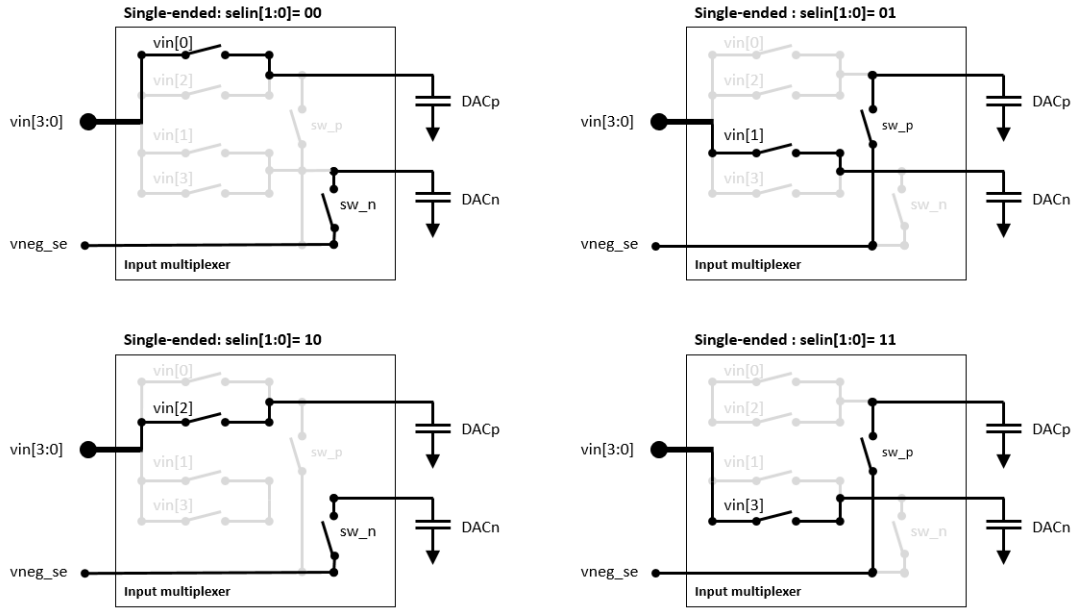


Fig 6. Analog input selection in single-ended input mode

8.3.3 Operational divide by 2 mode

The divide by 2 mode can be enabled in both differential and single-ended modes. In this mode the ADC input range is doubled. In this mode the ADC is fully functional and its converting analog signals to a digital code. When *clk* is low it is sampling and when *clk* is set high, first it starts dividing and after that it starts the conversion cycle until it is finished. When the SAR ADC is finished it resets its internal states and waits for the next conversion which starts at the falling edge of *clk*.

In this mode the allowed time for conversion is reduced by the time that is needed for performing the division. If the clock duty cycle is kept at 50% than the clock frequency needs to be reduced to 2.5MS/s. If the clock frequency is kept at 5MS/s than the clock duty cycle needs to be changed into 75%. The appropriate clock (frequency & duty cycle) for the chosen mode is given in Table 19.

The settings for divide by 2 mode are given in Table 7.

Table 7. divide by 2 mode settings

Pin name	setting	comments
clk	1/0	frequency: 50k - 2.5M Hz DC_{clk}= 50%
		frequency: >2.5M - 5M Hz DC_{clk}= 75%
enable_levelshifter	1	equal to V_{vdda_1v5}
enable_ldo_bypass	0	
power_enable	1	
sel_se_conv	Dont care	
sel_div2	1	
sel_in[1:0]	Dont care	

8.3.4 Power down mode

During power down mode all circuits including the LDO are turned off. All digital outputs of the C028AD10b5M are set low. The settings for power down mode are given in Table 8.

Table 8. power down mode settings

Pin name	setting	comments
clk	Dont care	
enable_levelshifter	1	equal to V_{vdda_1v5}
enable_ldo_bypass	Dont care	
power_enable	0	
sel_se_conv	Dont care	
sel_div2	Dont care	
sel_in[1:0]	Dont care	

The *enable_levelshifter* overrules all settings, when *enable_levelshifter* is low (equal to V_{vssa}) the C028AD10b5M is in power down mode regardless of the *power_enable* setting. The settings for this alternative power down mode are given in Table 9.

Table 9. alternative power down mode settings

Pin name	setting	comments
clk	Dont care	
enable_levelshifter	0	equal to V_{vssa}
enable_ldo_bypass	Dont care	
power_enable	Dont care	
sel_se_conv	Dont care	
sel_div2	Dont care	
sel_in[1:0]	Dont care	

8.3.5 Sleep mode

The sleep mode is meant for fast wake-up time. The LDO is kept enabled but the ADC is not converting. As the SAR ADC is a fully dynamic circuit, it basically means that the clock is set to low and the ADC is in continuous sampling mode. The settings for sleep mode are given in Table 10.

Table 10. sleep mode settings

Pin name	setting	comments
clk	0	
enable_levelshifter	1	equal to V_{vdda_1v5}
enable_ldo_bypass	Dont care	
power_enable	1	
sel_se_conv	Dont care	
sel_div2	Dont care	
sel_in[1:0]	Dont care	

The major difference between sleep mode and sampling during operational mode is the allowed maximum time for sampling. If *clk* is low for too long, internal circuits start to deviate too much due to leakage. The main advantage of the sleep mode over the power down mode is the reduced startup time as the LDO are kept enabled at the cost of some static current consumption.

8.3.6 LDO bypass mode

In LDO bypass mode, the LDO outputs are by passed. Effectively a switch shorts the LDO outputs to *ldo_bypass* pin and disables the LDO circuit. This mode can be used either to debug the SAR ADC core or to perform overvoltage stress test on the IP. In both cases the *ldo_bypass* pin can be configured as follow:

1. Connect to another supply voltage
In this configuration make sure that $V_{ldo\_bypass} \leq V_{vdda\_1v5}$.
This to prevent any leakage from V_{ldo_bypass} to V_{vdda_1v5} supply
(Through PMOS devices of which the bulk are connected to V_{vdda_1v5} supply and drain to *ldo_bypass* pin)
2. Short-circuit with the *vdd_0v9* pin of this IP
In this configuration make sure that $V_{ldo\_bypass} \leq V_{vdda\_1v5}$.
This to prevent any leakage from V_{ldo_bypass} to V_{vdda_1v5} supply
(Through PMOS devices of which the bulks are connected to V_{vdda_1v5} supply and drain to *ldo_bypass* pin)
3. Short-circuit with the *vdda_1v5* pin of this IP

8.3.6.1 Debug internal SAR ADC

The settings for debug SAR ADC core are given in Table 11.

Table 11. Debug internal SAR ADC settings

Pin name	setting	comments
enable_levelshifter	1	equal to V_{vdda_1v5}
enable_ldo_bypass	1	
power_enable	1	
clk	1/0	
all other pins	Dont care	

8.3.6.2 Overvoltage stress test

The settings for overvoltage test are given in Table 12.

Table 12. Overvoltage test settings

Pin name	setting	comments
enable_levelshifter	1	equal to V_{vdda_1v5}
enable_ldo_bypass	1	
power_enable	1	
clk	0	
set_ldo_vrefp[2:0]	011	
set_ldo_vdda[2:0]	011	
set_ldo_bias_vrefp[4:0]	01010	
set_ldo_bias_vdda[4:0]	01010	
sel_atb[1:0]	00	
debug_speed[2:0]	101	
clk_scantest	0	
logic_scantest	0	
async_disable	0	
all other pins	Dont care	

8.3.7 DfT XOR chain test mode

To enable the DfT XOR chain test mode, all levelshifters have to be enabled and internal supplies must be present. This implies that the DfT XOR mode is equal to the sleep mode as described in Section 8.3.5.It should be noted that several digital inputs are used in both GO1 and GO2 power domains and therefore will trigger both XOR chains simultaneously. Since the LDO settings are changed during this test it is advised to run a full power on cycle after this mode to ensure the correct LDO output voltage ($T_{start,pd}$).

9. Configuration

For further details check the managed IP website, see Ref. 1.

10. Deviations from CoReUse standards

Not applicable.

11. Hardware interface

11.1 Interface operation

The analog inputs *vin[3:0]* of the C028AD10b5M IP are DC coupled. Therefore the input load of the ADC changes between the sample and the other two (div2/convert) states. During the sample state the capacitive input load will be large, as large as the top-plate of the CR-DAC. During the div2/convert states the input has a high impedance.

The digital in- and outputs *d[10:0]*, *clk* and *timeout* operate at a maximum of 5MHz. Excessive loading of these pins can cause timing related issues.

The flip-flops of the SAR register in the digital part of the SAR ADC sub-circuit, have an asynchronous reset. This reset *rst_an* pin is not made available at the interface of the IP, but it is controlled by the *power_enable* signal and also active during startup of the IP.

11.1.1 Reset

The flip-flops of the SAR register in the C028AD10b5M have an asynchronous reset. If testing the ADC *async_disable* must be enabled (*async_disable* = *'1'*). The *async_disable* signal also disables the *rst_an* signal, this to avoid resetting the scan chain during scan test.

11.2 Interface timing

The output data *d[10:0]* can be captured by triggering on the clk or ready signal.

Triggering on **clk** signal:
1. Rising edge:
a) Data is (already) available
b) Suitable for only continuous conversion

2. Falling edge:
a) Data is available after a (worst case) delay of T_{skew}= 0.61 ns
b) Suitable for only continuous conversion

Triggering on **ready** signal:
1. Rising edge:
a) Data is available after a (worst case) delay of T_{skew}= 1.34 ns
b) Suitable for both continuous and single conversions

2. Falling edge:
a) Data is (already) available
b) Suitable for both continuous and single conversions

11.2.1 Divide by 2 mode disabled

The timing of the C028AD10b5M, where the divide by 2 mode is disabled, is shown in Figure 7. When *clk* is low the ADC starts sampling and when *clk* is set high, it starts the conversion cycle until it is finished. At the start of the sampling phase, at the falling edge of *clk*, the output data of the previous sample is set to the output. e.g. when conversion N+1 is performed, the output *d[10:0]* contains conversion data of sample N.

If the C028AD10b5M is not able to fully convert the sample due to metastability of the comparator, the output *timeout* will rise. e.g. the metastability detector triggers during the conversion of sample N+1. At the next falling edge of *clk*, *timeout* will be set high. The next sample N+2 is successfully converted without metastability, the *timeout* signal will become low again at the rising edge of *ready* when *clk is* high.

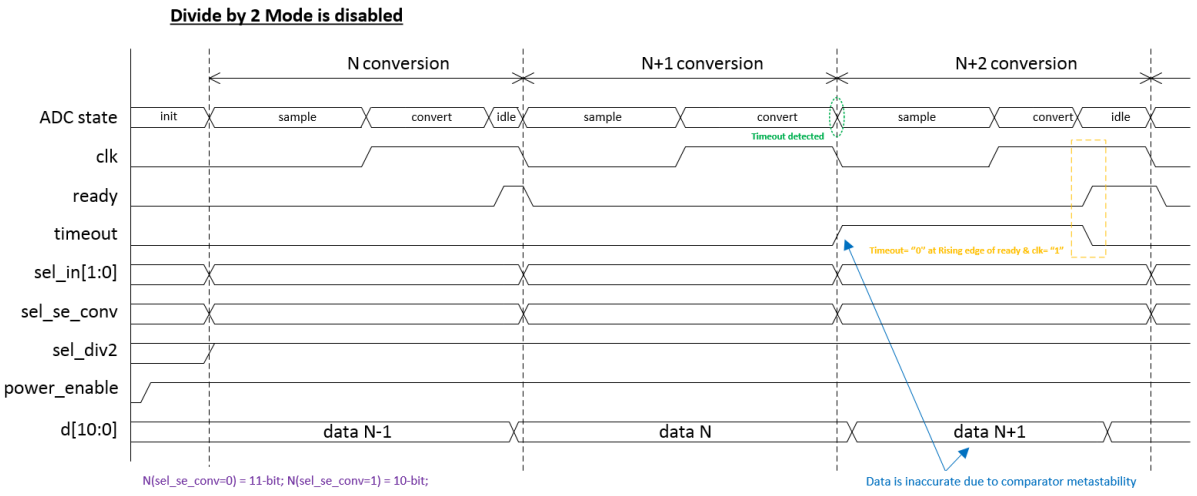


Fig 7. Timing diagram: divide by 2 mode is disabled

11.2.2 Divide by 2 mode enabled

The timing of the C028AD10b5M, where the divide by 2 mode is enabled, is shown in Figure 8. When *clk* is low the ADC starts sampling and when *clk* is set high, it starts first with dividing the sampled input signal by 2 and after that it starts the conversion cycle until it is finished. At the start of the sampling phase, at the falling edge of *clk*, the output data of the previous sample is set to the output. e.g. when conversion N+1 is performed, the output *d[10:0]* contains conversion data of sample N.

If the C028AD10b5M is not able to fully convert the sample due to metastability of the comparator, the output *timeout* will rise. e.g. the metastability detector triggers during the conversion of sample N+1. At the next falling edge of *clk*, *timeout* will be set high. The next sample N+2 is successfully converted without metastability, the *timeout* signal will become low again at the rising edge of *ready* when *clk is* high.

In this mode, the applied analog input voltages should be ≤ V_{vdda_1v5}.

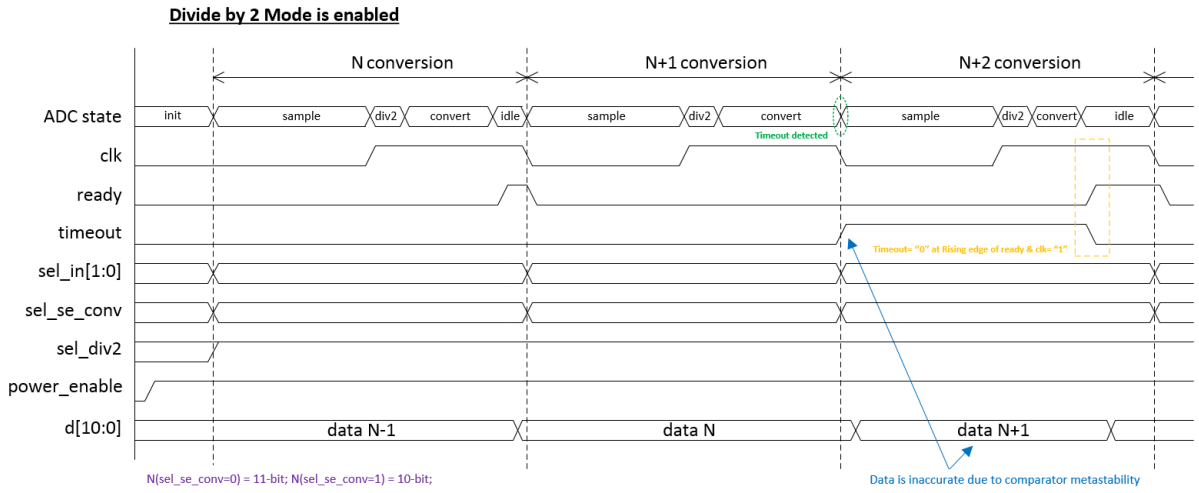


Fig 8. Timing diagram: divide by 2 mode is enabled

12. Product application information

12.1 Internal generated reference supply voltage

The C028AD10b5M uses default settings for the internal generated reference and supply voltage of typically 0.9V. These voltages are provided internally by the LDO sub-circuit. This LDO requires a single reference input voltage of 0.7 V. Changing these settings no longer guarantees correct functionality and are considered debug options.

The LDO sub-circuit consist of the following main parts:
1. Reference generation circuit.
2. Ref LDO core which generates the V_{ref_out} at LDO output *ref_out*.
3. Vdd LDO core which generates the V_{vdd_out} at LDO output *vdd_out*.

The two LDO core circuits are very similar in design. The ref LDO core output *ref_out* is optimized for fast settling and high DC accuracy.

The bias current and output voltages of both LDO core circuits can be programmed for debug purposes with their own settings.

The output voltages V_{ref_out} and V_{vdd_out} can be programmed with their input pins *set_ldo_vrefp[2:0]* and *set_ldo_vdda[2:0]* from 0.825V up to 1.0V, with a step size of 25mV, see Table 13.

Table 13. LDO output voltages selection

set_ldo_vrefp[2:0] / set_ldo_vdda[2:0]	V_{ref_out} / V_{vdd_out} [V]
000	0.825
001	0.850
010	0.875
011	0.90
100	0.925
101	0.950
110	0.975
111	1.0

The outputs of the LDO are observable at the differential atb access points *atb_outp* and *atb_outn* via the *sel_atb[1:0]* selection pins.

12.2 Debug pins

The C028AD10b5M has six debug settings. Changing these settings no longer guarantees correct functionality and are considered debug options. The default settings for these debug pins are given in Table 14

Table 14. Default settings debug pins

Pin name	setting	description
set_ldo_vrefp[2:0]	011	Settings LDO output voltage *ref_out*
set_ldo_vdda[2:0]	100	Settings LDO output voltage *vdd_out*
set_ldo_bias_vrefp[4:0]	01010	Settings LDO bias current *ref_out*

Table 14. Default settings debug pins

Pin name	setting	description
set_ldo_bias_vdda[4:0]	01010	Settings LDO bias current *vdd_out*
debug_speed[2:0]	001	ADC delay internal conversion loop
div2_cal[4:0]	10000	Division ratio calibration bits (in divide by 2 mode)

debug_speed[2:0] slows down the internal SAR conversion cycle loop, allowing more time for the DAC to settle and the comparator to reset. By slowing down the SAR conversion loop cycle, the chance of finishing a complete conversion decreases which then results in performance degradation. The default setting for *debug_speed[2:0]* is 001, which results in a minimum additional delay of 2ns in the SAR conversion loop cycle.

div2_cal[4:0] sets the division ratio of the applied analog input signal.This pin has only effect on the divide by 2 mode. The default setting is 1000, which results in a division factor of 1.99. The division factor can be changed with a step size of about 6.25mV.

set_ldo_vrefp[2:0] sets the voltage of the LDO output *ref_out*. The default setting is 011, which results in 0.9V. The output voltage can be changed with a step size of about 25mV.

set_ldo_vdda[2:0] sets the voltage of the LDO output *vdd_out*. The default setting is 100, which results in 0.925V. The output voltage can be changed with a step size of about 25mV.

set_ldo_bias_vrefp[4:0] sets the bias current of the LDO output *ref_out*, to handle higher load currents that is drawn by the internal DAC circuit. The default setting is 01010.

set_ldo_bias_vdda[4:0] sets the bias current of the LDO *output vdd_out*, to handle higher load currents drawn by the digital part of the SAR ADC. The default setting is 01010.

12.3 Analog Test Bus

To improve the analog test coverage, the internal LDO output voltages and ground can be differentially observed via the analog test busses *atb_outp* and *atb_outn.*

The desired internal analog signals can be selected with selection inputs *sel_atb[1:0],* as given in Table 15.

Table 15: Analog Test Bus selection

sel_atb[1:0]	*atb_oup*	*atb_oun*
00	Off (switches not selected)	Off (switches not selected)
01	vdda_0v9 (LDO vdd output)	vssa (Analog ground)
10	vref_0v9 (LDO ref output)	vssa (Analog ground)
11	Not used	Not used

The atb outputs should not be used to externally supply the internal SAR ADC or to supply other circuits besides the SAR ADC himself.

13. Product test information

13.1 Functional testing

13.1.1 CTAG.AMS

For test access the CTAG.AMS shell can be used. This CTAG.AMS shell consists of a Test Point Register (TPR) to access the digital terminals of the analog IP block and a Test Control Block (TCB) to control the test modes for the IP. More information on the content of the CTAG.AMS shell delivery can be found in Ref. 1. For IP specific information, such as the type of test points used, one is referred to the test shell documentation in the DOCUMENTS directory of the CTAG.AMS shell.

For more information on CTAG.AMS application please see Ref. 2.

13.2 Structural testing

13.2.1 Testing the digital part using the internal scan chain

For production test the scan chain can be used. To improve the test coverage of this scan chain, a “test mode” pin *logic_scantest* has been added. When *logic_scantest* is high there are internal feedback loops which are opened so the digital part is in “test mode”. It does not operate properly for the SAR ADC core but it can be scanned. When *logic_scantest* is low the digital part is in normal operation but it can’t be scanned.

To improve the test coverage in scan test mode an *async_disable* pin is added. The *async_disable* disables the internal *rst_an* signal to avoid resetting the scan chain during scan test because the flip-flops of the SAR register have an asynchronous reset. The *logic_scantest* disables the power down mode of the IP.

13.2.2 Levelshifter functionality check by XOR chain

levelshifter functionality by XOR chain is meant to detect missing connections to the IP. When an input is toggled, the output *dft_xor1_out* and/or *dft_xor1_out* should also toggle. If this does not happen either the input is not connected or the IP has a manufacturing defect.
For further information see Section 8.3.7

13.2.3 Testing the analog part using the internal analog test bus

To improve the analog test coverage, the internal LDO output voltages and ground can be differentially observed via the analog test busses *atb_outp* and *atb_outn.* The desired internal analog signals can be selected with *sel_atb[1:0]* input pin. For further information see Section 12.3.

13.2.4 Overvoltage

Overvoltage testing is enabled by bypassing the internal LDO outputs. The internal GO1 (0.9V domain) reference and supply will be shorted to *ldo_bypass* pin. For further information see Section 8.3.6.2. It is not recommended to operate the ADC functionally during the overvoltage testing.

14. Layout

14.1 Floor plan and size

Table 16: General characteristics

Parameter	Specification
Process	CLN28HPCP with Deep N-Well[1], 0.9V SVT and 1.8V GO2
Area	0.06mm^2 (pre-shrink)

[1] The Deep N-Well is implemented for functional reasons. Removing this layer will lead to loss of function. For more info on this subject please contact AMS-IP.

14.2 Pin coordinates and Layer usage

In the layout of the C028AD10b5M IP eight levels of metal are used. M1 up to M6 are used for routing and M7 and M8 power routing and shielding.

The IP is pre-tiled to meet density requirements. The DNW layer is used for functional reasons and substrate noise isolation. The SVT layer is used for most components inside the SAR ADC core. GO2 is used inside the LDO circuits. LB layer routing is allowed over the IP with exception of the DAC part of the internal SAR ADC core.

14.3 Layout constraints

The C028AD10b5M makes use of DNW to reduce sensitivity to ground bounce. Due to the nature of the SAR algorithm, internal GHz range switching currents are present, these can cause disturbance to other circuits. Low-ohmic star connected supplies and local decoupling can reduce this effect.

The best possible performance is guaranteed by taking the following considerations into account:

- Use short wires for inputs to avoid excessive (RC) loading
- Use an as clean as possible input clock signal (Section 3.1)
- Connect the differential inputs as symmetrically as possible
- Avoid signal routing near the analog input routing, additional shielding is advised but shielding, for example, will decrease the bandwidth of the input signal.
- Use an as clean as possible separate analog supply for *vdda_1v5*

15. Verification

15.1 Verilog AMS / Wreal simulation

The behavioural model of the C028AD10b5M is only to check the functionality and for architecture exploration! Thermal noise, non-linearity and mismatch are not modelled. It's also not meant for timing closure/verification, for this the delivered liberty files needs to be used.

More information on model can be found in the *amos_c028hpcp_ad10b5m_model_wreal* word file in DOCUMENTS directory.

The Verilog model contains the same coverage but is limited in functionality.

15.1.1 testbench

By running the run_nccoex script in nccoex directory, the script will automatically show the simulation results in a graphical display.

15.1.1.1 -v option

By using the -v option with the run_nccoex script the user chooses to simulate the Verilog behaviour model and the corresponding testbench.

15.1.1.2 -vams option

By using the -vams option with the run_nccoex script the user chooses to simulate the Verilog-AMS *wreal* behaviour model and the corresponding testbench.

15.2 Schematic simulation

The OA, schematic and symbol views only, database is available for simulation purposes only and is not meant for SoC integration.

16. CAD Tools

For specifics, please contact AMSIP (via Enovia design PDM), see Ref. 4.

17. Limiting values

All digital input and output pins are connected to GO1 0.9V transistors, except the input *enable_levelshifter* which is GO2 as it should be controlled from the *vdda_1v5* supply domain.

All analog inputs are connected to GO2 1.8V transistors.

For absolute maximum ratings see Ref. 3.

18. Static characteristics

This section describes the static characteristics of the C028AD10b5M.
In Figure 9 the specified characteristics are shown to aid design-in.

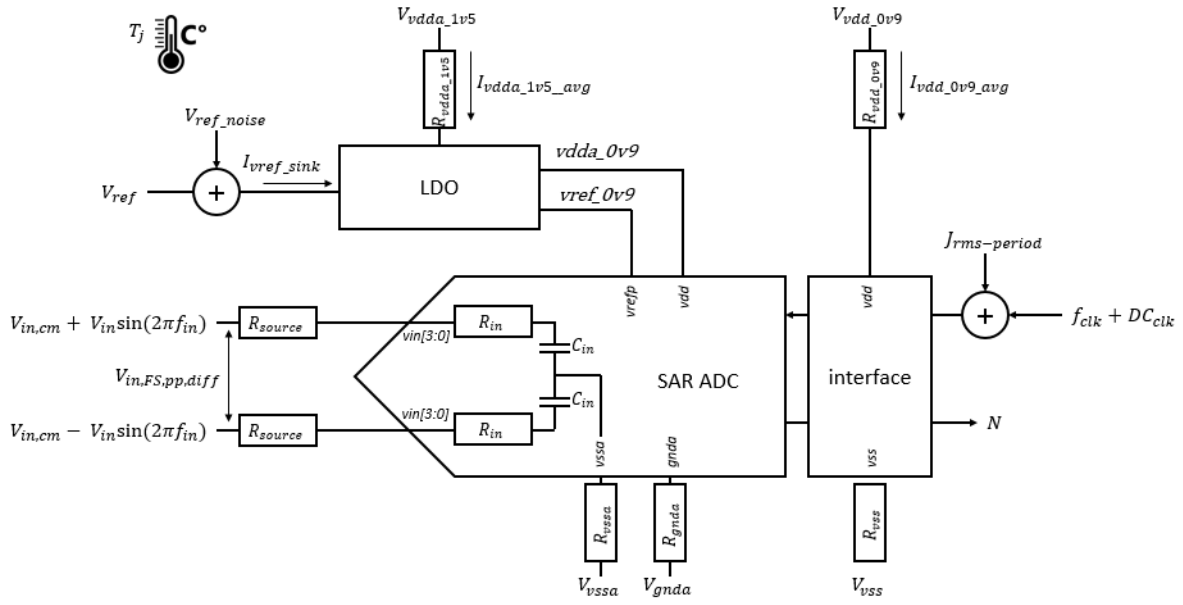


Fig 9. Definition of characteristics of the C028AD10b5M IP

Table 17. Static operating conditions
default: operational mode

Symbol	Parameter	TL[1]	Conditions	Min[3]	Typ[2]	Max[3]	Unit
static operating conditions							
T_j	Junction temperature	-		-40	25	150	°C
$T_{j,extend}$	extended junction temperature	-	no loss of function	-50		175	°C
V_{vdda_1v5}	clean analog supply voltage	-		1.425	1.5	1.98	V
V_{vdd_0V9}	digital interface voltage	-		0.81	0.9	0.99	V
V_{vssa}	clean analog ground voltage	-			0		V
V_{vss}	Digital interface ground voltage	-			0		V
V_{gnda}	Substrate voltage	-			0		V
ADC connections							
R_{source}[5][6]	Resistive source output load	-	sel_div2= 0 DC_{clk}= 60%, fclk= 5.0M DC_{clk}= 30%, fclk= 2.5M			 14.1 57.2	 kΩ kΩ
			sel_div2= 1 DC_{clk}= 80%, fclk= 5.0M DC_{clk}= 50%, fclk= 2.5M			 5.4 39.9	 kΩ kΩ
R_{vdda_1v5}	Impedance of analog supply	-				5	Ω
R_{vssa}	Impedance of analog ground	-				5	Ω
R_{vdd_0V9}	Impedance of digital supply	-				5	Ω

Table 17. Static operating conditions *...continued*

default: operational mode

Symbol	Parameter	TL[1]	Conditions	Min[3]	Typ[2]	Max[3]	Unit
R_{vss}	Impedance of digital ground	-				5	Ω
R_{gnda}	Impedance of substrate	-				5	Ω
LDO inputs and outputs							
V_{vref}	LDO reference input voltage	-		0.665	0.7	0.735	V
I_{vref_sink}	Current drawn from V_{vref}	-				1	nA
V_{ldo_bypass}	LDO bypass input voltage	-	$V_{ldo\_bypass} \leq V_{vdda\_1v5}$	1.425	1.5	1.98	V
V_{ref_out}	LDO reference output voltage[7]	II		0.855	0.9	0.945	V
V_{vdd_out}	LDO supply output voltage[7]	II		0.855	0.9	0.945	V
ADC inputs and outputs							
$V_{in,cm}$	DC input common mode voltage[8]	IV	sel_div2= 0, V_{vref}= 0.7V	0.38	0.45	0.60	V
$V_{in,FS,pp,se}$	Full scale single-ended input[8]	IV	sel_div2= 0, V_{vref}= 0.7V, $V_{in,cm}$= typ	0.76	0.8	0.82	V
$V_{in,FS,pp,diff}$	Full scale differential input[8]	IV	sel_div2= 0, V_{vref}= 0.7V, $V_{in,cm}$= typ	1.52	1.6	1.64	V
$Div2_{ratio}$	Division ratio in divide by 2 mode	IV		1.89	1.99	2.09	
C_{in}	Capacitive input load	IV			530	610	fF
R_{in}	Resistive input load	IV	clk = 0		1.9	3.2	kΩ
			clk = 1		250		GΩ

[1] Test Levels, see Section 21.1

[2] Typical conditions, unless stated otherwise: T_j = 27 °C, V_{vdda_1v5}= 1.5 V, V_{vdd_0v9}= 0.9V and nominal process with default settings

[3] Minimum and maximum values are bound by 4σ confidence bounds PVT

[4] T_j = 27 °C, process= ss

[5] Can be calculated using the Formula: $R_{source} = ((((100 - DC_{clk})/100) / f_{clk}) / (7.6*C_{in})) - R_{in}$

[6] To ensure settling error less than 0.5*Vlsb (7.6*τ)

[7] During startup: $V_{overshoot}$ <100mV; V_{settle}= ±2mV

[8] In divide by 2 mode: Input voltage should be ≤ V_{vdda_1v5} and multiplied by $Div2_{ratio}$

Table 18. Static characteristics
default: operational mode

Symbol	Parameter	TL[1]	Conditions	Min[3]	Typ[2]	Max[3]	Unit
static operating characteristics							
$I_{vdda\_1v5\_avg}$	Average current analog supply	II	operational mode		155	650	µA
			sleep mode		61	360	µA
			power down mode		0.01	15	µA
$I_{vdd\_0V9\_avg}$	Average current digital supply	II	operational mode		1	60	µA
			sleep mode		0.3	60	µA
			power down mode		0.3	60	µA
static ADC characteristics							
N	number of bits	-	differential input			11	bits
			single-ended input			10	bits
offset	offset error	III			0	±22	mV
e_{offset}	offset error drift	III	from 150°C to 27°C			±2	mV
			from -40°C to 27°C			±2	mV
gain	gain error	III			0	±50	mV
DNL	differential non-linearity	I	absolute DNL error		±0.5	±1	LSB
INL	integral non-linearity	I	absolute INL error		±0.5	±1	LSB

[1] Test Levels, see Section 21.1

[2] Typical conditions, unless stated otherwise: T_j = 27 °C, V_{vdda_1v5}= 1.5 V, V_{vdd_0v9}= 0.9V and nominal process with default settings

[3] Minimum and maximum values are bound by 4σ confidence bounds PVT

19. Dynamic characteristics

Table 19. Dynamic operating conditions
default: operational mode

Symbol	Parameter	TL[1]	Conditions	Min[3]	Typ[2]	Max[3]	Unit
dynamic operating conditions							
clock							
f_{clk}	clock frequency	-		0.05	2.5	5	MHz
DC_{clk}	clock duty cycle (indicates high time of f_{clk})	-	sel_div2= 0[4] fclk= 5.0M fclk= 2.5M Hz	 60 30			 % %
			sel_div2= 1[5] fclk= 5.0M fclk= 2.5M	 80 50			 % %
$J_{rms\text{-}period}$	Max RMS clock period jitter		0.1 ENOB reduction			300	ps
LDO							
V_{ref_noise}	rms noise at V_{ref}	-	0 - 1M Hz		50	100	µV

[1] Test Levels, see Section 21.1

[2] Typical conditions, unless stated otherwise: T_j = 27 °C, V_{vdda_1v5}= 1.5 V, V_{vdd_0v9}= 0.9V and nominal process with default settings

[3] Minimum and maximum values are bound by 4σ confidence bounds PVT

[4] Required minimum ADC convert state time= 110ns; divide by 2 mode is disabled

[5] Required minimum ADC convert state time= 160ns; divide by 2 mode is enabled

[6] In single-ended mode, the polarity between analog inputs vin[0], vin[2] and vin[1], vin[3] are the opposite of each other.

Table 20. Dynamic characteristics

default: operational mode

Symbol	Parameter	TL[1]	Conditions	Min[3]	Typ[2]	Max[3]	Unit
dynamic characteristics							
timing							
$T_{start,pd}$	start-up time from power down state (assuming V_{vref} is available)	IV			10	15	µs
T_{skew}	*clk* to *d[10:0]* skew	IV	falling edge, PssV0810T125_Cmax			0.61	ns
	ready to *d[10:0]* skew	IV	rising edge, PssV0810T125_Cmax			1.34	ns
$T_{latency}$	latency	IV			$1/f_{clk}$		ns
f_s	conversion rate	IV		0.05	2.5	5	MS/s
LDO							
PSRR	Power Supply Rejection Ratio	IV	from 10k to 40M Hz	30			dB
ADC							
f_{in}	input frequency	IV	ideal LP input filter	0		200	kHz
ENOB[4]	Effective Number Of Bits	I	single ended mode	9	9.5		bits
			differential mode	10	10.5		bits
SFDR[5]	Spurious Free Dynamic Range	I	single ended mode	65	67		dBc
			differential mode	69	70		dBc

[1] Test Levels, see Section 21.1

[2] Typical conditions, unless stated otherwise: T_j = 27 °C, V_{vdda_1v5}= 1.5 V, V_{vdd_0v9}= 0.9V and nominal process with default settings

[3] Minimum and maximum values are bound by 4σ confidence bounds PVT

[4] ENOB includes: SFDR + quantization noise + device noise + V_{ref_noise}
SINAD can be calculated by using the formula SINAD= (ENOB*6.02) +1.76

[5] Including harmonics

20. Abbreviations

Table 21. Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
AMS	Analog Mixed Signal
ATB	Analog Test Bus
BE	Back End
BW	Bandwidth
CAD	Computer Aided Design
CARM	Consolidated Addendum Rule Manual
CDM	Charge Device Model
CMOS	Complementary Metal-Oxide-Semiconductor
CR	Charge Redistribution
DAC	Digital to Analog Converter
DFM	Design for Manufacturability
DNL	Differential Non-Linearity
DNW	Deep Nwell
ENOB	Effective Number Of Bits
ESD	ElectroStatic Discharge
GO1	Thin Gate Oxide device
GO2	Thick Gate Oxide
INL	Integral Non-Linearity
IP	Intellectual Property
LDO	Low Drop Out regulator
OA	Open Access, Cadence IC 6 library standard
PCV	Process Corner Validated
PSRR	Power Supply Rejection Ratio
rms	root mean square
SAR	Successive Approximation Register
SF	Silicon Functional
SR2	Sub radix2
SINAD	Signal to Noise and Distortion Ratio
SVT	Standart Threshold Voltage
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SoC	System on Chip
SV	Silicon Validated
T&H or T/H	Track and Hold
TCB	Test Control Block
THD	Total harmonic Distortion, up to 5 Harmonics
TL	Test Level
TPR	Test Point Register

21. Glossary

21.1 Test levels

Table 22 lists the test levels, TL, that have been defined for analog IP blocks. Please note that these levels only indicate the maximum level to which a specification item will be tested over the total life cycle of the IP block. Which tests have been performed on a specific IP block depends on the maturity of this block.

Table 22. Test Level definitions

Test level	Definition
I	Tested over supply voltages and temperature, at multiple use-cases / settings
II	Tested over supply voltages and temperature, only at nominal bias settings
III	Tested over supply voltage and temperature, at nominal bias settings, statistics of parameter not tested
IV	Characterized by simulation only

22. References

[1] **Technology & Operations - AMS IP —** Analog IP information, ordering instructions and integration guidelines, nww.new.nxp.com/sites/business/how-we-work/rnd/ams-ip/analog_modules/Pages/default.aspx

[2] **Technology & Operations - CTAG.AMS —** CoReUse CTAG.AMS Cookbook, https://nww.wiki.nxp.com/display/DfTfX/Analog+Mixed+Signal

[3] **Technology & Operations - Design Services —** TSMC CLN28 Design Manual, https://nww.sharepoint.nxp.com/teams/65/SitePages/home.aspx

[4] **Enovia Design PDM —** Enovia Design Product Data Management, http://designpdm.nxp.com/

23. Revision history

Table 23. Revision history

Revision	Release date	Data sheet status
1.3	20210315	DfT XOR chain test mode added
1.2	20200123	Corrections/Changes that have been made: 1) Table 1 & section 12.2: pin set_ldo_vdda[2:0]: from 0.9V into 0.925V 1) section 12.2: from 6.25m into 6.25mV. 2) section 8.2.3.1: from sample & hold into T&H
1.1	20191023	Parameter offset, e_{offset} and $T_{start,pd}$ has been updated based on silicon results.
1.0	20181130	Preliminary data sheet

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 18 March 2021
Document identifier: -

24. Legal information

24.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://nww.ipyp.nxp.com.

24.2 Definitions

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