Additional information: <Delete this section of not required>

STRx ATB digital control IP

IP Design Report(AS)

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Document information

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Revision history

Rev	Date	Description
0.1	2019 01 06	Initial template proposal for IP AS
0.2	2020 06 01	Structure updated after review of RC_OSC design document. Still the old template, so another update is expected when the correct template becomes available; Structure based on assumption that a separate common control_top document is available in CNET (placeholder added); Integration section added.

Revision history

Rev	Date	Description

1. ATB Digital

1.1 Introduction

Control IPs for analog IPs are part of the RFE Dig. Figure 1 shows how a typical IP control module would be integrated in the RFE. It will be physically close to the analog IP, but it is part of RFE digital for supply and P&R.

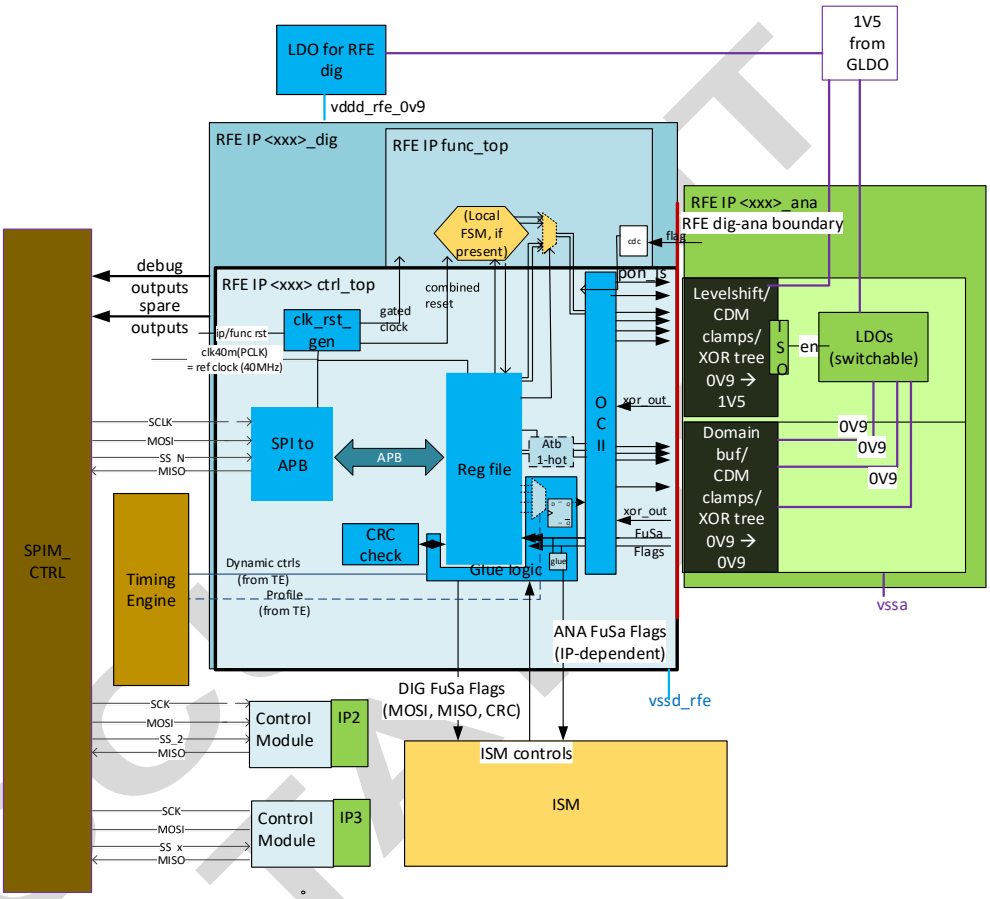

Figure 1: Digital Control IP for analog IPs in the RFE system – generic overview

The common part of all these RFE digital IPs is ctrl_top. The generic structure of ctrl_top and all its subIPs is described in detail in References:REF6.

1.2 Purpose of this IP

This IP controls the settings for the analog ATB.

1.3 IP architecture

ATB digital control consists of 2 parts: a control IP, named ida_mmw_rfe_atb_ctrl_top and a functional part named ida_mmw_rfe_atb_func_top. In the next sections these 2 subIPs will be addressed.

The block diagram of ATB-Dig and its relation to ATB-Ana are shown in Figure 2.

Note: not all details of ctrl_top are shown.

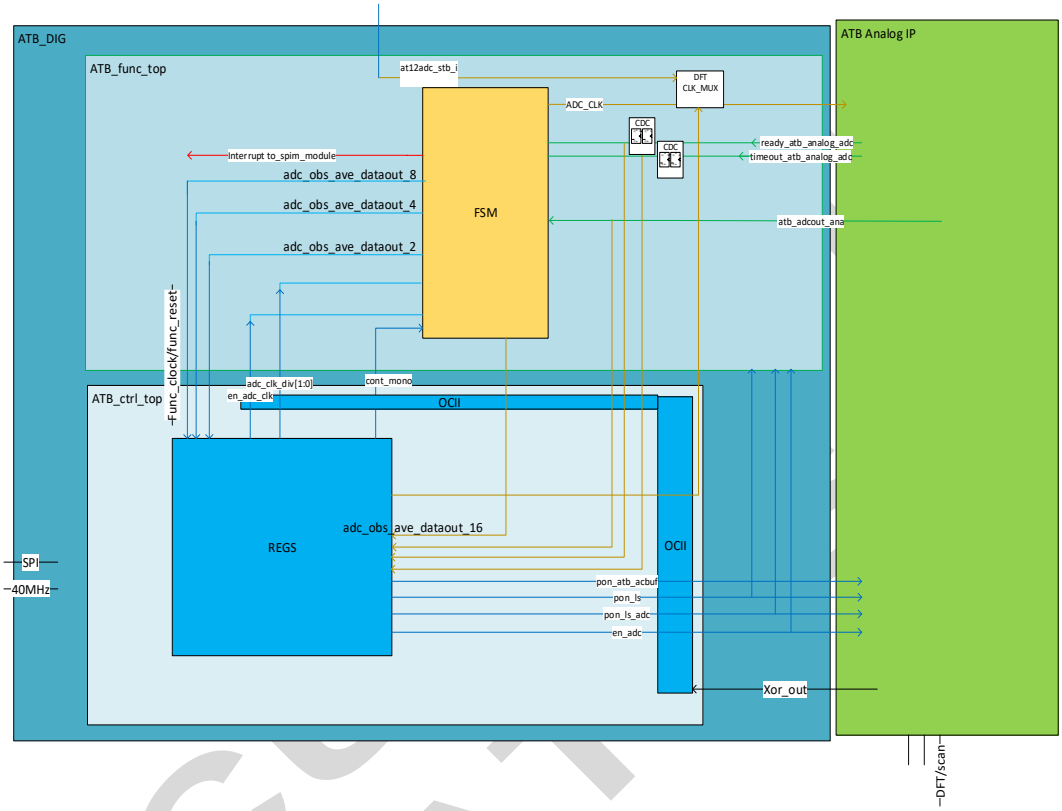

Figure 2: ATB DIG block diagram in its environment

1.3.1 IP interfaces

This digital IP interfaces with the following other IPs:

- ATB analog
- SPIM_CTRL
- ISM
- DFT control

See the Register map, Interface tab (References:REF5) for details.

1.3.2 Debug/Spare outputs from dig_top

For ATB, 6 debug outputs are currently used:

- Bit 0: adc1_ready_interrupt
- Bit 1: adc1_timeout
- Bit 2 : adc2_ready_interrupt
- Bit 3 : adc2_timeout
- Bit 4 : adc1_clock_en
- Bit 5 : adc2_clock_en

adc1/2_ready_interrupt, adc_1/2_timeout flags are the unlatched versions, straight from the analog IP.The spare outputs and spare inputs are unused. All unused outputs are tied off to 0; All unused inputs are dangling.

2. ATB ctrl_top

The IP control module will consist of the following subblocks:

1. Clock and reset generation unit
2. SPI slave with SPI2APB bridge
3. Register block with APB interface
4. CRC checker for the registers
5. OCII interface
6. ATB 1-hot decoder
7. Glue logic, handling the flags from the analog IP, OR-ing the power controls, etc.

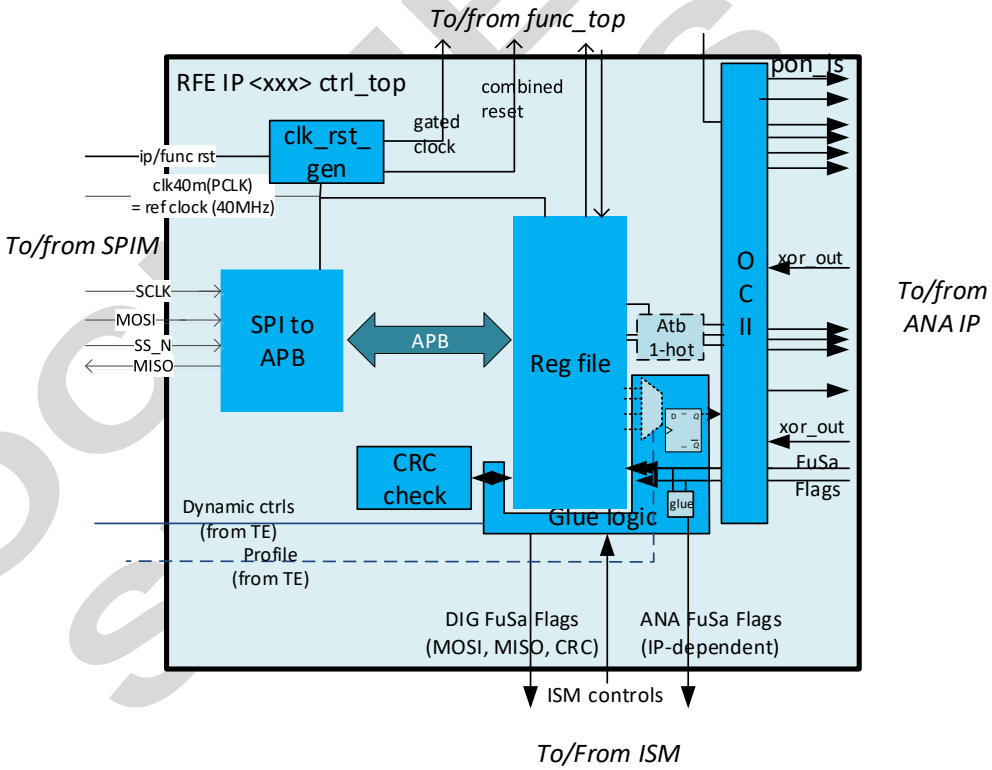

Figure 3: Generic view on a control IP (ctrl_top)

The register excel is the single source for most subblocks: register block, OCII, CRC are all generated based on this excel. Also the control IP interface will be included in the same excel, to avoid inconsistencies. The register map can be found on Collabnet, see also References:REF5.

2.1 Clock and reset generation unit

This is a standard subIP from ida_mmw_rfe_shared_dig_lib: ida_mmw_rfe_clk_rst_sync. Details of this subIP are provided in References:REF6.

2.2 SPI slave with SPI2APB bridge

The SPI slave is a standard subIP from ida_mmw_rfe_shared_dig_lib: ida_mmw_rfe_spi_to_apb. Details of this subIP are provided in References:REF6.

2.3 Register block

The register block will be generated using the Magillem tool flow. The input will be the IP excel file describing all registers, their widths, offset etc. The register excel for this IP can be found in References:REF5

Details of this subIP are provided in References:REF6.

2.4 CRC checker

The CRC block will be generated from the Register map using the Magillem tool flow. The core of the subIP uses a standard subIP from ida_mmw_rfe_shared_dig_lib: ida_mmw_rfe_reg_crc.

Details of this subIP are provided in References:REF6.

2.5 OCII interface

The OCII subIP is generated using the OCII tool in ida_ocii_global_lib - ida_global_ocii_generator_GEN2. This tool uses the OCII tab in the Register map. Details of this subIP are provided in References:REF6.

2.6 ATB 1-hot decoder

The ATB 1HOT decoder is a standard subIP from ida_mmw_rfe_shared_dig_lib: ida_mmw_rfe_atb_sel_dec.

Details of this subIP are provided in References:REF6.

2.7 Glue logic

The glue logic will be generated from the Register map using the Magillem tool flow.

The glue logic may contain various logic functions, as described in References:REF6.

- FuSa: Error flag masking, forcing, resetting
- Power-down/soft reset handling
- LDO bypass masking (from SPIM_CTRL)
- Profile muxing → not relevant for this IP
- Dynamic controls: PON control OR-ing (from Timing Engine and register map) → not relevant for this IP
- PON status flag towards ISM

In this section the deviations from the common ctrl_top glue control will be explained.

2.7.1 FuSa: Error masking, forcing, resetting

This IP has both analog and digital error flags.

All glue for force/reset/masking is according to the standard implementation.
Note that there are also some non-FuSa flags. These are not handled inside the glue logic. See section **Error! Reference source not found.** for details.

2.7.2 Power-down/soft reset handling

Standard implementation as described in References:REF6.

2.7.3 LDO bypass/cap_ctl masking

Like all IPs, the ATB contains controls that are OFF by default, and that should not be accidentally switched ON by SW. LDO bypass and cap_ctl (for Voltage stress) controls are in this section. Therefore a control from the SPIM, ldo_global_bypass_atb, is used to mask the LDO bypass register fields. Only if both controls are set to 1, the ldo_bypass output to the ATB will be set. A similar protection scheme is in place for all LDO_CAP_CTL fields, using the SPIM control ldo_global_cap_ctl_atb.

2.7.4 Profile multiplexing

Not relevant for the ATB

2.7.5 Dynamic controls from Timing Engine

Not relevant for the ATB

2.7.6 PON flag towards ISM

The PON flag towards the ISM is an AND combination of the levelshifter enable **pon_ctl_pon_ls** and **all** LDO enables.
In case of the ADC, part of the LDO enables are coming from the registers (LDOs that are NOT dynamically controlled.

The non-dynamic LDO enables are:

- ldo_0_ena_ldo1v35
- ldo_0_ena_ldo0v9
- pon_ls_adc_atb2
- pon_ls_adc_atb1
- pon_ls_atb

3. ATB functional

ATB Analog IP is having ADC, to sample the DC values of selected nodes across IP. The selection of the IP is done in SPIM_ISM IP. ADC data sampling and data averaging is implemented in ATB Functional block.

3.1 ADC CLK Generation:

ATB Analog ADC will be enabled when the register bit

ADC_CTL_FUNC(ADC1/2_CLOCK_EN) set to ‘1’. ATB Functional block generates the

ADC CLK of different clock frequencies 5 MHz, 4 MHz and 2.5 MHz based on the configuration set on **ADC_CTL_FUNC(ADC1/2_CLOCK_DIV)** and Duty cycle of 50 % and 75 % based on the configuration set on

ADC_CTL_FUNC(ADC1/2_DUTY_CYCLE_SET).

ADC clock generation will be handled via state machine.

3.1.1 ADC CLK generation FSM:

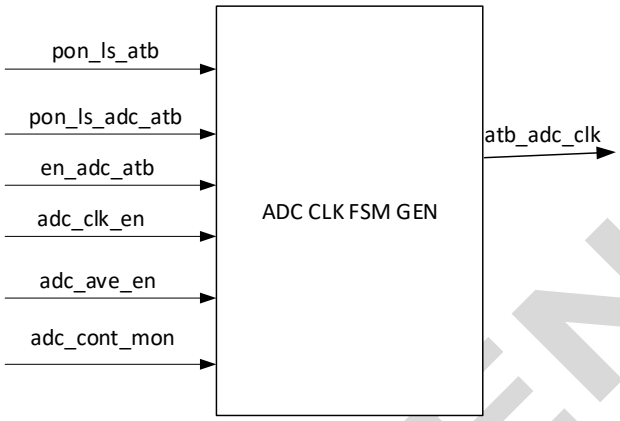

Figure 4 ADC CLK Generation Block Diagram

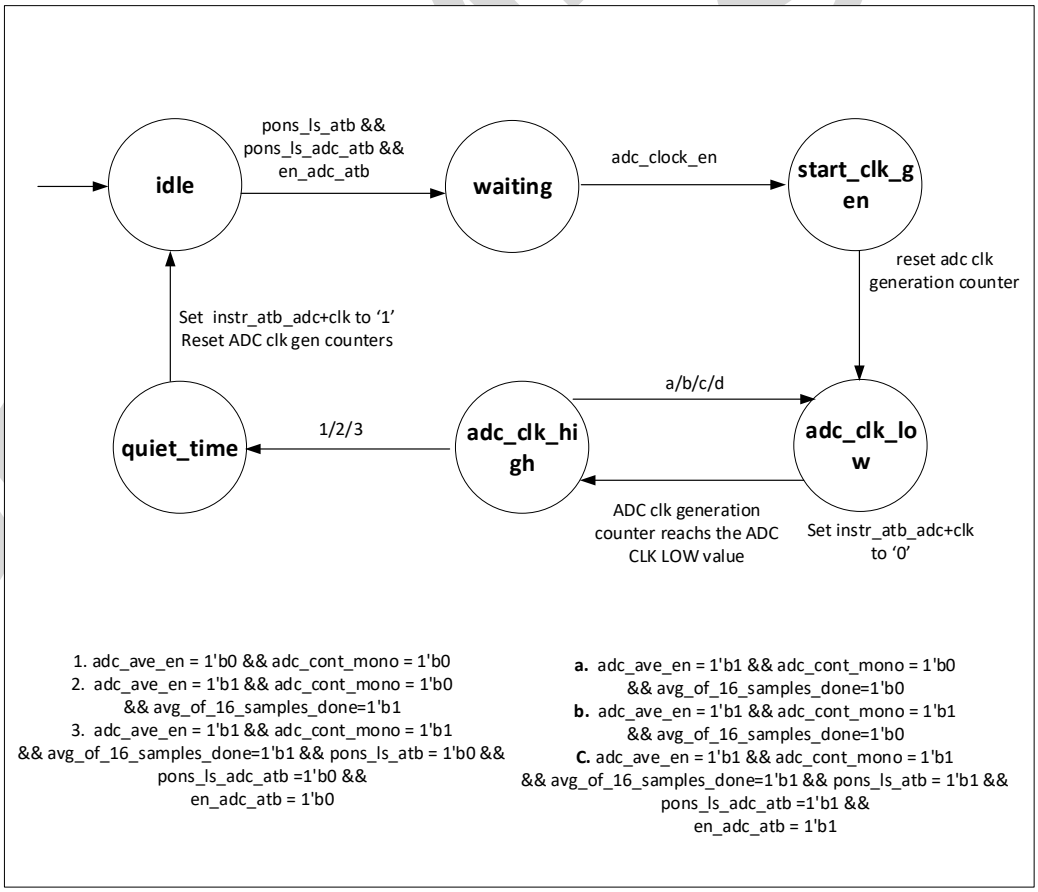

Figure 5 ADC CLK Generation FSM

3.2 ADC Data Averaging:

ADC data averaging is done in different modes.

3.2.1 MONO:

MONO mode is selected when the register bit **ADC_CTL_FUNC(ADC1/2_CONT_MONO)** to be set to ‘0’. In this mono mode there are 2 modes Average enable and Average dis-able.

ADC_RAW_SAMPLE: **ADC_OBS1(ADC1/2_DATA_OUT)** will update this register when

ADC1/2_READY (atb1_adc_ready_int) signal received from Analog ATB IP is set to ‘1’. ADC data (atb_adc1_data_out_ana) received from the Analog IP will be latched in this register on the falling edge of the ADC1/2_READY.

Average enable ADC_CTL_FUNC (ADC1/2_AVE_EN): When Average mode is enabled ATB, Functional block generates 16 ADC CLK. The sampled ADC data is averaged as follows

ADC_AVERGAE_2: **ADC_AVE_OBS2**(ADC1/2_DATA_OUT_2) registers will update with average of last 2 ADC samples. Hence this register will update 8 times with new values.

ADC_AVERGAE_4: **ADC_AVE_OBS4(**ADC1/2_DATA_OUT_4) registers will update with average of last 4 ADC samples, Hence this register will update 4 times with new values.

ADC_AVERAGE_8: **ADC_AVE_OBS8(**ADC1/2_DATA_OUT_8) registers will update with average of last 8 ADC samples, Hence this register will update 2 times with new values.

ADC_AVERAGE_16 : **ADC_AVE_OBS16(**ADC1/2_DATA_OUT_16) register will update with average of last 16 ADC samples. Hence this register will update only 1 time.

An interrupt is generated towards SPIM_ISM block once 16 ADC samples latched and average is done.

Average dis-able ADC_CTL_FUNC (ADC1/2_AVE_EN) : When Average mode is dis-abled ATB Functional block generate 1 ADC CLK. The sampled ADC values is stored in register **ADC_OBS1(ADC1/2_DATA_OUT)**. To re-initiate ADC sampled user need to set **ADC_CTL_FUNC(ADC1/2_CLOCK_EN)** set to ‘1’.

3.2.2 CONT:

CONT mode is selected when the register bit ADC_CTL_FUNC(ADC1/2_CONT_MONO) to be set to ‘1’ and average enable bit in the register ADC_CTL_FUNC (ADC1/2_AVE_EN) to be set to ‘1’. In this mode ATB Functional block generates ADC CLK continuously until ADC_CTL_FUNC(ADC1/2_CONT_MONO) bit is set to ‘0’.

ADC_AVERGAE_2: **ADC_AVE_OBS2**(**ADC1/2_DATA_OUT_2**) registers will update with average of last 2 ADC samples. Hence this register will update 8 times with new values.

ADC_AVERGAE_4: **ADC_AVE_OBS4(ADC1/2_DATA_OUT_4**) registers will update with average of last 4 ADC samples, Hence this register will update 4 times with new values.

ADC_AVERAGE_8: **ADC_AVE_OBS8(ADC1/2_DATA_OUT_8**) registers will update with average of last 8 ADC samples,

Hence this register will update 2 times with new values.

ADC_AVERAGE_16: **ADC_AVE_OBS16(ADC1/2_DATA_OUT_16**) register will update with average of last 16 ADC samples. Hence this register will update only one time.

All above register will hold previous averaged ADC values until the next 16 cycles going to start. An interrupt is generated towards SPIM_ISM block once 16 samples of ADC data is latched and averaged is done.

3.2.3 ADC Data Averaging FSM:

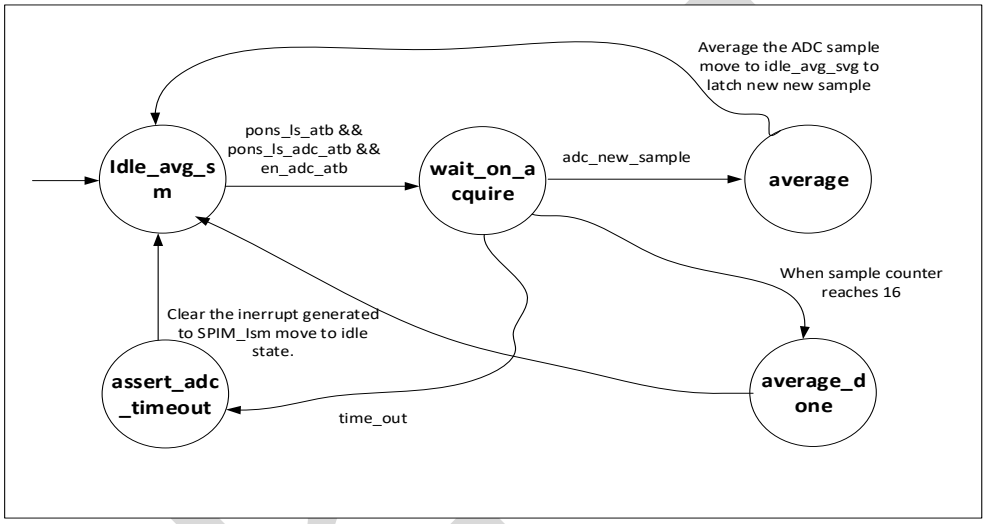

Figure 6 ADC Data Averaging FSM

4. Integration

4.1 Critical timing

This is a plain SPI IP. No critical timing for any signals.

4.2 Special considerations

5. References

Table 1: references

Ref number	Document section	Document description	Document Link
1.	RFE Control and Digital	RFE IP power controls	REF1 [link]
2.	RFE Control and Digital	RFE IP guidelines for registers	REF2 [link]
3.	RFE Control and Digital	M7 interface and SPI	REF3 [link]
4.	References	OCII specification	REF4 [link]
5.	Reg map XLS for all IPs	ATB register map	REF5 [LINK]
6.	IP design document	Common control top	placeholder

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