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TDC Func digital

IP Design Report(AS)

Rev. 0.6 — 21 July 2021 **Design Report**

Document information

Info	Content
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Department	BL-RFP, <site>
Keywords	STRX, <IP>
Abstract	Design description for the TDC digital functional IP
SGI	<value>
ECCN	<code>
US origin	No

Distribution information

Name	Department	Address

Revision history

Rev	Date	Description
0.1	2021 04 26	Updated template
0.2	2021 05 04	Updates FSM and timing diagram(Figure 2)
0.3	2021 05 27	Structure updated; Descriptions for error status flags and FSM added
0.5	2021 06 07	Updated after review. Status updated to PROPOSED
0.6	2021 07 21	FSM working flow updated

1. Tempsensor (TDC) digital

1.1 Introduction

Control Ips for analog Ips are part of the RFE Dig. Figure 1 shows how a typical IP digital control module would be integrated in the RFE. It will be physically close to the analog IP, but it is part of RFE digital for supply and P&R. Common part of all these RFE digital IPs is ctrl_top.

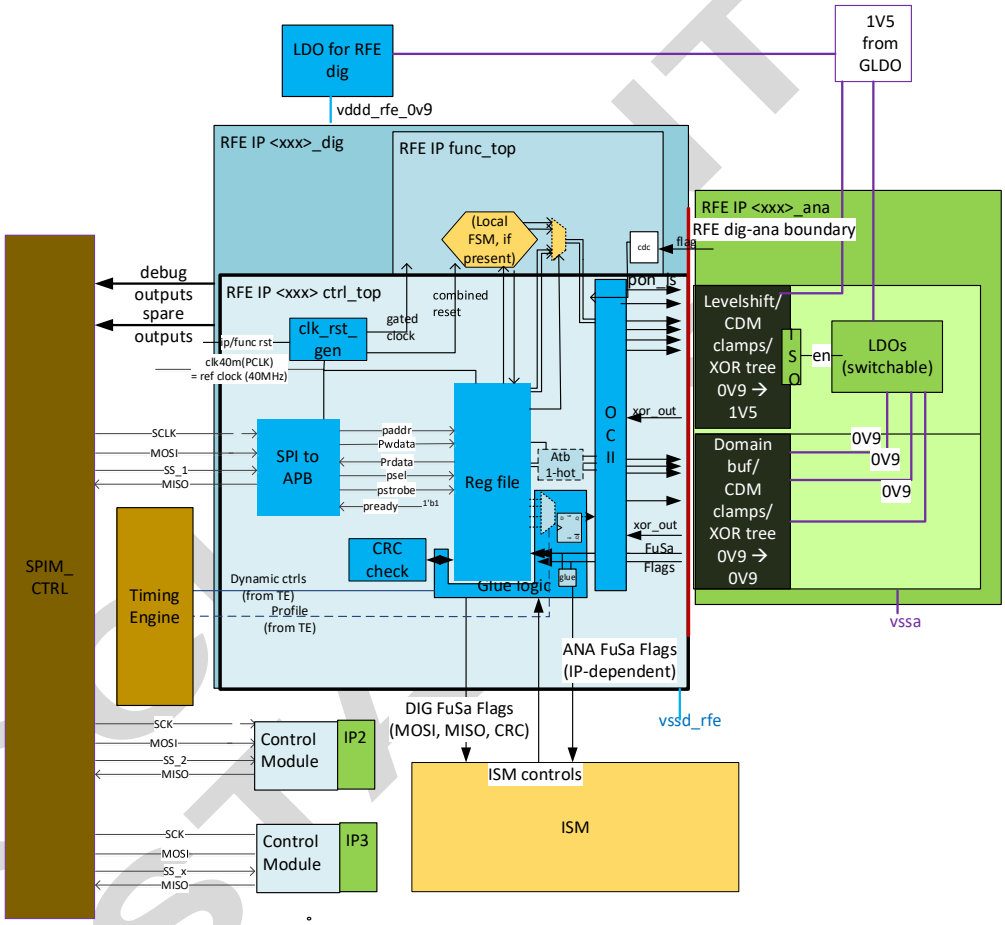

Figure 1: Digital Control IP for analog Ips in RFE system – generic overview

The generic structure of ctrl_top is described in detail in References: REF4.

1.2 IP architecture

TDC digital control consists of 2 parts: a control IP, named ida_mmw_rfe_tempsensor_ctrl_top and a functional part named ida_mmw_rfe_tempsensor_func_top. TDC Functional part will be addressed in this document.

2. Tempsensor Ctrl_top

The IP control_top is described in separate document. See REF1

3. Tempsensor functional: func_top

The Tempsensor functional block mainly contains state machine which is responsible to signals towards the temperature sensor, capture the readings and store the status in IP registers.

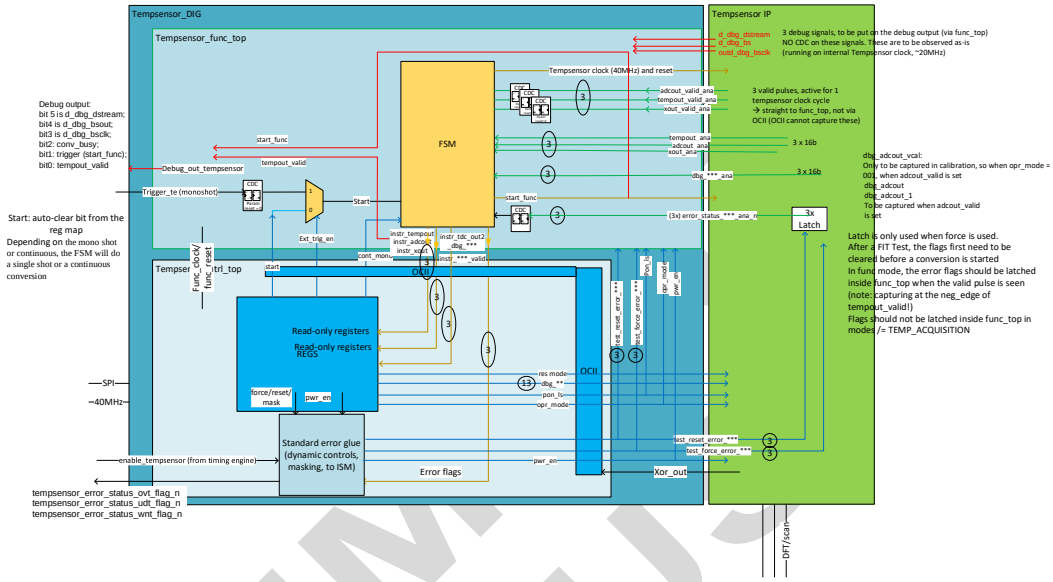

Figure 2: tempsensor DIG block diagram (consists ctrl_top and functional_top)

In TempSense func_top, the valid signals (adcout, xout and tempout) and error status signals from analog IP will be treated as asynchronous and will pass through CDC. The data from analog IP will be received when the valid signals are seen and the flow is given in FSM. The error status flags from analog IP are controlled by test_force_error and test_reset_error signals. After FIT test, the flags need to bleared before a conversion started. The error flags will be latched in func_top at falling edge of tempout_valid signal. These error flags can be cleared via the test_reset_error control and forced with test_force_error signal.

3.1 Tempsensor FSM

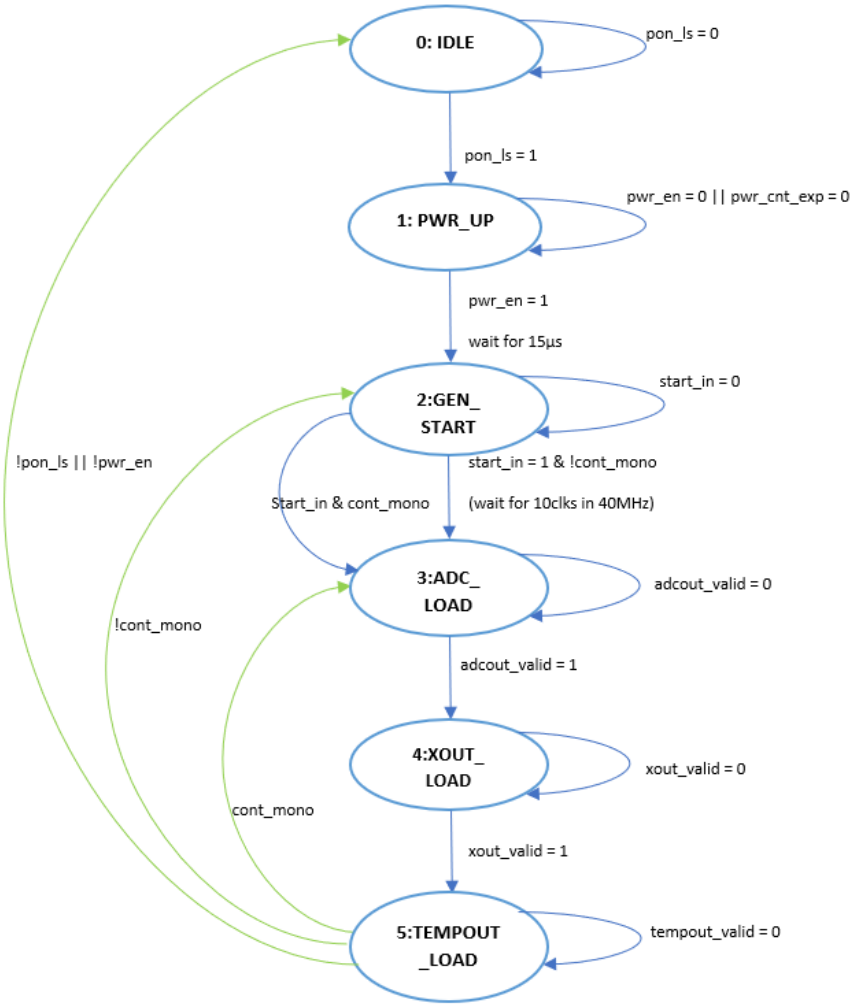

Figure 3: TDC functional State machine

0:IDLE
start_int = 0
tdc_status_conv_busy = 0
enable_pwrup_cnt = 0
tempout_valid_instr = 0

1: PWR_UP
start_int = 0
tdc_status_conv_busy = 0
enable_pwrup_cnt = 1
tempout_valid_instr = 0

2: GEN_START
2_a)start_int = 1
tdc_status_conv_busy = 1
enable_pwrup_cnt = 0
tempout_valid_instr = 0

2_b)start_int = 0
tdc_status_conv_busy = 0
enable_pwrup_cnt = 0
tempout_valid_instr = 0

3: ADCOUT_LOAD
start_int = 1/0
tdc_status_conv_busy = 1
enable_pwrup_cnt = 0
tempout_valid_instr = 0

4:XOUT_LOAD
start_int = 0/1
tdc_status_conv_busy = 1
enable_pwrup_cnt = 0
tempout_valid_instr = 0

5: TEMPOUT_LOAD
5_a)cont_mono = 1
start_int = 1
tdc_status_conv_busy = 1
enable_pwrup_cnt = 0
tempout_valid_instr = 1

5_b)cont_mono=0
start_int = 0
tdc_status_conv_busy = 0
enable_pwrup_cnt = 0
tempout_valid_instr = 1

The FSM runs on the system clock: 40MHz from Ctrl_top and the same will be given towards tempsensor but it runs on 20MHz clock which is divided inside the tempsensor analog IP. To ensure that signals from tempsensor towards FSM without issues, CDC (clock domain crossing) blocks are used.

State machine will run with some default values but can be programmed with control signals. The default mode of operation is acquisition mode and the conversion type is Single conversion. During the Load stage – the various status registers are updated with the values obtained after the temperature acquisition. The register map can be found in collabnet, see REF3.

For calibration the opr_mode<2:0> should be set to “001”. The same state machine above is executed in the calibration mode as well but in addition debug ADC value dbg_adcout_vcal will be captured to the register.

In FSM flow, all the signals are in reset state in IDLE and move to PWR_UP state once pon_ls is given. After pwr_en is high, the fsm will wait to finish the power_up counter in PWR_UP state. In GEN_START state, fsm will check for the mode of operation and follows the next states and will check for the next conversion in TEMPOUT_LOAD state. If power signals are low then fsm moves to IDLE state otherwise the next conversion starts based on conversion type.

If pon_ls is 0 , except in IDLE state it won’t affect the process, move to next state. Except IDLE and PWR_UP states, FSM remain in the same state if pwr_en is removed.

3.2 Timing diagram

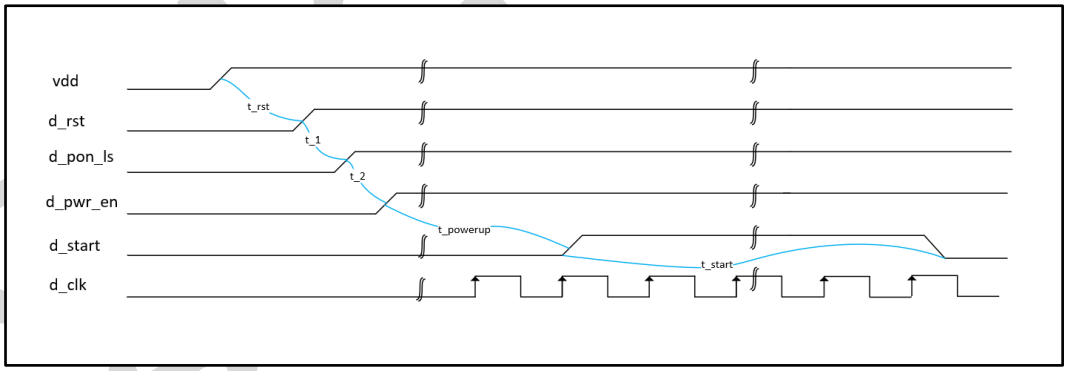

Figure 4: Internal Timing diagram : Initialization

The functional clock and the clock to Tempsensor is 40MHz. The signal func_rst_n is connected to power-on-reset (POR) output of the digital supply domain, this will make sure that TDC get reseted after powerup. The time t_rstn is then controlled by POR circuit after ramping up the digital power Vdd. After time t_1 pon_ls is enabled. The signals pon_ls and pwr_en are register controls, so the timing t_1 and t_2 are determined by software. Internal powerup counter will start incrementing when pwr_up signal rising edge is detected and counts till t_powerup (15µs) time to allow analog core to be properly power up before sending the start signal. The start signal should be high for a minimum time of t_start for a single conversion and can be held high to enable continuous conversion.

3.2.1.1 MONO (Single conversion)

MONO mode is selected when the register bit CONT_MONO is set to ‘0’. A conversion can be started by triggering either the start signal from control status register or timing engine (auto clear bit). Internal signal start_int generated using the start input and making the signal high for a minimum of 4 clock periods (with respect to 20MHz) and bring down the signal before the conversion ends. The FSM status signal tdc_status_conv_busy will be high until the conversion complete. In MONO mode, start to be triggered for every new conversion.

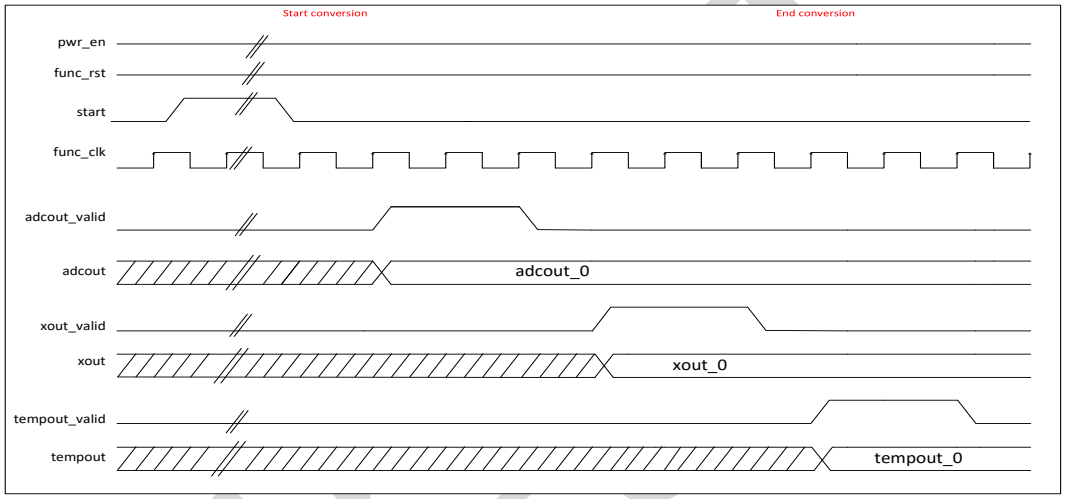

Figure 5: Single conversion timing diagram

3.2.1.2 CONT (continuous conversion)

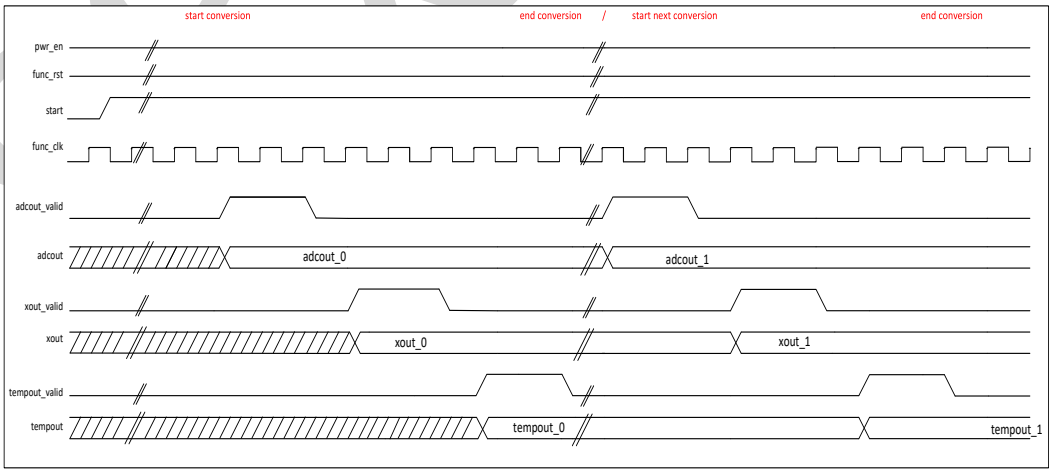

Figure 6: Continuous conversion timing diagram

CONT (continuous conversion)mode is selected when the register bit CONT_MONO is set to ‘1’. Continuous conversion can be started by keeping the start signal high and it can be stopped by setting CONT_MONO to ‘0’ (before last adcout_valid signal becomes low, to avoid extra conversion). When the start signal is removed before ending the

ongoing conversion, fsm will continue until the current conversion complete. TDC status signal and start to tempsensor will be removed in the last tempout_load state of the fsm.

3.2.2 Operation modes

The operation modes of tempsensor is controlled by opr_mode<2:0> input. Not all combinations are assigned to an actual mode of the IP and some are reserved for future use if necessary.

Table 1: Operation mode input selection

OPR_MODE<2:0>	CORRESPONDING OPERATION MODES
000	Temperature acquisition mode
001	Voltage calibration mode
010	BIST mode, test ADC
011	BIST mode, test BJT core
100	reserved, at this moment default to temperature acquisition mode
101	reserved, at this moment default to temperature acquisition mode
110	reserved, at this moment default to temperature acquisition mode
111	reserved, at this moment default to temperature acquisition mode

3.2.2.1 Temperature acquisition mode

Temperature acquisition mode will be selected when the opr_mode<2:0> is set to ‘000’. In this mode, temperature measurement reading can be done from sensor. Both MONO mode and CONT conversions can be done in temperature acquisition mode. Here, adcout_ana<15:0>, xout_ana<15:0> and tempout_ana<15:0> values will be read when corresponding adcout_valid, xout_valid and tempout_valid signals are available. The captured readings will be latched into registers.

3.2.2.2 Voltage calibration mode

Voltage calibration mode will be selected when opr_mode is set to ‘001’. In this mode, by using an external supply voltage, the internal voltage of TDC is determined and hence the die temperature in sensor block. In addition to the adcout_ana, xout_ana and tempout_ana readings from tempsensor, dbg_adcout_vcal will be captured in voltage calibration mode.

Refer the document REF2

3.2.2.3 BIST mode (test ADC, test BJT)

BIST mode detailed explanation available in the document REF2

3.3 Debug/Spare outputs

For Tempsensor, 6 debug outputs are used.

- bit 0: tempout_valid_intr
- bit 1: start_func
- bit 2: tdc_status_conv_busy
- bit 3: dbg_bsclk (from the analog)
- bit 4: dbg_bsout (from the analog)
- bit 5: dbg_dstream (from the analog)

The spare outputs and spare inputs are unused. All unused outputs are tied off to 0. All unused inputs are dangling.

4. References

Table 2: References

Ref number	Document section	Document description	Document Link
1.	RFE Control and Digital	Tempsensor control top	REF1 [Link]
2.	RFE Control and Digital	TDC analog	REF2 [Link]
3.	RFE Control and Digital	TDC register map	REF3 [Link]
4.	IP Design document	Common control top	REF4 [Link]

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7. Content

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Date of release: 21 July 2021
Document identifier: <DOC_ID>

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