rfe_fuSaFault_R1_sm4_bb_tx2_e rfe_fuSaFault_R1_sm4_bb_tx2_e rfe_fuSaFault_R1_sm5_bb_tx3_e rfe_fuSaFault_R1_sm8_paout_rtm_tx1_e rfe_fuSaFault_R1_sm8_paout_rtm_tx2_e rfe_fuSaFault_R1_sm8_paout_rtm_tx2_e rfe_fuSaFault_R1_sm8_paout_rtm_tx2_e rfe_fuSaFault_R1_sm8_paout_rtm_tx4_e rfe_fuSaFault_R1_sm1_paout_rtm_tx4_e rfe_fuSaFault_R1_sm11_bist_tx1_tx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm11_bist_tx1_phaseStep_sw_e rfe_fuSaFault_R1_sm11_bist_tx2_phaseStep_sw_e rfe_fuSaFault_R1_sm12_bist_tx2_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx3_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx3_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx3_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm14_bb_rx4_e rfe_fuSaFault_R1_sm15_bb_rx4_e rfe_fuSaFault_R1_sm16_bb_rx2_e rfe_fuSaFault_R1_sm18_bb_rx4_e rfe_fuSaFault_R1_sm18_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm20_or_gld1v4_gldo_e rfe_fuSaFault_R1_sm20_or_gld1v4_gldo_e rfe_fuSaFault_R1_sm20_or_gld1v4_gldo_e rfe_fuSaFault_R1_sm30_or_hld1v8_gldo_e rfe_fuSaFault_R1_sm30_or_hld1v8_gldo_e rfe_fuSaFault_R1_sm30_or_hld1v8_gldo_e rfe_fuSaFault_R1_sm30_or_hld1v8_gldo_e rfe_fuSaFault_R1_sm30_or_hld1v8_gldo_e rfe_fuSaFault_R1_sm30_or_hld1v8_gldo_e rfe_fuSaFault_R1_sm30_or_hld1v8_gldo_e rfe_fuSaFault_R1_sm30_or_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_leve	Fusa Pass - Validated List - SAF85xx_RFE_SW_EAR_0.8.18_D230823
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rfe_fuSaFault_R1_sm11_bist_tx1_phaseStep_sw_e rfe_fuSaFault_R1_sm12_bist_tx2_tx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm12_bist_tx2_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx3_tx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm13_bist_tx3_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm15_bb_rx1_e rfe_fuSaFault_R1_sm16_bb_rx2_e rfe_fuSaFault_R1_sm16_bb_rx4_e rfe_fuSaFault_R1_sm18_bb_rx4_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_alco_kchirp_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_alco_kchirp_e rfe_fuSaFault_R1_sm50_sucloc_kchirp_e rfe_fuSaFault_R2_sm60_sd_chirp_e rfe_fuSaFault_R2_sm60_sd_chirp_e rfe_fuSaFault_R2_sm60_sd_chirp_e rfe_fuSaFault_R2_sm80_sm60_reg_crc_e rfe_fuSaFault_R2_sm80_sm60_reg_crc_e rfe_fuSaFault_R2_sm80_sm80_m7_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_m7_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_m7_tcm_sram_e rfe_	
rfe_fuSaFault_R1_sm12_bist_tx2_tx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm12_bist_tx2_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx3_tx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm13_bist_tx3_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm15_bb_rx1_e rfe_fuSaFault_R1_sm16_bb_rx2_e rfe_fuSaFault_R1_sm16_bb_rx2_e rfe_fuSaFault_R1_sm17_bb_rx3_e rfe_fuSaFault_R1_sm18_bb_rx4_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm20_yo_gld1v3_gldo_e rfe_fuSaFault_R1_sm20_yo_gld1v4_gldo_e rfe_fuSaFault_R1_sm20_yo_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_ichirp_e rfe_fuSaFault_R1_sm50_ichirp_e rfe_fuSaFault_R1_sm50_ichirp_e rfe_fuSaFault_R1_sm50_ichirp_e rfe_fuSaFault_R1_sm50_ichirp_e rfe_fuSaFault_R1_sm50_ichirp_e rfe_fuSaFault_R2_sm60_sm60_reg_crc_e rfe_fuSaFault_R2_sm80_sm80_m7_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_m7_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_m7_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_m7_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_m7_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_m7_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_m7_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_m7_tcm_sram_e rfe_f	
rfe_fuSaFault_R1_sm12_bist_tx2_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx3_tx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm13_bist_tx3_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm15_bb_rx1_e rfe_fuSaFault_R1_sm15_bb_rx1_e rfe_fuSaFault_R1_sm15_bb_rx2_e rfe_fuSaFault_R1_sm16_bb_rx2_e rfe_fuSaFault_R1_sm18_bb_rx4_e rfe_fuSaFault_R1_sm18_bb_rx4_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm29_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_lock_chirp_e rfe_fuSaFault_R1_sm50_gc_irip_e rfe_fuSaFault_R1_sm50_gc_irip_e rfe_fuSaFault_R1_sm50_gc_irip_e rfe_fuSaFault_R1_sm50_gc_irip_e rfe_fuSaFault_R1_sm60_gc_irip_e rfe_fuSaFault_R2_sm60_gc_irip_e rfe_fuSaFault_R2_sm60_gc_irip_e rfe_fuSaFault_R2_sm80_sm60_reg_crc_e rfe_fuSaFault_R2_sm80_sm80_rre_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_mr_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_mr_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_mr_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_mr_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_mr_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_mr_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_mr_tcm_sram_e rfe_fuSaFault_R2_sm80_sm80_mr_tcm_sram_e rfe_fuSaFault_R2_sm80_sm0_ysi_ucretc_res_crc_sw_e rfe_fuSaFault_R2_sm80_sm0_ysi_ucretc	
rfe_fuSaFault_R1_sm13_bist_tx3_tx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm13_bist_tx3_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm15_bb_rx1_e rfe_fuSaFault_R1_sm16_bb_rx2_e rfe_fuSaFault_R1_sm16_bb_rx2_e rfe_fuSaFault_R1_sm17_bb_rx3_e rfe_fuSaFault_R1_sm18_bb_rx4_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_painDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm28_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_	
rfe_fuSaFault_R1_sm13_bist_tx3_phaseStep_sw_e rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm15_bb_rx1_e rfe_fuSaFault_R1_sm16_bb_rx2_e rfe_fuSaFault_R1_sm16_bb_rx3_e rfe_fuSaFault_R1_sm18_bb_rx4_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm58_cg_chirp_e rfe_fuSaFault_R1_sm50_sd_chirp_e rfe_fuSaFault_R1_sm50_sd_chirp_e rfe_fuSaFault_R1_sm50_sd_chirp_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm93_sbic_integrity_check_e rfe_fuSaFault_R2_sm93_sbic_integrity_check_e rfe_fuSaFault_R2_sm93_sbic_integrity_check_e rfe_fuSaFault_R2_sm93_sbic_integrity_check_e rfe_fuSaFault_R2_sm93_sbic_integrity_check_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm94_m7_message_e2e_c	
rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e rfe_fuSaFault_R1_sm15_bb_rx1_e rfe_fuSaFault_R1_sm16_bb_rx2_e rfe_fuSaFault_R1_sm17_bb_rx3_e rfe_fuSaFault_R1_sm27_bb_rx4_e rfe_fuSaFault_R1_sm28_bbr_x4_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_painDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm20_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm20_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm30_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R2_sm68_sm69_reg_ccc_e rfe_fuSaFault_R2_sm68_sm69_reg_ccc_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm98_sm89_m7_tcm_sram_e rfe_fuS	rfe_fuSaFault_R1_sm13_bist_tx3_tx4_phaseDiff_sw_e
rfe_fuSaFault_R1_sm15_bb_rx1_e rfe_fuSaFault_R1_sm16_bb_rx2_e rfe_fuSaFault_R1_sm17_bb_rx3_e rfe_fuSaFault_R1_sm18_bb_rx4_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_panseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm30_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R2_sm60_sd_chirp_e rfe_fuSaFault_R2_sm60_sd_chirp_e rfe_fuSaFault_R2_sm60_sd_chirp_e rfe_fuSaFault_R2_sm60_sd_chirp_e rfe_fuSaFault_R2_sm80_sm60_sd_chirp_e rfe_fuSaFault_R2_sm80_sm60_sd_chirp_e rfe_fuSaFault_R2_sm80_s	rfe_fuSaFault_R1_sm13_bist_tx3_phaseStep_sw_e
rfe_fuSaFault_R1_sm16_bb_rx2_e rfe_fuSaFault_R1_sm17_bb_rx3_e rfe_fuSaFault_R1_sm18_bb_rx4_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_level_high_chirp_e rfe_fuSaFault_R1_sm50_level_high_chirp_e rfe_fuSaFault_R1_sm50_gc_chirp_e rfe_fuSaFault_R1_sm50_gc_chirp_e rfe_fuSaFault_R1_sm50_gc_chirp_e rfe_fuSaFault_R1_sm50_gc_chirp_e rfe_fuSaFault_R1_sm50_gc_chirp_e rfe_fuSaFault_R1_sm50_gc_chirp_e rfe_fuSaFault_R1_sm50_gc_chirp_e rfe_fuSaFault_R2_sm60_gc_chirp_e rfe_fuSaFault_R2_sm80_gc_chirp_e rf	rfe_fuSaFault_R1_sm13_bist_tx4_phaseStep_sw_e
rfe_fuSaFault_R1_sm17_bb_rx3_e rfe_fuSaFault_R1_sm18_bb_rx4_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm28_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm54_level_hiph_chirp_e rfe_fuSaFault_R1_sm58_c_g_chirp_e rfe_fuSaFault_R1_sm58_c_chirp_e rfe_fuSaFault_R1_sm58_li_chirp_e rfe_fuSaFault_R1_sm58_li_chirp_e rfe_fuSaFault_R1_sm50_lockstep_te_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm98_sm9_m7_tcm_sram_e rfe_fuSaFault_R2_sm98_sm9_m7_tcm_sram_e rfe_fuSaFault_R2_sm98_sm9_m7_tcm_sram_e rfe_fuSaFault_R2_sm98_sm9_m7_tcm_sram_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_spi_write_check_fail_sw_e	rfe_fuSaFault_R1_sm15_bb_rx1_e
rfe_fuSaFault_R1_sm18_bb_rx4_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_uv_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm30_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm50_i_chirp_e rfe_fuSaFault_R1_sm50_i_chirp_e rfe_fuSaFault_R1_sm50_i_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm62_lockstep_te_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_sm9_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_sm9_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_sm9_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rf	rfe_fuSaFault_R1_sm16_bb_rx2_e
rfe_fuSaFault_R1_sm18_bb_rx4_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_uv_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm30_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm50_i_chirp_e rfe_fuSaFault_R1_sm50_i_chirp_e rfe_fuSaFault_R1_sm50_i_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm62_lockstep_te_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_sm9_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_sm9_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_sm9_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm89_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rf	rfe_fuSaFault_R1_sm17_bb_rx3_e
rfe_fuSaFault_R1_sm23_bist_rx1_rx2_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm50_i_chirp_e rfe_fuSaFault_R1_sm50_i_chirp_e rfe_fuSaFault_R1_sm50_i_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm99_spi_write_check_e rfe_fuSaFault_R2_sm99_spi_write_check_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_dd_m_rfe_m7_core_sw_redundancy_e	rfe_fuSaFault_R1_sm18_bb_rx4_e
rfe_fuSaFault_R1_sm23_bist_rx1_rx3_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_uv_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm54_level_high_chirp_e rfe_fuSaFault_R1_sm58_cg_chirp_e rfe_fuSaFault_R1_sm58_cg_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm50_ad_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm204_dm_rfe_m7_core_sw_redundancy_e	
rfe_fuSaFault_R1_sm23_bist_rx1_rx4_gainDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_uv_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm54_level_high_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm55_ucchirp_e rfe_fuSaFault_R1_sm50_ad_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm63_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm69_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_spi_write_check_fail_sw_e	
rfe_fuSaFault_R1_sm23_bist_rx1_rx2_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_uv_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm50_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm69_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm904_dm_rfe_m7_core_sw_redundancy_e	
rfe_fuSaFault_R1_sm23_bist_rx1_rx3_phaseDiff_sw_e rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_uv_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm54_level_high_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm58_cg_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm50_ichirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm83_rfe_test_mode_active_e rfe_fuSaFault_R2_sm83_rfe_test_mode_active_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e	
rfe_fuSaFault_R1_sm23_bist_rx1_rx4_phaseDiff_sw_e rfe_fuSaFault_R1_sm28_ov_gld1v3_gldo_e rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm54_level_high_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm58_cg_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm83_rfe_test_mode_active_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm98_sm7_pi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e	
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rfe_fuSaFault_R1_sm29_ov_gld1v4_gldo_e rfe_fuSaFault_R1_sm29_uv_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm46_xo_pllclk_det_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm54_level_high_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm92_sw_wdt_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_ddm_rfe_m7_core_sw_redundancy_e	
rfe_fuSaFault_R1_sm29_uv_gld1v4_gldo_e rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm46_xo_pllclk_det_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm54_level_high_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_mf9_tcm_e rfe_fuSaFault_R2_sm88_mf9_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm92_sw_wdt_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm94_m7_message_e2e_crc_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_ddm_rfe_m7_core_sw_redundancy_e	
rfe_fuSaFault_R1_sm31_ov_hld1v8_gldo_e rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm46_xo_pllclk_det_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm54_level_high_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm62_lockstep_te_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm89_m7_crc_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_ddm_rfe_m7_core_sw_redundancy_e	
rfe_fuSaFault_R1_sm31_uv_hld1v8_gldo_e rfe_fuSaFault_R1_sm46_xo_pllclk_det_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm54_level_high_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_ddm_rfe_m7_core_sw_redundancy_e	
rfe_fuSaFault_R1_sm46_xo_pllclk_det_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_max_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm54_level_high_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm83_rfe_test_mode_active_e rfe_fuSaFault_R2_sm87_m7_rfe_lockup_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm92_sw_wdt_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R1_sm94_m7_message_e2e_crc_sw_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e	
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rfe_fuSaFault_R1_sm50_adpll_dco_level_min_mcgen_e rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm54_level_high_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm58_cg_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm62_lockstep_te_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm70_mosi_miso_crc_e rfe_fuSaFault_R2_sm83_rfe_test_mode_active_e rfe_fuSaFault_R2_sm87_m7_rfe_lockup_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm92_sw_wdt_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R1_sm94_m7_message_e2e_crc_sw_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e	
rfe_fuSaFault_R1_sm54_level_low_chirp_e rfe_fuSaFault_R1_sm54_level_high_chirp_e rfe_fuSaFault_R1_sm54_level_high_chirp_e rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm58_cg_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm62_lockstep_te_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm70_mosi_miso_crc_e rfe_fuSaFault_R2_sm83_rfe_test_mode_active_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm98_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R1_sm94_m7_message_e2e_crc_sw_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_spi_write_check_fail_sw_e	
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rfe_fuSaFault_R1_sm55_unlock_chirp_e rfe_fuSaFault_R1_sm58_cg_chirp_e rfe_fuSaFault_R1_sm58_cg_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm62_lockstep_te_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm88_sm69_reg_crc_e rfe_fuSaFault_R2_sm83_rfe_test_mode_active_e rfe_fuSaFault_R2_sm87_m7_rfe_lockup_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm92_sw_wdt_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R1_sm94_m7_message_e2e_crc_sw_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm204_dm_rfe_m7_core_sw_redundancy_e	rfe_fuSaFault_R1_sm54_level_low_chirp_e
rfe_fuSaFault_R1_sm58_cg_chirp_e rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm62_lockstep_te_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm70_mosi_miso_crc_e rfe_fuSaFault_R2_sm70_mosi_miso_crc_e rfe_fuSaFault_R2_sm83_rfe_test_mode_active_e rfe_fuSaFault_R2_sm87_m7_rfe_lockup_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm92_sw_wdt_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R1_sm94_m7_message_e2e_crc_sw_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm90_dm_rfe_m7_core_sw_redundancy_e	
rfe_fuSaFault_R1_sm59_li_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm62_lockstep_te_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm70_mosi_miso_crc_e rfe_fuSaFault_R2_sm70_mosi_miso_crc_e rfe_fuSaFault_R2_sm83_rfe_test_mode_active_e rfe_fuSaFault_R2_sm87_m7_rfe_lockup_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm92_sw_wdt_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R1_sm94_m7_message_e2e_crc_sw_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm204_dm_rfe_m7_core_sw_redundancy_e	rfe_fuSaFault_R1_sm55_unlock_chirp_e
rfe_fuSaFault_R1_sm60_sd_chirp_e rfe_fuSaFault_R1_sm62_lockstep_te_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm70_mosi_miso_crc_e rfe_fuSaFault_R2_sm83_rfe_test_mode_active_e rfe_fuSaFault_R2_sm87_m7_rfe_lockup_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm92_sw_wdt_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R1_sm94_m7_message_e2e_crc_sw_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm204_dm_rfe_m7_core_sw_redundancy_e	rfe_fuSaFault_R1_sm58_cg_chirp_e
rfe_fuSaFault_R1_sm62_lockstep_te_e rfe_fuSaFault_R2_sm63_te_swt_radar_pipeline_e rfe_fuSaFault_R2_sm68_sm69_reg_crc_e rfe_fuSaFault_R2_sm70_mosi_miso_crc_e rfe_fuSaFault_R2_sm83_rfe_test_mode_active_e rfe_fuSaFault_R2_sm87_m7_rfe_lockup_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm88_sm89_m7_tcm_sram_e rfe_fuSaFault_R2_sm92_sw_wdt_e rfe_fuSaFault_R2_sm93_xbic_integrity_check_e rfe_fuSaFault_R1_sm94_m7_message_e2e_crc_sw_e rfe_fuSaFault_R2_sm98_m7_spi_access_ana_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm204_dm_rfe_m7_core_sw_redundancy_e	rfe_fuSaFault_R1_sm59_li_chirp_e
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rfe_fuSaFault_R2_sm99_spi_write_check_fail_sw_e rfe_fuSaFault_R2_sm204_dm_rfe_m7_core_sw_redundancy_e	
rfe_fuSaFault_R2_sm204_dm_rfe_m7_core_sw_redundancy_e	
rfe fuSaFault R2 sm435 generic sw e	
	rfe_fuSaFault_R2_sm435_generic_sw_e