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STRX TDC digital

IP Design Report

Rev. 1.2 — 09 Sept 2021 **Design Report**

Document information

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0.1	2019 01 06	Initial template proposal for IP AS
0.2	2020 04 23	Some updates
0.3	2021 01 20	TDC Dig
0.4	2021 03 08	Updated the glue descriptions for the dynamic controls and PON flag; updated the glue figure
0.5	2021 05 04	Standard glue figures updated
0.6	2021 05 26	Structure updated after review of RC_OSC design document. Still the old template, so another update is expected when the correct template becomes available; Structure based on assumption that a separate common control_top document is available in CNET (placeholder added); Integration section added
1.0	2021 06 04	Updated after review. Status updated to PROPOSED; Broken links corrected
1.1	2021 07 06	Added reference to the generic control IP document in the References section
1.2	2021 09 09	Updated after review for GOLD. REF3 fixed

1. Tempsensor (TDC) digital

1.1 Introduction

Control IPs for analog IPs are part of the RFE Dig. Figure 1 shows how a typical IP digital control module would be integrated in the RFE. It will be physically close to the analog IP, but it is part of RFE digital for supply and P&R.

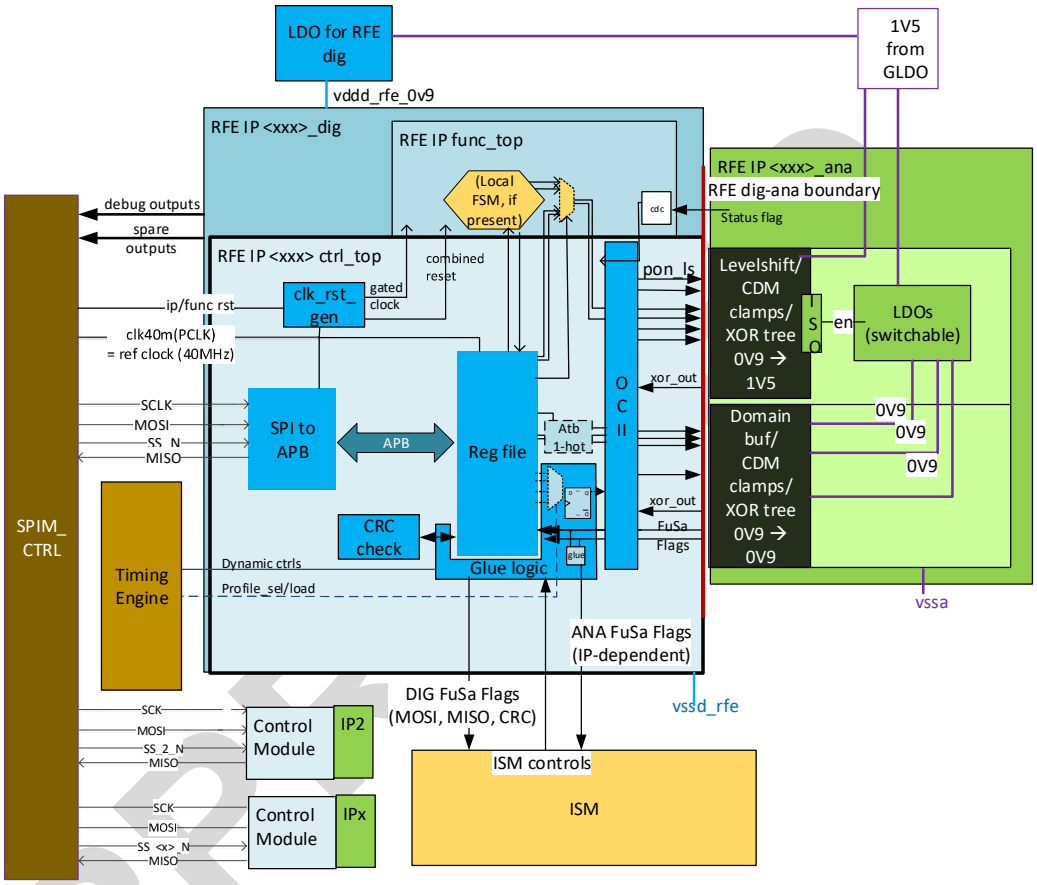

Figure 1: Digital Control IP for analog IPs in the RFE system – generic overview

The common part of all these RFE digital IPs is ctrl_top. The generic structure of ctrl_top and all its subIPs is described in detail in References:REF7.

1.2 Purpose of this IP

This IP controls the settings for the Temperature sensor and takes care of the data capturing and error flag handling.

1.3 IP architecture

Tempsensor digital control consists of 2 parts: a control IP, named ida_mmw_rfe_tempsensor_ctrl_top and a functional part named ida_mmw_rfe_tempsensor_func_top. In the next sections these 2 subIPs will be addressed.
The Tempsensor Dig block diagram is shown in Figure 2.

Note: not all details of ctrl_top are shown here.

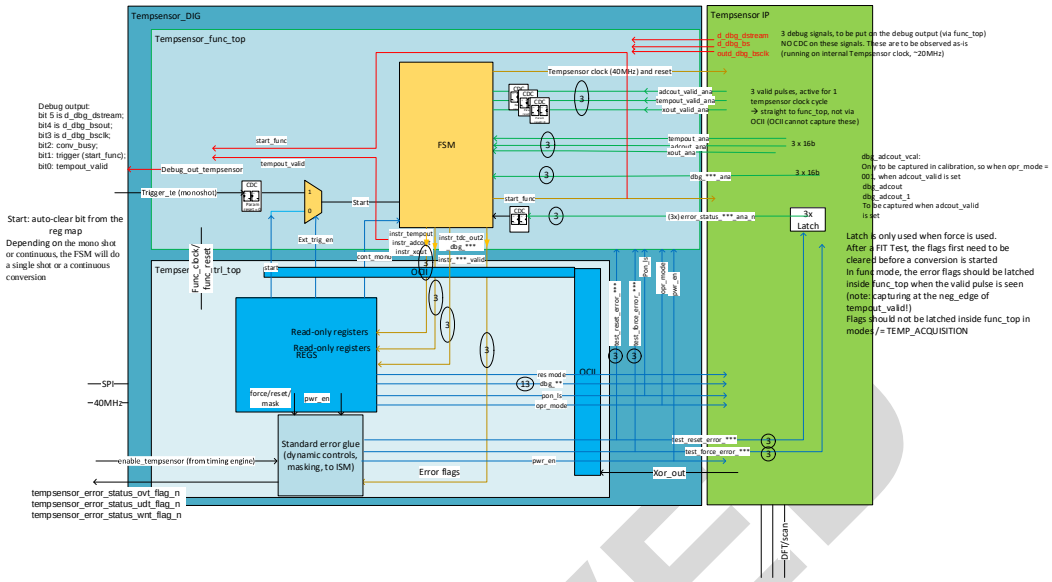

Figure 2: Tempsensor DIG block diagram, consisting of ctrl_top and func_top

1.4 Clock and reset generation unit

This is a standard subIP from ida_mmw_rfe_shared_dig_lib: ida_mmw_rfe_clk_rst_sync. Details of this subIP are provided in References:REF7.

1.4.1 IP interfaces

This digital IP interfaces with the following other IPs:

- TDC analog
- SPIM_CTRL
- ISM
- DFT control

See the Register map, Interface tab Debug/Spare outputs (References:REF5) for details

1.4.2 Debug/Spare outputs

For the tempsensor the following 6 debug outputs are used, all via func_top:

- Bit 0: tempout_valid_intr (extended pulse of tempout_valid_ana)
- Bit 1:start_func
- Bit 2: tdc_status_conv_busy
- Bit 3: dbg_bsclk (from the analog)
- Bit 4: dbg_bsout (from the analog)
- Bit 5: dbg_dstream (from the analog)

The spare outputs and spare inputs are unused. All unused outputs are tied off to 0; All unused inputs are dangling

2. Tempsensor Ctrl_top

The IP ctrl_top module will consist of the following subblocks:

1. Clock and reset generation unit
2. SPI slave with SPI2APB bridge
3. Register block with APB interface
4. CRC checker for the registers
5. OCII interface
6. ATB 1-hot decoder
7. Glue logic, handling the flags from the analog IP, OR-ing the power controls, etc.

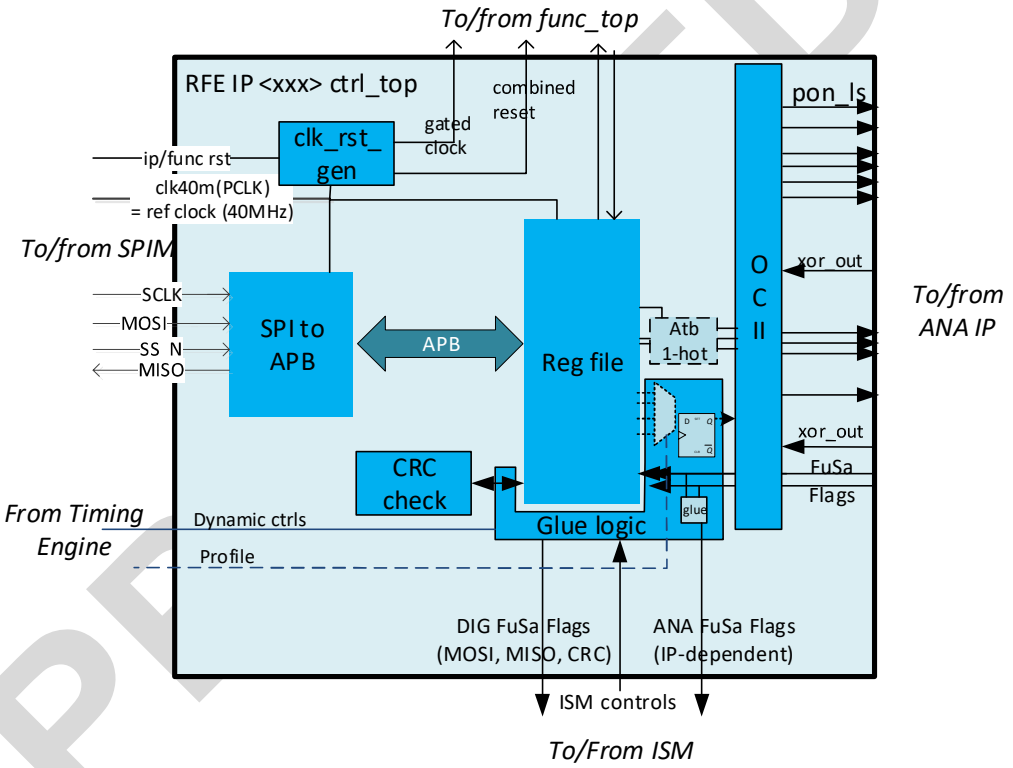

Figure 3: Generic view on a control IP (ctrl_top)

The register map is the single source for most subblocks: register block, OCII, CRC are all generated based on this excel. Also the control IP interface will be included in the same excel, to avoid inconsistencies. The register map can be found on Collabnet, see also References:REF5.

2.1 Clock and reset generation unit

This is a standard subIP from ida_mmw_rfe_shared_dig_lib: ida_mmw_rfe_clk_rst_sync. Details of this subIP are provided in References:REF7.

2.2 SPI slave with SPI2APB bridge

The SPI slave is a standard subIP from ida_mmw_rfe_shared_dig_lib: ida_mmw_rfe_spi_to_apb. Details of this subIP are provided in References:REF7.

2.3 Register block

The register block will be generated using the Magillem tool flow. The input will be the IP register map describing all registers, their widths, offset etc. The register map for this IP can be found in References:REF5.

Details of this subIP are provided in References:REF7.

2.4 CRC checker

The CRC block will be generated from the Register map using the Magillem tool flow. The core of the subIP uses a standard subIP subIP from ida_mmw_rfe_shared_dig_lib: ida_mmw_rfe_reg_crc.

Details of this subIP are provided in References:REF7.

2.5 OCII interface

The OCII subIP is generated using the OCII tool in ida_ocii_global_lib - ida_global_ocii_generator_GEN2. This tool uses the OCII tab in the Register map.

Details of this subIP are provided in References:REF7.

2.6 ATB 1-hot decoder

The ATB 1HOT decoder is a standard subIP from ida_mmw_rfe_shared_dig_lib: ida_mmw_rfe_atb_sel_dec.

Details of this subIP are provided in References:REF7.

2.7 Glue logic

The glue logic will be generated from the Register map using the Magillem tool flow.

The glue logic may contain various logic functions, as described in References:REF7.

- FuSa: Error flag masking, forcing, resetting
- Power-down/soft reset handling
- LDO bypass masking (from SPIM_CTRL)
- Profile muxing → not relevant for this IP
- Dynamic controls: PON control OR-ing (from Timing Engine and register map) → relevant for this IP
- Pon status flag towards ISM

In this section the deviations from the common ctrl_top glue control will be explained.

2.7.1 FuSa: Error masking, forcing, resetting

This IP has both analog and digital error flags.

All glue for force/reset/masking for the digital error flags is according to the standard implementation described in References:REF7.

The analog error and warning flags are handled in a non-standard way.

There are latches for these error flags inside the analog IP, but these latches are only used when the force_error_* is used. After a FIT Test, the flags first need to be cleared before a conversion is started. In functional mode, the error flags should be latched inside func_top when the valid pulse is seen (note: capturing at the neg_edge of tempout_valid!). The reset_error_* controls are used both inside the analog IP (to clear the latch after a force_error_*) and inside func_top.

See Figure 2 and References:REF6.

2.7.2 Power-down/soft reset handling

Standard implementation as described in References:REF7.

2.7.3 LDO bypass/cap_ctl masking

Since the Tempsensor does not contain an LDO, this part is not relevant for the control IP.

2.7.4 Profile multiplexing

This is not relevant for this IP.

2.7.5 Dynamic controls from Timing Engine

For the Tempsensor, the dynamic controls ensure that the Timing engine can also enable/trigger the Tempsensor IP.
For this, the trigger is handled via func_top (see Figure 2). The enable_tempsensor from the TE is OR-ed with the register field PON_CTL.PWR_EN before it is passed to the OCII and to the pon_tempsensor (see section 2.7.6).

2.7.6 PON flag towards ISM

The PON flag towards the ISM is an AND combination of the levelshifter enable **pon_ctl_pon_ls** and **all** LDO enables.
Since the tempsensor does not contain any LDOs, the power_enable control has been used instead:

- pon_ctl_pwr_en (the OR-ed version, see section 2.7.5)

3. Tempsensor functional: func_top

Tempsensor func_top is described in a separate document. See References:REF6.

Note: Spare cells are also implemented inside func_top. The number of spare cells is based on the flipflop count in the IP.

4. Integration

4.1 Critical timing

This IP provides a clock to the analog: clk_tempsensor. Although this is the same 40MHz clock also used inside the IP, there is no strict timing requirement. The clocked signals from the analog will all be treated as asynchronous, flags will pass through a CDC.

4.2 Special considerations

No special considerations known

5. References

Table 1: references

Ref number	Document section	Document description	Document Link
1.	RFE Control and Digital	RFE IP power controls	REF1 [link]
2.	RFE Control and Digital	RFE IP guidelines for registers	REF2 [link]
3.	RFE Control and Digital	M7 interface and SPI	REF3 [link]
4.	References	OCII specification	REF4 [link]
5.	Reg map XLS for all IPs	Tempsensor register map	REF5 [link]
6.	Documents for all RFE IPs	Design description of Tempsensor func_top	REF6 [link]
7.	IP design document	Common control top	REF7 [link]

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8. List of Abbreviations

SPI	Serial Peripheral Interface
SPIM	SPI Master
APB	Advanced Peripheral Bus
CRC	Cyclic Redundancy Check
OCII	On-Chip Instrument Interface
FSM	Finite State Machine
ATB	Analog Test Bus
PON_LS	Power-ON Levelshifters
RFE	Radar Front-End
TE	Timing Engine
FIT	Fault Injection Test

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