C028HPCP_TDC1DG10K

C028HPCP High Accuracy Temperature-to-Digital Converter

Rev. 1.4 — 14 October 2021 Detailed technical specification

COMPANY INTERNAL

Document information

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Revision	Date	Description (latest at top of table)	Author
1.4	20211014	Updated atb secion. Updated leakage current section and operating current section based on design update	Sha Xia
1.3	20201101	Updated operation modes and FuSa modes. slight change in the pinning as input_mode are now changed to operation_mode<2:0>	Sha Xia
1.2	20201030	Updated pinning and blockdiagram, timing diagrams, etc.	Sha Xia
1.1	20200729	Updated pinning and blockdiagram	Sha Xia
1.0	20200513	approved version at IP-PPA	Sha Xia
0.4	20200422	modified draft version based on comment from Haridas	Sha Xia
0.3	20200318	modified draft version	Sha Xia
0.2	20200106	modified draft version after consulting customer, in preparation for IP-PPA	Sha Xia
0.1	20190917	Initial draft version in preparation for IP-PPA	Sha Xia

1 Introduction

This is a high-speed high-accuracy Temperature-to-Digital Converter (TDC) IP.

1.1 General description

The purpose of the amos_c028hpcptdc1dg10k is to provide an accurate temperature-to-digital conversion in the field of radar chips. During radar transmission large currents are drawn generating a lot of heat in a short time, therefore accurate and low-latency temperature information is key in the thermal management of radar chips. The aim is to provide an TDC IP with +/- 1 °C of accuracy over an operating temperature range from -40 °C to 150 °C. This level of accuracy should be obtained after a single-temperature-point voltage trim. The trimming can be done either at room temperature (25 °C), or, if preferred, at higher temperature (up to 150 °C).

This IP will be designed in the C028HPCP process from TSMC. Thick oxide (GO2) devices are used to allow an analog supply voltage higher than 0.9 V (1.5 V).

1.2 Technology & options

Table 1. Technology Information

Technology Settings	
Technology & Technology flavor	CLN28HPCP
Technology options beyond baseline	Deep N-well, thick oxide (GO2) devices, LVT devices.
Metal layers used in the IP	M1 to M8
DPP / DEC Version	TS_CLN28HPCP_1D8_1P8M_5X2ZALRDL_DEC_1.30 with CLN28HPCP_PDK_2.3.0.EA3
Pre-tiled layers	Tiling of the IP will be done to AMS-IP insight
Target DFM level	DFM+analog for analog part of the IP, minimum for digital part of the IP
Supported automotive grade	Compliant to Grade 1 (T_{junc}: -40°C ~150°C)

1.3 IP starting point

For the amos_c028hpcp_tdc1dg10k IP, the amos_c14tdc IP architecture is used as the basis. The BJT frontend design will borrow a lot from the amos_c14tdc IP, while the zoom ADC in the amos_c14tdc IP will be replaced by a conventional sigma-delta ADC. The main reason is that at the high operating temperature, normal sigma-delta operation is more energy efficient compared to zoomADC. This might be a bit counter-intuitive, but for zoomADC the resolution degrades quite a lot at high temperatures, while for normal sigma-delta ADC the resolution is more flat over temperature range and resolution is better at higher temperatures. The second important reason for moving to normal sigma-delta is that considerably less switches are present in the signal chain and this is beneficial for reducing error from leakage current, which is worse at high temperatures.

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Although the two TDCs have similar specification in terms of temperature accuracy, the amos_c028hpcp_tdc1dg10k IP has a much lower conversion time specification which is almost 100 times lower compared to that of the amos_c14tdc IP. This means that the reusability is limited and achieving the speed requirement is challenging.

Table 2. Overview of IP that can be re-used to develop this new IP

IP name	Technology	Re-use description	Maturity
amos_c14tdc	CMOS14	Architecture	IP-SV

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2 Features

2.1 Key features

- Output code directly in degree Celsus (°C)
- Good temperature accuracy of ± 1°C
- Temperature range from -40 °C to 150 °C
- Single-temperature-point voltage calibration
- Calibration requires no accuracte temperature control
- Over-temperature and under-temperature flagging
- Programmable temperature threshold detector in digital domain
- Digital interface
- Parallel digital word indicating instantaneous temperature
- Low conversion time of 100 µs
- High temperature resolution of 100 mK_{rms}

2.2 Key applications

- Car radar transceiver thermal management
- Clock speed optimisation
- General purpose stand-alone TDC
- Processor high-accuracy thermal management
- Temperature threshold detector

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3 Block diagram

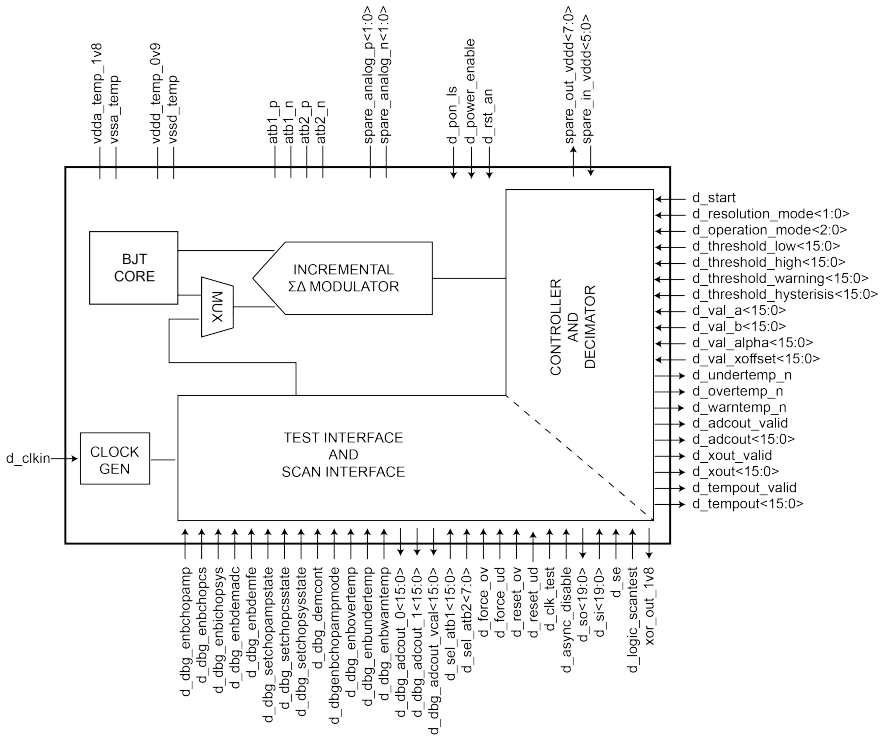

Figure 1. Block diagram

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4 Pinning information

Table 3. Top-level pinning list

Symbol[1]	Type/domain	In/out	Function
Supply signals			
vdda_temp_1v8	Supply	INOUT	Analog supply GO2 domain, 1.62V to 1.98V
vssa_temp	Ground	INOUT	Analog ground
vddd_temp_0v9	Supply	INOUT	Digital supply GO1 domain 0.9V nominal
vssd_temp	Ground	INOUT	Digital ground
Clock signals			
d_clkin	Digital	IN	System clock, this will be a 40 MHz clock input
Digital interface signals			
d_rst_an	Digital	IN	Reset block to initial conditions (low active)
d_pon_ls	Digital	IN	Power up level shifter
d_power_enable	Digital	IN	Power up IP (also functions as reset for the IP)
d_start	Digital	IN	Start conversion
d_resolution_mode<1:0>	Digital	IN	Setting for different resolution mode, the length of the conversion time is configured through this setting. Longer conversion time will translate into higher resolution. More detailed information can be found in section Resolution modes.
d_operation_mode<2:0>	Digital	IN	Setting different operation modes of the TDC. More detailed information can be found in section Operation modes.
d_threshold_low<15:0>	Digital	IN	low temperature threshold for triggering undertemp warning (interrupt)
d_threshold_high<15:0>	Digital	IN	high temperature threshold for triggering overtemp warning (interrupt)
d_threshold_warning<15:0>	Digital	IN	warning temperature threshold for triggering warntemp warning (interrupt)
d_threshold_hysteresis<15:0>	Digital	IN	temperature threshold hysteresis for all interrupt
d_val_a<15:0>	Digital	IN	Input parameter for fitting parameter 'A'
d_val_b<15:0>	Digital	IN	Input parameter for fitting parameter 'B'
d_val_alpha<15:0>	Digital	IN	Input parameter for fitting parameter 'alpha'
d_val_xoffset<15:0>	Digital	IN	Input parameter for trimming parameter 'X_offset'
d_adcout_valid	Digital	OUT	ADC output valid indication
d_adcout<15:0>	Digital	OUT	16-bit word ADC output (<msb:lsb>), used during calibration mode

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Symbol[1]	Type/domain	In/out	Function
d_xout_valid	Digital	OUT	parameter X output valid indication
d_xout<15:0>	Digital	OUT	16-bit word output code for parameter X (<msb:lsb>), whereas X = 1/adcout, used during calibration mode
d_tempout_valid	Digital	OUT	temperature output valid indication
d_tempout<15:0>	Digital	OUT	16-bit word indication of measured temperature (<msb:lsb>) , used during nromal mode
d_undertemp_n	Digital	OUT	indicates temperature below a programmable threshold threshold_low, low active, updated with each new tempout
d_overtemp_n	Digital	OUT	indicates temperature above a programmable threshold threshold_high, low active, updated with each new tempout
d_warntemp_n	Digital	OUT	indicates temperature above a programmable threshold threshold_warning, low active, updated with each new tempout
d_dbg_adcout_0<15:0>	Digital	OUT	16-bit word indication of adcout (<msb:lsb>) in the first sub-conversion, used for debugging
d_dbg_adcout_1<15:0>	Digital	OUT	16-bit word indication of adcout (<msb:lsb>) in second sub-conversion, used for debugging
d_dbg_adcout_vcal<15:0>	Digital	OUT	16-bit word indication of adcout (<msb:lsb>) in the voltage calibration mode, used for debugging
Test interface signals			
d_dbg_enbchopamp	Digital	IN	Control bit to enable chopping for the ota in frontend
d_dbg_enbchopcs	Digital	IN	Control bit to enable system-level chopping
d_dbg_enbchopsys	Digital	IN	Control bit to enable system-level chopping
d_dbg_enbdemadc	Digital	IN	Control bit to enable DEM algorithm for sampling caps in ADC
d_dbg_enbdemfe	Digital	IN	Control bit to enable DEM algorithm for BJTs (vertical PNPs) in frontend
d_dbg_setchopampstate	Digital	IN	Control bit to set the chopper state of ota to '1' or '0'
d_dbg_setchopcsstate	Digital	IN	Control bit to set the system-level chopper state to '1' or '0'
d_dbg_setchopsysstate	Digital	IN	Control bit to set the system-level chopper state to '1' or '0'
d_dbg_demcont	Digital	IN	Control bit to continue the DEM counter over sub-conversions
d_dbg_enbchopampmode	Digital	IN	Control bit to enable chopamp to be different from chopsys
d_dbg_enbovertemp	Digital	IN	Control bit to enable overtemp flag
d_dbg_enbundertemp	Digital	IN	Control bit to enable undertemp flag
d_dbg_enbwarntemp	Digital	IN	Control bit to enable warntemp flag
d_dbg_dstream	Digital	OUT	Manchester-encoded bitstream out

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Symbol[1]	Type/domain	In/out	Function
d_dbg_bsout	Digital	OUT	Bitstream output
d_dbg_bsclk	Digital	OUT	Bitstream clk output
d_sel_atb1<15:0>	Digital	IN	Control bit to select analog testbus 1 signals, see Section 5.5
d_sel_atb2<7:0>	Digital	IN	Control bit to select analog testbus 2 signals, see Section 5.5
d_enbl_atb1	Digital	IN	Control bit to enable analog testbus 1
d_enbl_atb2	Digital	IN	Control bit to enable analog testbus 2
atb1_p	Analog	INOUT	Analog testbus 1 positive branch
atb1_n	Analog	INOUT	Analog testbus 1 negative branch
atb2_p	Analog	INOUT	Analog testbus 2 positive branch
atb2_n	Analog	INOUT	Analog testbus 2 negative branch
Scan interface signals			
d_logic_scantest	Digital	IN	Static signal to set block into scan test mode
d_se	Digital	IN	Scan test enable
d_si<23:0>	Digital	IN	Scan test input
d_so<23:0>	Digital	OUT	Scan test output
d_async_disable	Digital	IN	Disable asynchronous set/reset
d_clk_test	Digital	IN	Test shell clock
xor_out_1v8	Digital	OUT	XOR-tree output for level-shifters
FuSa-related signals			
d_force_ov	Digital	IN	Force overtemp condition, the
d_force_ud	Digital	IN	Force undertemp condition
d_reset_ov	Digital	IN	Reset overtemp condition
d_reset_ud	Digital	IN	Reset undertemp condition
Spare signals			
spare_in_vddd_0v9<7:0>	Digital	IN	Spare input signal (not used)
spare_out_vddd_0v9<7:0>	Digital	OUT	Spare output signal (not used)
spare_analog_p1	Analog	INOUT	Spare analog signal (only used in testchip)
spare_analog_n1	Analog	INOUT	Spare analog signal (only used in testchip)
spare_analog_p0	Analog	INOUT	Spare analog signal (only used in testchip)
spare_analog_n0	Analog	INOUT	Spare analog signal (only used in testchip)

[1] The contents of this table may be updated before schematic review

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5 Modes of operation

This section elaborates the operations of the TDC IP.

5.1 Basic functions

The main functions of the IP includes measureing the temperature and raise over-temperature and under-temperature flags.

5.2 Main blocks

The main blocks of the IP includes the BJT core, an incremental sigma-delta modulator, a clock generator and the digital.

5.3 Operation modes

The operation modes of the TDC IP is controlled by d_operation_mode<2:0> input. Not all combination has been assigned to an actual mode of the IP and some are reserved for later to add more modes if necessary.

Table 4. Operation mode input selection

d_operation_mode<2:0>	Corresponding operation modes
000	Temperature acquisition mode
001	Voltage calibration mode
010	BIST mode, test BJT core
011	BIST mode, test ADC
100	reserved, at this moment default to temperature acquisition mode
101	reserved, at this moment default to temperature acquisition mode
110	reserved, at this moment default to temperature acquisition mode
111	reserved, at this moment default to temperature acquisition mode

5.3.1 Temperature acquisition mode

In temperature acquisition mode, temperature measurement can be done. A single measurement can be started by making the signal *d_start* high (for at least 4 clock periods). If signal *d_start* is held high during and after one measurement is finished, continous measurements will be taken as long as signal *start* remains high. When signal *d_start* becomes low before a measurement is completed, the measurement will stop after the ongoing measurement is complete.

Before the conversion starts and when the *d_start* signal is low, the clock generator block inside the TDC IP is also disabled, to avoid creating possible interference to tha radar signal.

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5.3.2 Functional Safety, DfT, BIST mode

The functionality of the IP can be checked at any time by putting the IP into functional safety (FuSa) mode. The TDC IP supports standard fault-injection,fault-detection function, which can be used to test the connectivity of the IP. Appart from this basic function, the TDC IP also enables fusing the DfT with FuSa. Specifically, the performance of the analog part are tested by extending the DfT idea to analog domain. To enable test in motion, the analog portion of the design features a BIST mode, where no external signal are needed and the performance matrix of the IP can be tested. This BIST mode can be used in both testing and functional safety mode to extend the test coverage of the IP.

The detailed explanation of the principle of those modes can be found in section BIST for use in FuSa and DfT .

5.3.3 Voltage calibration mode

In voltage calibration mode, an external reference voltage needs to be supplied, to determine the internal voltage of the TDC and hence the die temperature.

The detail explanation of both the calibration procedure and the voltage calibration mode can be found in section Calibration & Trimming.

5.3.4 Debug mode

There are varias debug modes that can be set (signals that starts with d_dbg_), those inputs enables/disables certain functions of the IP and can be very useful during lab characterization/measurement/debugging. For normal operation all dubugging inputs should be set to '1'. In pinout section the meanings of those debug modes are briefly described.

5.3.5 Power-down mode

When signal *d_power_enable* is low the IP is in power-down mode. In analog supply domain all analog blocks are put in power down. The digital blocks will also get a reset.

5.4 Resolution modes

This section gives information about the resolution mode settings and the corresponding conversion time and temperature resolution in the form of a table.

Table 5. Resolution mode input

d_resolution_mode<1:0>	conversion time	T resolution(rms)	T resolution(pp)
00	51.6µs	40~65 m°C_{rms}	±0.16~0.26 °C
01	102.8µs	25~35 m°C_{rms}	±0.1~0.14 °C
10	205.2µs	20~25 m°C_{rms}	±0.08~0.1 °C
11	410.0µs	15~20 m°C_{rms}	±0.06~0.08 °C

The conversion time in the table denotes the time it takes from start conversion to *adcout* becomes available. If the internal calculation engine is used to obtain *xout* and *tempout*, then there is aditional delay associated with getting these outputs. Specifically it takes 3.5µs to obtain *xout* and another 3.5µs to obtain the final *tempout*. If the microprocessor

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has sufficient calculation power, in principle the microprocessor can do the conversion from *adcout* to *tempout*, which can be faster.

The detail conversion formulas from *adcout* to *tempout* can be found in section Calibration & Trimming.

The rms resolution range is corresponding to the variation over the temperature range. The resolution is better (smaller rms) at high temperatures and degrades towards lower temperautres.

The pp resolution can be considered to be limted by thermal noise in all resolution settings, and is taken as ±4σ of the rms value here in this document.

5.5 ATB signals

This section gives information about the ATB signals

Table 6. d_sel_atb1 input

d_sel_atb1<15:0>	signals on atb1_p	signals on atb1_n	Comment
0000 0000 0000 0001	vbe_r	vbe_l	dynamic signal used for debugging
0000 0000 0000 0010	vbe_t	vbe_b	dynamic signal used for debugging
0000 0000 0000 0100	vbefe_r	vbefe_l	dynamic signal used for debugging
0000 0000 0000 1000	vint1_p	vint1_n	dynamic signal used for debugging
0000 0000 0001 0000	vint2_p	vint2_n	dynamic signal used for debugging
0000 0000 0010 0000	vadder_p	vadder_n	dynamic signal used for debugging
0000 0000 0100 0000	vcm1	vcm2	two common-mode voltages
0000 0000 1000 0000	vdda	vddd	two supply voltages
0000 0001 0000 0000	vtrim_p	vtrim_n	used to apply trimming voltage

Table 7. d_sel_atb2 input

d_sel_atb2<7:0>	signals on atb2_p	signals on atb2_n	Comment
0000 0001	vtrim_p	vtrim_n	used to measure trimming voltage

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5.6 Timing diagrams

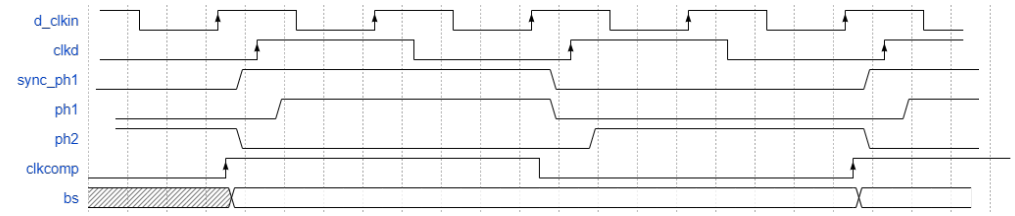

Figure 2. Clock phase relation

In the clock generator inside the TDC IP multiple clock phases are derived from a single system input clock clkin. clk_d is the input for the digital portion of the TDC. Clock ph1 and ph2 are a pair of non-overlapping clock required for the proper operation of the incremental sigma-delta converter. The rising edge of clkd is sitting between the non-overlapping period of clock ph1 and ph2. Clock sync_ph1 is used to indicate to the digital which rising edge of the clkd is corresponding to ph1. Clock signal clkcomp triggers the comparator in the sigma-delta to do conversion of bit-stream signal bs. Clock signal clkout and clknout can be used to log the bs signal for debugging purposes.

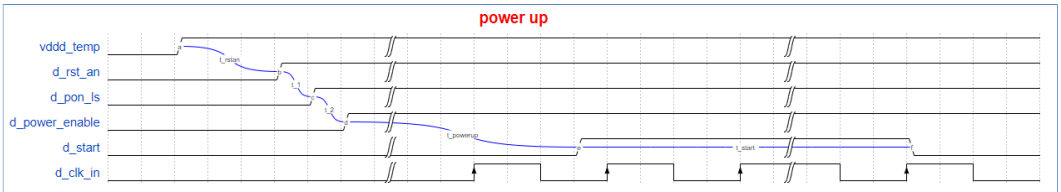

Figure 3. Initialisation

The signal *d_rst_an* is meant to be connected to a power-on-reset (POR) output of the digital supply domain, this will make sure that the digital part of the TDC gets reseted after power up. The time *t_rstan* is then controlled by the POR circuit after ramping up the digital power vddd_temp. The TDC does not have a separate LDO so its digital supply will be supplied by the STRX digital. After *t_1*, the signal *d_pon_ls* enables the level-shifters, and after *t_2*, the signal *d_power_enable* enables the IP. The analog portion of the TDC will wakeup from power_down mode and the digital portion of the TDC will also get a reset. A minimum time $t_{powerup}$ should be waited to allow the analog core to be properly power up before sending the *d_start* signal to start the conversion. The *d_start* signal should be high for a minimum time of *t_start*, and can be held high to enable continouse conversion mode (see below).

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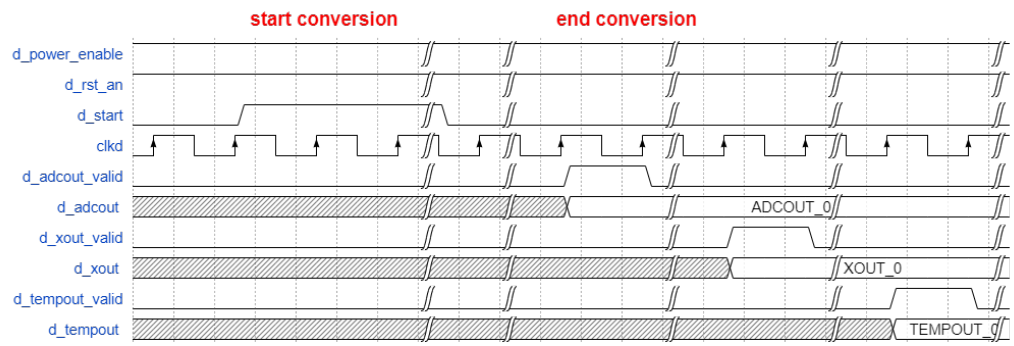

Figure 4. Single conversion

Bring down the start signal low before one conversion ends to have single conversion mode.

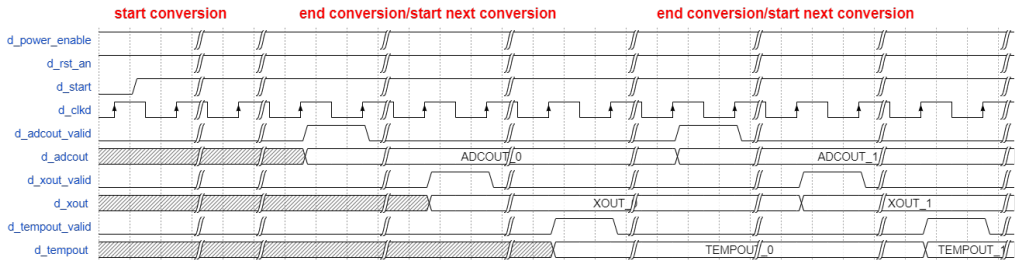

Figure 5. Continuous conversion

Keep the start signal high to have continous conversion. When the start signal is made low before the on-going conversion has ended, the TDC will continou until the current conversion is finished.

5.7 General timing specifications

Table 8. General timing specifications

Symbol[1]	Parameter	Conditions	TL	Min	Typ[2]	Max	Unit
f_{clk}	Input clock frequency	to be provided by system	-	35	40	45	MHz
f_s	Sample frequency		-		9.7		ksps
$t_{powerup}$	Power-up requirement for the analog core	limited by worst-case powerup time	IV	15			µs
t_{rstan}	Reset assertion time		IV	1			µs
t_{start}	Conversion start input duration		IV	0.1			µs

[1] The contents of this table may be updated before schematic review. The values of parameters will become available during the digital design phase.
[2] Typical means simulations at typical conditions, unless stated otherwise: T_{junc} = 25 °C, V_{dda} = V_{dd} = 1.8 V and process = nominal

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6 Electrical specifications

6.1 General specifications

Table 9. General specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Area	IP area	Design target			0.084	mm^2
Metal layers	Allowable metal layers		-		8	-
T_{junc}	Junction Temperature	Temperature range in which the IP is within specification.	-50	25	160	°C
$f_{in,max}$	Temperature change rate	expected temperature change rate during chirp generation			1	°C/ms
Aging		According to mission profile			10	Years

6.2 Limiting values

For absolute maximum ratings see design manual.

6.3 Characteristics

Table 10. Key specifications

Symbol[1]	Parameter	Conditions	TL	Min	Typ[2]	Max	Unit
Static characteristics							
V_{dda}	Analog power supply		-	1.674[3]	1.8	1.98	V
$V_{dda,ripple}$	Analog power supply ripple peak-to-peak		-			300	µV
V_{dd}	Digital power supply		-	0.81	0.9	0.99	V
$V_{ref,acc}$	Reference voltage accuracy	Norminal voltage of V_{ref} = 1.25 V, voltage calibration at 150°C			0.3	1[4]	mV
I_{off}	Off current	T = 25°C, V_{dda} = 1.5 V	II		1000	5000[5]	nA
I_{conv}	Active supply current	T = 25°C and f_{clk} = 40 MHz	II		180	260[5]	µA
T_{acc}	Temperature accuracy	T from -40°C to 150°C, 1-point voltage calibration at room temperature	I	-1		1	°C
T_{res}	Temperature resolution	At 100µs conversion time, 1σ	III		50	100	mK_{rms}
Dynamic characteristics							
f_{clk}	Input clock frequency		-	35	40	45	MHz
f_s	Sample frequency		-			10	ksps

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Symbol[1]	Parameter	Conditions	TL	Min	Typ[2]	Max	Unit
$t_{powerup}$	Powerup time	worst-case powerup time at -40 °C slow corner	IV			15	µs
t_{conv}	Conversion time		IV		110		µs
PSRR	Power supply rejection ratio	Translated from V_{dda},ripple specification, so that at worst-case supply ripple, the resulting temperature error will be less than 0.1 °C	III			0.33	°C/V

[1] The contents of this table may be updated before schematic review
[2] Typical means simulations at typical conditions, unless stated otherwise: T_{junc} = 25 °C, V_{dda} = V_{dd} = 1.8 V and process = nominal
[3] The lower limit of the supply voltage could still vary during the design process mainly due to the limitation of the BJT core
[4] The specified value will result in about 0.3°C of temperature error at the calibration point
[5] T_{junc} = 150°C, V_{dda} = 1.8 V

6.4 Critical parameters/functions

The temperature accuracy after calibration T_{acc} is the critical parameter. To obtain the specified accuracy with the proposed voltage calibration, an accurate reference voltage during calibration is needed. Details of possible ways to guarantee this is discussed with the customer and test engineers. In the end, it is important the the total error budget is not dominanted by the error introduced by the calbiration step.

6.5 Functional safety parameters

6.5.1 Functional safety classification

Case 1.

The TDC IP core will be developed as a case 1 block, however, extra functions will enable it to be qualified as a case 3 block.

The definitions for functional safety case numbers can be found in the glossary of this document, in which more information can be found.

6.5.2 Functional safety measures

For STRX it is desired to have functional safety function built into the IP. Our approach is to build a normal case 1 TDC IP, and with functional extension that makes the IP functional safety case 3.

The idea is to have a combination of fault injection and fault detection mechanism and built-in self test (BIST) built into the TDC IP. Since it is not practical to inject temperature variation to test the IP, the error injection is only happening in digital domain. By observing whether the corresponding flags are raised by the IP or not, we can quickly test if the connection and communication with the TDC IP is (still) OK or not.

With BIST mode extension the test can be extended to cover the analog part of the TDC IP. These tests can be done at any time if required, but is most suitable/advisable to be done during power up checks. The detailed explanation of the principle of those modes and examples of how these modes can be done to aid functional safty test can be found in section BIST for use in FuSa and DfT .

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For more information on Functional Safety and application in IP development, see Automotive Functional Safety Management Procedure

6.5.3 Tools

Default tools as offered in the design environment will be used.

6.6 ESD

The pins listed below can be connected to external pins of the IC this IP is integrated in.

- vdda_temp_1v8
- vssa_temp
- vddd_temp_0v9
- vssd_temp

When the IP supply and reference voltages are delivered through external pins, connected to the IP pin pairs appropriate supply pads need to be used with ESD protection.

Aherence to ESD/ERC rules will be checked with NX-PERC.

6.7 EMC

The critical parts of this IP will be shielded with metal mesh that is grounded. The clock frequency of this IP is derived from and synchronized with the system clock to avoid disturbance inside the signal band.

6.8 Reliability

6.8.1 Mechanical stress

This IP is susceptible to mechanical stress due to the fact that the key component for temperature sensing, namely the BJT, is sensitive to mechanical stress. Package stress will give some shift to BJT characteristic, this needs to be further characterized since the exact scale of effect depends on the specific package type. On top of this, soldering stress is known to further affect the BJT characteristic, however, limited data is available from our previous customer for the amos_c14tdc IP (which is PL PH). For this reason, the vertical PNP has been chosen as the sensing element due to their somewhat smaller sensitivity to stress. It is advised to carefully evaluate those effects.

Bump stress simulations are not always available in a technology and the results are not always accurate. Our advice is to avoid the placement of bumps in the vicinity of the TDC IP to avoid the bump stress issue.

6.8.2 Aging & Electro Migration

For aging simulations, customer has provided the mission profile as input. The effect of aging on the IP will be simulated using Presto.

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6.9 HTOL test

To enable accelerated HTOL testing, this IP will be designed to be functional at 175 °C. performance degradation of design parameters is acceptable at this higher temperature.

HTOL profiles products

6.10 Vstress test

Vstress voltage is 1.6 times nominal Vdd.

Vstress coverage is above 80%.

6.11 Standards

There are no specific standards this IP needs to adhere to.

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7 Test information

7.1 CTAG.AMS

For test access the CTAG.AMS shell can be used. This CTAG.AMS shell consists of a Test Point Register (TPR) to access the digital terminals of the analog IP block and a Test Control Block (TCB) to control the test modes for the IP. More information on the content of the CTAG.AMS shell delivery can be found in Ref. 1. For IP specific information, such as the type of test points used, one is referred to the test shell documentation in the DOCUMENTS directory of the CTAG.AMS shell. For more information on CTAG.AMS application please see Ref. 2.

7.2 Analog DFT mode

The TDC IP will have a analog DFT mode that checks the connectivity of both the BJT core and the ADC of the TDC IP. This test is based on the correct functionality of the sigma-delta converter and the correct value of the BJT frontend voltage. This test can be done during the wafer test, where the temperature is brought to roughly 150 °C, prior to the trimming. This test can also be done everytime the chip is powered up because it requires no external input signal.

For more detail please see section FuSa, DfT and BIST.

7.3 HTOL

No specific functionality for HTOL besides being functional at 175 °C junction temperature is required.

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8 Other requirements

8.1 Restrictions/limitations

N.A.

8.2 Modeling of the IP

Table 11. Model type overview

Model type	Required (Yes/No)?	Purpose (What to cover)?
Verilog	Yes	RTL code for the controller and an ideal behavior description of the analog blocks
SystemVerilog	No	
Wreal	Yes	Wreal is needed. What is needed is a WREAL model of the analog top-entity. It is not necessary to model the hierachical structure, although this would be optional. All pins and under-lying functional behavior should be modelled, including DFT. In the case of TDC the temperature behavior is important. All analog signals including the supplies should be WREAL signals, all digital signasl should be logic signals.
VerilogA	No	
VAMS	No	
Simulink/Matlab	No	

8.3 Simulation agreements

8.3.1 Package modelling

The performance of the TDC will be verified using first-order estimates of the parasitics (resistance/capacitance/inductance) connected to the input, reference and supply pins.

8.3.2 Noise aggressor

To avoid interference with radar TX the clock frequency is chosen appropriately; The internal clock generator can be switched off after the conversion.

8.3.3 Co-simulation

When a database (or analog model) of the LDO is provided by BL-IDA the TDC will be additionally verified using that.

8.4 Verification agreements

All parameters listed in table. 6 will be covered by the verification plan. All sub-blocks will be simulated across PVT and monte-carlo were applicable with extracted layout parasitics. The complete IP will be simulated using a mixed-signal simulation using a

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verilog description of the controller and extracted layout parasitics for the other blocks. Due to practical limitations on simulation time/resources only a reduced set of conditions can be verified using the complete IP. The details will be in the verification plan which will be shared with BL-IDA before IP-CV delivery or, if requested by BL-IDA, at an earlier time frame.

To show the validity of the proposed calibration method, AMSIP will follow the verification method mentioned below:

1. A limited number of monte-carlo runs will be made, (about 20). Their average temperature-output relationship will be used to extract mapping paramters A, B, and alpha. At the same time this average temperature-output relationship will be used as ideal relationship for further calibration steps.
2. After the first step a full monte-carlo simulation will be run. The temperature-output relationship of each sample will be trimmed to the ideal relationship obtained in step 1.
3. The simulation should show that after trimming the mapping paramters A, B, alpha should result in all samples in step 2 to be within the temperature accuracy specification.

8.4.1 Physical verification

DRC/ERC switche settings will be according to the guidelines provided by STRX OneNote file deliverables.

8.5 Deliveries and receivables

8.5.1 Deliveries

The following deliverables from AMSIP have been agreed:

1. All the views as per the IP delivery tabel of the IP creation process description.

8.5.2 Receivables

It has been agreed that the customer will provide the following items:

1. Mission profile for the targeted product. (has been deliverred)
2. List of devices which are not allowed to be used for the given process. (restrictions on MOS transistors, resistors, capacitors, DNW options, etc.) (has been received)
3. Pakage information, and if available, package parasitic. (has been received)

8.6 Review involvement

Table 12. List of core reviewers

Name	Organization	Role
Cicero Vaucher	BL-IDA	Architect
Marc Klaassen	BL-IDA	Product architect
Berry Buter	AMS-IP	Competence lead
Sha Xia	AMS-IP	IP owner

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Table 13. List of optional reviewers

Name	Organization	Role
Athon Zanikopoulos	BL-IDA	Customer project lead
Robert van Veldhoven	AMS-IP	Cluster architect
Dobson Simanjuntak	AMS-IP	Designer
Maoqiang Liu	AMS-IP	Designer

8.6.1 Architecture review

Attendees:

See Table 8.

8.6.2 Schematic review

Attendees:

See Table 8.

8.6.3 Layout review

Attendees:

See Table 8.

8.6.4 Integration review

For the integration review, the persons from AMS-IP listed in Table 8. should be invited.

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9 Application & Integration information

9.1 SoC integration

This TDC IP is designed to be placed close to the circuit whose temperature are to be observed. The orientation of the IP should not affect the accuracy of the trimmed TDC.

The metal layers utilised in this IP is up to and including Metal8. Metal1 to Metal8 are manually tiled and have blocking layers over the entire IP area and any additional routing on these layers, within the perimeter of the block, is trictly prohibited. This requirement is from the point of view of stress.

The DNW is not used inside the TDC IP, however the whole IP will be put inside a DNW for interference considerations.

For general information on how to integrate analog IP, see Ref. 1, section 15.

9.2 Design review

It is strongly recommended to involve AMSIP in both top level schematic and layout design reviews to avoid poor performance due to wrong sharing of pins and/or routing. The following design reviews are suggested:

- Schematic review: use of pad cells and sharing of pins by multiple analog and/or digital circuits.
- Floor plan review: placement of analog blocks w.r.t. each other and the pad ring, orientation of analog blocks.
- Final Place and Route review: cross talk issues for sensitive analog nets, interconnect resistances.

9.3 Integration constraints

Care should be taken when routing top metal across the IP. Placement of solder bump, which introduces stress, should also be avoided in the vicinity of this IP.

For general integration guidelines see: General Analog IP Integration Guidelines

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10 BIST for use in FuSa and DfT

The TDC IP supports a build-in self-test (BIST) mode that can be used for multiple purposes including FuSa and Testing to extend the coverage of the tests. This section provides more detail on this modes.

The standard FuSa function of fault injection and fault observation are supported. However this will not check the analog core functionality. This is used as a means to check the connectivity and communication of the TDC IP. To broaden the coverage of the test, the BIST mode can be engaged. The digital outputs of the TDC IP can be used to check whether the IP analog portion is functional, and it can be even used to verify some specs of the IP.

The BIST function is egaged by setting the *operation_mode* input to '010' and '011', which enables the BIST mode to test the ADC and the BJT core respectively. As can be seen the *operation_mode* input has also reserved modes, those modes are reserved for future modes if necessary.

The BIST mode is in principle just a special conversion with special configuration. To judge if the IP is OK or not, the output of those conversions should be looked at. The judgement should be done with API by the microprocessor.

For better understanding and reference, the temperature acquisition mode is shown there. The BJT core generates two different Vbe voltages by passing two identical curents through two BJTs with different emitter areas. One BJT is a single BJT while the other is the parallel connection of 5 BJTs. The ADC applies 6 times gain to ΔV_{BE} signal and compares that to the reference signal V_{BE} . The ADC output *adcout<15:0>* will correspond to the ratio of $6 \times \Delta V_{BE}$ and V_{BE}:

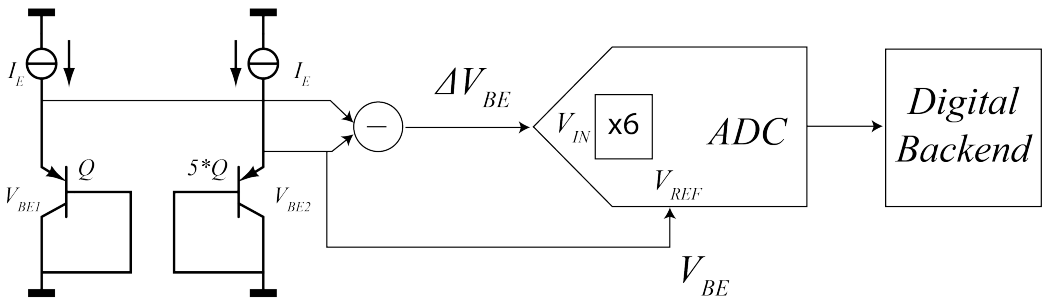

Figure 6. Temperature acquisition mode

$$adcout = \frac{N_{adc} \cdot \Delta V_{BE}}{V_{REF}}$$

N_{adc} is the internal gain stage of the ADC inside the TDC and the value is 6 for this design.

The digital backend will use *adcout* to calculate *xout* which is an intermediate variable and is very convinient for processing.

$$xout = \frac{N_{adc}}{adcout}$$

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The digital backend will further do trimming and calculate temperature based on *xout*. The detail explanation of both the calibration procedure and the voltage calibration mode can be found in section Calibration & Trimming.

10.1 BIST mode, test ADC

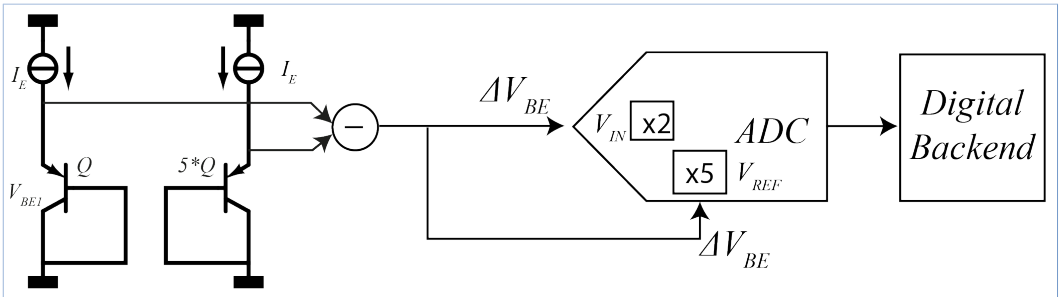

Figure 7. BIST ADC mode

The first BIST mode is egaged by setting the *operation_mode* input to '010', and test both the connectivity and the performance of the ADC. In this mode both the input and the reference voltage of the ADC are connected to the same volage ΔV_{BE}. The gain stage of the ADC is adjusted in this mode to make sure that the input voltage is smaller than the reference voltage. 2 over 5 is chosen here as there are in total 7 unit sampling capacitors. If all connectivities are correct the *adcout* will be close to 2/5 due to the ratiomatric nature of the ADC. In fact, if all dynamic error cancellation techniques are working fine the *adcout* will be close to 2/5 to better than 16-bit. If for instance there are open or short inside the ADC, the *adcout* will be a different value than 2/5. Therefore not only can this test be used to test the connectivity of the ADC, it can also be used as a linearity test. Both results are valuable to FuSa and DfT. Since no external signal is needed, this test is a BIST.

This test should be done before the next BIST test, because the next test relies on the ADC being functional and within spec.

Note this test does not test the BJT core. Because even if there are connection errors in the BJT core, this test can still be carried out. The test of the BJT core is handled in the next BIST test mode.

It is recommended to make use of the microprocessor and API to issue and evaluate the result of this test.

10.2 BIST mode, test BJT core

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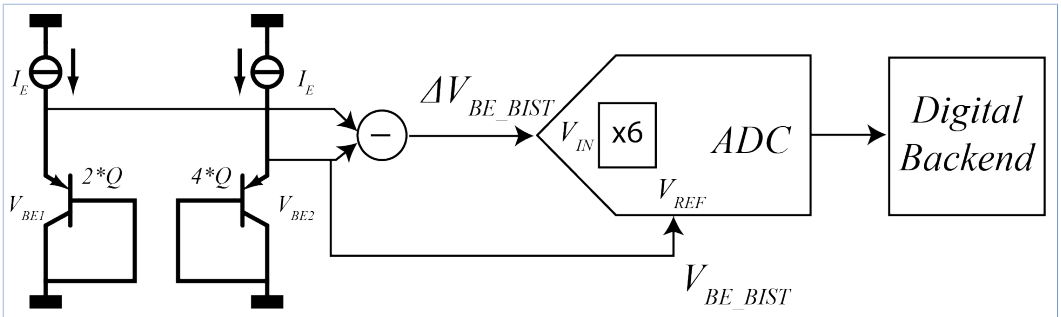

Figure 8. BIST ADC mode

The second BIST mode is egaged by setting the *operation_mode* input to '011', and test both the connectivity and the performance of the BJT frontend. In this test the ADC gain is returned to the configuration in the temperature acquisition mode, and the configuration in the BJT core has changed this time, from 1:5 to 2:4 (effectively 1:2). This will change both the ΔV_{BE} and V_{BE} to ΔV_{BE_BIST} and V_{BE_BIST} respectively. At the same temperature, this will result in a different ADC output $adcout_{BIST}$ and $xout_{BIST}$. The test works by observing the difference between a normal temperauture acquisition mode output *xout* and the BIST BJT core mode output $xout_{BIST}$. Of course, *adcout* can also be used but *xout* has the simplist equation.

So after the circuit passed the first test (BIST ADC, *operation_mode* input = '010'), the TDC IP should carry out two conversions, one in temperature acquisition mode (*operation_mode* input = '000'), and one in BIST mode BJT core (*operation_mode* input = '011'). The two conversions should be sufficiently close to each other in time because it relies on the temperature of the two tests being practically the same.

The two conversion results are denoted *xout* and $xout_{BIST}$. They should satisfy the following relationship governed by the law of physics and math, maybe a little bit of chemistry as well. And the chance that there is connection error while the circuit still satisfy this relationship is practically zero:

$$xout_{BIST} = \frac{\ln(5)}{\ln(2)} \cdot (xout + \frac{\ln(1.25)}{\ln(5)}) = 2.321928*(xout+0.138647)$$

This relationship agrees at all temperatures and all corners to a good degree. The discrepency simulated should be less than **0.1**.

It is recommended to make use of the microprocessor and API to issue and evaluate the result of this test.

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11 Calibration & Trimming

11.1 Calibration

In order to achieve better than 1 °C accuracy for the TDC over process corners, the TDC IP needs to be individually trimmed. To trim a TDC, it is important to obtain information on the die temperature at the time of trimming. This is traditionally done by controlling and measuring the temperature with an accurate reference temperature sensor sitting close to the die. This method, however, is difficult to implement in production environment because the temperature control can introduce as much as 2~3 °C of error at the calibration point.

To solve this problem, this TDC IP provides an alternative method to obtain the die temperature information: by measuring its own ΔV_{BE} voltage against an externally provided reference voltage during calibration. This can be done because the relationship between ΔV_{BE} and die temperature T_{die} is well-defined in our TDC IP.

A number of parameters are needed for mapping the output of the ADC inside the TDC into temperature in Celsius and do the calibration. The value of those parameters can not be obtained by means of simulation and are also specific to the type of package used, due to the cross sensitivity of BJT transistors to stress. These parameters will be determined in a lab environment through careful device characterization process, which will also be covered by AMSIP upon receiving samples. The obtained parameters will work for all future samples using the same type of package. The parameters to be determined are val_a, val_b, val_alpha. Those are used to translate the output of the ADC (adcout and xout) into Celsius temperature readings.

11.2 Trimming procedure

Individual trimming can either be done during wafer test or during final test, depending on the preference. Individual trimming done during wafer test (absence pakage stress) is described below:

The trimming procedure requires the calculation of trimming parameters based on measurements during the trimming. The formula for the calculation is a result of the lab characterization process. We suggest making the calculation with the microcontroller. **The exact implementation needs further discussion.**

- The whole wafer is placed on the chuck, the chuck needs to be brought to the desired calibration temperature (150 °V) and the chuck temperature should be stablilised (not changing very fast during the following calibration sequence). The dies on the wafer should be supplied with a typical VDDA supply voltage.
- The IP is placed into calibration mode by putting input_mode to '1' ('0' is for normal temperature calibration).
- A stable 1.25 V voltage reference is applied to the IP through atb1_p and atb1_n input. At the same time this applied voltage is connected to atb2_p and atb2_n and should be measured by the tester with the best available voltage measurement equipment in terms of accuracy.
- This reference voltage can be optionally accurately measured to improve the voltage calibration accuracy. However, this is not mandatory. ± 1 mV of error on V_{ref} translates into ± 0.3 °C of temperature error which is acceptable for ± 1 °C of error budget.
- It is adviced to set the resolution mode to maximum ('11') for optimum calibration accuracy.

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- Start calibration by setting start signal to high and hold it for at least 4 clock cycles. When input_mode is set to '1', start signal will trigger TDC to convert with V_{ref} as reference.
- A calculation is then performed using the digital output of the ADC adcout of the previous conversion and the value of the V_{ref} to obtain the actual die temperature T_{die}. This information is then used to calculate the ideal value of xout, namely, xout_ideal, at this actual die temperature T_{die}.
- The IP is then immediately placed into normal operating mode by putting input_mode to '0'. A normal temperature conversion is run by setting start signal to high and hold it for at least 4 clock cycles. The die temperature should not change much between these two measurements, hence we can assume that the temperature conversion is performed with die temperature equal to T_{die}. The actual output of xout, namely xout_real, is saved.
- The difference between xout_ideal and xout_real is used to calculate parameter val_xoffset: val_xoffset = xout_real - xout_ideal.
- The IP is calibrated with the val_xoffset.

Notes: This trimming needs to be performed on each die on a wafer during production test to meet specified accuracy. Multiple dies can be trimmed at the same time as long as val_xoffset is calculated for each specific die.

11.3 Trimming equations

Equations used during individual trimming is described below in this section:

The chip characterization step done by AMSIP will generate fitting parameters val_a, val_b, and val_alpha for translate the ADC out adcout of of the TDC into (untrimmed) temperature reading in degrees Celsus (°C):

$$xout = \frac{N_{adc}}{adcout}$$

N_{adc} is the internal gain stage of the ADC inside the TDC and the value is 6 for this design.

$$T_{untrim} = val\_a \cdot \frac{val\_alpha}{val\_alpha + xout} + val\_b$$

For a untrimmed device, the trimming parameter val_xoffset is zero.

During calibration process, the die temperature T_{die} during calibration can be found by measuring ΔV_{BE}. When *d_operation_mode* is '001' and the stable 1.25 V ± 1 mV voltage reference V_{ref} is applied to the IP from ATB bus, the ADC output $adcout_{CAL}$ of the TDC is related to the ratio between ΔV_{BE} and V_{REF}:

$$adcout_{CAL} = \frac{N_{adc} \cdot \Delta V_{BE}}{V_{REF}}$$

N_{adc} is the internal gain stage of the ADC inside the TDC and the value is 6 for this design.

In theory, ΔV_{BE} is proportional to absolute temperature (PTAT). However, in practice, the relationship between ΔV_{BE} and temperature is not exactly linear due to various practical reasons (non-idealities which are captured by the non-ideality factor, etc.).

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Therefore AMSIP will also characterize the relationship between ΔV_{BE} and temperature. A polynomial fitting will be used to fit the measured ΔV_{BE} response as a function of die temperature. It is not exactly known at this moment what order of polonomial fitting should be used for this fitting, but his will become clear during the characterization process. In simulation, a 3rd order fitting is enough to capture the curvature of the ΔV_{BE} voltage. For the moment we just note this relationship as a function f:

$$T_{die} = f(\Delta V_{BE})$$

After obtainning T_{die}, we can use the relationship between T and xout to calculate the ideal xout: $xout_{ideal}$ at this temperature:

$$xout_{ideal} = val\_a \cdot \frac{val\_alpha}{T_{die} - val\_b} + val\_alpha$$

So the val_xoffset can be calculated as:

$$val\_xoffset = xout_{real} - xout_{ideal}$$

The value val_xoffset should be stored as trimming parameters and the temperature after trimming is:

$$T_{trim} = val\_a \cdot \frac{val\_alpha}{val\_alpha + xout - val\_xoffset} + val\_b$$

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12 Assumptions and issues

For voltage calibration to work, there is an important assumption that is made.

In C14 technology, the modeling of the BJT transistors have an ideality factor n_f that does not spread across process corners. In fact, according to our former colleague Dick Wind, who was in charge of C14 modeling, NXP in-house technologies does not model spread in ideality factor n_f because it is very reproduciable. TSMC and Global Fundary however, put a very big spread on n_f of their BJTs over corners. There was an earlier investigation on BJTs in GF40 done by Hans Tuinhout and his colleague, showing that the spread in the fundary PCM data is mainly caused by temperature inaccuracy during the measurement, not by the device itself. This is communicated to TSMC modeling team, however, it is not clear when the model could be updated at this moment.

The assumption here is that the spread in the BJT ideality factor in C028HPCP model is not realistic. If it were true, then that means there is no way to make voltage calibration work, because the error from n_f spread alone will contributes to ± 1 °C of error in voltage calibration.

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13 Abbreviations

This paragraph explains the abbreviations used in this document.

Table 14. Abbreviations

Abbreviation	Meaning	Further info
General Items:		
DFM	Design For Manufacturability	
DfT	Design for testing	
EMC	Electromagnetic compatibility	
ESD	Electrostatic discharge	
HTOL	High Temperature Operating Life	
LDO	Low drop out (regulator)	
LVT	Low threshold voltage (VT)	
PSRR	Power supply rejection ratio	
N.A.	Not Applicable	
TBD	To be defined	
TDC	Temperature-to-Digital Converter	
TL	Test level	
IP specification items:		
BJT	Bipolar junction transistor	
PTAT	Proportional to absolute temperature	

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14 Glossary

14.1 Test levels

Table 15. Test levels

Test level	Definition release date 20190404	
I	Tested over supply voltages and temperature, at multiple use-cases / settings	The key specs of the IP. The first thing you want to know when you get silicon back.
II	Tested over supply voltages and temperature, only at nominal bias settings	Parameter with at least one guaranteed limit.
III	Tested over supply voltage and temperature, at nominal bias settings, statistics of parameter not tested	Parameter that will only have at least a typical value
IV	Characterized by simulation only	Parameter that cannot be measured on silicon

14.2 Functional Safety classification

For more information on Functional Safety and application in IP development, see Automotive Functional Safety Management Procedure

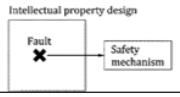
Case 1	The IP does not include any Safety requirements and is not developed per ISO26262.	
Case 2	The IP include Safety requirements and shall be compliant to ISO26262, but it does not include Safety mechanisms inside the IP. The IP is developed as a Safety Element out of Context (SEooC).	
Case 3	The IP include Safety requirements and shall be compliant to ISO26262, and it includes Safety mechanisms inside the IP. The IP is developed as a Safety Element out of Context (SEooC).	

Figure 9. Classification of IP w.r.t. Functional Safety

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15 References

Table 16. References

Number	Document title	Info to be found
1	AMS-IP website	Analog IP information, ordering instructions and integration guidelines
2	CoReUse_5.0_CTAG_Cookbook.pdf	CoReUse CTAG.AMS Cookbook
3	Mission Profile Library.xlsm	Reliability Mission Profile Library
4	AMSIP-DE-P-0010.docx	AMS-IP Analog IP creation process

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16 Approval of this document

Table 17. Accepted by (internal AMSIP)

Name	Role	Date
Sha Xia	IP owner	20190918
Berry Buter	Competence lead	20190923
Stefan Menten	Validation competence lead	20200303
Robert van Veldhoven	Cluster architect	20190928

Table 18. Accepted by (Customer)

Name	Role	Date
Athon Zanikopoulos	Customer project lead	20200422
Marc Klaassen	Product architect	20200129
Cicero Vaucher	Architect	20200129
Frank van der Velden	DFT engineer	20200211
Haridas Vilakathara	Functional safety manager	20200501

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