Baugh Wooley Multiplier

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Abstract:

Multiplications are less common than addition. Multiplier is essential for Microprocessors, Digital signal processors, graphic engines. Multiplication is a key bottleneck in most digital signal processing systems. With technological advancements, numerous researchers have attempted and continue to attempt to build multipliers that give high speed, low power consumption, and therefore less area in one multiplier, making them appropriate for different high speed, low power, and compact implementations. For signed multiplication, the Baugh Wooley Multiplication approach was applied to boost speed. Because of the intricacy of its construction, it is rarely extensively utilized.

1. Introduction:

Data representations are critical!

A decent representation for negative integers can make designing subtraction hardware considerably easier. It is simple to construct a single circuit for both using two's complement. Subtraction and addition

There are various considerations to consider when working with signed numbers.
- Signed overflow differs greatly from unsigned overflow.
- To appropriately "lengthen" negative values, sign extension is required.

In signed multiplication the length of the partial products and the number of partial products will be very high. So, an algorithm was introduced for signed multiplication called as Baugh Wooley algorithm. The Baugh-Wooley multiplication is one amongst the cost-effective ways to handle the sign bits. This method has been developed to reduce complexity than regular multipliers, suited to 2's compliment numbers.

1. Signed 2’s complement is widely used because if the result is within the limits, we can neglect the intermediate overflows, underflows.
2. Used mostly in microprocessors and DSP processors.
3. The goal of this research is to find a decent multiplier that will produce a physically compact, high-speed, low-power device.
4. As a key component of arithmetic processing units, multipliers are in high demand due to their fast speed and low power consumption.
5. Today's digital signal processing and other applications rely heavily on multipliers.

The Baugh-Wooley multiplier is a well-known and simple algorithm. Booth multiplier is the simplest and quickest algorithm.

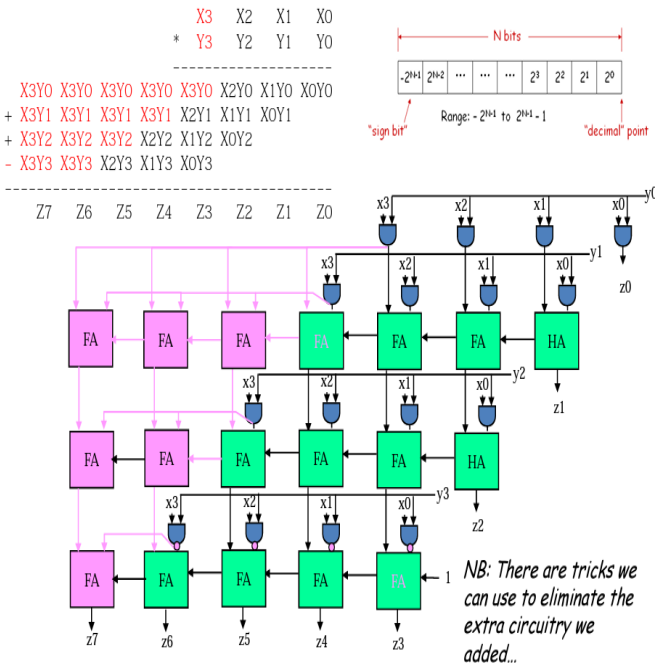
2.1 Combinational Multiplier (signed):

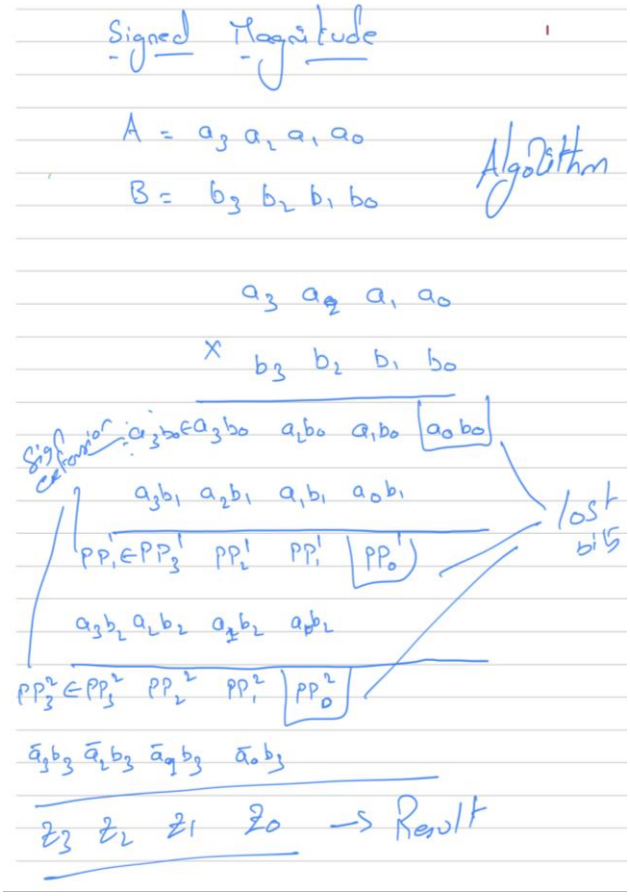
Signed multiplication •Requires special consideration for negative (2's complement) numbers.

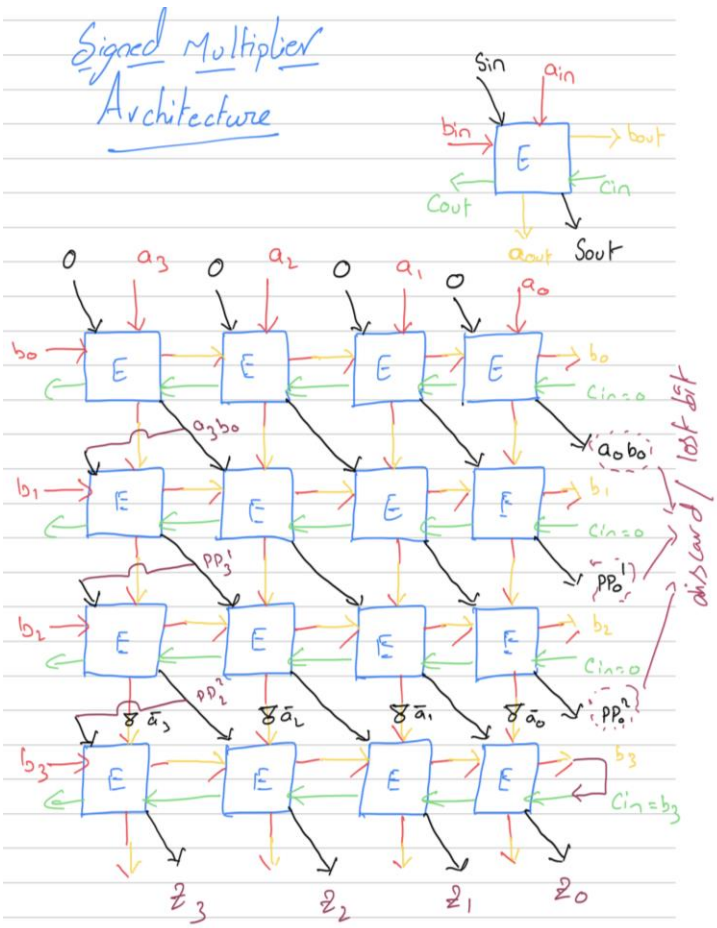
The additional values out to the MSB position is called sign extension

•This is true for both positive and negative numbers.

•We just don't usually write out the 0's.







2.1 2's Complement Multiplication (Baugh-Wooley Multiplier):

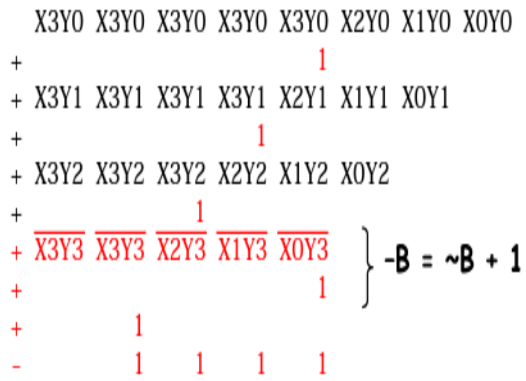
The construction of iterative arrays becomes more complicated when the operands are in two's complement form since the sign bit is contained in the integer itself. Direct two's complement multiplication arrays have been proposed, in which the cells are either more complicated or the number of cells is much more than in positive-number multiplier arrays.

Baugh and Wooley changed the multiplication matrix such that it only contains positively weighted partial products. This necessitates the use of both the operands' true and complement values. There is also a modest increase in the number of adding cells and the time required for multiplication. However, the resultant array only contains Type 0 complete adder cells. This homogeneity is especially beneficial for LSI implementation. Adding two 2's complement numbers together.

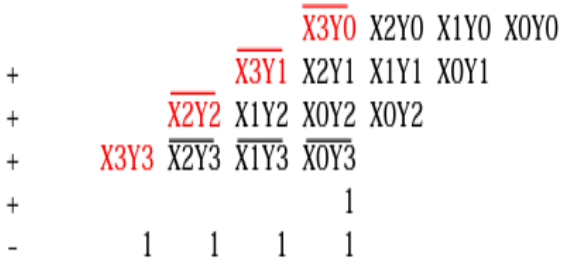
- Step 1: use two's complement operands such that the highest order bit is -2N-1. It is necessary to sign extend partial products and remove the last one.

```
                          X3    X2    X1    X0
                      *   Y3    Y2    Y1    Y0
                      ------------------------
   X3Y0  X3Y0  X3Y0  X3Y0  X3Y0  X2Y0  X1Y0  X0Y0
+  X3Y1  X3Y1  X3Y1  X3Y1  X2Y1  X1Y1  X0Y1
+  X3Y2  X3Y2  X3Y2  X2Y2  X1Y2  X0Y2
-  X3Y3  X3Y3  X2Y3  X1Y3  X0Y3
---------------------------------------------
    Z7    Z6    Z5    Z4    Z3    Z2    Z1    Z0
```

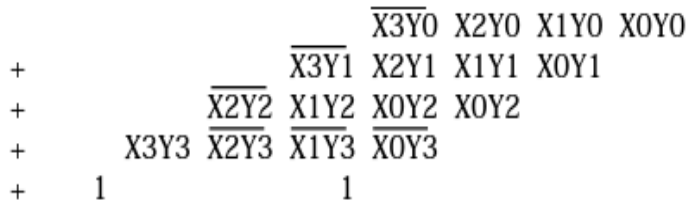
- Step 2: To avoid all those additional adds, add a properly chosen constant and remember to remove it at the end. Subtraction is converted into the addition of (complement + 1).



- Step 3: combine the ones and propagate the carries. All the sign extension pieces are removed!



- Step 4: Complete the constants computation... As a result, multiplying 2's complement operands requires almost the same hardware as multiplying unsigned operands!



2.2.1 Formulation:

- The Baugh-Wooley multiplication technique is an effective method for dealing with sign bits. This approach was created in order to create multipliers for 2's complement numbers. Consider the following two n-bit integers. A and B should be multiplied. A and B can be written as:

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i$$

$$B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i$$

$$\begin{aligned} P &= A \times B \\ &= \left(-a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i\right) \times \left(-b_{n-1}2^{n-1} + \sum_{j=0}^{n-2} b_j 2^j\right) \\ &= a_{n-1}b_{n-1}2^{2n-2} + \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} a_i b_j 2^{i+j} \\ &\quad -2^{n-1}\sum_{i=0}^{n-2} a_i b_{n-1}2^i - 2^{n-1}\sum_{j=0}^{n-2} a_{n-1}b_j 2^j \end{aligned}$$

$$\begin{aligned} P &= a_{n-1}b_{n-1}2^{2n-2} + \sum_{i=0}^{n-2}\sum_{j=0}^{n-2} a_i b_j 2^{i+j} + \\ &\quad 2^{n-1}\sum_{i=0}^{n-2} \overline{b_{n-1}a_i}2^i + 2^{n-1}\sum_{j=0}^{n-2} \overline{a_{n-1}b_j}2^j + \\ &\quad -2^{2n-1} + 2^n \end{aligned}$$

2.2.2 Structure of n×n bit Baugh-Wooley multiplier:

To compute the likely concept, the switching activity is computed while one input operand is maintained constant and the other receives random data. Each partial bit in the Booth multiplier is combined with the vector adder. The quantity of partial products will also impact a system's power dissipation. As a result, we may lower the non-zero partial products to save energy.

Normally, the number of partial products and their length are substantially greater in the signed multiplication approach. As a result, the Baugh Wooleyalgorithm was developed for signed multiplication. The Baugh-Wooley multiplication is a good and inexpensive way to do signed bit operations. This algorithm was created to create regular multipliers with 2's complement integers. This multiplication procedure employs a left shift algorithm as well as a multiplexer to choose the multiplication bit.

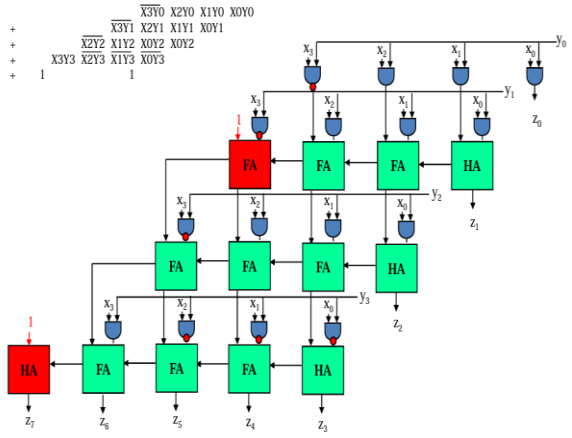
2.2.3 Considering 4 bit number where n=4:

Substitute the n value as 4 in equation p, after simplification we will get the equation mentioned below.

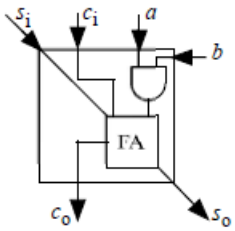
$$\begin{aligned} P &= a_3b_3 2^6 + \sum_{i=0}^{2}\sum_{j=0}^{2} a_i b_j 2^{i+j} + \\ &\quad 2^3\sum_{i=0}^{2} \overline{b_3 a_i}2^i + 2^3\sum_{j=0}^{2} \overline{a_3 b_j}2^j + \\ &\quad -2^7 + 2^4 \end{aligned}$$

2.2.4 Implementation:

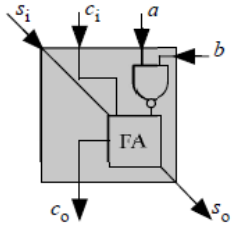
Implementing the architucture using algorithm:



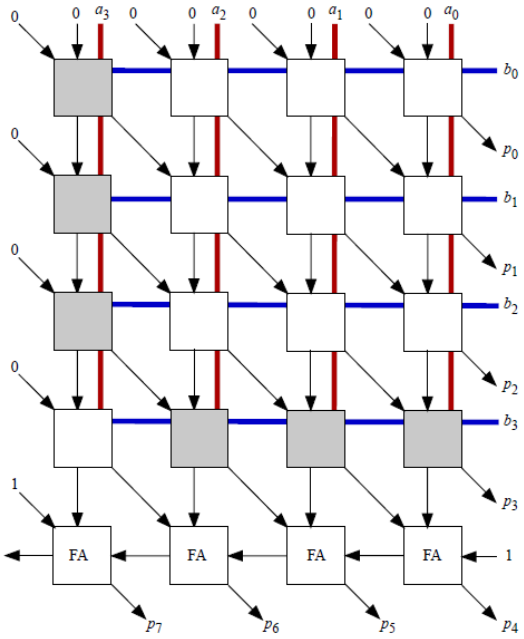
Another way to implement the design:



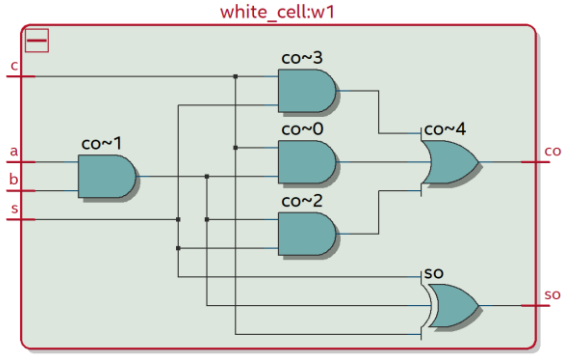
White cell



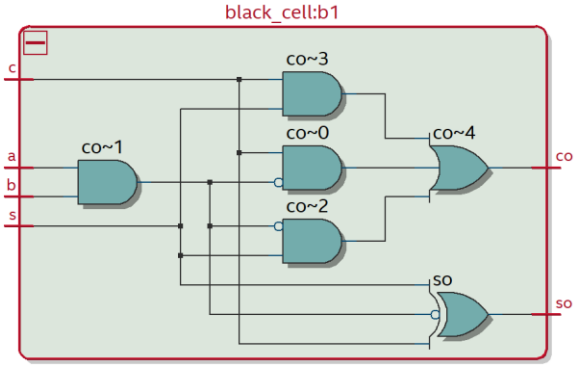
Grey cell

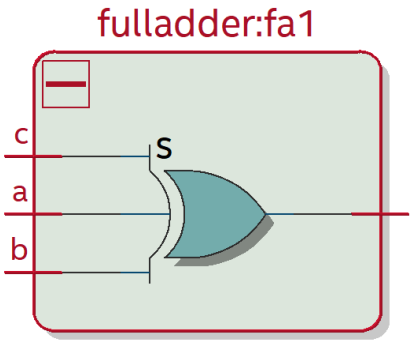


Block diagram for 4x4 Baugh wooley Multipler



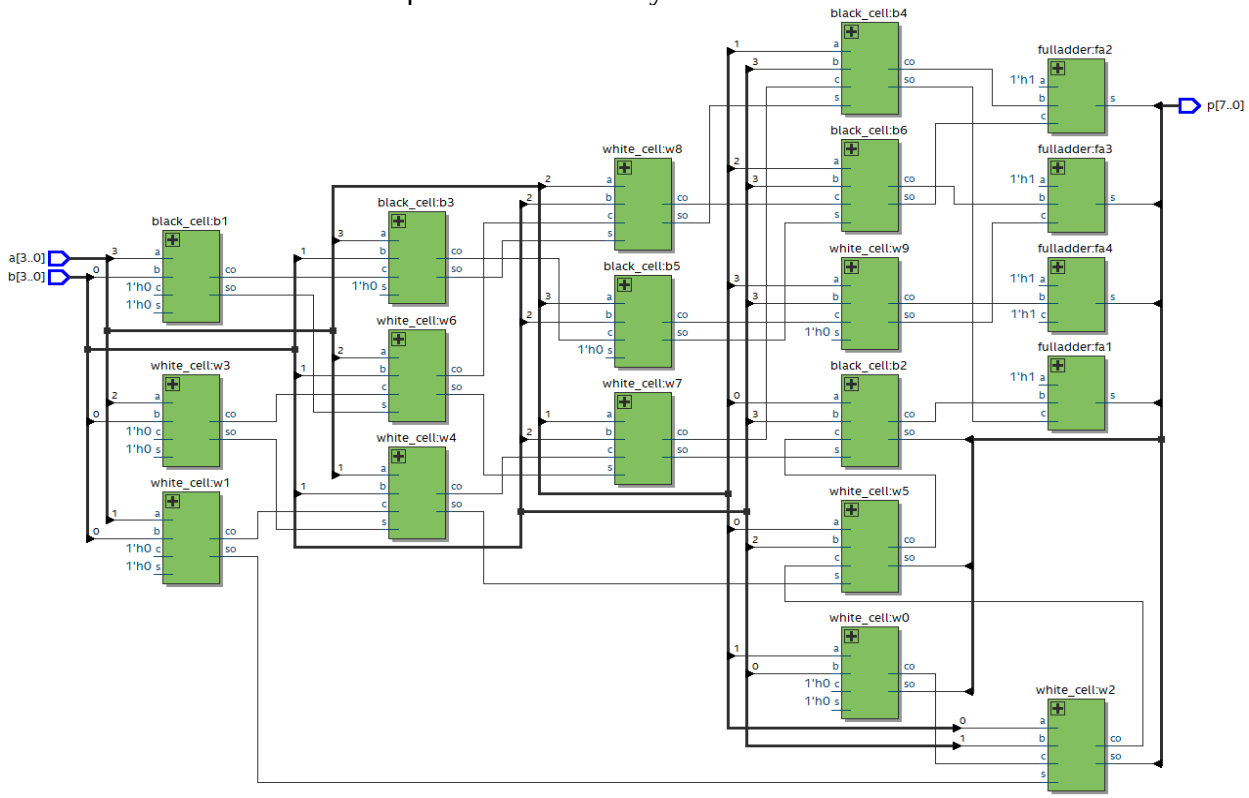
Implemention of ecah cell and internal logic for each cell.





3. Simulations and Results:

Simulations for 2's complement 4 bit binary.



4. Conclusion:

This proposed design which are presented the design of a n-bit Baugh Wooley Multiplier using the based Adder's. And here we implemented the 4-bit Baugh Wooley multiplier. Key component of arithmetic processing units, multipliers are in high demand due to their fast speed and low power consumption.

5. References:

[1] Ravindra P Rajput and M.N Shanmukha Swamy, (2012) "High Speed Modified Booth Encoder multiplier for signed and unsigned numbers". IEEE, International Conference on Modelling and Simulation, pp. 649-654.

[2] R. Bajaj, S. Chhabra, S. Veeramachaneni and M B Srinivas, "A Novel, Low-Power Array Multiplier Architecture",International Institute of Information Technology-Hyderabad.

[3] Class presentstion – by professor mirzeai

[4] Implementation of Low power Baugh-Wooely Multiplier and Modified Baugh Wooely Multiplier Using Cadence (Encounter) RTL in DSM Technology