top1

synchronizer

clock	fifo_full
data_in[1:0]	soft_reset_0
detect_add	soft_reset_1
empty_0	soft_reset_2
empty_1	vld_out_0
empty_2	vld_out_1
full_0	vld_out_2
full_1	write_enb[2:0]
full_2	
read_enb_0	
read_enb_1	
read_enb_2	
resetn	
write_enb_reg	

router_sync

router_top